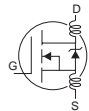


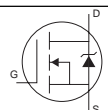
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.11 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑤ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.036 | Ω | $V_{GS} = 10V, I_D = 23A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 14 | — | — | S | $V_{DS} = 25V, I_D = 22A$ ⑤ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 100V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| Q_g | Total Gate Charge | — | — | 110 | nC | $I_D = 22A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 15 | | $V_{DS} = 80V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 58 | | $V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 11 | — | ns | $V_{DD} = 50V$ |
| t_r | Rise Time | — | 56 | — | | $I_D = 22A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 45 | — | | $R_G = 3.6\Omega$ |
| t_f | Fall Time | — | 40 | — | | $R_D = 2.9\Omega$, See Fig. 10 ④ ⑤ |
| L_D | Internal Drain Inductance | — | 5.0 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 13 | — | | |
| C_{iss} | Input Capacitance | — | 1900 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 450 | — | | $V_{DS} = 25V$ |
| C_{riss} | Reverse Transfer Capacitance | — | 230 | — | | $f = 1.0\text{MHz}$, See Fig. 5 ⑤ |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|---------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 42 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① ⑤ | — | — | 140 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 23A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 180 | 270 | ns | $T_J = 25^\circ\text{C}, I_F = 22A$ |
| Q_{rr} | Reverse Recovery Charge | — | 1.2 | 1.8 | μC | $di/dt = 100A/\mu s$ ④ ⑤ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}, L = 1.7\text{mH}$
 $R_G = 25\Omega, I_{AS} = 22A$. (See Figure 12)
- ③ $I_{SD} \leq 22A, di/dt \leq 180A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF1310N data and test conditions

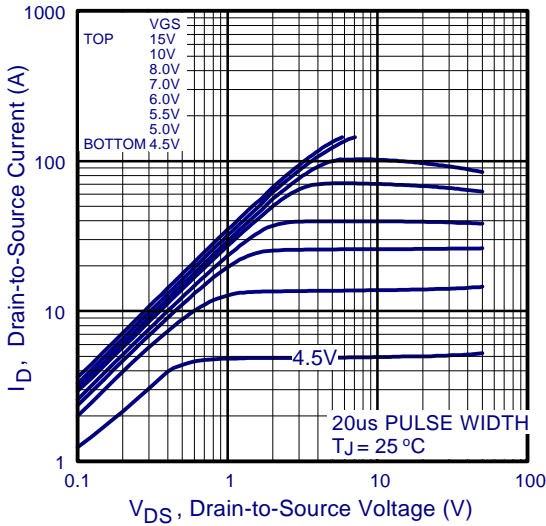


Fig 1. Typical Output Characteristics

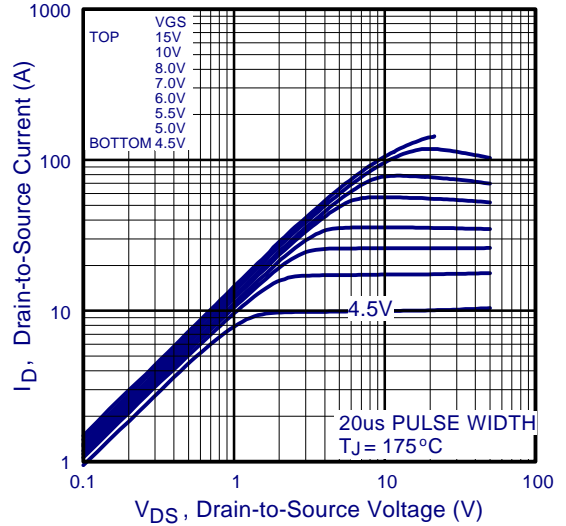


Fig 2. Typical Output Characteristics

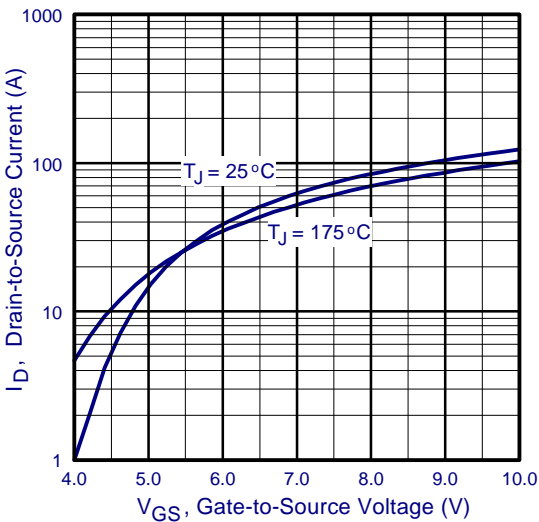


Fig 3. Typical Transfer Characteristics

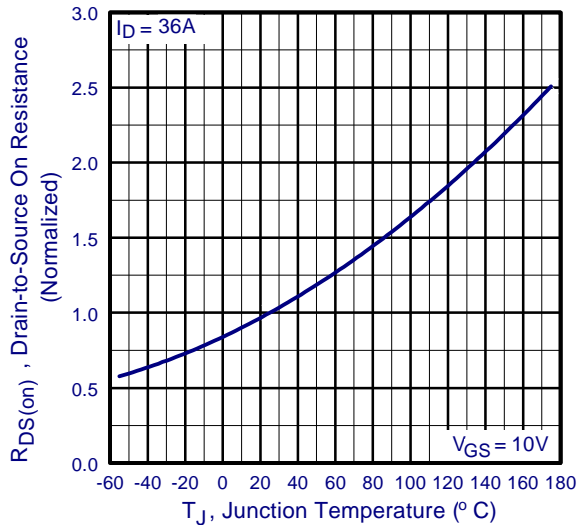


Fig 4. Normalized On-Resistance Vs. Temperature

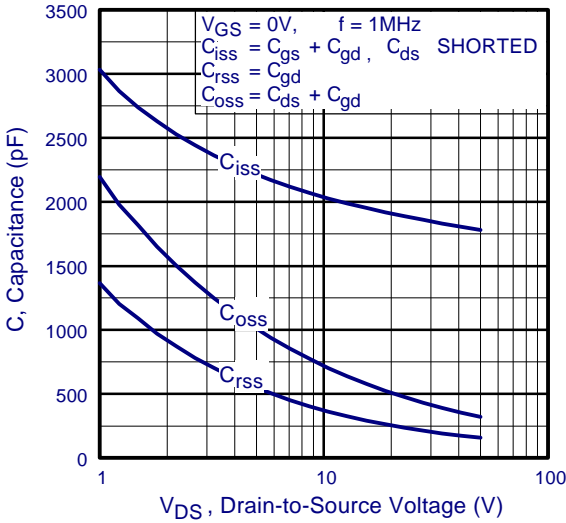


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

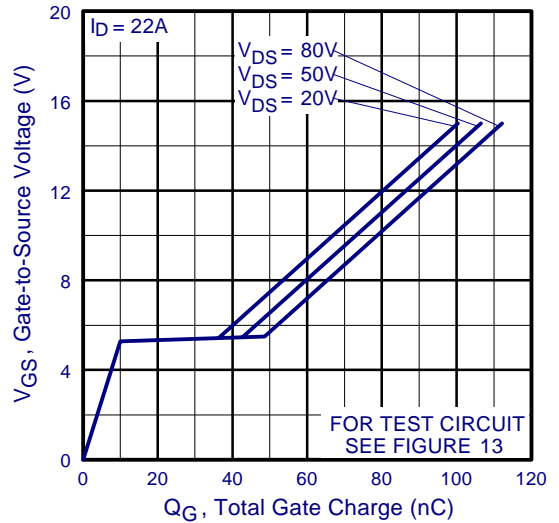


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

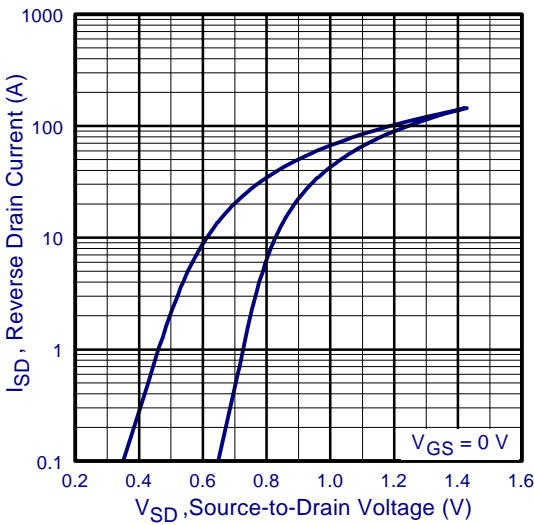


Fig 7. Typical Source-Drain Diode Forward Voltage

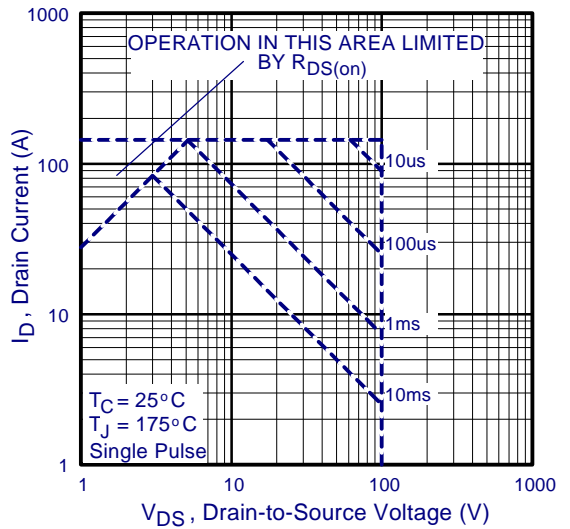


Fig 8. Maximum Safe Operating Area

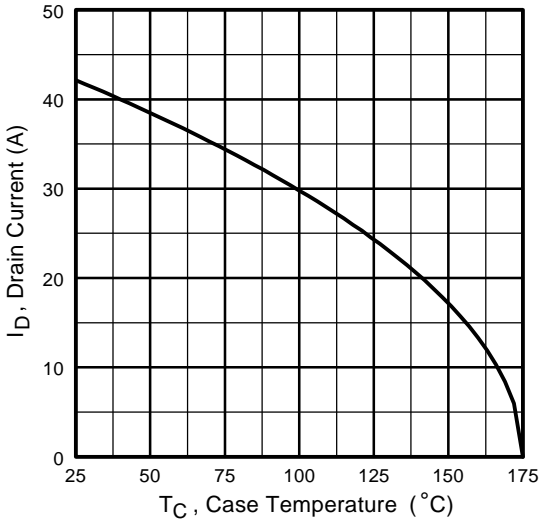


Fig 9. Maximum Drain Current Vs. Case Temperature

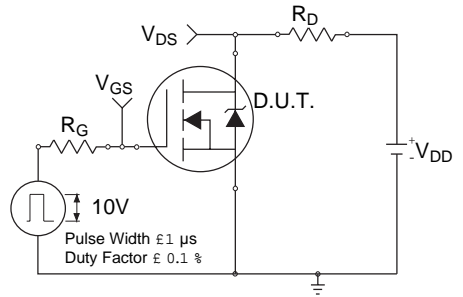


Fig 10a. Switching Time Test Circuit

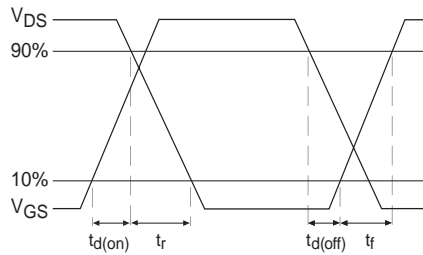


Fig 10b. Switching Time Waveforms

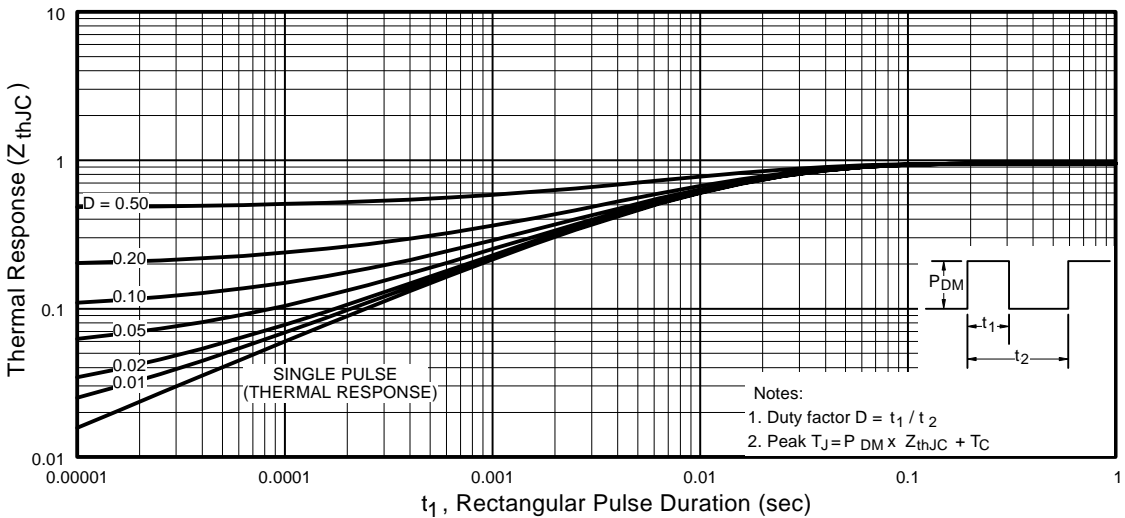


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

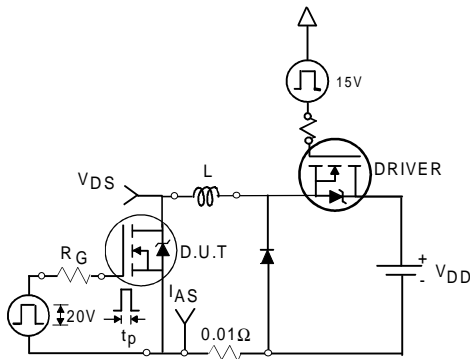


Fig 12a. Unclamped Inductive Test Circuit

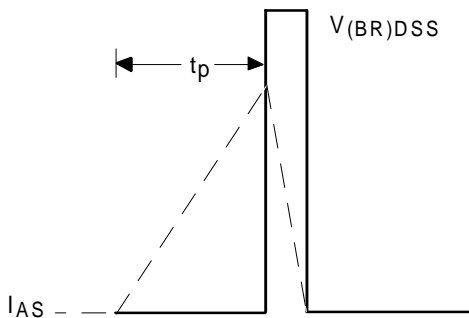


Fig 12b. Unclamped Inductive Waveforms

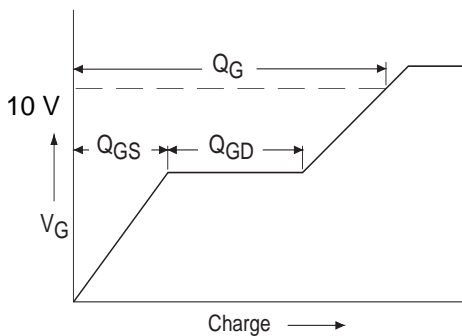


Fig 13a. Basic Gate Charge Waveform

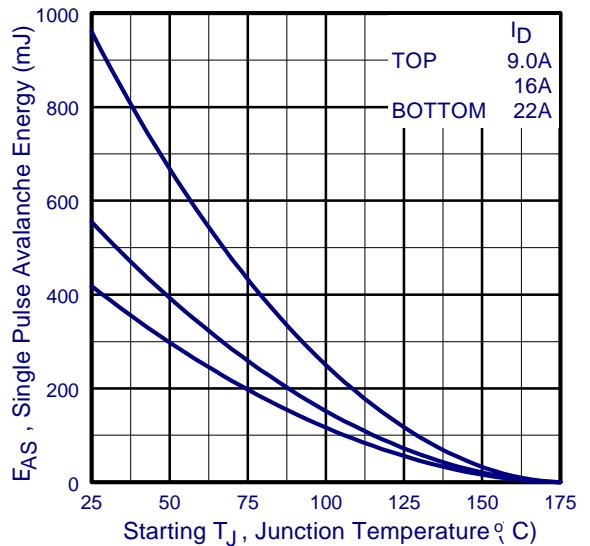


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

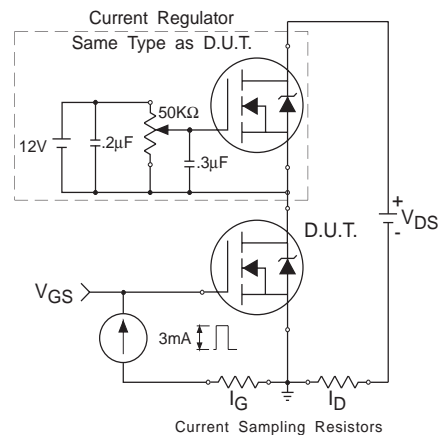
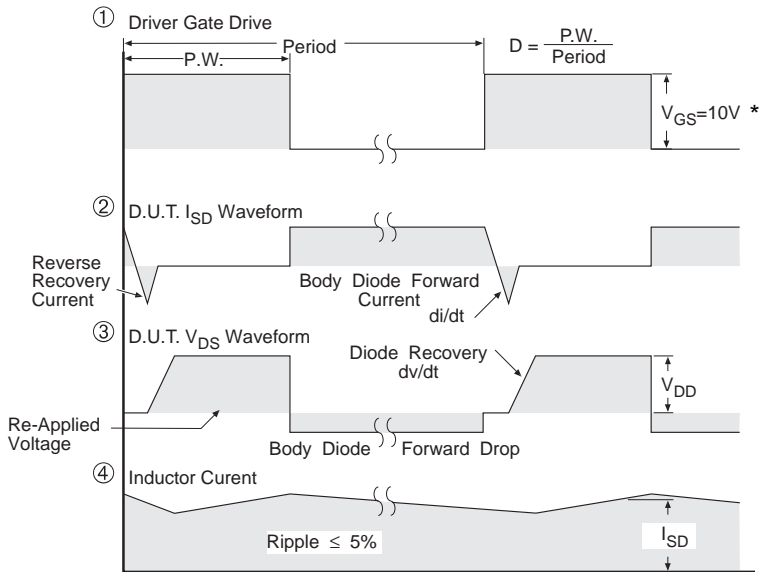
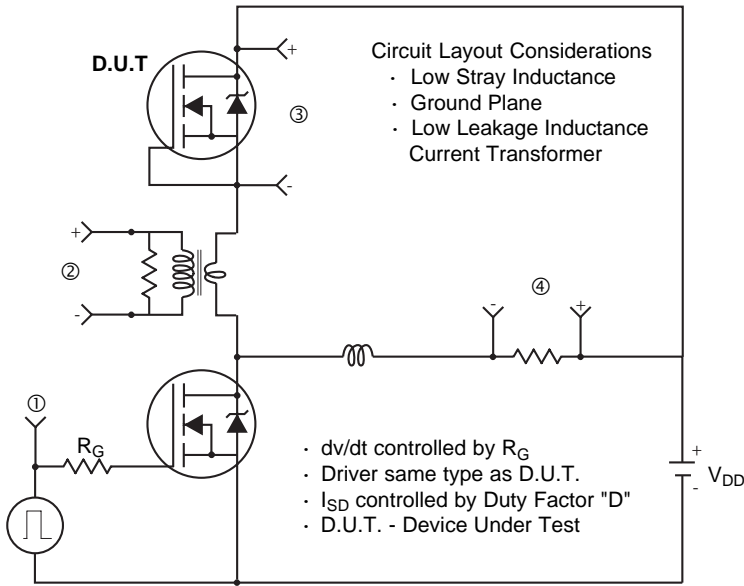


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



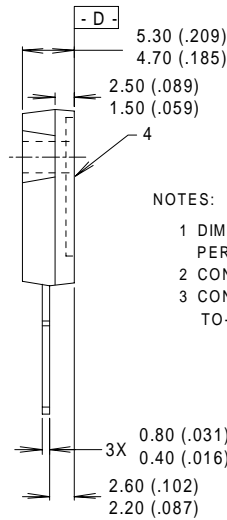
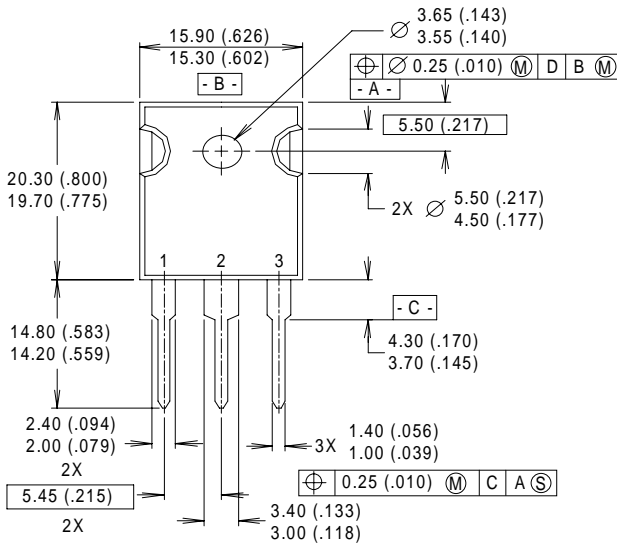
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-247AC Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

Part Marking Information

TO-247AC

EXAMPLE : THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 3A1Q

