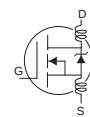
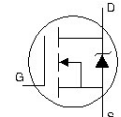


Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified) ⑤

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	24	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	80	100	m Ω	$V_{GS} = 10V, I_D = 5.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	4.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-12	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 5.5A$
Q_g	Total Gate Charge	—	19	29	nC	$V_{DS} = 100V$ $V_{GS} = 10V$ $I_D = 5.5A$ See Fig. 6 and 15
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	4.9	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	0.95	—		
Q_{gd}	Gate-to-Drain Charge	—	5.8	—		
Q_{godr}	Gate Charge Overdrive	—	7.4	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	6.8	—		
$R_{G(int)}$	Internal Gate Resistance	—	3.0	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	8.4	—	ns	$V_{DD} = 100V, V_{GS} = 10V$ ③ $I_D = 5.5A$ $R_G = 2.4\Omega$
t_r	Rise Time	—	8.0	—		
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		
t_f	Fall Time	—	4.0	—		
C_{iss}	Input Capacitance	—	1240	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig.5 $V_{GS} = 0V, V_{DS} = 0V$ to 160V
C_{oss}	Output Capacitance	—	130	—		
C_{rss}	Reverse Transfer Capacitance	—	28	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	110	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		

**Diode Characteristics ⑤**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	9.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	36		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 5.5A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	76	110	ns	$T_J = 25^\circ\text{C}, I_F = 5.5A, V_{DD} = 160V$
Q_{rr}	Reverse Recovery Charge	—	230	350	nC	$di/dt = 100A/\mu s$ ③

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 8.6mH$, $R_G = 25\Omega$, $I_{AS} = 5.5A$.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ Specifications refer to single MosFET.

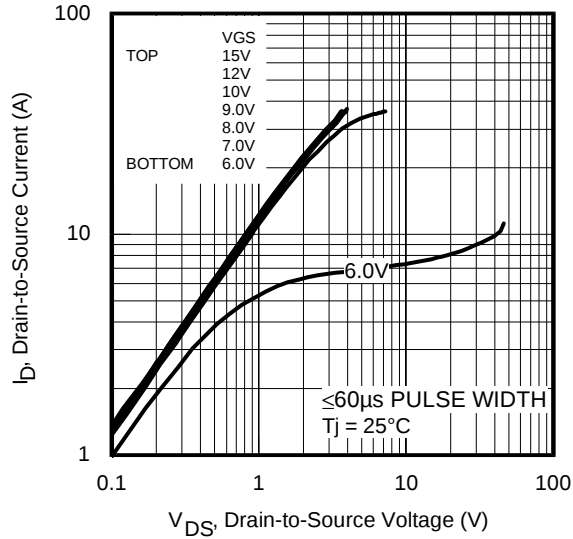


Fig 1. Typical Output Characteristics

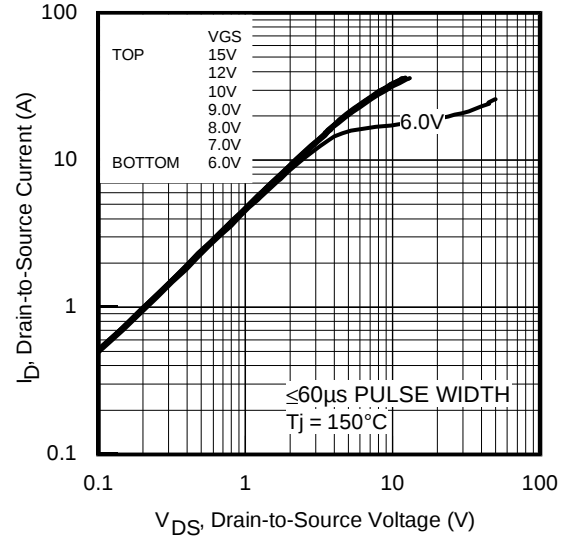


Fig 2. Typical Output Characteristics

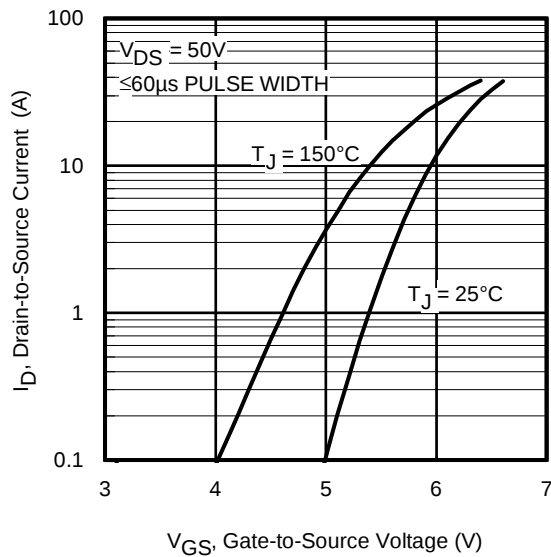


Fig 3. Typical Transfer Characteristics

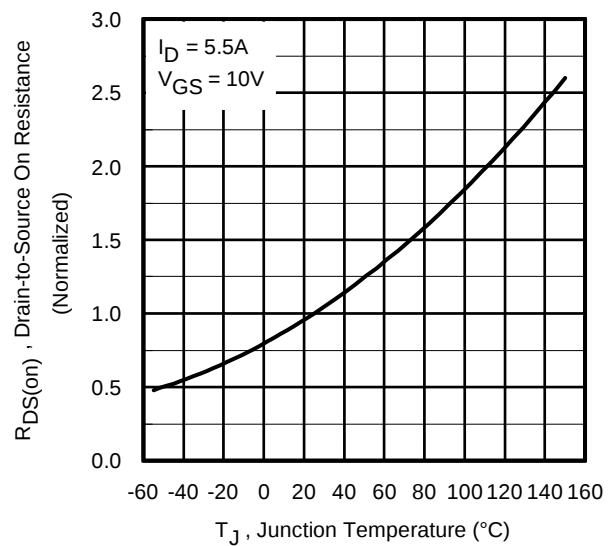


Fig 4. Normalized On-Resistance vs. Temperature

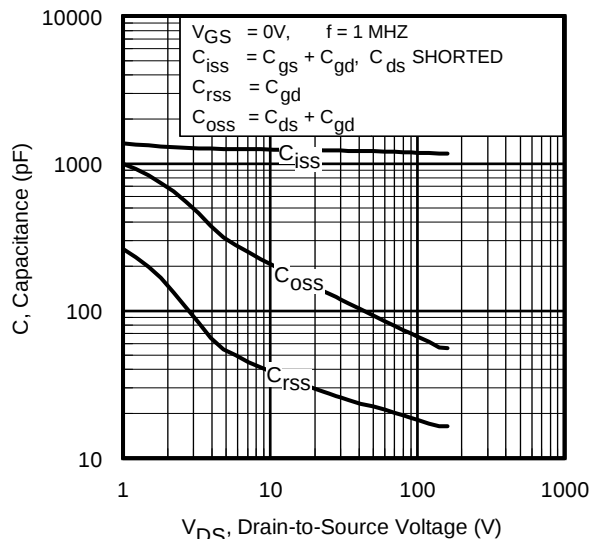


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
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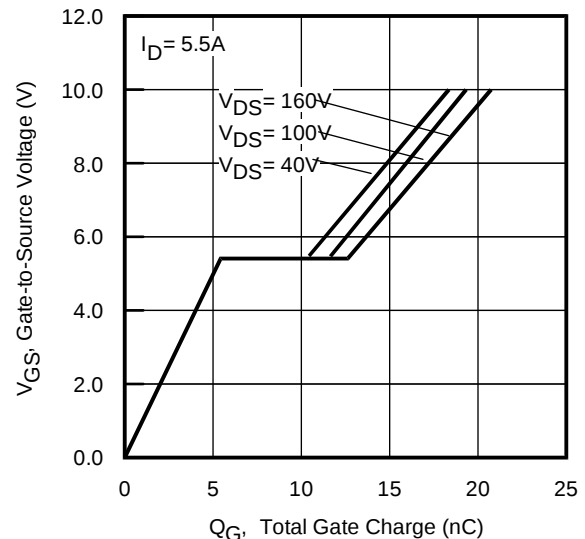
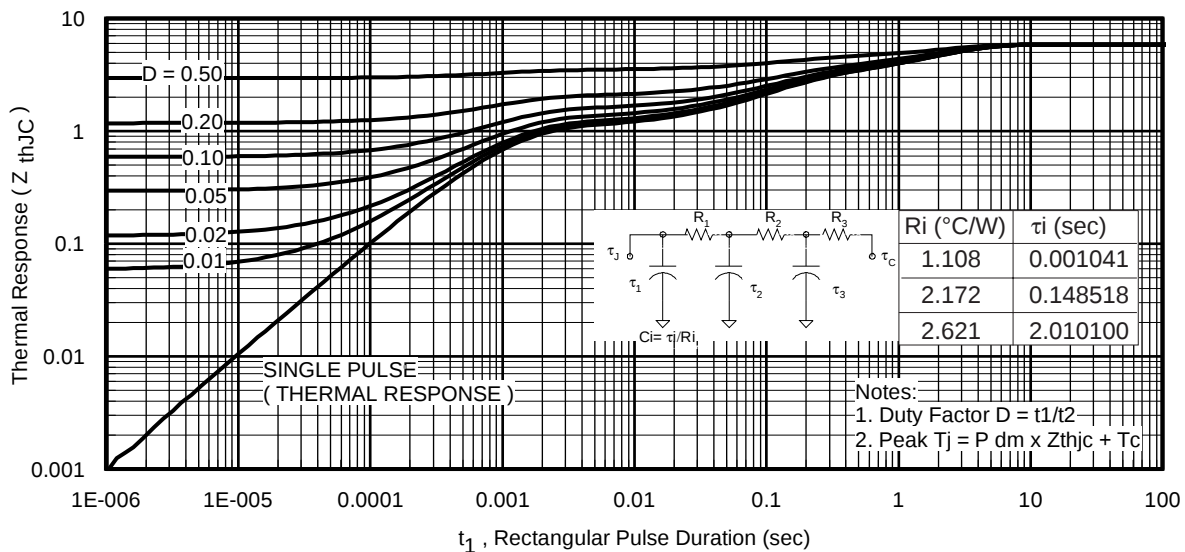
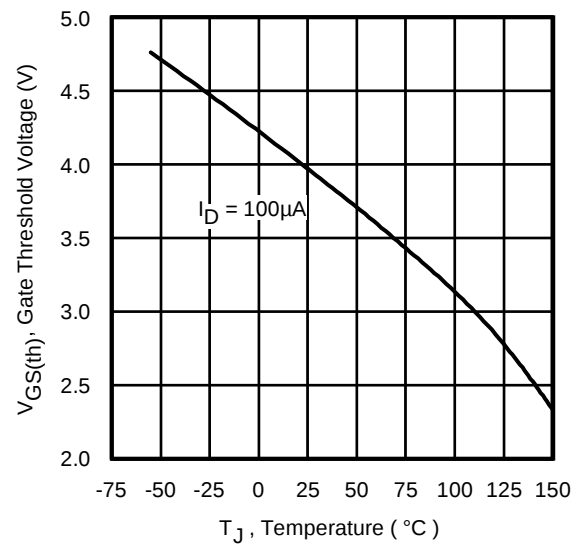
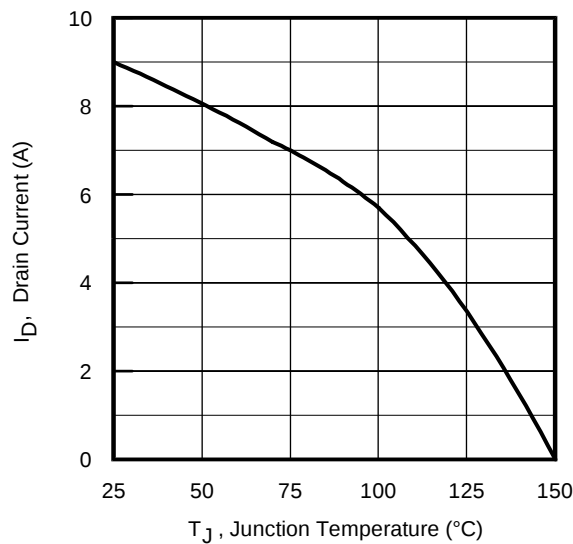
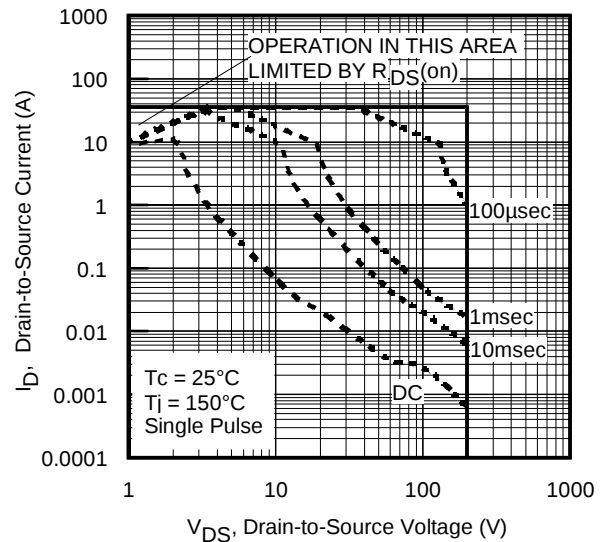
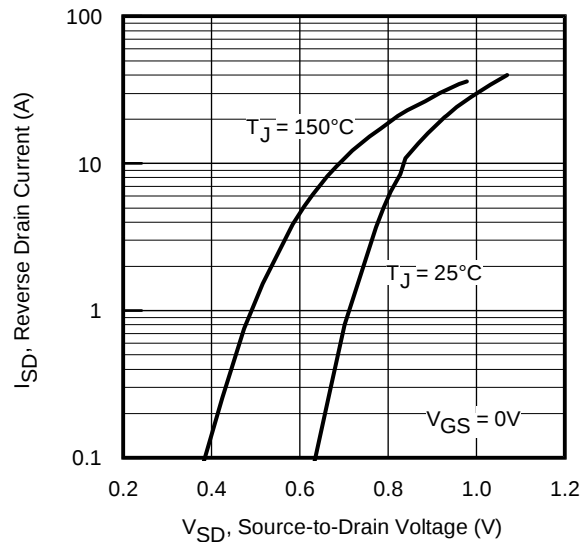


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



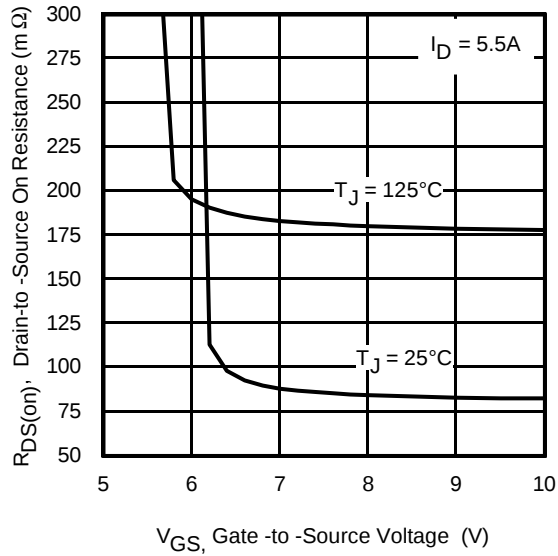


Fig 12. On-Resistance vs. Gate Voltage

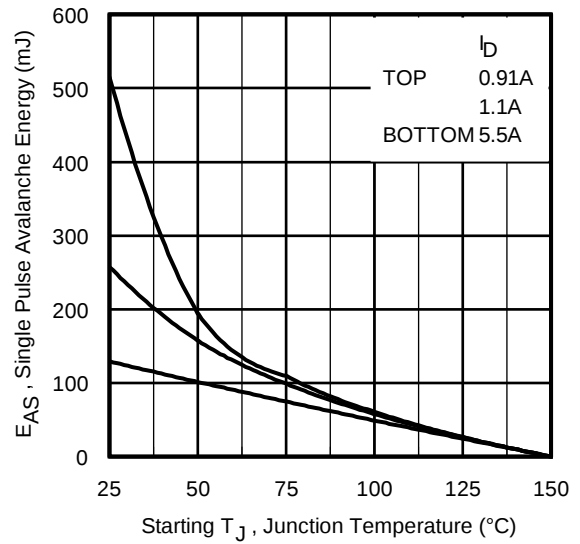


Fig 13a. Maximum Avalanche Energy vs. Drain Current

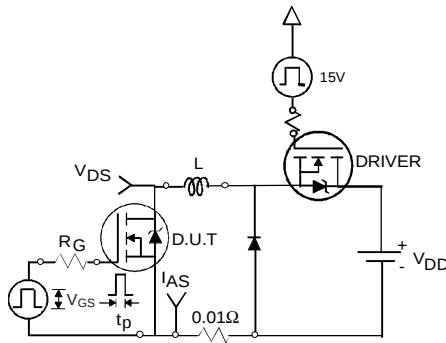


Fig 13b. Unclamped Inductive Test Circuit

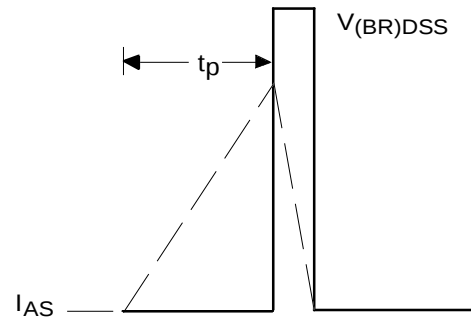


Fig 13c. Unclamped Inductive Waveforms

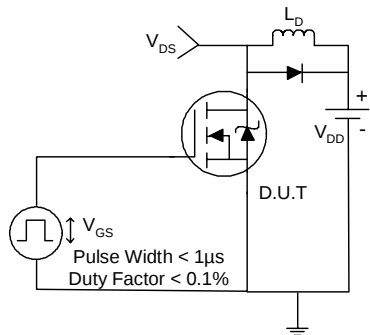


Fig 14a. Switching Time Test Circuit

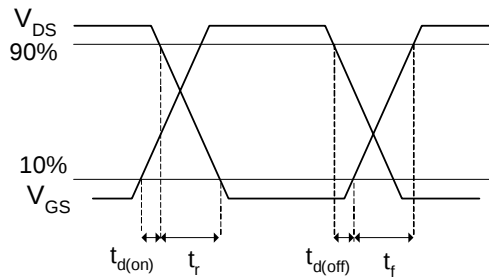


Fig 14b. Switching Time Waveforms

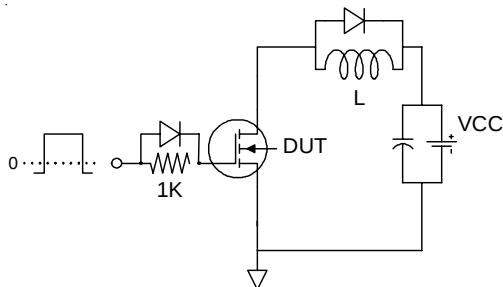


Fig 15a. Gate Charge Test Circuit

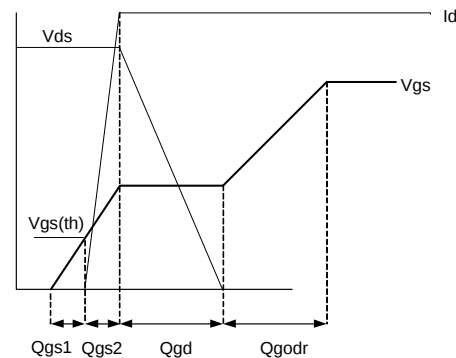
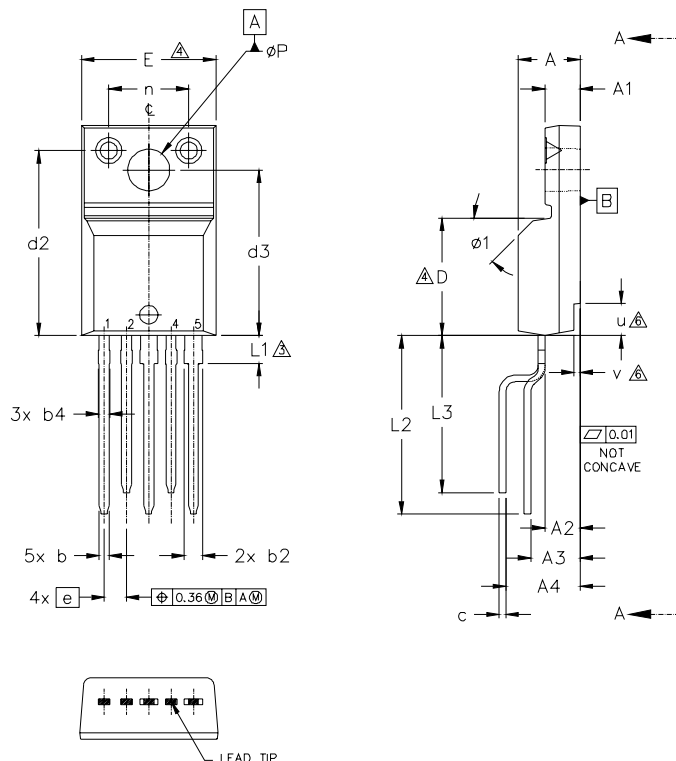


Fig 15b Gate Charge Waveform

IRFI4020H-117P

TO-220 Full-Pak 5-Pin Package Outline, Lead-Form Option 117

(Dimensions are shown in millimeters (inches))



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.83	.101	.111	
A2	2.51	2.85	.099	.112	
A3	3.73	4.24	.147	.167	
A4	5.79	6.29	.228	.248	
b	0.61	0.95	0.24	.037	
b1	0.56	0.90	.022	0.35	5
b2	1.13	1.48	0.44	.058	
b3	1.08	1.43	0.42	.056	5
b4	0.76	1.06	.030	.042	
b5	0.71	1.01	.028	.040	5
c	0.33	0.63	.013	.025	
c1	0.28	0.58	.011	.023	5
D	8.65	9.80	.341	.386	4
d1	15.80	16.12	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.92	.484	.509	
E	9.63	10.63	.379	.419	4

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
	e	1.70 BSC		.067 BSC	
L	13.20	13.73	.520	.541	3
L1	1.91	2.31	.075	.091	
L2	12.7	13.46	.500	.530	
L3	10.92	11.68	.430	.460	
n	6.05	6.15	.238	.242	6
øP	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	
v	0.40	0.50	.016	.020	
ø1	—	45°	—	45°	

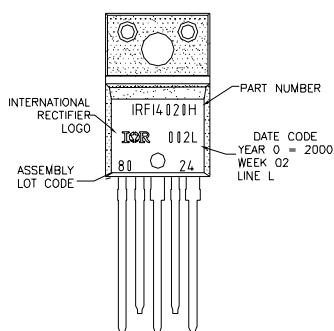
LEAD ASSIGNMENTS

- 1 - SOURCE 2
- 2 - GATE 2
- 3 - DRAIN 2 / SOURCE 1
- 4 - GATE 1
- 5 - DRAIN 1

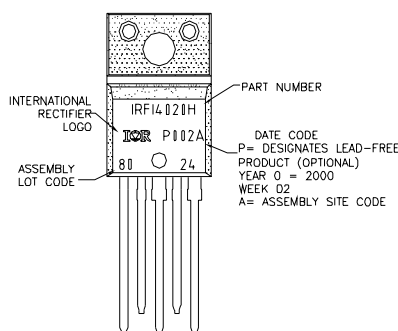
TO-220 Full-Pak 5-Pin Part Marking Information

EXAMPLE: THIS IS AN IRFI4020H WITH
LOT CODE 8024
ASSEMBLED ON WW02,2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead Free"



OR



TO-220AB Full-Pak 5-Pin package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed for the Consumer market.
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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