Ordering Options

SO-5 Package	Standard DIP	SO-8 Package
HCPL-M452	HCPL-4502	HCPL-0452
HCPL-M453	HCPL-4503	HCPL-0453

NOTE: These devices equivalent to 6N135/6N136 devices but without the base lead.

Ordering Information

HCPL-M452 and HCPL-M453 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Tape and Reel	Quantity
	RoHS Compliant	non-RoHS Compliant				
HCPL-M452	-000E	No option	SO-5	X		100 per tube
HCPL-M453	-500E	#500		X	X	1500 per tube

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-M452-500E to order product of SO-5 surface mount package in tape and reel packaging and RoHS compliant.

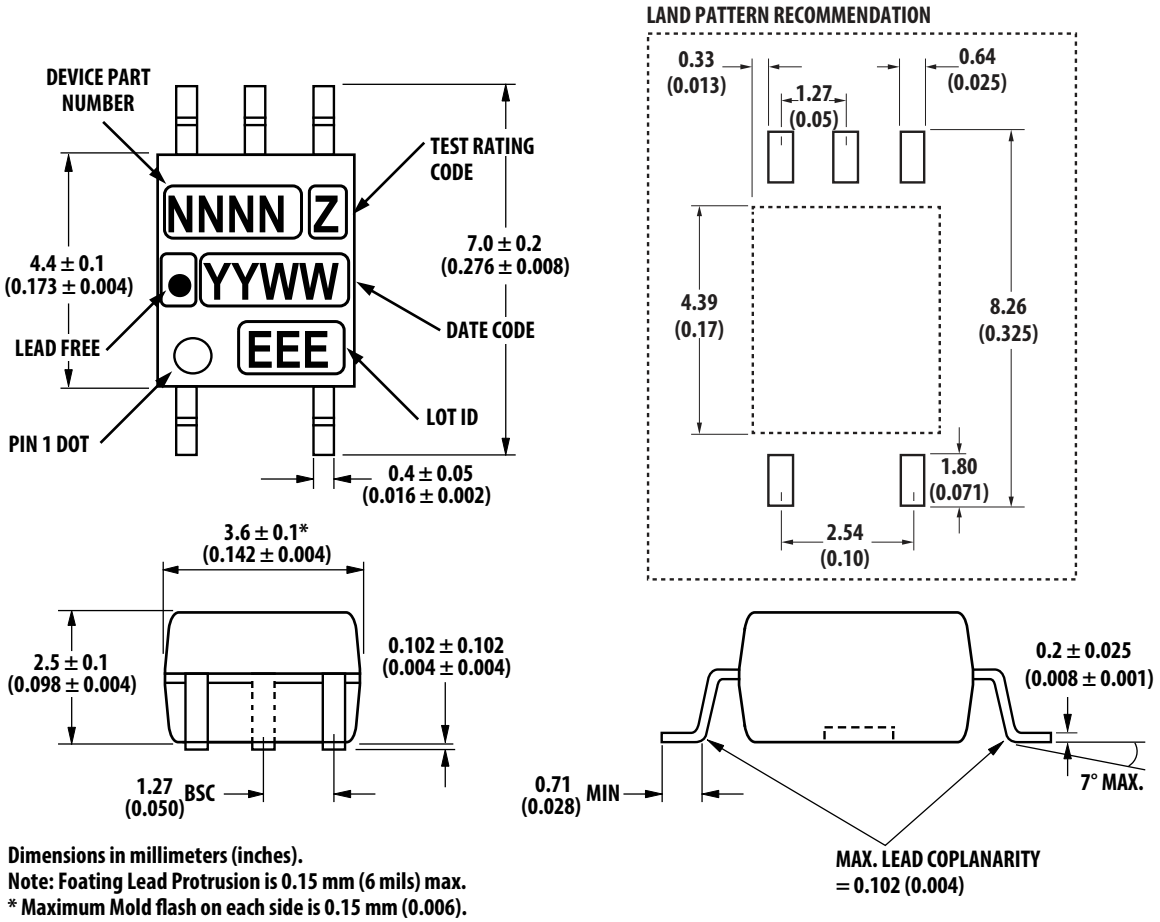
Example 2:

HCPL-M452 to order product of SO-5 surface mount package in tube packaging and non-RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information

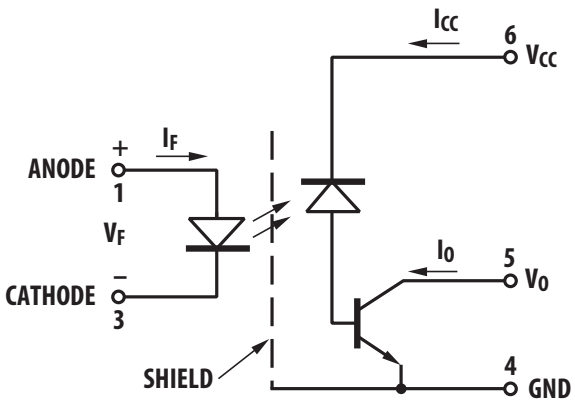
NOTE: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use ‘–XXXE.

Outline Drawing (JEDEC MO-155)

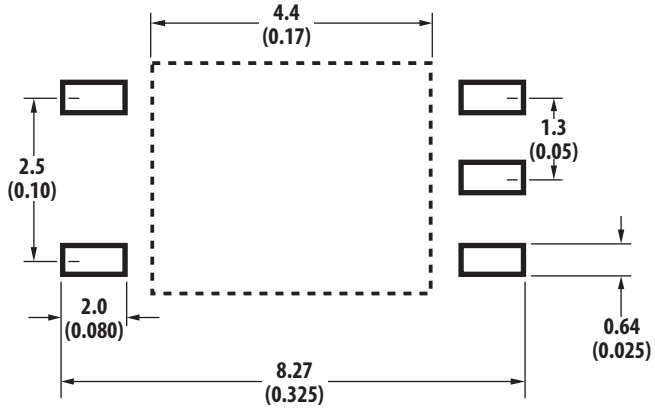


Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.
*** Maximum Mold flash on each side is 0.15 mm (0.006).**

Schematic

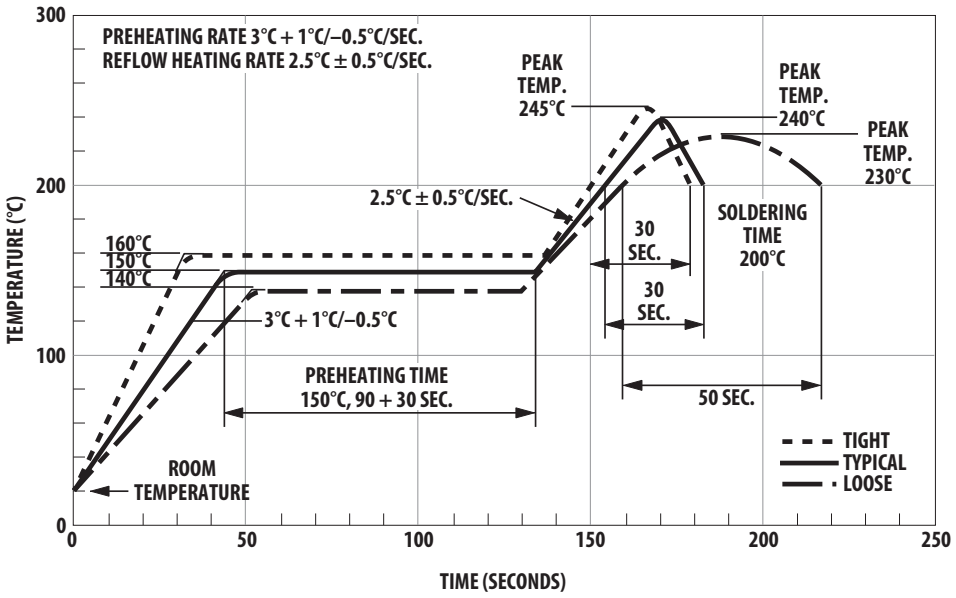


Land Pattern Recommendation



Dimensions in millimeters and (in.).

Solder Reflow Thermal Profile



NOTE: Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile

The recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Non-halide flux should be used.

Regulatory Information

The HCPL-M452/M453 are approved by the following organizations:

UL	Approved under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS} expected prior to product release.
CSA	Approved under CSA Component Acceptance Notice #5.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min External Air Gap (Clearance)	L(IO1)	≥ 5	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥ 5	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Absolute Maximum Ratings

No derating required up to 85°C.

Storage Temperature	–55°C to +125°C
Operating Temperature	–55°C to +100°C
Average Input Current – I_F	25 mA[a]
Peak Input Current – I_F	50 mA[b] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F	1.0A (1 µs pulse width, 300 pps)
Reverse Input Voltage – V_R (Pin3-1)	5V
Input Power Dissipation	45 mW[c]
Average Output Current – I_O (Pin 5)	8 mA
Peak Output Current	16 mA
Output Voltage – V_O (Pin 5-4)	–0.5V to 20V
Supply Voltage – V_{CC} (Pin 6-4)	–0.5V to 30V
Output Power Dissipation	100 mW[d]
Infrared and Vapor Phase Reflow Temperature	See below

a. Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C.

b. Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C.

c. Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C.

d. Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

NOTE: Use of a 0.1-µF bypass capacitor connected between pins 4 and 6 is recommended.

Parameter	Symbol	Min.	Typ.[a]	Max.	Units	Test Conditions			Figure	Note
Current Transfer Ratio	CTR	20	24	50	%	T_A = 25°C	V_O = 0.4V	V_{CC} = 4.5V	1, 2, 4	b
		15	25	—			V_O = 0.5V	I_F = 16 mA		
Logic Low Output Voltage	V_{OL}	—	0.1	0.4	V	T_A = 25°C	I_O = 3.0 mA			
		—	—	0.5			I_O = 2.4 mA			
Logic High Output Current	I_{OH}	—	0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5V	I_F = 0 mA	7	
		—	0.01	1.0		T_A = 25°C	V_O = V_{CC} = 5.5V			
		—	—	50						
Logic Low Supply Current	I_{CCL}	—	50	200		I_F = 16 mA	V_o = Open	V_{CC} = 15V		c
Logic High Supply Current	I_{CCH}	—	0.02	1		T_A = 25°C	I_F = 0 mA	V_{CC} = 15V		c
		—	0.02	2			V_O = open			
Input Forward Voltage	V_F	—	1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
		—	1.5	1.8						
Input Reverse Breakdown Current	BV_R	5	—	—	V	I_R = 10 µA				
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.6	—	mV/°C	I_F = 16 mA				
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz	V_F = 0V			
Input-Output Insulation Voltage	V_{ISO}	3750	—	—	V_{RMS}		RH < 50% T_A = 25°C	t = 1 min		d, e
Resistance (Input-Output)	R_{I-O}	—	10^{12}	—	Ω	V_{I-O} = 500 Vdc				d
Capacitance (Input-Output)	C_{I-O}	—	0.6	—	pF	f = 1 MHz				d

a. All typicals at T_A = 25°C.

b. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.

c. Use of a 0.1-µF bypass capacitor connected between pins 4 and 6 is recommended.

d. Device considered a two-terminal device: Pins 1 and 3 shorted together and Pins 4, 5 and 6 shorted together.

e. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, I_{i-e} ≤ 5 µA).

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) V_{CC} = 5V, I_F = 16 mA unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.[a]	Max.	Units	Test Conditions			Figure	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		—	0.2	0.8	µs	T_A = 25°C	R_l = 1.9kΩ		5., 6, 10	b
			—	0.2	1.0						
Propagation Delay Time to Logic High at Output	t_{PLH}		—	0.6	0.8		T_A = 25°C	R_l = 1.9kΩ		5, 6, 10	b
			—	0.6	1.0						
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	HCPL-M452	—	1	—	kV/µs		V_{CM} = 10 V_{P-P}	I_F = 0 mA T_A = 25°C R_L = 1.9 kΩ	11	b, c
		HCPL-M453	15	30	—			V_{CM} = 1500 V_{P-P}			
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	HCPL-M452	—	1	—			V_{CM} = 10 V_{P-P}	I_F = 16 mA T_A = 25°C R_L = 1.9 kΩ	11	b, c
		HCPL-M433	15	30	—		T_A = 25°C	V_{CM} = 1500 V_{P-P}			
Bandwidth	BW		—	3	—	MHz		R_L = 100 kΩ See Test Circuit		8, 9	d

a. All typicals at T_A = 25°C.

b. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.

c. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (that is, V_O > 2.0V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, VCM to assure that the output will remain in a Logic Low state (that is, V_O < 0.8V).

d. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.

Figure 1: dc and Pulsed Transfer Characteristics

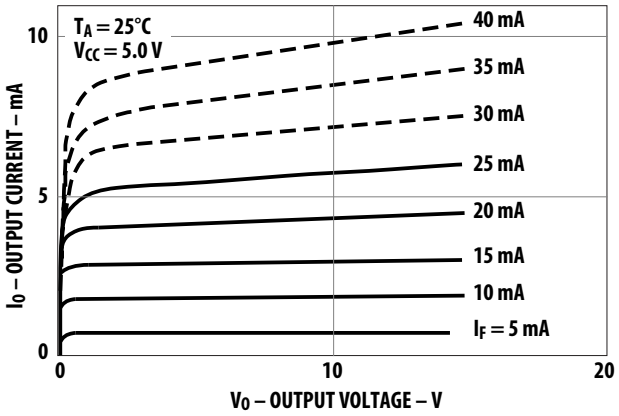


Figure 2: Current Transfer Ratio vs. Input Current

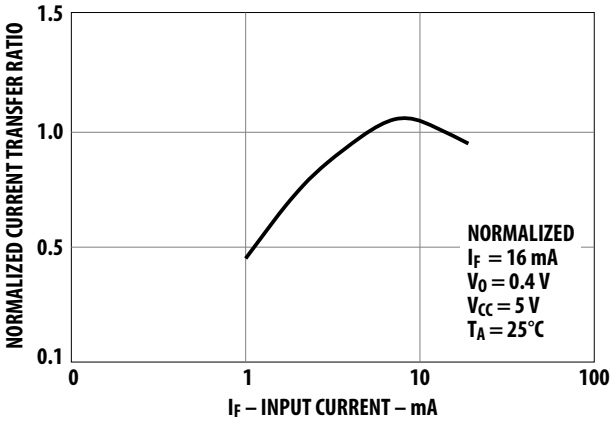


Figure 3: Input Current vs. Forward Voltage

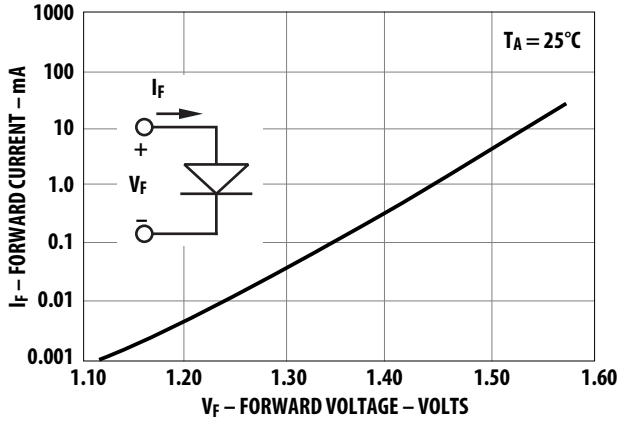


Figure 4: Current Transfer Ratio vs. Temperature

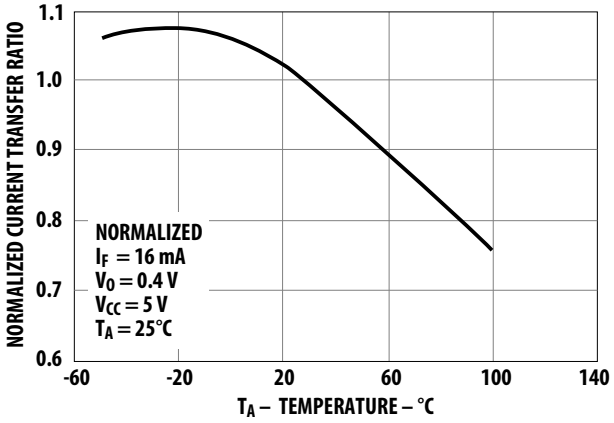


Figure 5: Propagation Delay vs. Temperature

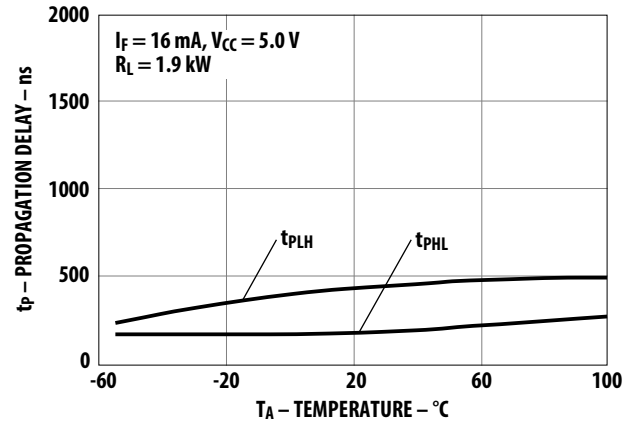


Figure 6: Propagation Delay Time vs. Load Resistance

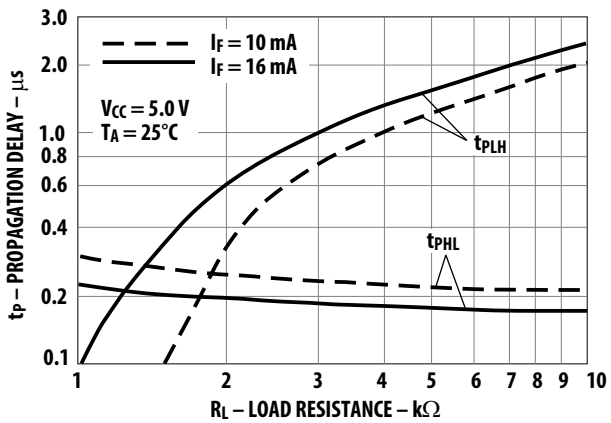


Figure 7: Logic High Output Current vs. Temperature

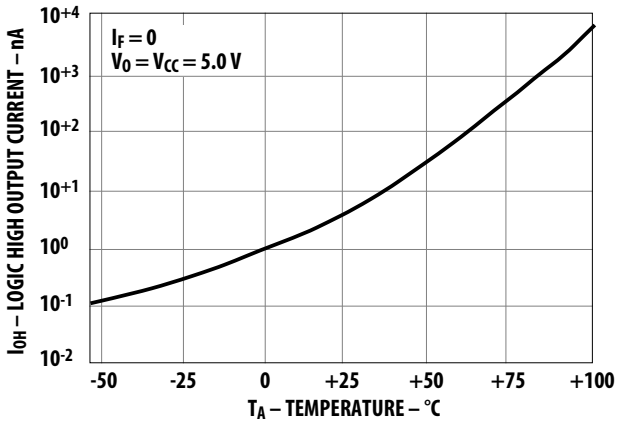


Figure 8: Small-Signal Current Transfer Ratio vs. Quiescent Input Current

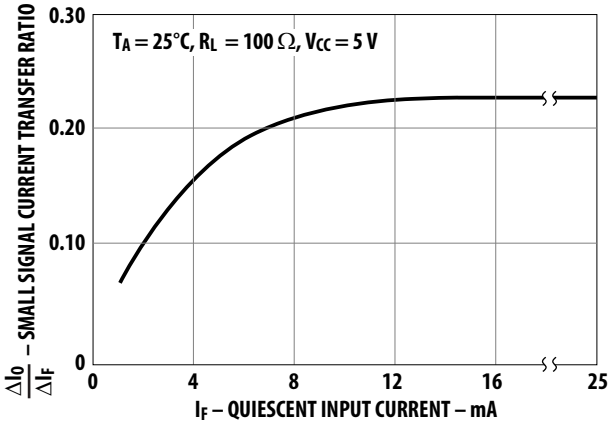
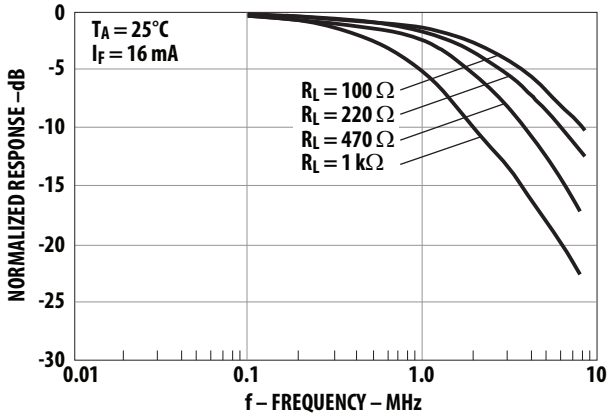


Figure 9: Frequency Response



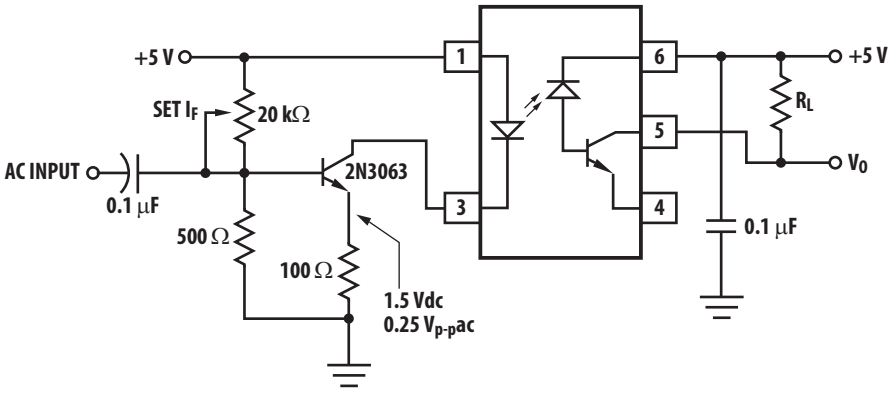


Figure 10: Switching Test Circuit

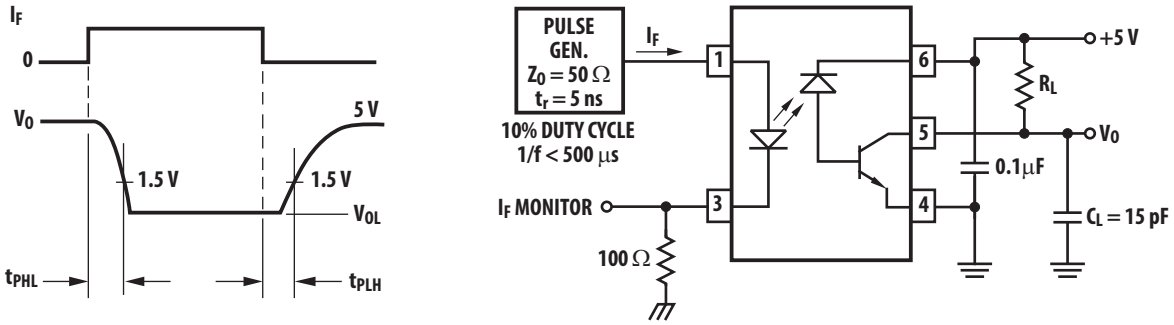
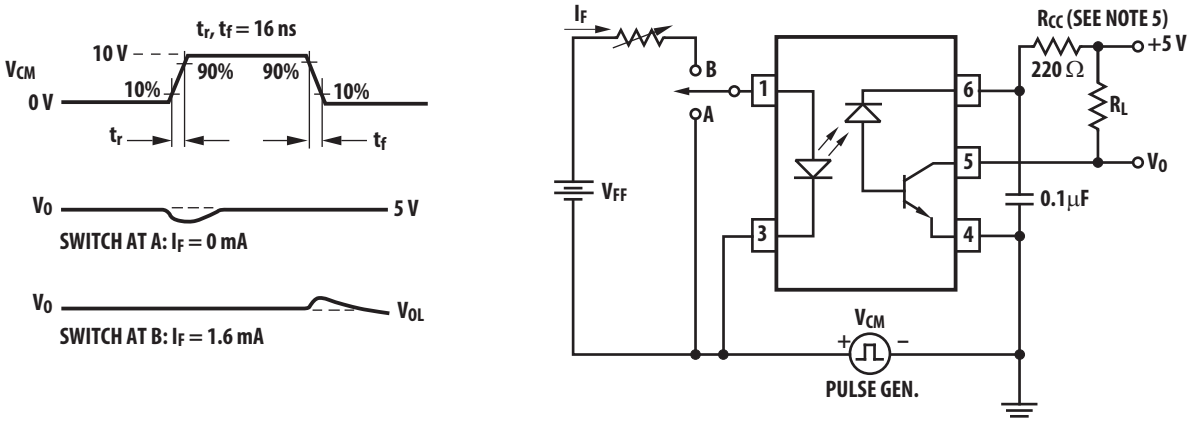


Figure 11: Test Circuit for Transient Immunity and Typical Waveforms



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