



ON Semiconductor®

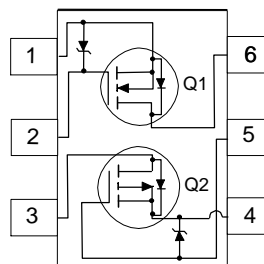
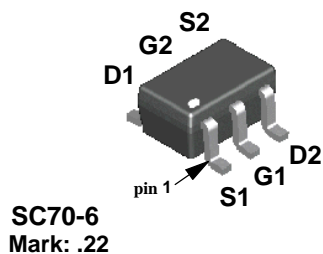
## FDG6322C Dual N & P Channel Digital FET

### General Description

These dual N & P-Channel logic level enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

### Features

- N-Ch 0.22 A, 25 V,  $R_{DS(ON)} = 4.0 \Omega @ V_{GS} = 4.5 \text{ V}$ ,  
 $R_{DS(ON)} = 5.0 \Omega @ V_{GS} = 2.7 \text{ V}$ .
- P-Ch -0.41 A, -25V,  $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 \text{ V}$ ,  
 $R_{DS(ON)} = 1.5 \Omega @ V_{GS} = -2.7 \text{ V}$ .
- Very small package outline SC70-6.
- Very low level gate drive requirements allowing direct operation in 3 V circuits ( $V_{GS(th)} < 1.5 \text{ V}$ ).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DS}$	Drain-Source Voltage	25	-25	V
$V_{GS}$	Gate-Source Voltage	8	-8	V
$I_D$	Drain Current - Continuous	0.22	-0.41	A
	- Pulsed	0.65	-1.2	
$P_D$	Maximum Power Dissipation (Note 1)	0.3		W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6		kV

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note1)	415	$^\circ\text{C/W}$
-----------------	---	-----	--------------------

**DMOS Electrical Characteristics** ( $T_A = 25\text{ }^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units	
OFF CHARACTERISTICS								
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	25			V	
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	P-Ch	-25				
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25 °C	N-Ch		25		mV/°C	
		I <sub>D</sub> = -250 μA, Referenced to 25 °C	P-Ch		-22			
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	N-Ch			1	μA	
						10		
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C	P-Ch			-1	μA	
						-10		
I <sub>GSS</sub>	Gate - Body Leakage Current	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V	N-Ch			100	nA	
		V <sub>GS</sub> = -8 V, V <sub>DS</sub> = 0 V	P-Ch			-100	nA	
ON CHARACTERISTICS (Note 2)								
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.65	0.85	1.5	V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.65	-0.82	-1.5		
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25 °C	N-Ch		-2.1		mV/°C	
		I <sub>D</sub> = -250 μA, Referenced to 25 °C	P-Ch		2.1			
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.22 A T <sub>J</sub> =125°C	N-Ch		2.6	4	Ω	
					5.3	7		
		V <sub>GS</sub> = 2.7 V, I <sub>D</sub> = 0.19 A			3.7	5		
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.41 A T <sub>J</sub> =125°C	P-Ch		0.85	1.1		
					1.2	1.9		
		V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = -0.25 A			1.15	1.5		
I <sub>D(ON)</sub>	On-State Drain Current	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V	N-Ch	0.22			A	
		V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> = -5 V	P-Ch	-0.41				
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 0.22 A	N-Ch		0.2		S	
		V <sub>DS</sub> = -5 V, I <sub>D</sub> = -0.5 A	P-Ch		0.9			
DYNAMIC CHARACTERISTICS								
C <sub>iss</sub>	Input Capacitance	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch		9.5		pF	
			P-Ch		62			
C <sub>oss</sub>	Output Capacitance		P-Channel f = 1.0 MHz	N-Ch		6		
				P-Ch		34		
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	N-Ch		1.3			
			P-Ch		10			

## Electrical Characteristics (continued)

### SWITCHING CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	N-Channel $V_{DS} = 5\text{ V}$ , $I_D = 0.5\text{ A}$ ,	N-Ch		5	10	nS
		$V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 50\ \Omega$	P-Ch		7	15	
$t_r$	Turn - On Rise Time	$V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 50\ \Omega$	N-Ch		4.5	10	nS
			P-Ch		8	16	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel $V_{DS} = -5\text{ V}$ , $I_D = -0.5\text{ A}$ ,	N-Ch		4	8	nS
		$V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 50\ \Omega$	P-Ch		55	80	
$t_f$	Turn - Off Fall Time	$V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 50\ \Omega$	N-Ch		3.2	7	nS
			P-Ch		35	60	
$Q_g$	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}$ , $I_D = 0.22\text{ A}$ ,	N-Ch		0.29	0.4	nC
		$V_{GS} = 4.5\text{ V}$	P-Ch		1.1	1.5	
$Q_{gs}$	Gate-Source Charge	P-Channel $V_{DS} = -5\text{ V}$ , $I_D = -0.41\text{ A}$ ,	N-Ch		0.12		nC
		$V_{GS} = -4.5\text{ V}$	P-Ch		0.31		
$Q_{gd}$	Gate-Drain Charge	$V_{DS} = -5\text{ V}$ , $I_D = -0.41\text{ A}$ , $V_{GS} = -4.5\text{ V}$	N-Ch		0.03		nC
			P-Ch		0.29		

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.25	A
			P-Ch			-0.25	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 0.5 A (Note 2)	N-Ch		0.8	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.5 A (Note 2)	P-Ch		-0.85	-1.2	

Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA} = 415^\circ\text{C/W}$  on minimum mounting pad on FR-4 board in still air.
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics: N-Channel

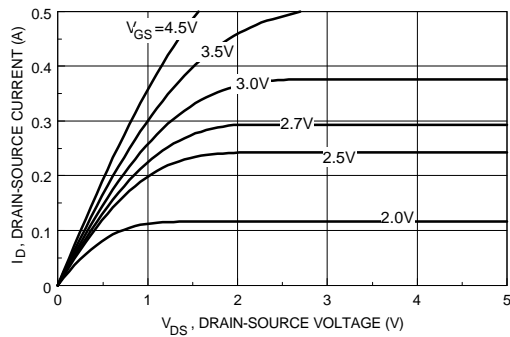


Figure 1. On-Region Characteristics.

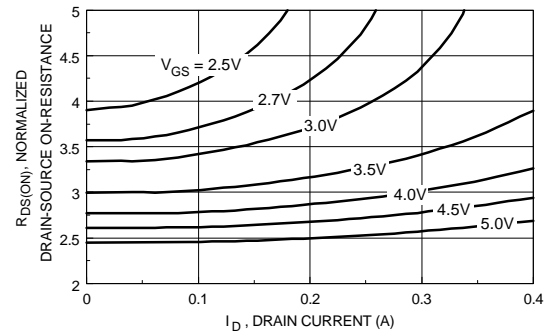


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

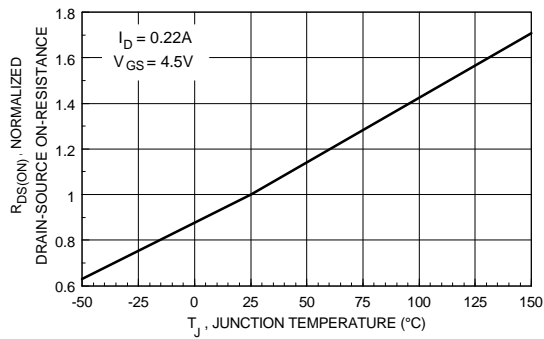


Figure 3. On-Resistance Variation with Temperature.

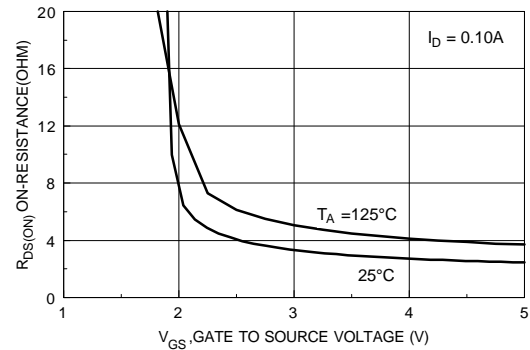


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

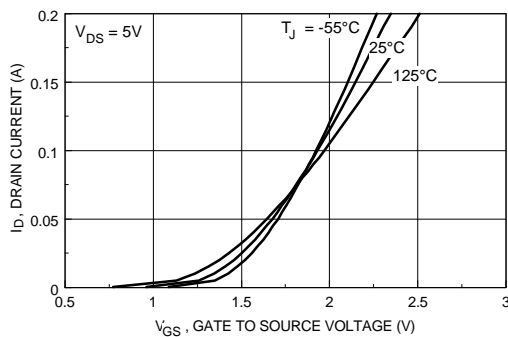


Figure 5. Transfer Characteristics.

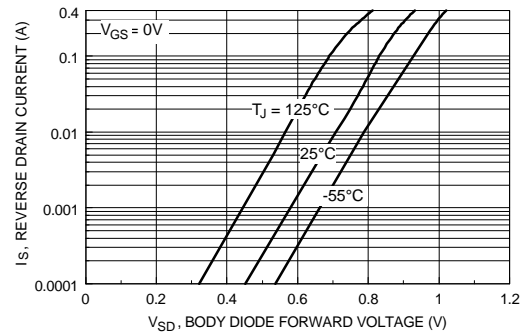


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics: N-Channel (continued)

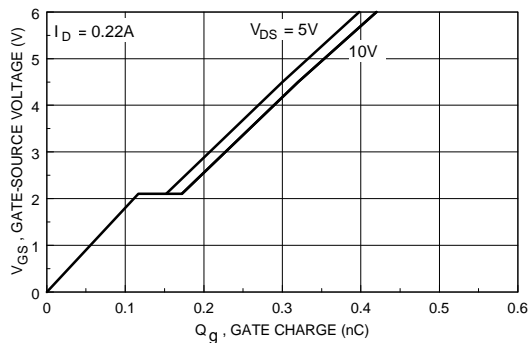


Figure 7. Gate Charge Characteristics.

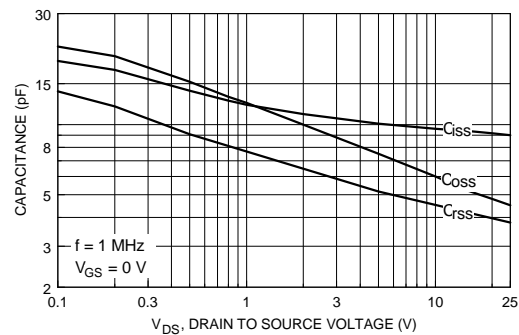


Figure 8. Capacitance Characteristics.

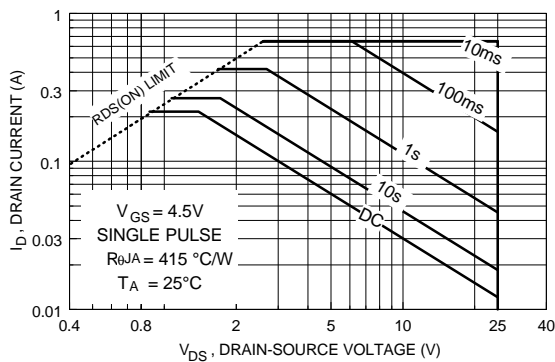


Figure 9. Maximum Safe Operating Area.

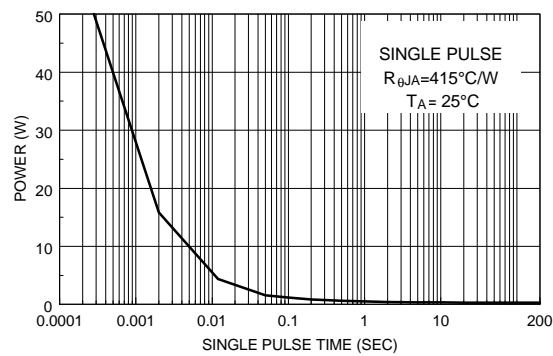


Figure 10. Single Pulse Maximum Power Dissipation.

## Typical Electrical Characteristics: P-Channel

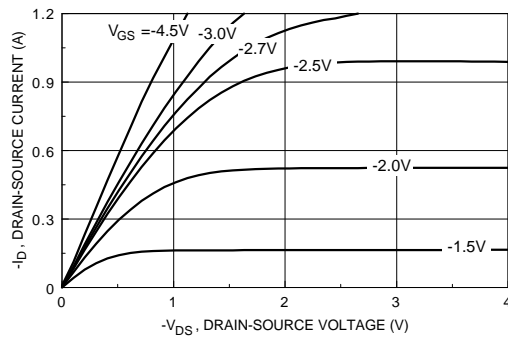


Figure 11. On-Region Characteristics.

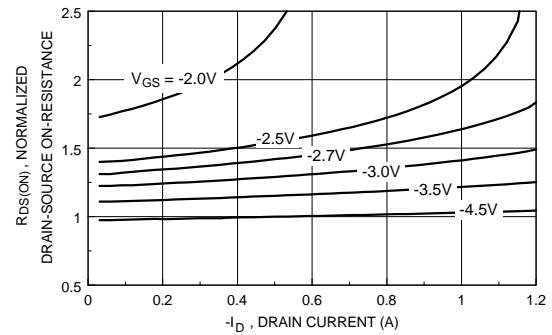


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

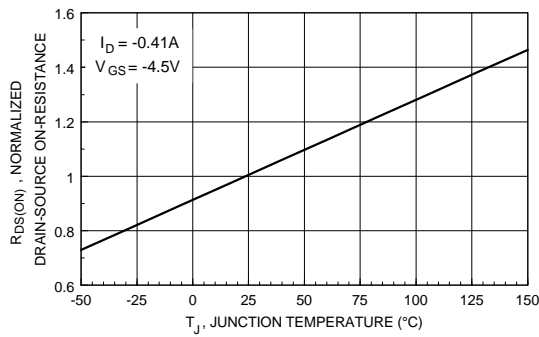


Figure 13. On-Resistance Variation with Temperature.

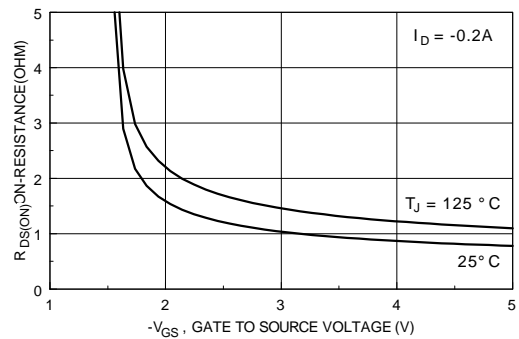


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

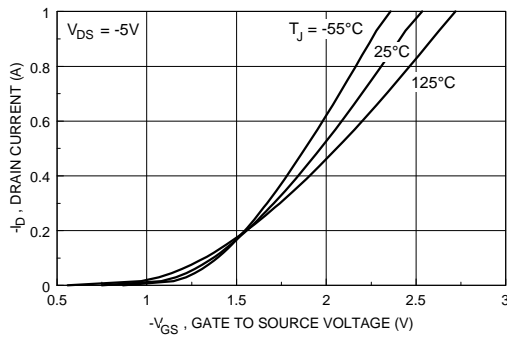


Figure 15. Transfer Characteristics.

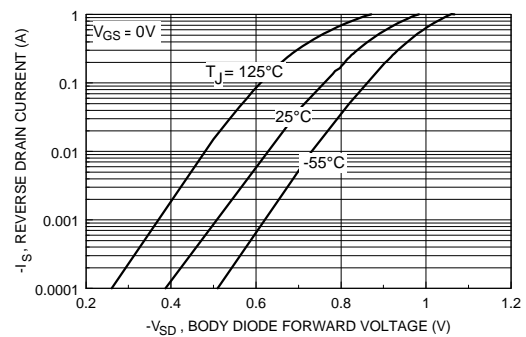


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

## 1 Typical Electrical Characteristics: P-Channel (continued)

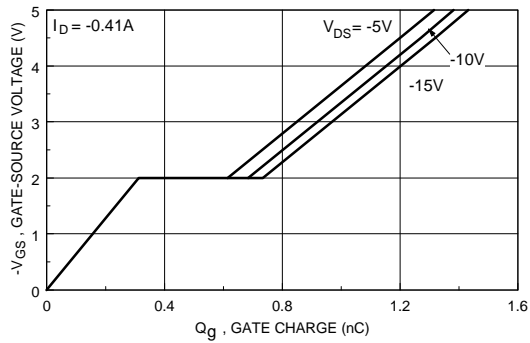


Figure 17. Gate Charge Characteristics.

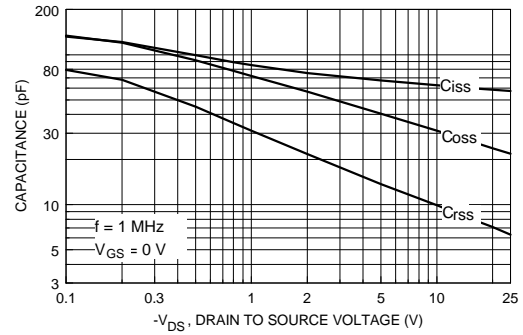


Figure 18. Capacitance Characteristics.

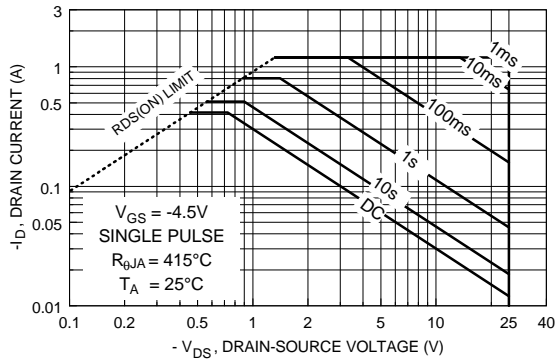


Figure 19. Maximum Safe Operating Area.

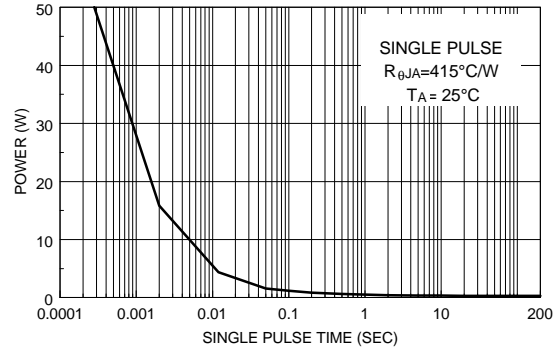
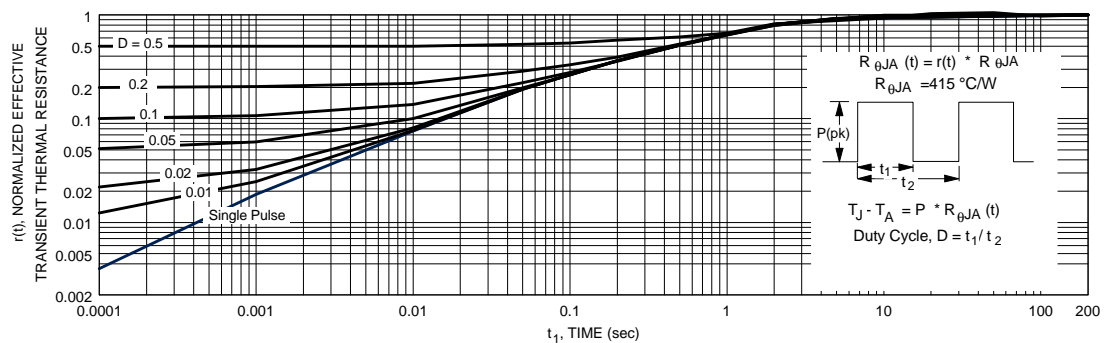


Figure 20. Single Pulse Maximum Power Dissipation.

## Typical Thermal Characteristics: N & P-Channel (continued)



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1.  
Transient thermal response will change depending on the circuit board design.



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative