FAIRCHILD
SEMICONDUCTOR®

November 2013

FCP7N60 / FCPF7N60

N-Channel SuperFET® MOSFET

600 V, 7 A, 600 mΩ

Features

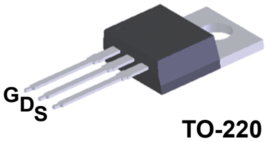
- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 530 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 23 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 60 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

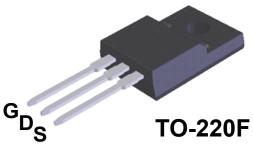
- LCD/LED/PDP TV
- Solar Inverter
- AC-DC Power Supply

Description

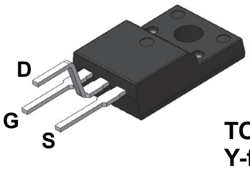
SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



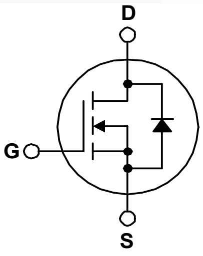
TO-220



TO-220F



TO-220F
Y-formed



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCP7N60	FCPF7N60 / FCPF7N60YDTU	Unit
V_{DSS}	Drain-Source Voltage		600		V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	7 4.4	7* 4.4*	A A
I_{DM}	Drain Current	- Pulsed (Note 1)	21	21*	A
V_{GSS}	Gate-Source voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		230		mJ
I_{AR}	Avalanche Current (Note 1)		7		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		8.3		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate Above 25°C	83 0.67	31 0.25	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP7N60	FCPF7N60 / FCPF7N60YDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.5	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP7N60	FCP7N60	TO220	Tube	N/A	N/A	50 units
FCPF7N60	FCPF7N60	TO220F	Tube	N/A	N/A	50 units
FCPF7N60YDTU	FCPF7N60	TO-220F (Y-formed)	Tube	N/A	N/A	50 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25°C	600	--	--	V
		V_{GS} = 0 V, I_D = 250 μA, T_J = 150°C	--	650	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 7 A	--	700	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V V_{DS} = 480 V, T_C = 125°C	-- --	-- --	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	--	0.53	0.6	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 3.5 A	--	6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	--	710	920	pF
C_{oss}	Output Capacitance		--	380	500	pF
C_{rss}	Reverse Transfer Capacitance		--	34	--	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	--	22	29	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	--	60	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 7 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	--	35	80	ns
t_r	Turn-On Rise Time		--	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	75	160	ns
t_f	Turn-Off Fall Time		--	32	75	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 7 A, V_{GS} = 10 V (Note 4)	--	23	30	nC
Q_{gs}	Gate-Source Charge		--	4.2	5.5	nC
Q_{gd}	Gate-Drain Charge		--	11.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 7 A, dI_F/dt =100 A/μs	--	360	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.5	--	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 3.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq$ 7 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

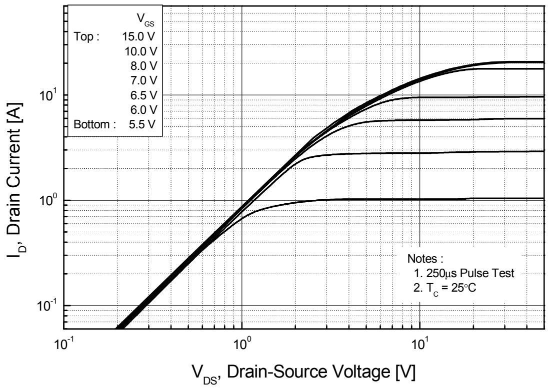


Figure 2. Transfer Characteristics

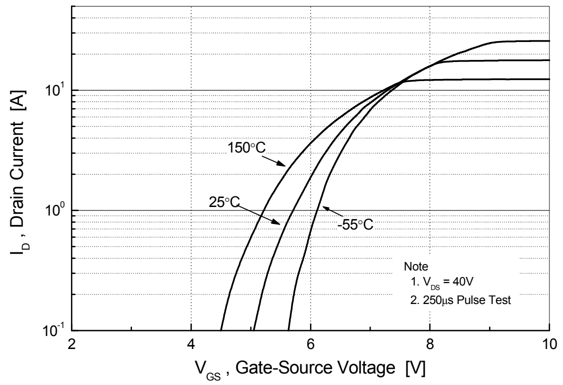


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

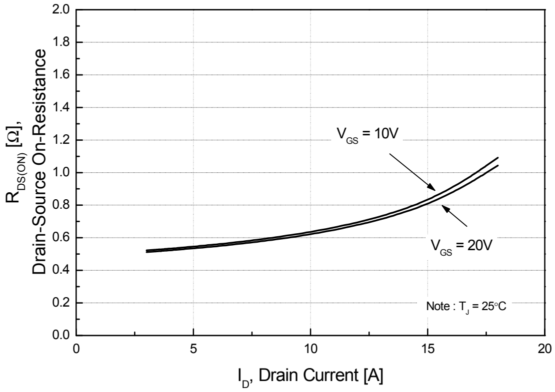


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

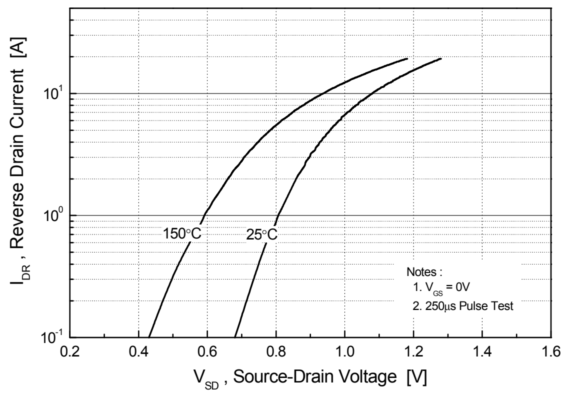


Figure 5. Capacitance Characteristics

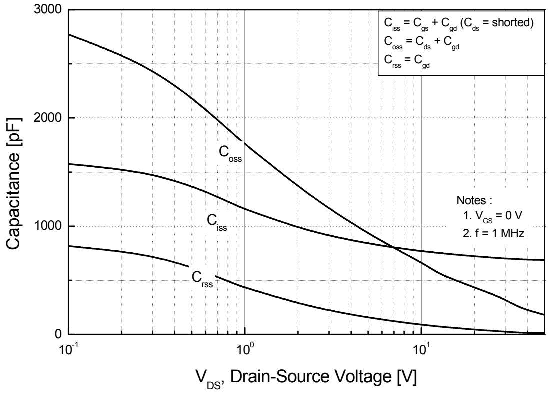
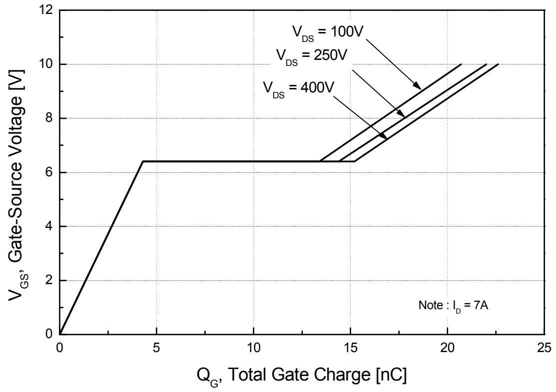


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

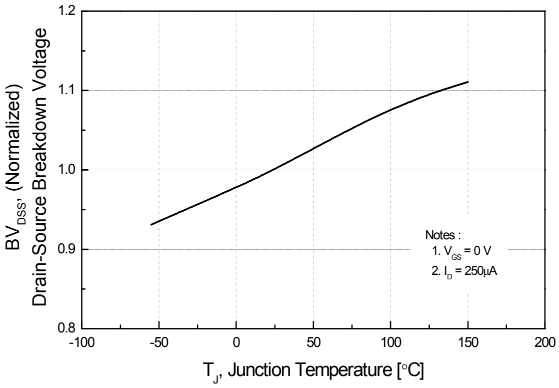


Figure 8. On-Resistance Variation vs. Temperature

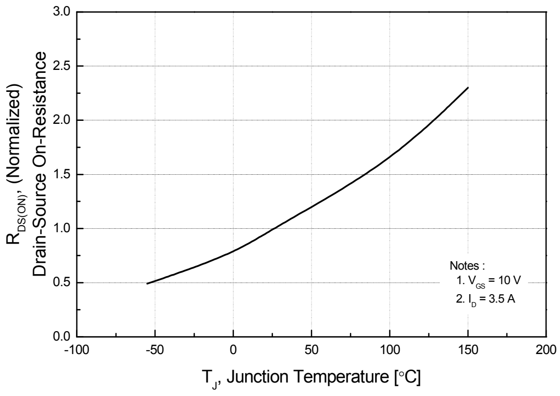


Figure 9-1. Maximum Safe Operating Area for FCP7N60

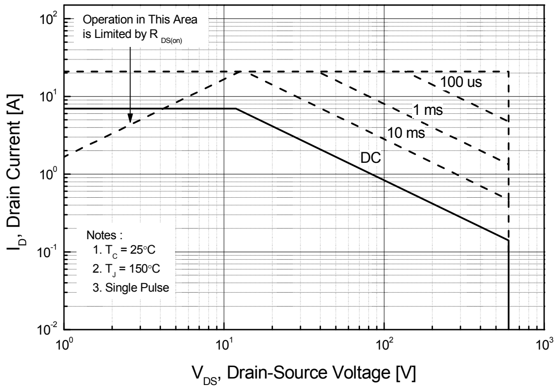


Figure 9-2. Maximum Safe Operating Area for FCPF7N60

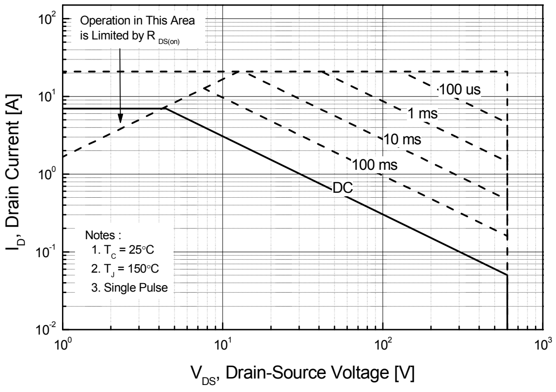
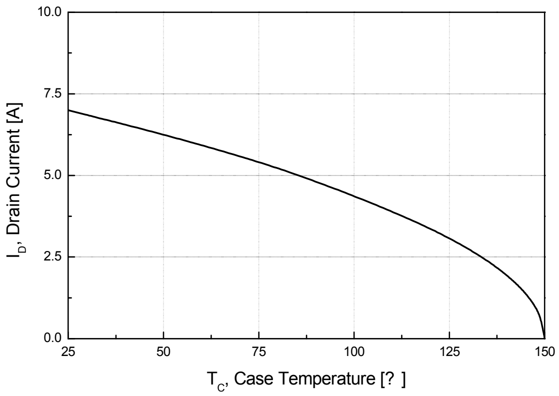
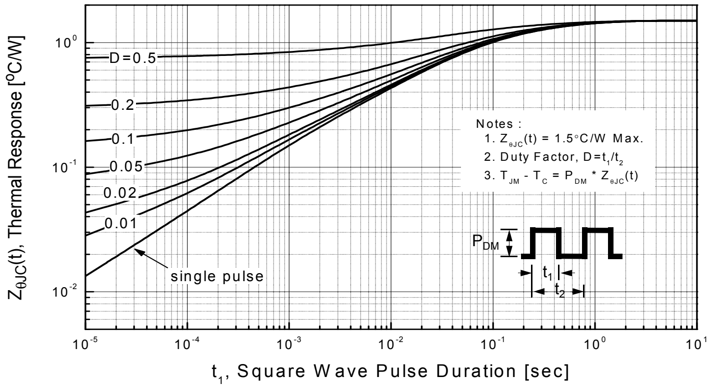


Figure 10. Maximum Drain Current vs. Case Temperature



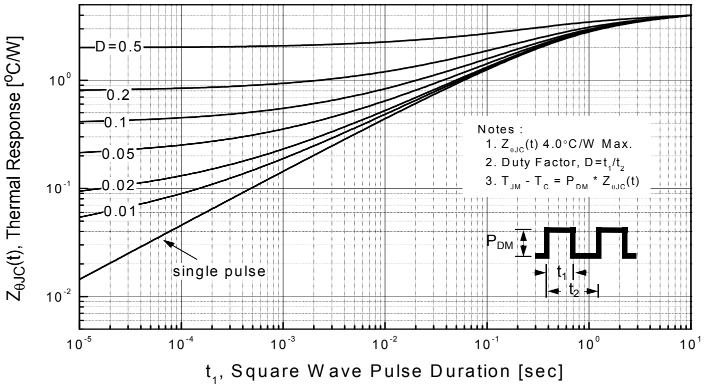
Typical Performance Characteristics (Continued)



Notes :

1. $Z_{\theta JC}(t) = 1.5°C/W$ Max.
2. Duty Factor, $D=t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 11-1. Transient Thermal Response Curve for FCP7N60



Notes :

1. $Z_{\theta JC}(t)$ 4.0°C/W Max.
2. Duty Factor, $D=t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 11-2. Transient Thermal Response Curve for FCPF7N60

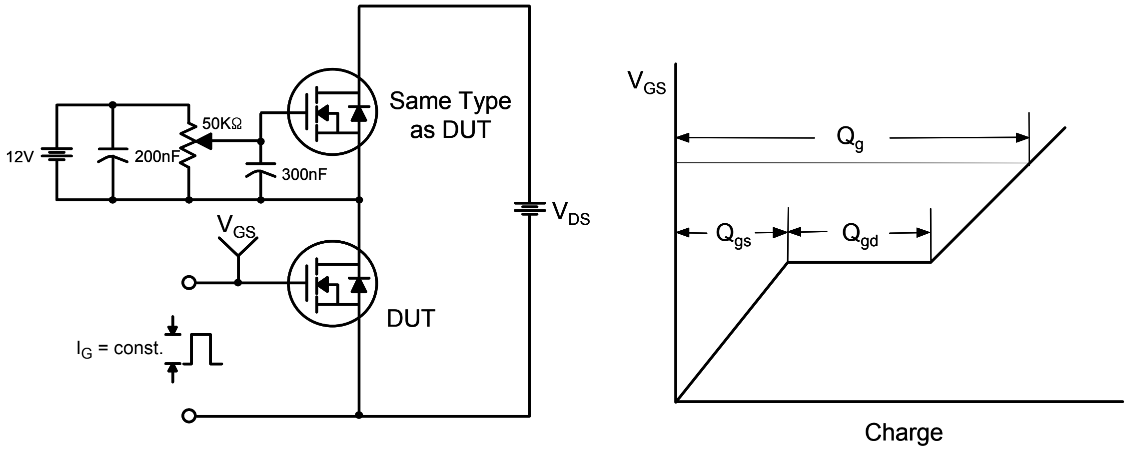


Figure 12. Gate Charge Test Circuit & Waveform

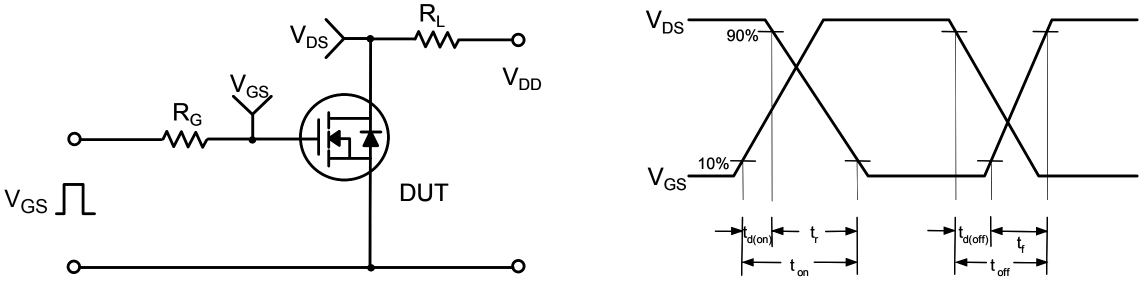


Figure 13. Resistive Switching Test Circuit & Waveforms

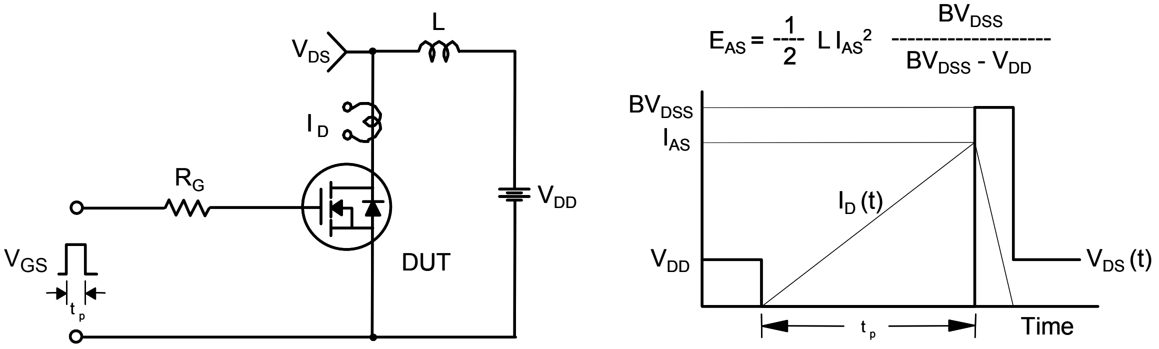


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

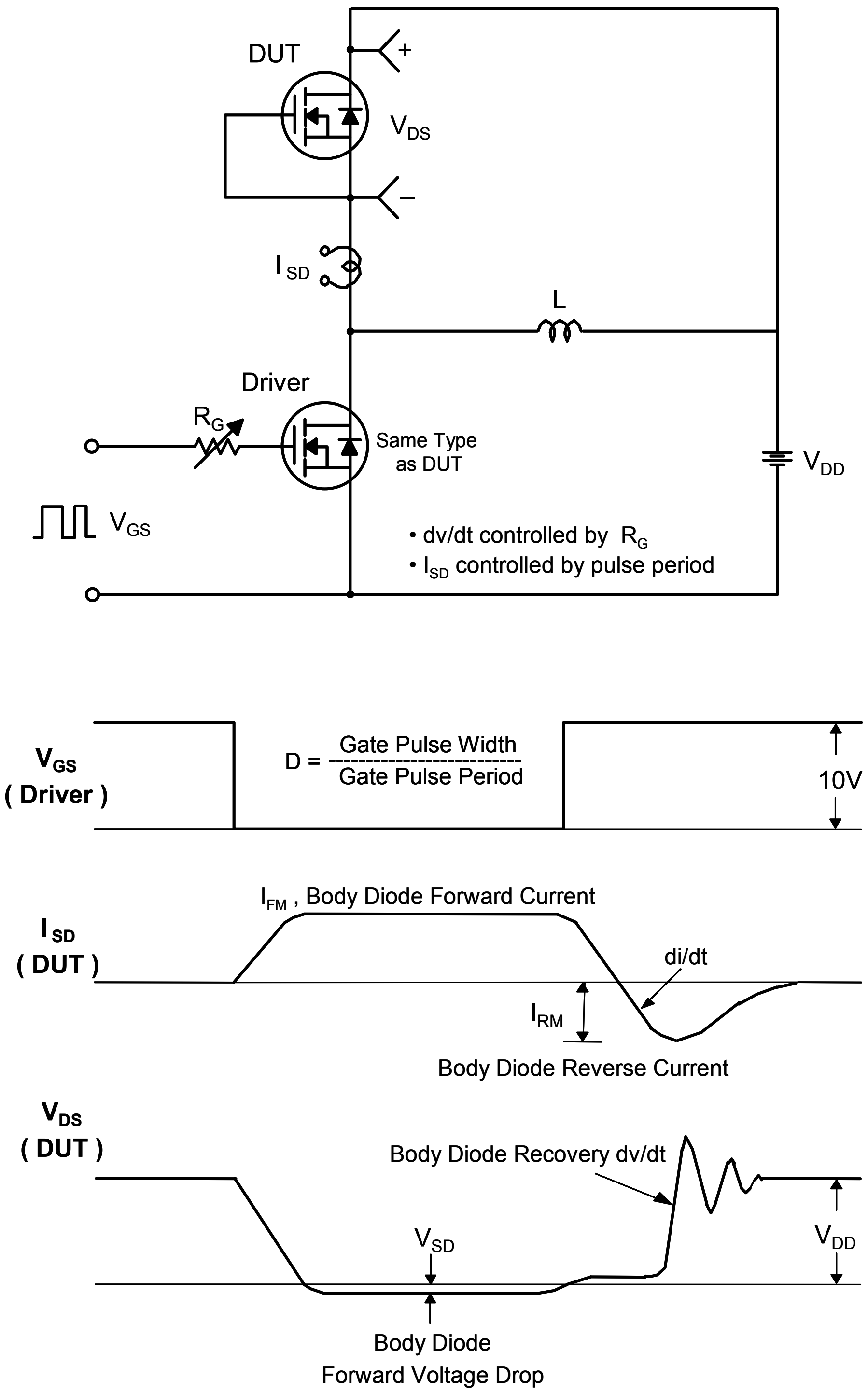
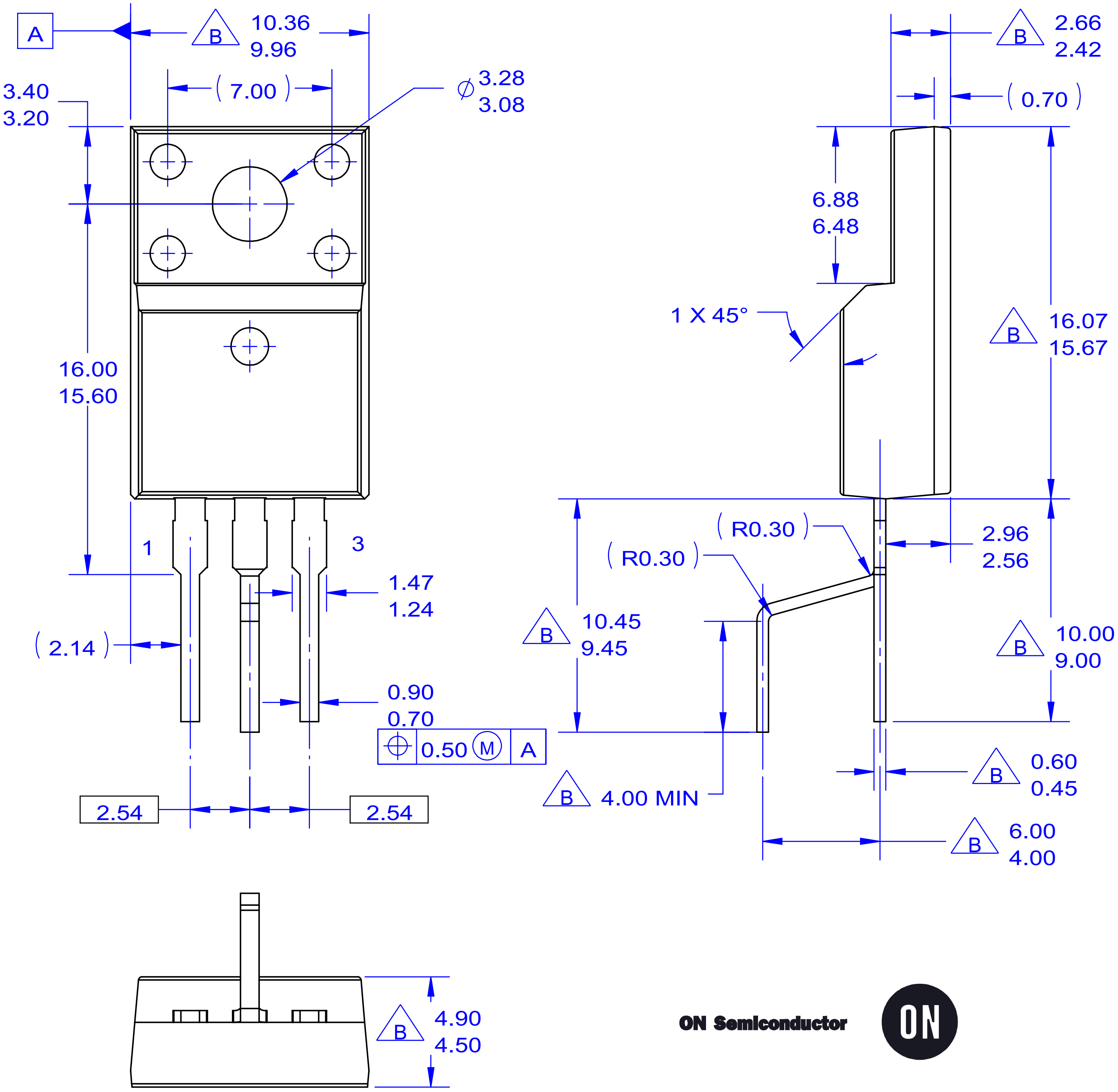


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO
EIAJ SC91A.

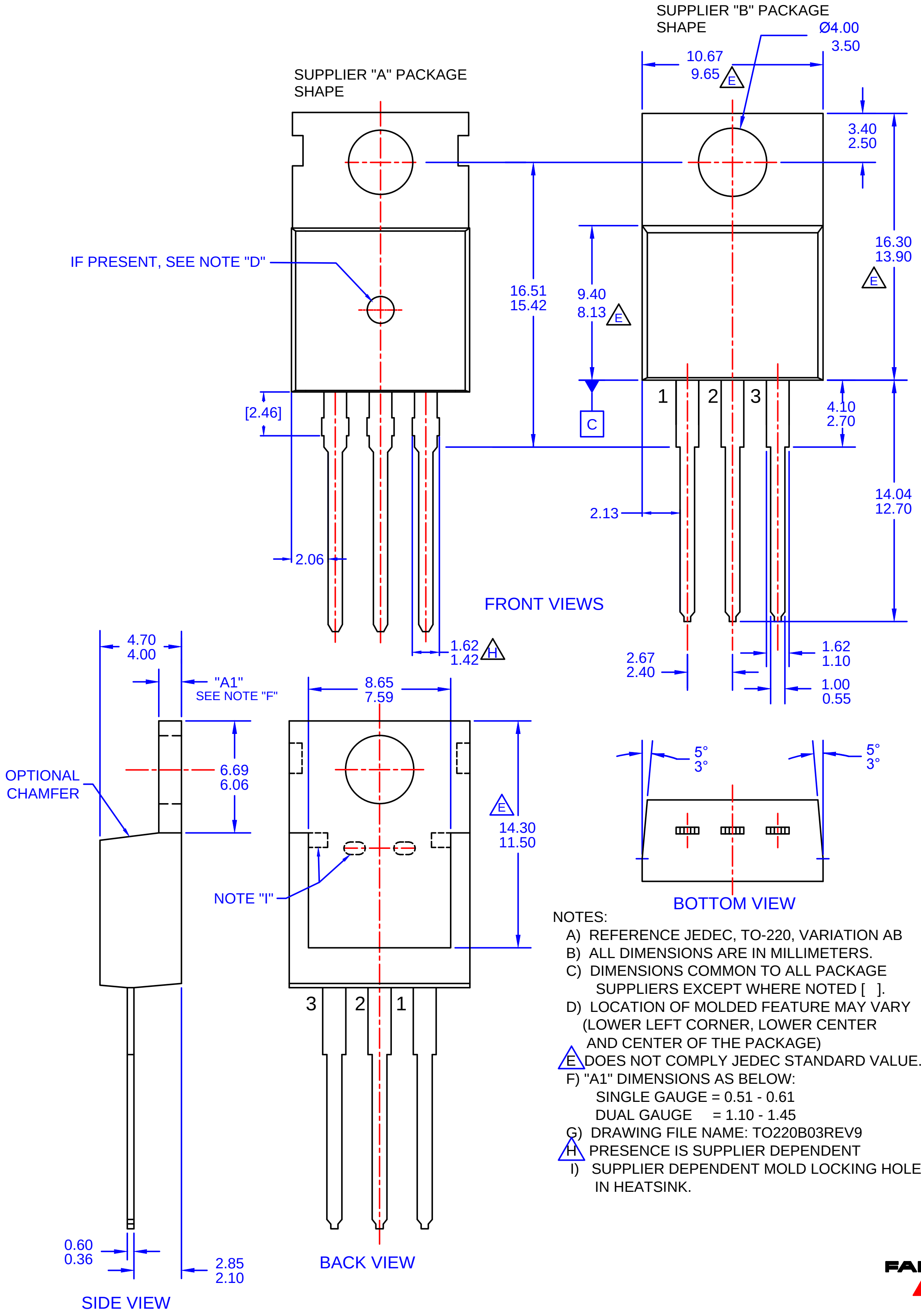
B DOES NOT COMPLY EIAJ STD. VALUE.

C. ALL DIMENSIONS ARE IN MILLIMETERS.

D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR PROTRUSIONS.

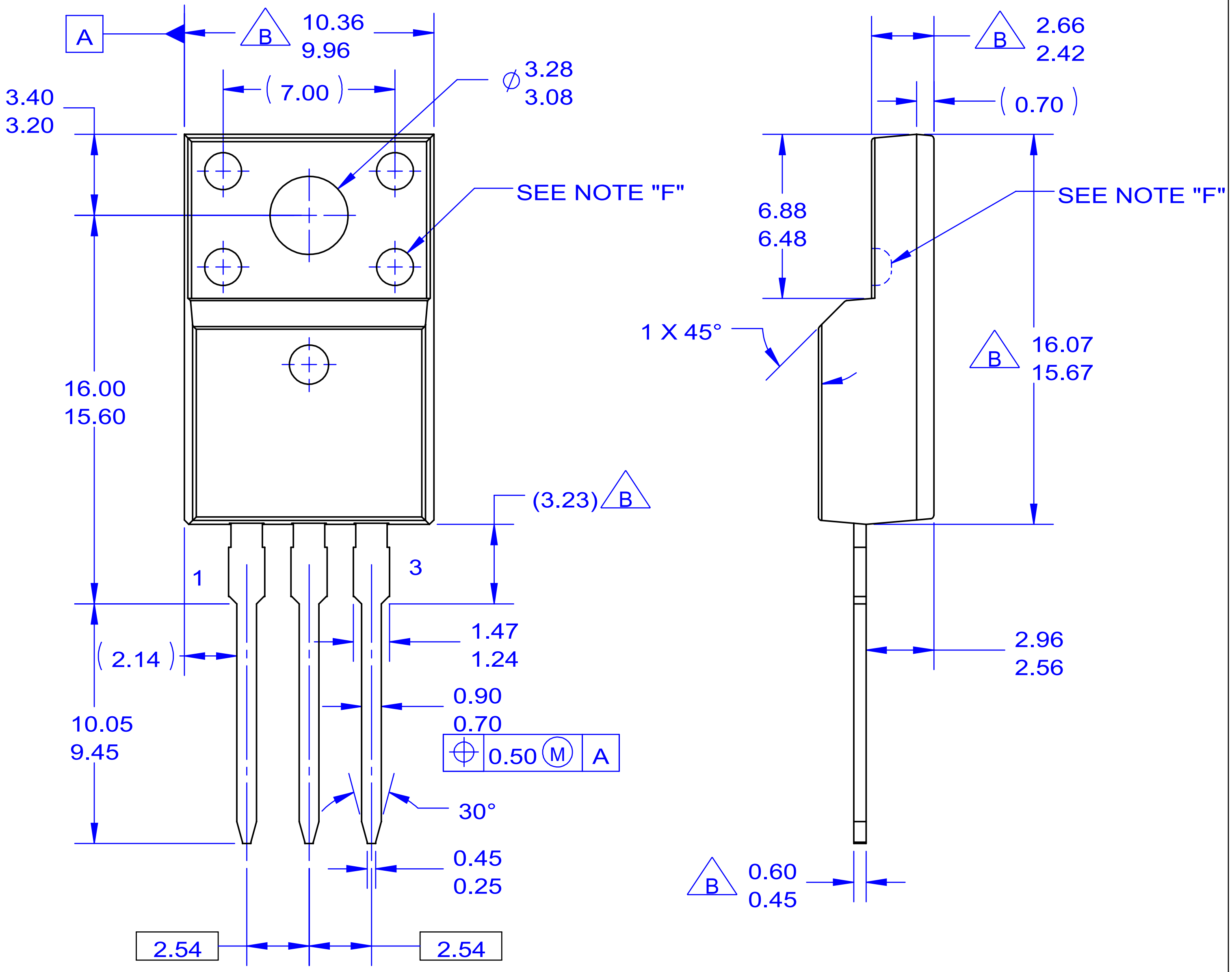
E. DIMENSION AND TOLERANCE AS PER ASME
Y14.5-1994.

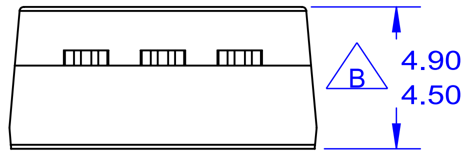
F. DRAWING FILE NAME: TO220Q03REV2



NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
    SINGLE GAUGE = 0.51 - 0.61
    DUAL GAUGE = 1.10 - 1.45
G) DRAWING FILE NAME: TO220B03REV9
△H PRESENCE IS SUPPLIER DEPENDENT
I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.





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NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV5

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