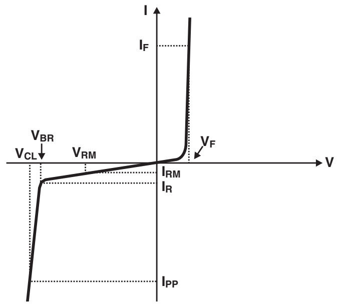
1 Characteristics

Table 1. Absolute ratings (limiting values at T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{PP}	**Internal pins** ESD discharge IEC 61000-4-2 air discharge ESD discharge IEC 61000-4-2 contact discharge **External pins and V_{CC}** ESD discharge IEC 61000-4-2 air discharge ESD discharge IEC 61000-4-2 contact discharge **All pins** MIL STD 883G - Method 3015-7 Class 3A (human body model)	 2 2 15 8 4	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	
V_{BR}	Breakdown voltage	
I_{RM}	Leakage current @ V_{RM}	
V_{RM}	Stand-off voltage	
V_{CL}	Clamping voltage	
I_{PP}	Peak pulse current	
$R_{I/O}$	Series resistance between input and output	
C_{line}	Input capacitance per line	

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6		7.9	V
I_{RM}	V_{RM} = 3 V			0.2	µA
R_1, R_3	Tolerance ± 20%		100		Ω
R_2	Tolerance ± 20%		47		Ω
C_{line}	V_R= 0 V, F = 1 MHz, V_{OSC} = 30 mV		17	20	pF

Figure 3. S21(db) attenuation (RST line)

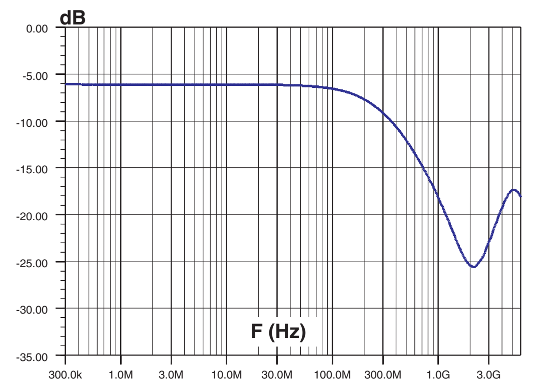


Figure 4. S21(db) attenuation (CLK line)

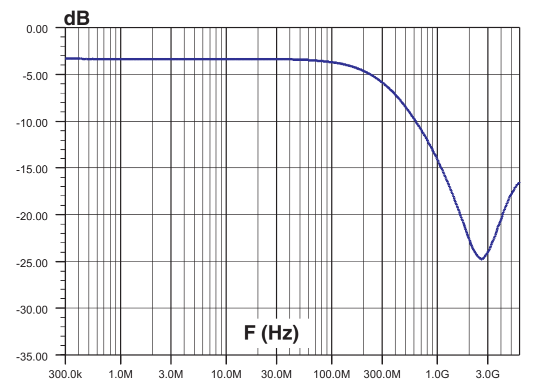


Figure 5. S21(db) attenuation (DATA line)

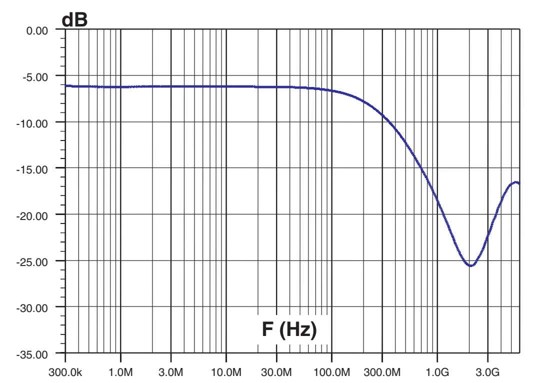


Figure 6. Analog cross talk measurements

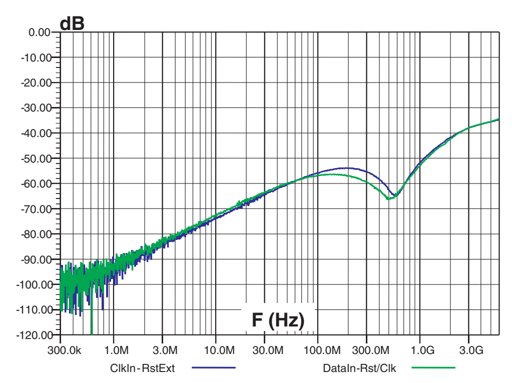


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) applied to external pin

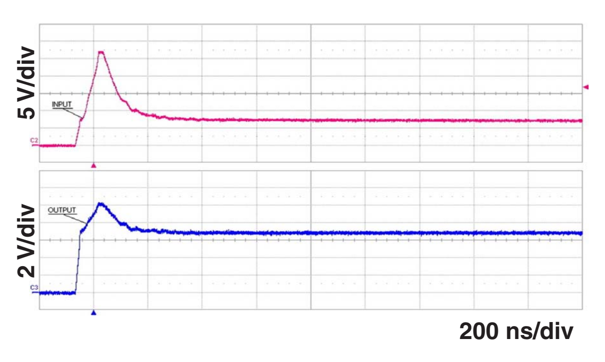


Figure 8. ESD response to IEC 61000-4-2 (-15 kV air discharge) applied to external pin

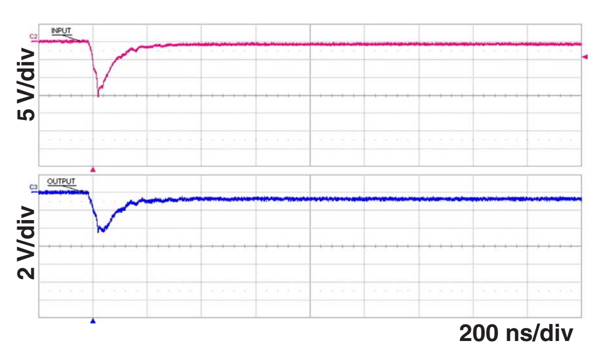


Figure 9. ESD response to IEC 61000-4-2 (+2 kV air discharge) applied to internal pin

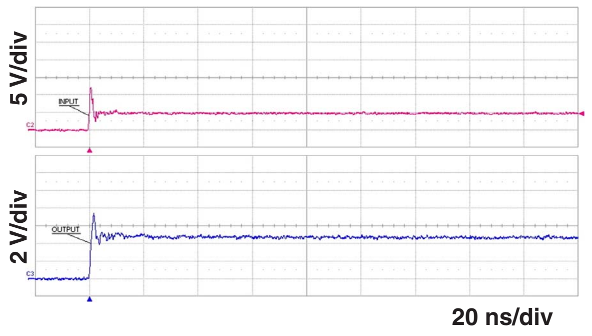
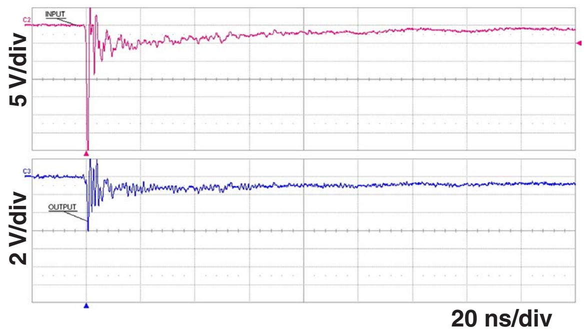
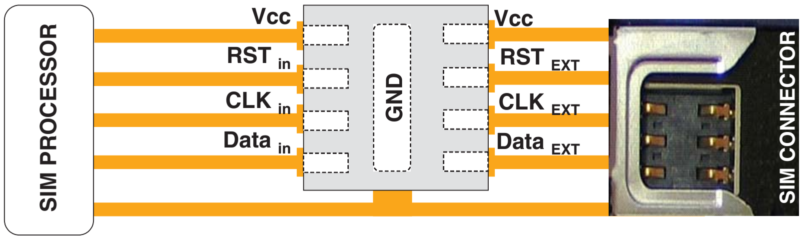


Figure 10. ESD response to IEC 61000-4-2 (-2 kV air discharge) applied to internal pin



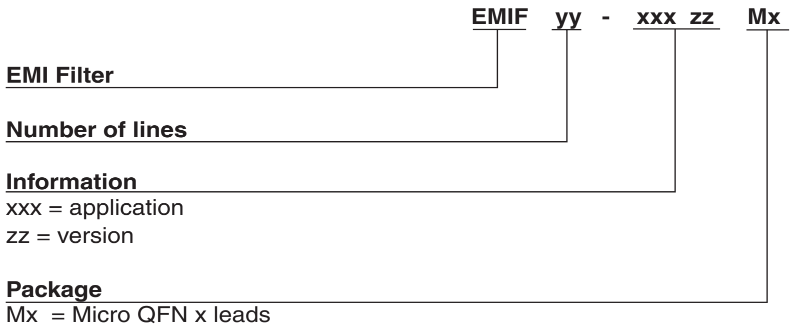
2 Application schematic

Figure 11. Application schematic



3 Ordering information scheme

Figure 12. Ordering information scheme



EMI Filter

Number of lines

Information
xxx = application
zz = version

Package
Mx = Micro QFN x leads

4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. QFN 1.7 x 1.5 package dimensions

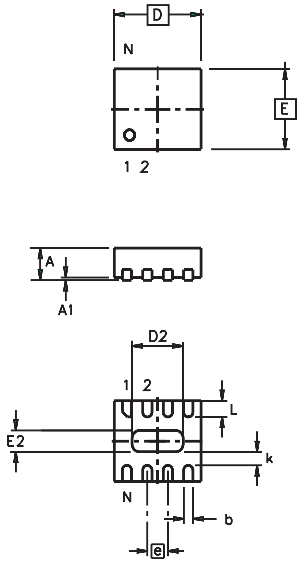
	Ref	Dimensions					
		Millimeters			inches		
		MIN	TYP	MAX	MIN	TYP	MAX
	A	0.50	0.55	0.60	0.20	0.22	0.24
	A1	0.00	0.02	0.05	0.00	0.01	0.02
	b	0.15	0.18	0.25	0.06	0.07	0.10
	D		1.70			0.67	
	D2	0.9	1.00	1.10	0.35	0.39	0.43
	E		1.50			0.59	
	E2	0.30	0.40	0.50	0.12	0.16	0.24
	e		0.40			0.16	
	k	0.20			0.08		
	L	0.25	0.30	0.35	0.10	0.12	0.14

Figure 13. Footprint (dimensions in mm)

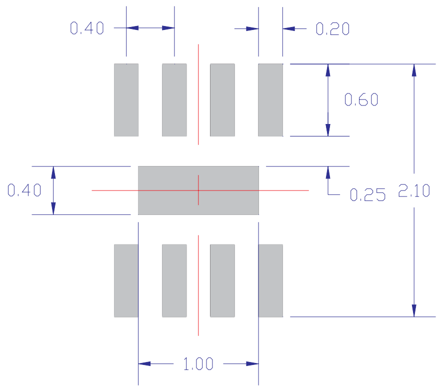
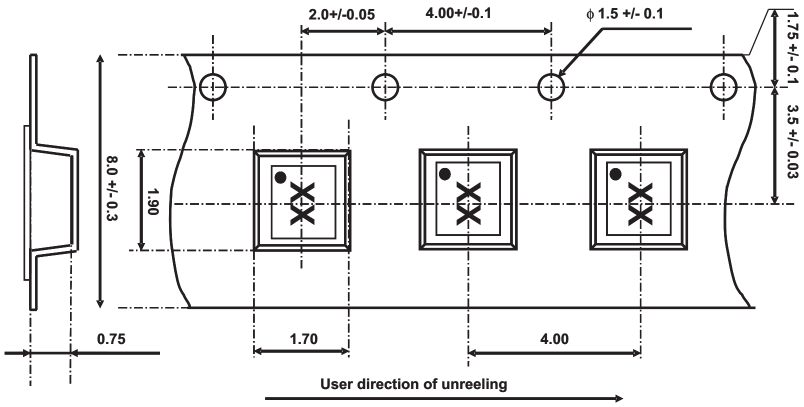


Figure 14. Marking

Dot: Pin 1 Identification

Figure 15. Tape and reel specification



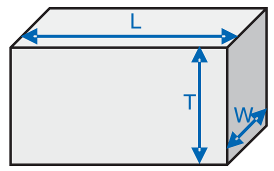
Note: *Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*

5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 16. Stencil opening dimensions



b) General Design Rule

Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
      Example: Stencil opening L = 680 µm, W = 300 µm
      Footprint (see *Figure 13*) L = 1000 µm, W = 400 µm
   c) Stencil opening for leads: Opening to footprint ratio is 90%.
      Example: Stencil opening L = 570 µm, W = 190 µm
      Footprint (see *Figure 13*) L = 600 µm, W = 200 µm

5.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

5.3 Placement

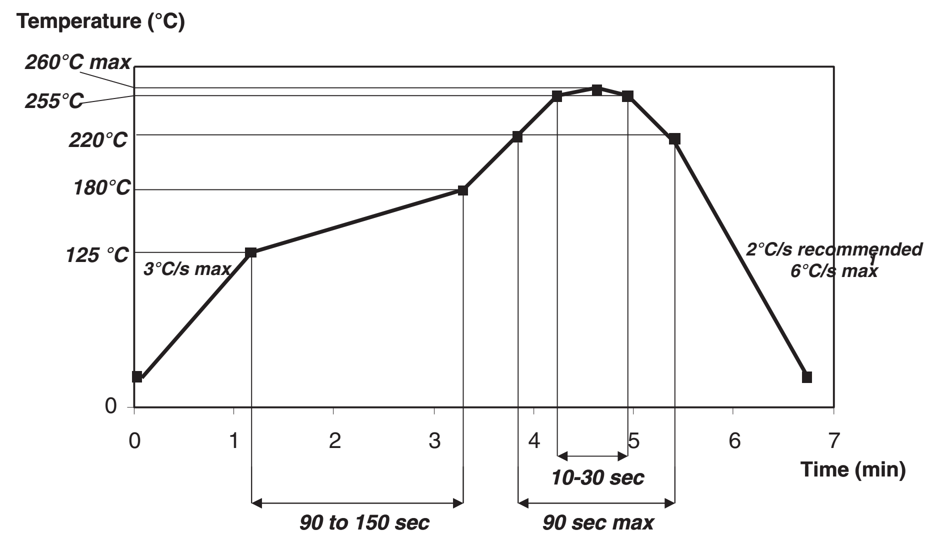
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 17. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM02M8	HA	Micro QFN	4 mg	3000	Tape and reel (7”)

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Oct-2007	1	Initial release.

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