

into eight 1-Wire time slots, thereby increasing the data throughput significantly. In addition, the DS2480B can be set to communicate at four different data rates, including 115.2kbps, 57.6kbps, and 19.2kbps, with 9.6kbps being the power-on default. Command codes received from the host's crystal controlled UART serve as a reference to continuously calibrate the on-chip timing generator. The DS2480B uses a unique protocol that merges data and control information without requiring control pins. This approach maintains compatibility to off-the-shelf serial to wireless converters, allowing easy realization of 1-Wire media jumpers. The various control functions of the DS2480B are optimized for 1-Wire networks and support the special needs of all current 1-Wire devices including EPROM-based add-only memories, EEPROM devices, and 1-Wire thermometers. See *Application Note 192: Using the DS2480B Serial 1-Wire Driver* for detailed software examples.

DETAILED PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	GND	Ground Pin. Common ground reference and ground return for 1-Wire bus
2	1-W	1-Wire Input/Output Pin. 1-Wire bus with slew-rate-controlled pulldown, active pullup, ability to switch in V_{PP} to program EPROM, and ability to switch in V_{DD} through a low-impedance path to program EEPROM, or perform a temperature conversion.
3	N.C.	No Connection
4	V_{DD}	Power Input Pin. Power supply for the chip and 1-Wire pullup voltage, 5V $\pm 10\%$, must always be lower than or equal to V_{PP} . V_{DD} should be derived from V_{PP} by a separate voltage regulator whenever possible.
5	V_{PP}	EPROM Programming Voltage. 12V supply input for EPROM programming. If EPROM programming is not required, connect this pin directly to the system's 5V supply.
6	POL	RXD/TXD Polarity Select. RXD/TXD polarity select; tied to GND for RS232 (12V or 5V) connection; tied to V_{DD} for direct connection to UART chip.
7	TXD	Serial Data from UART. Data input from host (inverted or true); maximum voltage swing -0.3V to $V_{DD} + 0.3V$; for logic thresholds see DC specifications.
8	RXD	Serial Data to UART. Signal output to host; push-pull driver with CMOS compatible levels; for true $\pm 12V$ RS232 systems an external level translator must be provided.

OVERVIEW

The DS2480B directly interfaces a 5V serial communication port with its lines TXD (transmit) and RXD (receive) to a 1-Wire bus. In addition the device performs a speed conversion allowing the data rate at the communication port to be different from the 1-Wire data rate. Several parameters relating to the 1-Wire port and its timing as well as the communication speed at both the port and the 1-Wire bus are configurable. The circuit to achieve these functions is outlined in the block diagram (see Figure 1).

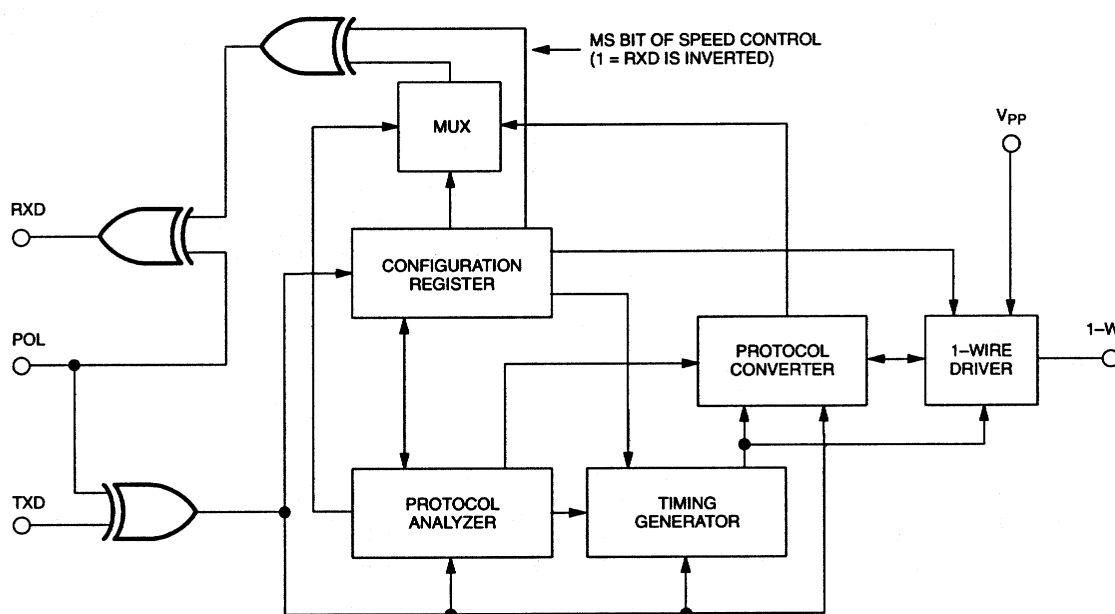
The device gets its input data from the serial communication port of the host computer through pin TXD. For compatibility with active-high as well as active-low systems, the incoming signal can be inverted by means of the polarity input POL. The polarity chosen by hard-wiring the logic level of this pin is also valid for the output pin RXD. If for minimizing the interface hardware an asymmetry between RXD and TXD is desired, this can be achieved by setting the most significant bit of the speed control parameter to a 1 (see *Configuration Parameter Value Codes*). With the MS bit of the speed control set to 1, the polarity at TXD is still selected by the logic level at POL, but the polarity at RXD will be the opposite of what the logic level at POL specifies.

As data enters the core of the DS2480B's logic circuitry, it is analyzed to separate data and command bytes and to calibrate the device's timing generator. The timing generator controls all speed relations of the communication interface and the 1-Wire bus as well as the waveforms on the 1-Wire bus.

Command bytes either affect the configuration setting or generate certain waveforms on the 1-Wire bus. Data bytes are simply translated by the protocol converter into the appropriate 1-Wire activities. Each data byte generates a return byte from the 1-Wire bus that is communicated back to the host through the RXD pin as soon as the activity on the 1-Wire bus is completed.

The 1-Wire driver shapes the slopes of the 1-Wire waveforms, applies programming pulses or strong pullup to 5V and reads the 1-Wire bus using a non-TTL threshold to maximize the noise margin for best performance on large 1-Wire networks.

Figure 1. DS2480B BLOCK DIAGRAM

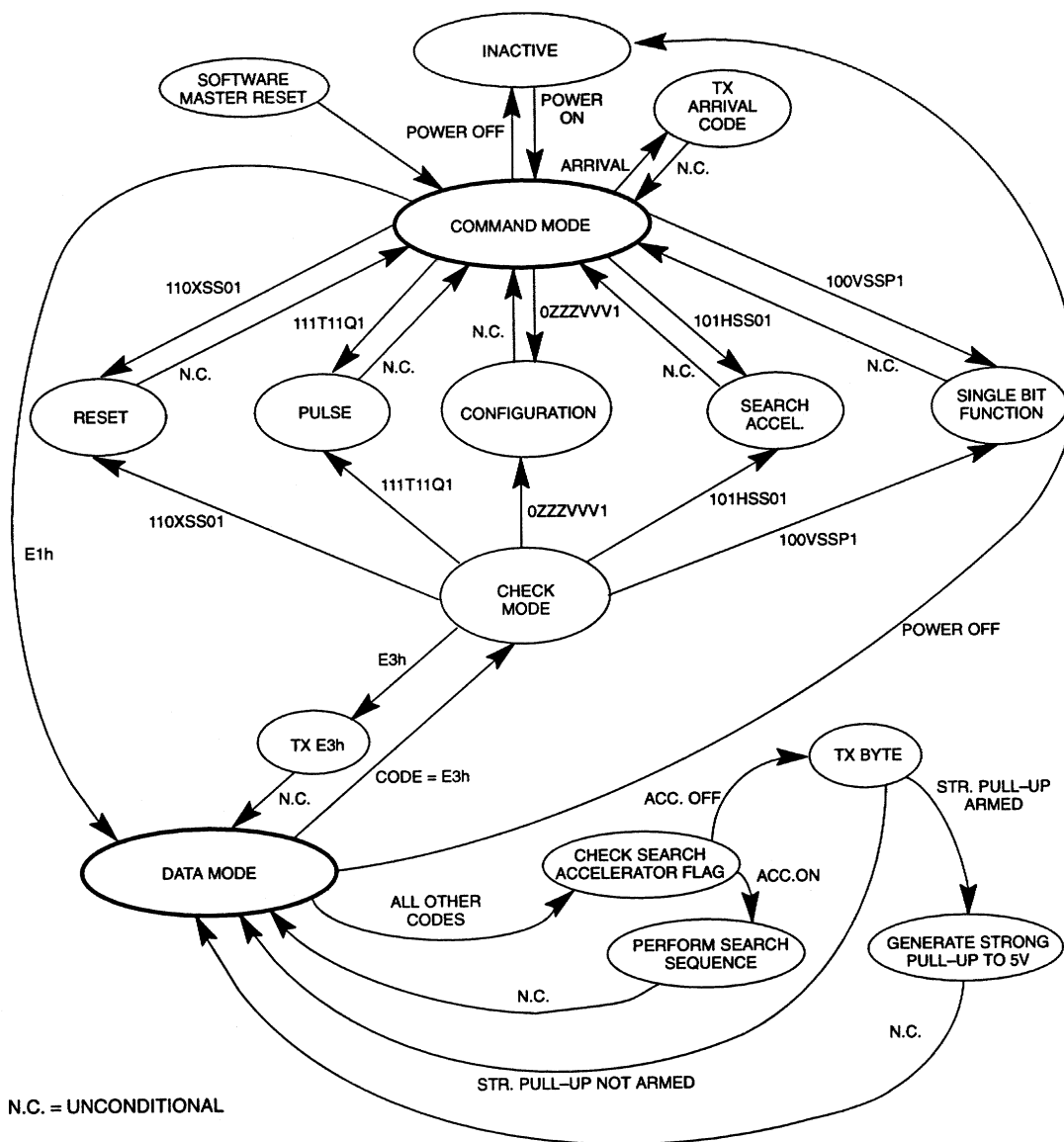


DEVICE OPERATION

The DS2480B can be described as a complex state machine with two static and several dynamic states. Two device-internal flags as well as functions assigned to certain bit positions in the command codes determine the behavior of the chip, as shown in the state transition diagram (Figure 2). The DS2480B requires and generates a communication protocol of 8 data bits per character, 1 stop bit and no parity. It is permissible to use 2 stop bits on the TXD line. However, the DS2480B only asserts a single stop bit on RXD.

When powering up, the DS2480B performs a master reset cycle and enters the **Command Mode**, which is one of the two static states. The device now expects to receive one 1-Wire reset command on the TXD line sent by the host at a data rate of 9600bps (see *Communication Commands* section for details). This command byte is required solely for calibration of the baud rate timing generator the DS2480B and is not translated into any activity on the 1-Wire bus. After this first command byte the device is ready to receive and execute any command as described later in this document. NOTE: Baud rate calibration is valid only for the V_{DD} operating voltage at which calibration is performed. Post-calibration changes in V_{DD} by more than 5% may cause calibration error to exceed ±5%. The DS2480B requires a 1-Wire reset command sent by the host at a data rate of 9600bps for calibration. Data rates of 115200bps or higher during calibration may put the DS2480B in an undefined state, requiring a power-down reset to restore normal operation.

Figure 2. STATE TRANSITION DIAGRAM



LEGEND:	V	BINARY VALUE (TYPE OF WRITE TIME SLOT)
	SS	1-WIRE SPEED SELECTION CODE
	P	IF LOGIC 1, GENERATES STRONG PULLUP TO 5V IMMEDIATELY FOLLOWING THE TIME SLOT
	T	TYPE OF PULSE; 0 = STRONG PULLUP (5V), 1 = PROGRAMMING PULSE (12V)
	Q	1 = ARM STRONG PULLUP AFTER EVERY BYTE; 0 = DISARM
	H	SEARCH ACCELERATOR CONTROL; 1 = ACCELERATOR ON, 0 = ACCELERATOR OFF
	ZZZ	CONFIGURATION PARAMETER CODE (WRITE), 000 = READ CONFIGURATION PARAMETER
	VVV	CONFIGURATION PARAMETER VALUE CODE (WRITE), CONFIGURATION PARAMETER CODE (READ)
	X	DON'T CARE

A master reset cycle can also be generated by means of software. This may be necessary if the host for any reason has lost synchronization with the device. The DS2480B will perform a master reset cycle equivalent to the power-on reset if it detects start polarity in place of the stop bit. The host has several options to generate this condition. These include making the UART generate a break signal, sending a NULL character at a data rate of 4800bps and sending any character with parity enabled and selecting space polarity for the parity bit. As with the power-on reset, the DS2480B requires a 1-Wire reset command sent by the host at a data rate of 9600bps for calibration.

After the DS2480B has reached the Command Mode, the host can send commands such as 1-Wire Reset, Pulse, Configuration, Search Accelerator, and Single Bit functions or switch over to the second static state called **Data Mode**. In Data Mode the DS2480B simply converts bytes it receives at the TXD pin into their equivalent 1-Wire waveforms and reports the results back to the host through the RXD pin. If the Search Accelerator is on, each byte seen at TXD will generate a 12-bit sequence on the 1-Wire bus (see *Search Accelerator* section for details). If the strong pullup to 5V is enabled (see *Pulse Command*), each byte on the 1-Wire bus will be followed by a pause of predefined duration where the bus is pulled to 5V via a low-impedance transistor in the 1-Wire driver circuit.

While being in the Data Mode the DS2480B checks each byte received from the host for the reserved code that is used to switch back to Command Mode. To be able to write any possible code (including the reserved one) to the 1-Wire bus, the transition to the Command Mode is as follows: After having received the code for switching to Command Mode, the device temporarily enters the **Check Mode** where it waits for the next byte. If both bytes are the same, the byte is sent **once** to the 1-Wire bus and the device returns to the Data Mode. If the second byte is different from the reserved code, it will be executed as command and the device finally enters the Command Mode. As a consequence, if the reserved code that normally switches to Command Mode is to be written to the 1-Wire bus, this code byte must be sent twice (duplicated). This detail must be considered carefully when developing software drivers for the DS2480B.

After having completed a memory function with a device on the 1-Wire bus it is recommended to issue a Reset Pulse. This means that the DS2480B has to be switched to Command Mode. The host then sends the appropriate command code and continues performing other tasks. If during this time a device arrives at the 1-Wire bus it will generate a presence pulse. The DS2480B will recognize this unsolicited presence pulse and notify the host by sending a byte such as XXXXXX01b. The Xs represent undefined bit values. The fact that the host receives the byte unsolicited together with the pattern 01b in the least significant 2 bits marks the bus arrival. If the DS2480B is left in Data Mode after completing a memory function command it will not report any bus arrival to the host.

COMMAND CODE OVERVIEW

The DS2480B is controlled by a variety of commands. All command codes are 8 bits long. The most significant bit of each command code distinguishes between communication and configuration commands. Configuration commands access the configuration registers. They can write or read any of the configurable parameters. Communication commands use data of the configuration register in order to generate activity on the 1-Wire bus and/or (dis)arm the strong pullup after every byte or (de)activate the Search Accelerator without generating activity on the 1-Wire bus. Details on the command codes are included in the State Transition diagram (Figure 2). A full explanation is given in the subsequent *Communication Commands* and *Configuration Commands* sections.

In addition to the command codes explained in the subsequent sections the DS2480B understands the following reserved command codes:

E1h	switch to Data Mode
E3h	switch to Command Mode
F1h	pulse termination

Except for these reserved commands, the Search Accelerator control and the first byte after power-on reset or master reset cycle, every legal command byte generates a response byte. The pulse termination code triggers the response byte of the terminated pulse command. Illegal command bytes do not generate a command response byte.

COMMUNICATION COMMANDS

The DS2480B supports four communication function commands: Reset, Single Bit, Pulse, and Search Accelerator control. Details on the assignment of each bit of the command codes are shown in Table 1. The corresponding command response bytes are detailed in Table 2. The Reset, Search Accelerator Control and Single Bit commands include bits to select the 1-Wire communication speed (standard, flexible, Overdrive). Even if a command does not generate activity on the 1-Wire bus, these bits are latched inside the device and will take effect immediately.

Reset

The Reset command must be used to begin all 1-Wire communication. The speed selection included in the command code immediately takes effect. The response byte includes a code for the reaction on the 1-Wire bus (bits 0 and 1) and a code for the chip revision (bits 2 to 4).

Single Bit

The Single Bit command is used to generate a single time slot on the 1-Wire bus at the speed indicated by bits 2 and 3. The type of the time slot (Write-0 or Write-1) is determined by the logic value of bit 4. A Read Data time slot is identical to the Write-1 time slot. Bits 0 and 1 of the response byte transmitted by the DS2480B at the end of the time slot reveal the value found on the 1-Wire bus when reading.

For a time slot without a subsequent strong pullup, bit 1 of the command must be set to 0. For a time slot immediately followed by a strong pullup bit 1 must be set to 1. As soon as the strong pullup is over, the device will send a second response byte, code EFh (read 1) or ECh (read 0), depending on the value found on the 1-Wire bus when reading.

Table 1. COMMUNICATION COMMAND CODES

FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3, BIT 2	BIT 1	BIT 0
Single Bit	1	0	0	0 = write 0 1 = write 1	00 reg. speed 01 flex. speed 10 OD. speed 11 reg. speed	See Text	1
Search Accelerator Control	1	0	1	0 = accelerator off 1 = accelerator on See Text	00 reg. speed 01 flex. speed 10 OD. speed 11 reg. speed	0	1
Reset	1	1	0	(don't care)	00 reg. speed 01 flex. speed 10 OD. speed 11 reg. speed	0	1
Pulse	1	1	1	0 = 5V strong pullup 1 = 12V prog. pulse	11 pulse	See Text	1

Table 2. COMMUNICATION COMMAND RESPONSE

FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Single Bit	1	0	0	same as sent			1-Wire read back, both bits same value	
Reset	1	1	X	0	1	1	00 = 1-Wire shorted 01 = presence pulse 10 = alarming presence pulse 11 = no presence pulse	
Pulse	1	1	1	same as sent			undefined	

X: This bit is reserved and undefined. In previous data sheet versions this bit was used to indicate that a programming voltage was present.

Search Accelerator Control

The Search Accelerator Control command is used to set or reset the Search Accelerator control flag. Bit 4 of the command code contains the state to which the accelerator control flag is to be set. If the flag is set to a 1 (on) the device translates every byte received in Data Mode into a 12-bit sequence on the 1-Wire bus. For details on how the Search Accelerator works please refer to the section Search Accelerator Operation. Before activating the Search Accelerator, one must make sure that the strong pullup after every byte is disarmed (see *Pulse Command*). The Search Accelerator command does not generate a command response byte.

Although the Search Accelerator Control command itself does not generate any 1-Wire activity, it can be used to select the communication speed on the 1-Wire bus. The speed selection (if different from the previous setting, e.g., from a Reset command) will take effect immediately.

Pulse

The Pulse command serves several functions that are selected by the contents of bit 1 and bit 4 of the command code. The main functions are generating a strong pullup to 5V and generating 12V programming pulses for EPROM devices (if the 12V are available at the V_{PP} pin). The secondary function

Maxim Integrated 7

of the pulse command is arming and disarming a strong pullup after every subsequent byte in Data Mode. The arm/disarm function is controlled by bit 1 of the command code. Bit 4 determines whether the device will generate a strong pullup to 5V or a 12V programming pulse. The table below summarizes these options.

BIT 4	BIT 1	FUNCTION
0	0	Strong pullup to 5V and disarm
1	0	12V programming pulse and disarm
0	1	Strong pullup to 5V and arm
1	1	12V programming pulse and arm

The strong pullup to 5V is required to program EEPROM devices or to operate special function devices that require a higher current for a limited time after having received a “go and convert” command. Therefore, and because it significantly reduces the effective data throughput on the 1-Wire bus, the strong pullup is disarmed most of the time. Although arming or disarming is simultaneously possible while generating a programming pulse, this is not recommended since it is likely to destroy the DS2480B if non-EEPROM devices are connected to the 1-Wire bus.

The duration of the strong pullup or programming pulse is determined by configuration parameters and ranges from a few microseconds up to unlimited (see *Configuration Commands* section). However, unlimited duration is not allowed in conjunction with arming the strong pullup after every byte. As long as the DS2480B is in Command Mode the host may terminate a strong pullup or programming pulse prematurely at any time by sending the command code F1h.

The response byte is generated as soon as the strong pullup or programming pulse is over (either because the predefined time has elapsed, the high current demand is over, or due to termination by the host). The response byte mainly returns the command code as sent by the host, but the 2 least significant bits are undefined.

If the strong pullup is armed and the device is in Data Mode, the end of the strong pullup will be signaled as code F6h if the most significant bit of the preceding data byte on the 1-Wire bus is a 1 and 76h otherwise. The host will see this response byte in addition to the response on the data byte sent (see also *Waveforms* section later in this document).

SEARCH ACCELERATOR INTRODUCTION

The Search Accelerator is a logic block inside the DS2480B that allows using the Search ROM function very efficiently under modern operating systems. Without the DS2480B all 1-Wire port adapters have to involve the computer’s CPU for every single time slot or pulse to be generated on the 1-Wire bus.

Under some operating systems it may take several milliseconds or more to get the first time slot generated on the 1-Wire bus when sending commands to the UART. Every subsequent time slot will be generated in much less time, since the computer simply sends out “streams”—a long chain of bytes. This works reasonably well when reading or writing large blocks of data.

Searching the 1-Wire bus to identify all ROM IDs of the devices connected, however, requires reading 2 bits, making a decision and then writing a bit. This procedure is to be repeated 64 times to identify and address a single device. With the overhead of modern operating systems this fairly simple process takes a lot of time, reducing the discovery rate of devices on the 1-Wire bus. To solve this problem the Search Accelerator was developed.

During the execution of the Search ROM function, the Search Accelerator receives from the host information on the preferred path to choose as one contiguous chain of bytes and then translates it into the appropriate time slots on the 1-Wire bus. In addition, the Search Accelerator reports back to the host the ROM ID of the device actually addressed and the bit positions in which conflicts were found. (If the ROM ID of one device has a 0 in a bit position where another device has a 1, this is called a “conflict” on the electrical level and “discrepancy” on the logical level. See Application Note 187 for a more detailed discussion of the Search ROM.) This helps the host to select the preferred path for the next Search ROM activity.

Since the ROM ID of all 1-Wire/iButton devices is 64 bits long and a conflict may occur in any of these bits, the total length of data reported to the host is 128 bits or 16 bytes. To avoid data overrun (if the CPU sends data faster than it can be processed) the protocol for the Search Accelerator operation was defined so that one has to send as many bytes as one will receive. This way the CPU sends 16 bytes for each path and the UART guarantees the correct data timing and frees the CPU for other tasks while the DS2480B performs a Search ROM function.

SEARCH ACCELERATOR OPERATION

After the Search Accelerator is activated and the Data Mode is selected, the host must send 16 bytes to complete a single Search ROM pass on the 1-Wire bus. These bytes are constructed as follows:

first byte

7	6	5	4	3	2	1	0
r ₃	x ₃	r ₂	x ₂	r ₁	x ₁	r ₀	x ₀

et cetera

16th byte

7	6	5	4	3	2	1	0
r ₆₃	x ₆₃	r ₆₂	x ₆₂	r ₆₁	x ₆₁	r ₆₀	x ₆₀

In this scheme, the index (values from 0 to 63, “n”) designates the position of the bit in the ROM ID of a 1-Wire/iButton device. The character “x” marks bits that act as filler and do not require a specific value (“don’t care” bits). The character “r” marks the path to go at that particular bit in case of a conflict during the execution of the ROM Search.

For each bit position n (values from 0 to 63) the DS2480B will generate three time slots on the 1-Wire bus. These are referenced as:

- b0 for the first time slot (Read Data)
- b1 for the second time slot (Read Data) and
- b2 for the third time slot (Write Data).

The type of time slot b2 (write 1 or write 0) is determined by the DS2480B as follows:

- b2 = r_n if conflict (as chosen by the host)
 = b_0 if no conflict (there is no alternative)
 = 1 if error (there is no response)

The response the host will receive during a complete pass through a Search ROM function using the Search Accelerator consists of 16 bytes as follows:

first byte

7	6	5	4	3	2	1	0
r'_3	d_3	r'_2	d_2	r'_1	d_1	r'_0	d_0

et cetera

16th byte

7	6	5	4	3	2	1	0
r'_{63}	d_{63}	r'_{62}	d_{62}	r'_{61}	d_{61}	r'_{60}	d_{60}

As before, the index (values from 0 to 63, “n”) designates the position of the bit in the ROM ID of a 1-Wire/iButton device. The character “d” marks the discrepancy flag in that particular bit position. The discrepancy flag will be 1 if there is a conflict, or no response in that particular bit position, and 0 otherwise. The character “r” marks the actually chosen path at that particular bit position. The chosen path is identical to b2 for the particular bit position of the ROM ID.

To perform a Search ROM sequence one starts with all bits r_n being 0s. In case of a bus error, all subsequent response bits r'_n are 1s until the Search Accelerator is deactivated. Thus, if r'_{63} and d_{63} are both 1, an error has occurred during the search procedure and the last sequence has to be repeated. Otherwise r'_n ($n = 0 \dots 63$) is the ROM code of the device that has been found and addressed.

For the next Search ROM sequence one reuses the previous set r_n ($n = 0 \dots 63$) but sets r_m to 1 with “m” being the index number of the highest discrepancy flag (that is, 1) and sets all r_i to 0 with $i > m$. This process is repeated until the highest discrepancy occurs in the same bit position for two consecutive passes.

The table below shows an example for the communication between host and DS2480B to perform one pass through the Search ROM function using the Search Accelerator. After a device has been identified and addressed, a memory function (not specified here) is executed and finally a reset pulse is generated. This example assumes that the DS2480B was in Command Mode and that standard 1-Wire speed is used.

Search Accelerator Usage Example

Action Sequence	Host TX	Host RX
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Search ROM command	F0	(as sent)
Set Command Mode	E3	(nothing)
Search Accelerator On	B1	(nothing)
Set Data Mode	E1	(nothing)
Send 16 bytes	data	(response)
Set Command Mode	E3	(nothing)
Search Accelerator Off	A1	(nothing)
Set Data Mode	E1	(nothing)
Do Memory Function		
Set Command Mode	E3	(nothing)
Generate Reset Pulse	C1	CD or ED

CONFIGURATION COMMANDS

The DS2480B is designed to be configurable for the varying requirements of its application. When the device powers up and/or performs a master reset cycle, the hard-wired default configuration settings take effect. These settings will work on a short 1-Wire bus and assume standard 1-Wire communication speed. To change these default settings and to verify the current settings, the logic of the DS2480B supports configuration commands. A summary of the available configuration parameters, their default settings at standard and Overdrive speed and their applicability is shown in Table 3.

Parameters not related to the communication speed on the 1-Wire bus specify the duration of the 12V programming pulse, the duration of the strong pullup to 5V, and the baud rate on the interface that connects the DS2480B to the host. The remaining three parameters are used to modify the 1-Wire communication waveforms if one selects “Flexible Speed” (see *Communication Commands* for speed selection).

Flexible speed is implemented to improve the performance of large 1-Wire Networks. This is accomplished by:

- limiting the slew rate on falling edges (e. g., at the beginning of time slots, to reduce ringing),
- extending the Write-1 low time (allows the current flow through the network to end slowly, to prevent voltage spikes from inductive kickback),
- delaying the time point when reading a bit from the 1-Wire bus (gives the network more time to stabilize, to get a higher voltage margin) and
- adding extra recovery time between Write-0 time slots (allows more energy transfer through the network, to replenish the parasite power supply of the devices on the bus).

The latter two functions are controlled by a single parameter. Taking advantage of flexible speed requires changing one or more of these parameters from their default values. Otherwise the waveforms will be identical to those at standard speed.

Each configuration parameter is identified by its 3-bit parameter code and can be programmed for one of a maximum eight different values using a 3-bit value code. A matrix of parameter codes and value codes with the associated physical values is shown in Table 4.

Table 3. CONFIGURATION PARAMETER OVERVIEW

Parameter Description	Par. Code	Configurable at			Default	
		Standard	Flexible	Overdrive	Reg./Flex.	Overdrive
Pulldown Slew Rate Control	001		√		15V/μs	15V/μs
Programming Pulse Duration	010	√	√	√	512μs	512μs
Strong Pullup Duration	011	√	√	√	524ms	524ms
Write-1 Low Time	100		√		8μs	1μs
Data Sample Offset and Write 0 Recovery Time	101		√		3μs 3μs	1μs 3μs
RS232 Baud Rate	111	√	√	√	9.6kbps	9.6kbps

The numbers given for parameter 001 (Pulldown Slew Rate Control) are nominal values. They may vary to some extent and are almost independent of the load on the 1-Wire bus. Information on how to select the optimum value of this parameter is given in the *Controlled Edges* section .

For the parameters 010 (Programming Pulse Duration) and 011 (Strong Pullup Duration) one may select indefinite duration. This value, however, should only be selected if one is not going to switch the device to Data Mode. As long as the device stays in Command Mode, any pulse function (programming or strong pullup) that uses one of these parameters can be terminated by sending the command code F1h. Termination is not possible if the device is in Data Mode.

Parameter 111 (RS232 Baud Rate) has two functions. It selects the baud rate and allows inversion of the signal at the RXD pin. Using one of the value codes 100 to 111 will set the polarity at RXD to the opposite of what is defined by the logic level at the POL pin (asymmetry bit, see Figure 1). This may reduce the component count in some applications of the device. Note that when changing the baud rate, the DS2480B will send the command response byte at the new data rate.

A short explanation on the use of parameters 100 (Write-1 Low Time) and 101 (Data Sample Offset/Write-0 Recovery Time) is given in the *Timing Diagrams* section later in this document.

Table 4. CONFIGURATION PARAMETER VALUE CODES

Parameter Code	Value Codes								Unit
	000	001	010	011	100	101	110	111	
001 (PDSRC)	15	2.2	1.65	1.37	1.1	0.83	0.7	0.55	V/ μ s
010 (PPD)	32	64	128	256	512	1024	2048	∞	μ s
011 (SPUD)	16.4	65.5	131	262	524	1048	Note	∞	ms
100 (WILT)	8	9	10	11	12	13	14	15	μ s
101 (DSO/WORT)	3	4	5	6	7	8	9	10	μ s
110 (LOAD)	1.8	2.1	2.4	2.7	3.0	3.3	3.6	3.9	mA
111 (RBR)	9.6	19.2	57.6	115.2	9.6	19.2	57.6	115.2	kbps

Note: The value code 110 of parameter 011 (Strong Pullup Duration) must not be used since it could cause unexpected results.

The syntax of configuration commands is very simple. Each 8-bit code word contains a 3-bit parameter code to specify the parameter and the 3-bit value code to be selected. Bit 7 of the command code is set to 0 and bit 0 is always a 1. To read the value code of a parameter, one writes all 0s for the parameter code and puts the parameter code in place of the parameter value code. Table 5 shows the details.

The configuration command response byte is similar to the command byte itself. Bit 0 of the response byte is always 0. When writing a parameter, the upper 7 bits are the echo of the command code. When reading a parameter, the current value code is returned in bit positions 1 to 3 with the upper 4 bits being the same as sent (see Table 6).

Table 5. CONFIGURATION COMMAND CODES

FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write Parameter	0	parameter code			parameter value code			1
Read Parameter	0	0	0	0	parameter code			1

Table 6. CONFIGURATION COMMAND RESPONSE BYTE

FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Write Parameter	0	same as sent			same as sent			0
Read Parameter	0	same as sent			parameter value code			0

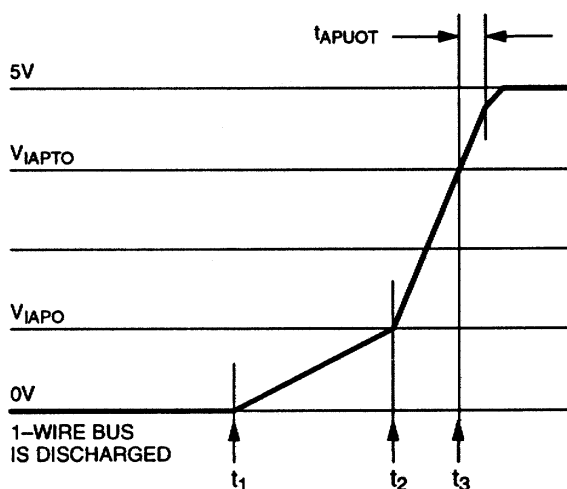
CONTROLLED EDGES

One of the tasks of the DS2480B is to actively shape the edges of the 1-Wire communication waveforms. This speeds up the recharging of the 1-Wire bus (rising edges) and reduces ringing of long lines (falling edges). The circuitry for shaping rising edges is always on. The slew rate of falling edges is actively controlled only at flexible speed and requires the parameter for slew rate control being different from its power-on default value.

All Rising Edges

The active pullup of the rising edges reduces the rise time on the 1-Wire bus significantly compared to a simple resistive pullup. Figure 4 shows how the DS2480B is involved in shaping a rising edge.

Figure 4. ACTIVE PULLUP

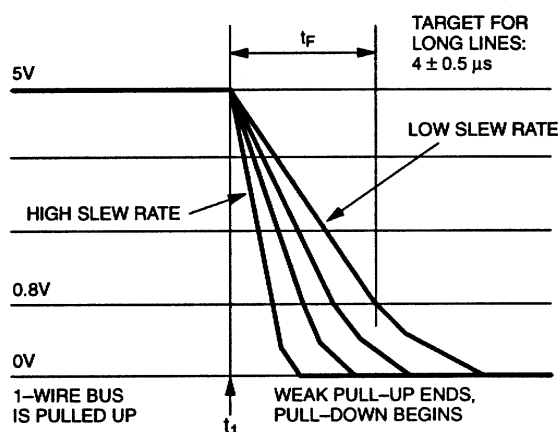


The circuit operates as follows: At t_1 the pulldown (induced by the DS2480B or a device on the bus) ends. From this point on the 1-Wire bus is pulled high by the weak pullup current I_{WEAKPU} provided by the DS2480B. The slope is determined by the load on the bus and the value of the pullup current. At t_2 the voltage crosses the threshold voltage V_{IAP0} . Now the DS2480B switches over from the weak pullup current I_{WEAKPU} to the higher current I_{ACTPU} . As a consequence, the voltage on the bus now rises faster. As the voltage on the bus crosses the threshold V_{IAPTO} at t_3 , a timer is started. As long as this timer is on (t_{APUOT}), the I_{ACTPU} current will continue to flow. After the timer is expired, the DS2480B will switch back to the weak pullup current. Excessive noise on the 1-Wire line at the V_{IAPTO} level can cause an undesirable trip of the active pullup. External R-C filtering as discussed in the *HARDWARE APPLICATION EXAMPLES* section and *Application Note 148* should be used to prevent false triggering.

Falling Edges (DS2480B-initiated)

Whenever the DS2480B begins pulling the 1-Wire bus low to initiate a time slot, for example, it first turns off the weak pullup current I_{WEAKPU} . Then, at standard and Overdrive speeds it will generate a falling edge at a slew rate of typically $15V/\mu s$. This value is acceptable for short 1-Wire busses and adequate for communication at Overdrive speed. For 1-Wire networks of more than roughly 30m length one should always use flexible speed. One of the parameters that is adjustable at flexible speed is the slew rate of DS2480B-initiated falling edges. The effect of the slew rate control is shown in Figure 5.

Figure 5. SLEW RATE CONTROL



As extensive tests have shown, 1-Wire networks at a length of up to 300m will perform best if the fall time t_F is in the range of $4 \pm 0.5\mu s$. This translates into a slew rate of approximately $1V/\mu s$. This slew rate is typically achieved by setting the configuration parameter 001 (Pulldown Slew Rate Control) to a value of 100 (see Table 4). If the actual measured fall time is longer than the target value, one should use a value code of 011 or lower. If the fall time is shorter, one should use a value code of 101 or higher.

Once determined, the value code for the Pulldown Slew Rate Control parameter should be stored in the host and always be loaded into the DS2480B after a power-on or master reset cycle.

TIMING DIAGRAMS

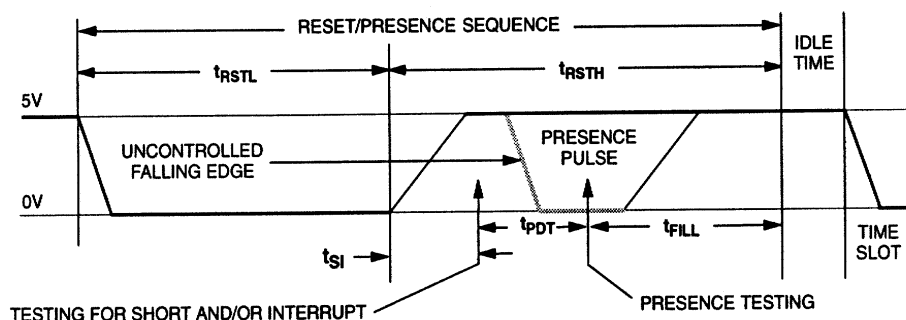
This section explains the waveforms generated by the DS2480B on the 1-Wire bus in detail. First the communication waveforms such as the Reset/Presence Detect Sequence and the time slots are discussed. After that follows a detailed description of the pulse function under various conditions.

1-WIRE COMMUNICATION WAVEFORMS

One of the major features of the DS2480B is that it relieves the host from generating the timing of the 1-Wire signals and sampling the 1-Wire bus at the appropriate times. How this is done for the reset/presence detect sequence is shown in Figure 6a. This sequence is composed of four timing segments: the reset low time t_{RSTL} , the short/interrupt sampling offset t_{SI} , the presence detect sampling offset t_{PDT} and a delay time t_{FILL} . The timing segments t_{SI} , t_{PDT} and t_{FILL} comprise the reset high time t_{RSTH} where 1-Wire slave devices assert their presence or interrupt pulse. During this time the DS2480B pulls the 1-Wire bus high with its weak pullup current.

The values of all timing segments for all 1-Wire speed options are shown in the table. Since the reset/presence sequence is slow compared to the time slots, the values for standard and flexible speed are the same. Except for the falling edge of the presence pulse all edges are controlled by the DS2480B. The shape of the uncontrolled falling edge is determined by the capacitance of the 1-Wire bus and the number, speed and sink capability of the slave devices connected.

Figure 6a. RESET/PRESENCE DETECT



Speed	t_{RSTL}	t_{SI}	t_{PDT}	t_{FILL}	t_{RSTH}
Standard	512 μ s	8 μ s	64 μ s	512 μ s	584 μ s
Overdrive	64 μ s	2 μ s	8 μ s	64 μ s	74 μ s
Flexible	512 μ s	8 μ s	64 μ s	512 μ s	584 μ s

After having received the command code for generating a reset/presence sequence, the DS2480B pulls the 1-Wire bus low for t_{RSTL} and then lets it go back to 5V. The DS2480B will now wait for the short/interrupt sampling offset t_{SI} to expire and then test the voltage on the 1-Wire bus to determine if there is a short or an interrupt signal. If there is no short or interrupt (as shown in the picture), the DS2480B will wait for t_{PDT} and test the voltage on the 1-Wire bus for a presence pulse. Regardless of the result of the presence test, the DS2480B will then wait for t_{FILL} to expire and then send the command response byte to the host.

If the test for interrupt or short reveals a logic 0, the DS2480B will wait for 4096 μ s and then test the 1-Wire bus again. If a logic 0 is detected, the 1-Wire bus is shorted and a command response byte with the code for SHORT will be sent immediately. If a logic 1 is detected, the device will wait for t_{FILL} to expire, after which it will send the command response byte with the code for an alarming presence pulse. No additional testing for a presence pulse will be done. The DS2480B will perform the short/interrupt testing as described also at Overdrive speed, although interrupt signaling is only defined for standard speed.

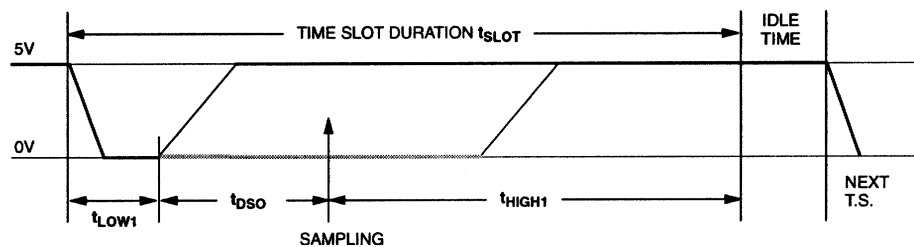
The idle time following the Reset/Presence Detect sequence depends on the serial communication speed and the host's response time.

A Write-1 and Read Data time slot is comprised of the segments t_{LOW1} , t_{DSO} and t_{HIGH1} . During Write-1 time slots, after the Write-1 low time t_{LOW1} is over, the DS2480B waits for the duration of the data sample offset and then samples the voltage at the 1-Wire bus to read the response. After this, the waiting time t_{HIGH1} must expire before the time slot is complete. A Write-0 time slot only consists of the two segments t_{LOW0} and t_{RECO} .

If the network is large or heavily loaded, one should select flexible speed and extend t_{LOW1} to more than $8\mu\text{s}$ to allow the 1-Wire bus to completely discharge. Since a large or heavily loaded network needs more time to recharge, it is also recommended to delay sampling the bus for reading. A higher value for t_{DSO} will increase the voltage margin and also provide extra energy to the slave devices when generating a long series of write 0 time slots. However, the total of $t_{LOW1} + t_{DSO}$ should not exceed $22\mu\text{s}^*$. Otherwise the slave device responding may have stopped pulling the bus low when transmitting a logic 0.

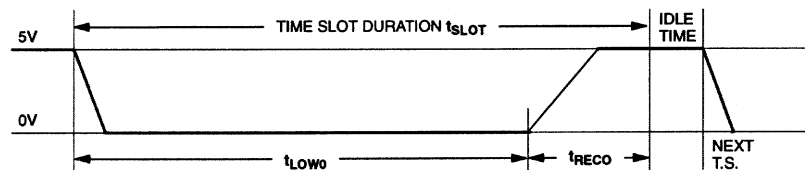
The idle time between time slots within a byte or during a 12-bit sequence while the Search Accelerator is on is 0. Between bytes, 12-bit search sequences and single bits the idle time depends on the RS232 data rate and the host's response time. The response byte is sent to the host as soon as the last time slot of a byte, 12-bit sequence or the command is completed.

Figure 6b. WRITE-1 AND READ DATA TIME SLOT



Speed	t_{LOW1}	t_{DSO}	t_{HIGH1}	t_{SLOT}^*
Standard	$8\mu\text{s}$	$3\mu\text{s}$	$49\mu\text{s}$	$60\mu\text{s}$
Overdrive	$1\mu\text{s}$	$1\mu\text{s}$	$8\mu\text{s}$	$10\mu\text{s}$
Flexible	$8\mu\text{s}$ to $15\mu\text{s}$	$3\mu\text{s}$ to $10\mu\text{s}$	$49\mu\text{s}$	$60\mu\text{s}$ to $74\mu\text{s}$

Figure 6c. WRITE-0 TIME SLOT



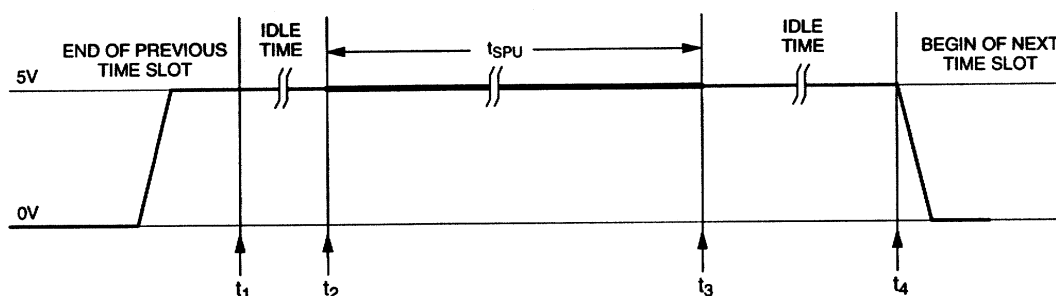
Speed	t_{LOW0}	t_{RECO}	t_{SLOT}^*
Standard	$57\mu\text{s}$	$3\mu\text{s}$	$60\mu\text{s}$
Overdrive	$7\mu\text{s}$	$3\mu\text{s}$	$10\mu\text{s}$
Flexible	$57\mu\text{s}$	$3\mu\text{s}$ to $10\mu\text{s}$	$60\mu\text{s}$ to $67\mu\text{s}$

*In a 5V environment ($\pm 1\text{V}$, full temperature range) the tolerance of the internal time base of 1-Wire slave devices is much narrower than what it is when operated at the minimum voltage of 2.8V. Therefore, the timing generated by the DS2480B is in compliance with the requirements of all 1-Wire/iButton 1-Wire devices.

PULSE WAVEFORMS, DISARMED

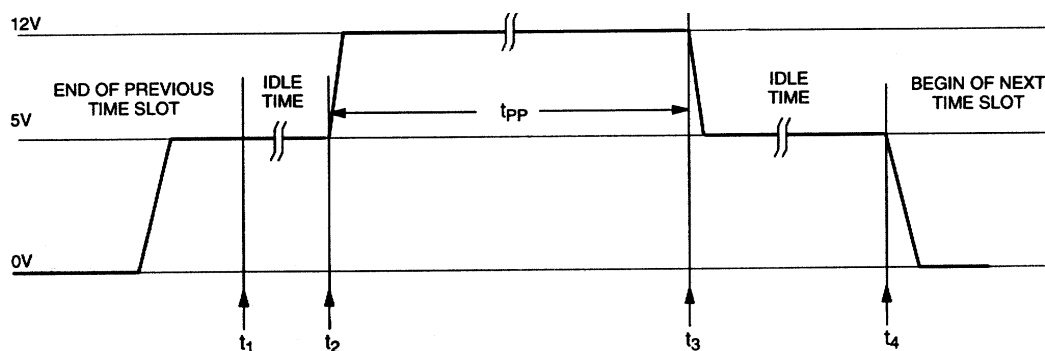
The Pulse command can be used to generate a strong pullup to 5V and a 12V programming pulse, respectively. The duration of the pulse is predefined if the parameter value code of parameter 010 (Programming Pulse Duration) has a value from 000 to 110, and parameter 011 (Strong Pullup Duration) has a value from 000 to 101 (see Table 4). Figures 7a and 7b show the timing of a pulse with predefined duration, which should be considered the normal case. If infinite duration is chosen (parameter value code 111), the host must terminate the Pulse command, as shown in Figures 7c and 7d. All versions of Figure 7 assume that bit 1 of the pulse command is 0, i.e., disarmed mode. See the *Communication Commands: Pulse* section for more details on possibilities of the Pulse command.

Figure 7a. STRONG PULLUP TO 5V, PREDEFINED DURATION



The processing of a pulse command is essentially the same, regardless if a strong pullup or a programming pulse is requested. At t_1 the host starts sending the pulse command byte. At t_2 the DS2480B has received the command and immediately generates the pulse. The pulse ends at t_3 and the DS2480B sends out the command response byte to inform the host that the command is completed. The idle time between t_1 and t_2 is determined by the time to transmit the command byte at the selected baud rate. The idle time between t_3 and t_4 is comprised of the time to transmit the response byte, plus the response time of the host plus the time to transmit the command and/or data to generate the next time slot.

Figure 7b. 12V PROGRAMMING PULSE, PREDEFINED DURATION



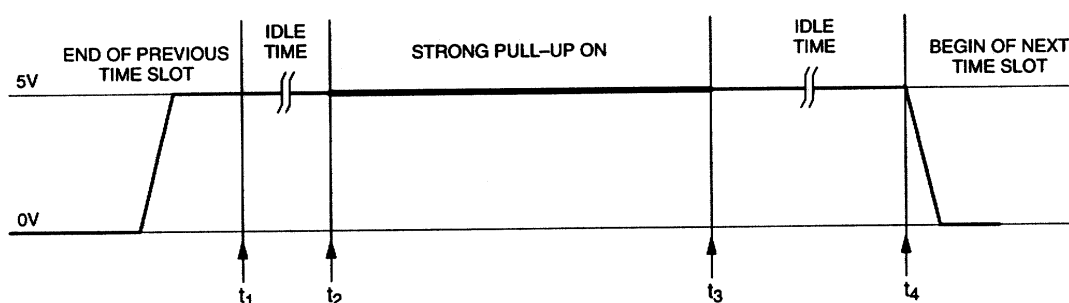
A correct programming pulse can only be generated if the 12V programming voltage is available at the V_{PP} pin of the DS2480B. The rising and falling edges of the programming pulse are actively controlled by DS2480B. The slew rate is approximately 14V/ μ s and meets the requirements of 1-Wire EPROM devices.

For EPROM programming, only a single slave device should be connected to the 1-Wire bus and the cable must be short, not to exceed a few meters. One should not attempt generating a programming pulse with a non-EPROM device on the bus; this may damage the device as well as the DS2480B.

Certain applications may require a duration for a strong pullup or programming pulse that cannot be realized using one of the predefined values. Selecting infinite duration allows the host to generate pulses of any length. As a consequence, however, the host becomes responsible to actively control the duration of the pulse. Failing to do so may require a power-on reset or master reset cycle of the DS2480B. For this reason, infinite duration should only be used if absolutely necessary.

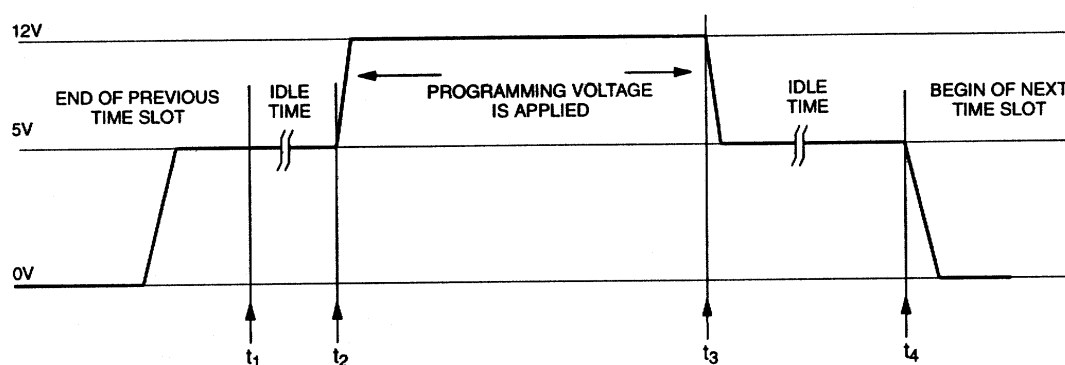
The time to end a pulse of infinite duration strongly depends on the baud rate of the communication between host and DS2480B. Neglecting the response time of the host, the minimum pulse durations are: 86.8 μ s at 115.2kbps, 173.6 μ s at 57.6kbps, 520 μ s at 19.2kbps, and 1.04ms at 9.6kbps.

Figure 7c. STRONG PULLUP TO 5V, INFINITE DURATION



As before, processing the command is essentially the same, regardless if it is for a strong pullup or a programming pulse. At t_1 the host starts sending the Pulse command byte. At t_2 the DS2480B has received the command and immediately activates the strong pullup or switches in the 12V programming voltage. To end the pulse, the DS2480B must receive a Termination command, code F1h, which occurs at t_3 . The Termination command does not generate a response byte. The DS2480B will immediately end the pulse and send out the response byte of the pulse command. The idle time between t_1 and t_2 is determined by the time to transmit the command byte at the selected baud rate. The idle time between t_3 and t_4 is comprised of the time to transmit the pulse response byte, plus the response time of the host plus the time to transmit the command and/or data to generate the next time slot.

Figure 7d. 12V PROGRAMMING PULSE, INFINITE DURATION



PULSE WAVEFORM, ARMED

As explained in the *Communication Commands* section, bit 1 of the Pulse command allows the arming of a strong pullup to 5V if the bit is set to 1. If the strong pullup is armed and the device is switched to Data Mode, there will be a strong pullup immediately following every byte on the 1-Wire bus. This mode is implemented to provide extra energy when writing to EEPROM devices or to do a temperature conversion with the DS1920 temperature iButton, for example. These devices need a strong pullup immediately after the power-consuming activity has been initiated by a command code.

To arm the strong pullup, one usually generates a “dummy” pulse with bit 1 being 1 while the device is in Command Mode. To save time, the dummy pulse may immediately be terminated by sending the Termination command, code F1h. Then one switches to Data Mode and sends a command code that makes one or more slaves on the 1-Wire bus require extra energy. After the command execution is finished, one switches back to Command Mode and disarms the strong pullup by generating another dummy pulse. A complete temperature conversion sequence that shows the use of the armed pulse is included in the *Software Driver Examples* section.

Figure 8. STRONG PULLUP TO 5V, ARMED, PREDEFINED DURATION

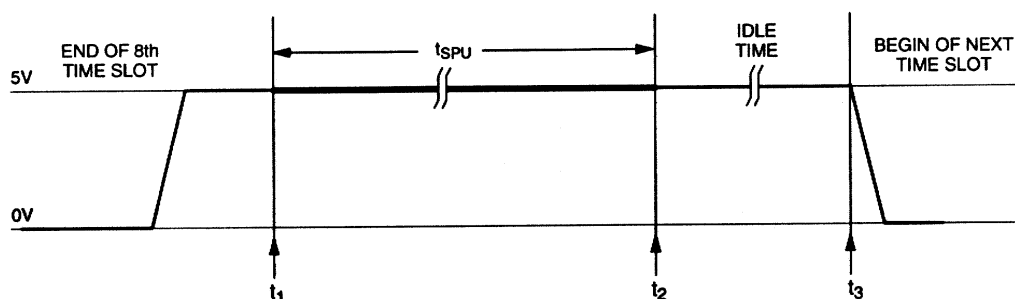


Figure 8 shows the timing of the strong pullup in Data Mode. At t_1 the 8th time slot of the byte sent to the 1-Wire bus is completed. Without any delay the DS2480B now activates the strong pullup and simultaneously starts sending the data response byte to the host. At t_2 the strong pullup ends and the DS2480B sends a pulse response byte to the host. The idle time between t_2 and t_3 is comprised of the time to transmit the pulse response byte, plus the response time of the host plus the time to transmit the command and/or data to generate the next time slot. Since in Data Mode the Pulse Termination command is not applicable, the duration of the strong pullup must be limited. See Table 4, parameter 011 (Strong Pullup Duration) for details.

Infinite duration, if accidentally selected, will require a power-on or master reset cycle to get the DS2480B back to communicating with the host.

SINGLE BIT WITH STRONG PULLUP

Similar to the Pulse command, the Single Bit command also allows generating a strong pullup immediately following a time slot. The strong pullup of the Single Bit command, however, is controlled directly by bit 1 of the command code and therefore needs not be armed. Since the DS2480B remains in Command Mode when using the Single Bit command, any duration of the strong pullup including infinite may be selected.

Figure 9a. SINGLE BIT WITH STRONG PULLUP, PREDEFINED DURATION

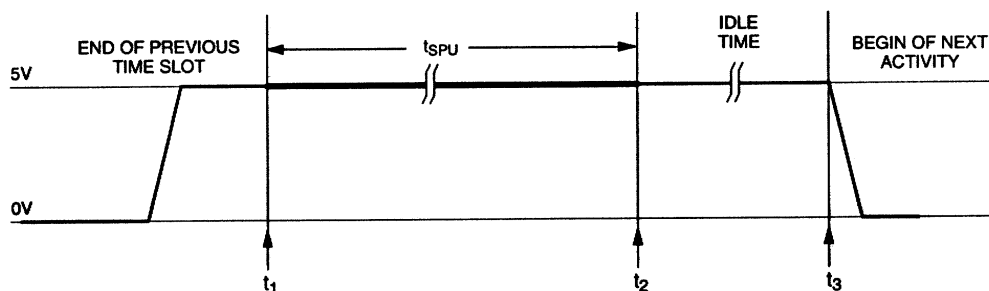
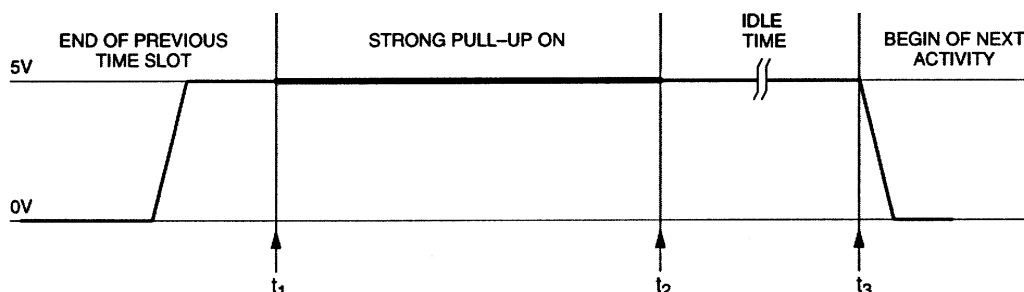


Figure 9 shows the timing of the Single Bit command immediately following strong pullup. For predefined duration (Figure 9a) the timing is as follows: At t_1 the time slot is completed. Now the DS2480B activates the strong pullup and simultaneously starts sending the response byte of the Single Bit command to the host. At t_2 the strong pullup ends and the DS2480B sends out a pulse response byte. The idle time between t_2 and t_3 is comprised of the time to transmit the pulse response byte, plus the response time of the host plus the time to transmit the command and/or data to generate the next time slot.

Figure 9b. SINGLE BIT WITH STRONG PULLUP, INFINITE DURATION



For infinite duration (Figure 9b) the strong pullup also begins immediately after the time slot is completed. To end the strong pullup, the DS2480B must receive a Termination command, code F1h, which occurs at t_2 . The termination command does not generate a response byte. The DS2480B will then immediately end the strong pullup and send out a pulse response byte. Everything else is the same as with predefined duration.

The minimum duration of a strong pullup of infinite duration strongly depends on the baud rate of the communication between host and DS2480B. The host must first receive the response byte of the Single Bit command, react to it and then transmit the termination command. Neglecting the host's response time, the shortest duration of an infinite strong pullup therefore is 173.6 μ s at 115.2kbps, 347.2 μ s at 57.6kbps, 1.04ms at 19.2kbps, and 2.08ms at 9.6kbps.

SOFTWARE DRIVER EXAMPLES

The DS2480B requires a software driver that translates the activities to be generated on the 1-Wire bus into the appropriate commands. The examples below cover typical situations, such as reading the ROM, writing to the scratchpad of a Memory iButton, reading the memory of a Memory iButton, programming an Add-Only iButton EPROM and performing a temperature conversion with the DS1920 temperature iButton. An example for the use of the Search Accelerator is included in the Search Accelerator section found earlier in this document.

The DS2480B command codes used in these examples are valid for standard speed and will work properly on short 1-Wire buses (<10m). The response byte on the reset command assumes a normal presence pulse, no alarm or short.

The DS2480B includes a 1-byte buffer that stores a byte received from the host while the previous byte is being translated into activity on the 1-Wire bus. For this reason the host may send another byte even without having received the response byte. Sending bytes faster than they can be translated into 1-Wire activities may result in loss of data and/or synchronization and therefore should be avoided.

READ ROM SEQUENCE

Action Sequence	Host TX	Host RX
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Read ROM Command	33	(as sent)
Read ROM ID (8 bytes)	FF (x8)	ROM ID
Set Command Mode	E3	(nothing)
Generate Reset Pulse	C1	CD or ED

WRITE SCRATCHPAD SEQUENCE

Write 2 bytes to scratchpad at memory locations 16h and 17h

Action Sequence	Host TX	Host RX
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Skip ROM Command	CC	CC
Write Scratchpad Command	0F	(as sent)
Starting Address TA1	16	(as sent)
Starting Address TA2	00	(as sent)
Write to the Scratchpad	(2 bytes)	(as sent)
Set Command Mode	E3	(nothing)
Generate Reset Pulse	C1	CD or ED

READ MEMORY SEQUENCE

Action Sequence	Host TX	Host RX
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Skip ROM Command	CC	CC
Read Memory Command	F0	(as sent)
Starting Address TA1	40	(as sent)
Starting Address TA2	00	(as sent)
Read 8 Bytes of Data	FF (x8)	(data)
Set Command Mode	E3	(nothing)
Generate Reset Pulse	C1	CD or ED

WRITE EPROM SEQUENCE (DS2505)

Write memory starting at address 40h

Action Sequence	Host TX	Host RX
Set Vpp dur. = 512μs	29	28
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Skip ROM Command	CC	(as sent)
Write Memory Command	0F	(as sent)
Starting Address TA1	40	(as sent)
Starting Address TA2	00	(as sent)
*** Send Data Byte	(data)	(as sent)
Receive CRC16	FF (x2)	CRC16
Set Command Mode	E3	(nothing)
Generate Program Pulse	FD	response
Set Data Mode	E1	(nothing)
Read Written Byte	FF	(data)
Go to *** to write the next byte or end the sequence as shown below		
Set Command Mode	E3	(nothing)
Generate Reset Pulse	C1	CD or ED

TEMPERATURE CONVERSION SEQUENCE

Action Sequence	Host TX	Host RX
Set pullup dur. = 524ms	39	38
Generate Reset Pulse	C1	CD or ED
Set Data Mode	E1	(nothing)
Skip ROM Command	CC	(as sent)
Set Command Mode	E3	(nothing)
Arm Strong Pullup	EF	(nothing)
Terminate Pulse	F1	response
Set Data Mode	E1	(nothing)
Convert Temperature	44	(as sent)
Wait for Pulse Response	(nothing)	response
Set Command Mode	E3	(nothing)
Disarm Strong Pullup	ED	(nothing)
Terminate Pulse	F1	response
Generate Reset Pulse	C1	CD or ED

HARDWARE APPLICATION EXAMPLES

This section discusses five typical application scenarios. The DS2480B can be configured for EPROM programming as well as for 5V operation only.

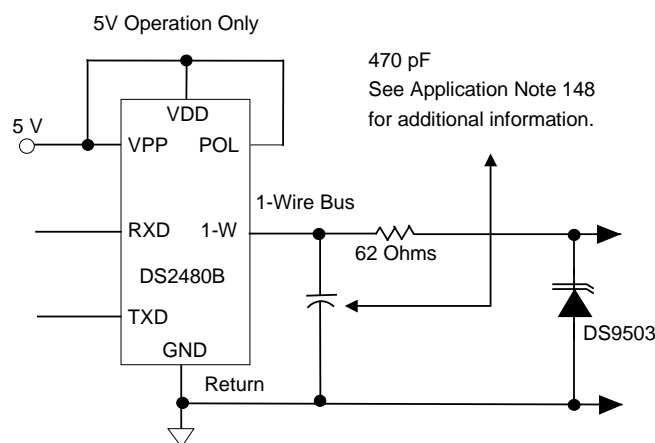
OUTPUT FILTERING

As described in the *CONTROLLED EDGES* section, the DS2480B employs an active pullup on the rising edges of the 1-Wire waveform.

Excessive noise on the 1-Wire line in the region of the pullup trip voltage, V_{IAPTO} , can cause an undesirable trip of the active pullup, which can disrupt 1-Wire communication. External R-C filtering as shown in Figure 10 should be added to all DS2480B configurations with the exception of those that perform EPROM programming.

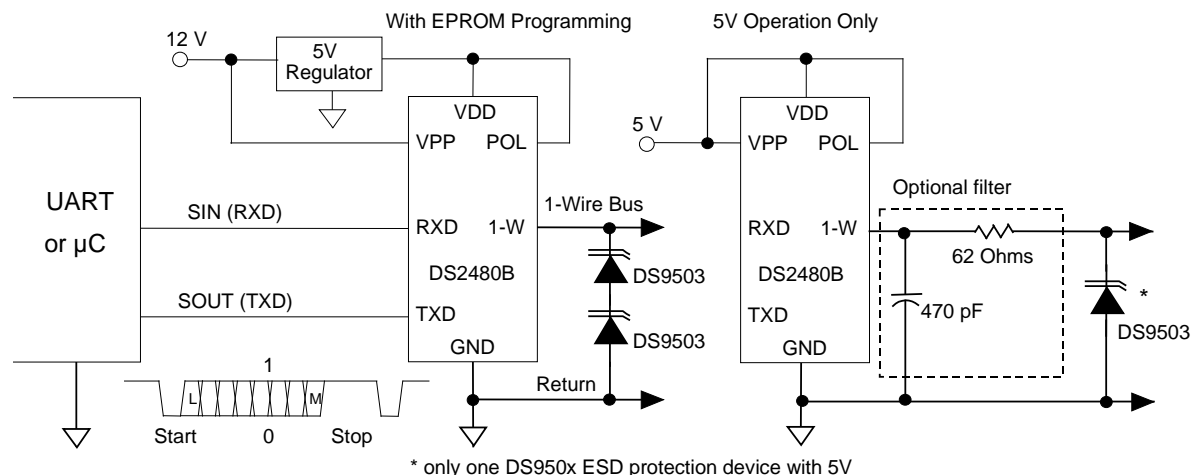
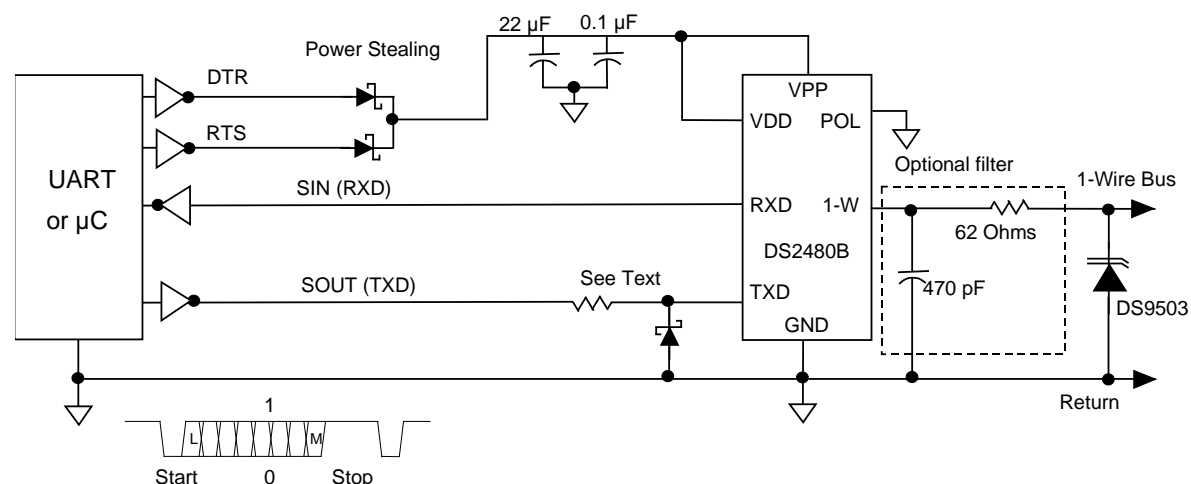
For EPROM programming configurations the R-C filter cannot be used due to the voltage drop that will develop across the 100Ω resistor during programming.

Figure 10. R-C FILTERING



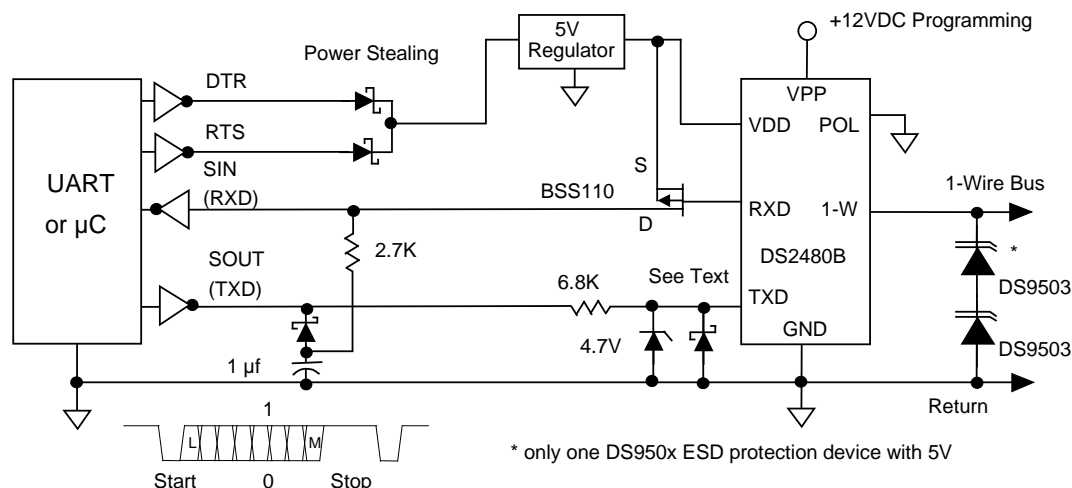
To protect the 1-Wire port of the DS2480B from electrostatic discharge it is recommended to use a low-capacitance ESD protection diode, such as the DS950x devices. For 5V operation a single device is sufficient. For EPROM programming two DS950x devices must be connected in series to achieve a high enough breakdown voltage.

Figures 11a-c are examples of connecting the DS2480B directly to a UART or RS232C interface. The circuit becomes more complex if a 1-Wire bus is to be interfaced to a port that provides and expects inverted signals, but does not necessarily meet the RS232C ($\pm 12V$) standard (Figure 11b).

Figure 11a. UART DIRECT**Figure 11b. $\pm 5V$ RS232**

The signals DTR and RTS provide the power to operate the DS2480B. The resistor in the TXD line and the Schottky diode limit the negative voltage at the TXD pin of the DS2480B to 0.3V maximum. The resistor is typically 4.7k Ω . If the inverting driver is current-limited to 1mA the resistor is not required.

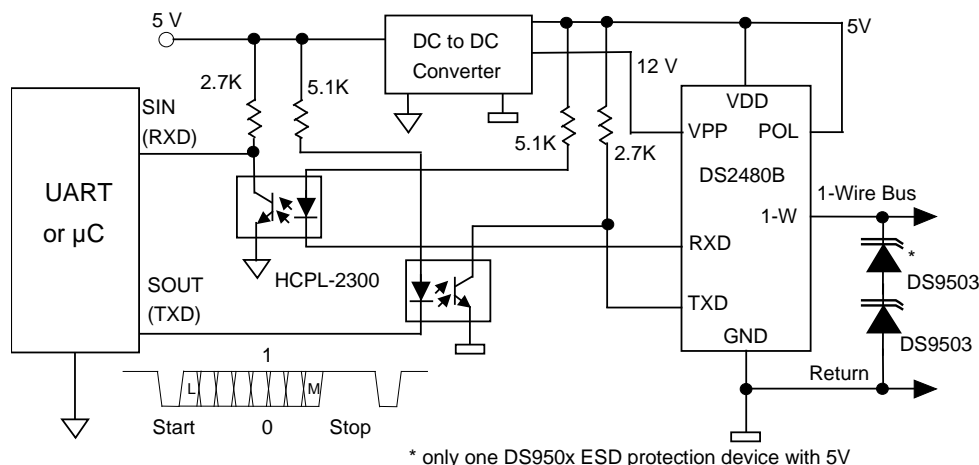
From the DS2480B's perspective, this circuit will work with inverted signals of $\pm 5V$ as well as 0 to 5V. Depending on the voltage levels the host expects, it may be necessary to generate a negative voltage on the RXD line. Figure 11c shows how this can be accomplished for a true RS232C system.

Figure 11c. $\pm 12\text{V}$ RS232

In the interface to a true RS232C system ($\pm 12\text{V}$, Figure 11c) the power for the DS2480B is stolen from DTR and RTS. The software must make sure that at least one of these signals constantly provides the 12V operating voltage. The 6.8k Ω resistor and the 4.7V Zener diode in the TXD line limit the positive voltage at the TXD pin of the DS2480B. The Schottky diode limits the negative voltage to 0.3V maximum. The Schottky diode in series with capacitor forms a parasitic supply to generate the negative bias for the host's receive channel. The positive signal is switched in through the P-channel MOSFET that connects to the RXD output of the DS2480B. In this circuit diagram the MOSFET switches the RXD line to +5V, which normally is sufficient for RS232C systems.

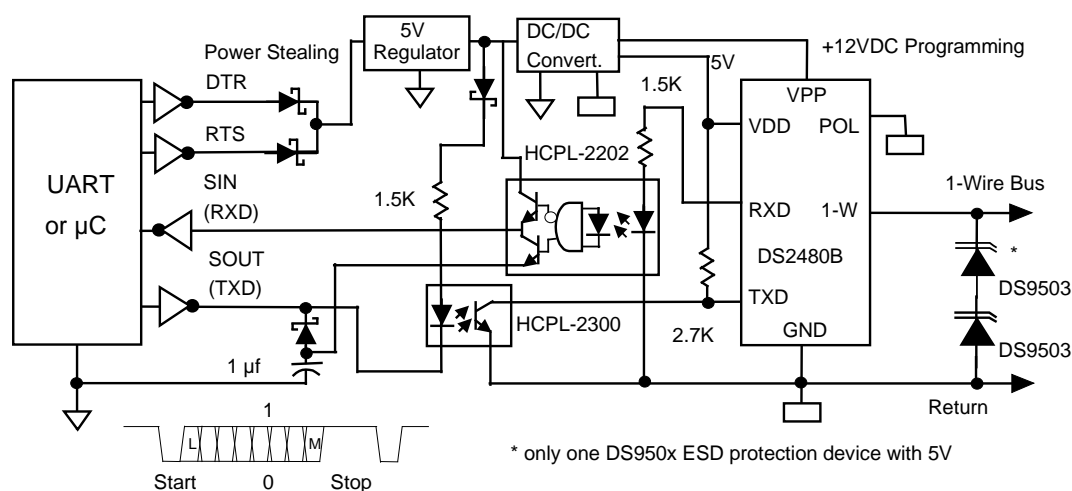
Switching to 12V is also possible, but requires a P-channel transistor with a different threshold voltage. The signal inversion caused by the transistor is compensated through the DS2480B by using a value code of 100, 101, 110, or 111 for the RS232 baud rate setting.

Figure 11d. UART DIRECT OPTO-ISOLATED



The circuit in Figure 11d is essentially the same as in Figure 11a. The main difference is the opto-isolation. The characteristics of the opto-isolators are not very critical. Using a different type will affect the values of the resistors that limit the current through the LEDs and bias the photo transistors.

Figure 11e. ± 5 TO 12V RS232 OPTO-ISOLATED



The circuit in Figure 11e combines the true RS232C interface with opto-isolation. The energy to power the LED in the TXD channel and to provide the positive voltage for the host's RXD input is stolen from DTR and RTS. The negative voltage for the RXD input is taken from the TXD line through a parasitic supply consisting of a Schottky diode in series with a capacitor. The HCPL-2202 opto-isolator has a totem pole output that allows switching in positive as well as negative voltage. The ± 5 V are sufficient for most RS232C systems. Switching in 12V requires an opto-isolator with different voltage characteristics.

In the schematic the HCPL-2202 opto-isolator is sourced by the RXD pin of the DS2480B. It can as well be connected the traditional way where the DS2480B sinks the current through the LED. This, however, causes a signal inversion that has to be compensated through the DS2480B by using a value code of 100, 101, 110, or 111 for the RS232 baud rate setting. Using other types of opto-isolators than shown in the schematic will at least require changing the values of the resistors.

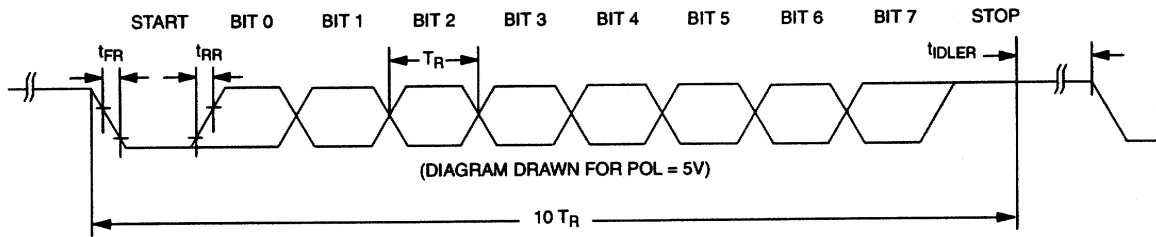
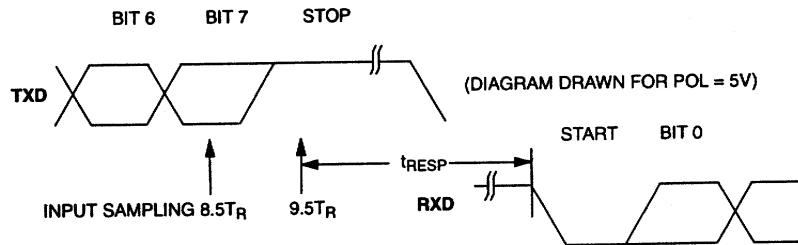
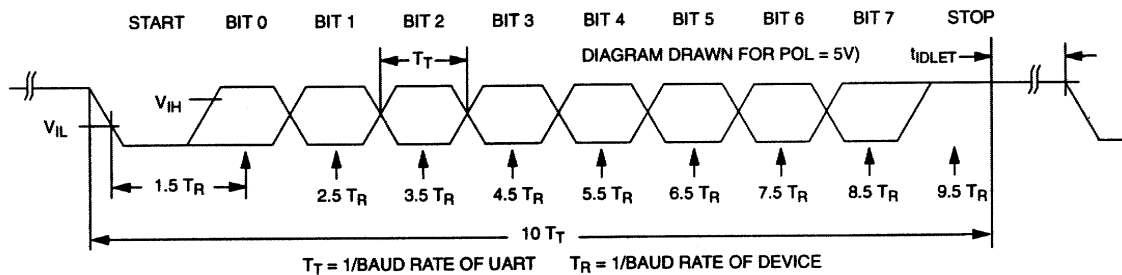
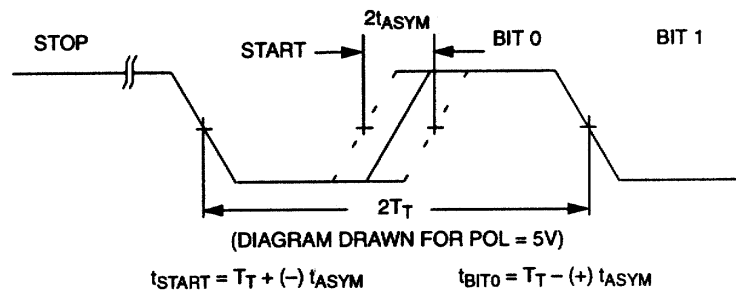
Figure 12. RS232 DATA TIMING RXD LINE**Figure 13. RECEIVE DELAY TIMING****Figure 14. RS232 DATA TIMING TXD LINE****Figure 15. TXD LINE ASYMMETRY**

Table 7. FUNCTION AND SPEED MATRIX

Baud Rate	1-Wire Speed			Function
	Standard	Flexible	Overdrive	
9600bps	√	√	√	Search
	√	√	√	Command/Data
19200bps	X	X	√	Search
	√	X	√	Command/Data
57600bps	X	X	√	Search
	X	X	√	Command/Data
115200bps	X	X	X	Search
	X	X	√	Command/Data

√ t_{IDLE} is guaranteed by the UART; no precautions necessary.

X Not recommended unless t_{IDLE} is controlled by the host through a wait function.

ABSOLUTE MAXIMUM RATINGS*

Voltage on 1-W to Ground	-0.5V to +14.0V
Voltage on VPP to Ground	-0.5V to +12.5V
Voltage on VDD, RXD, TXD, POL to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = 4.5V$ to $5.5V$; $-40^{\circ}C$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
Programming Voltage	V_{PP}		12.0	12.25	V	1
Operating Current	I_{DD}		3.0	5.0	mA	
Idle Current on V_{PP}	I_{PP}		20		μA	2
Active Pullup Timer Threshold	V_{IAPTO}	$V_{DD} - 1.4$	$V_{DD} - 1.1$		V	
Active Pullup On Threshold	V_{IAPO}		0.95	1.2	V	15
1-Wire Input High	V_{IH1}	3.4			V	
1-Wire Input Low	V_{IL1}			1.8	V	
TXD/POL Input Resistor	R_I	30			k Ω	3
TXD/POL Input Levels	V_{IH}	2.7			V	
TXD/POL Input Levels	V_{IL}			0.8	V	
1-Wire Weak Pullup Current	I_{WEAKPU}	1.5	3.0	5.4	mA	15
1-Wire Active Pullup Current	I_{ACTPU}	7	15		mA	
Strong Pullup Voltage Drop @ 10mA load on 1-W	ΔV_{STRPU}			0.6	V	4
Programming Voltage Drop @ 10mA load on 1-W	ΔV_{PROG}			0.30	V	5
RXD Sink Current @ 0.4V	I_{OLR}	6			mA	
RXD Source Current @ $V_{DD}-0.4V$	I_{OHR}	-4			mA	
Power On Reset Trip Point	V_{POR}			3.3	V	

CAPACITANCES ($T_A = 25^{\circ}C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TXD/POL Input Capacitance	C_{IN}		5		pF	17
1-Wire Input Capacitance	C_{IN1}		10		pF	17

AC ELECTRICAL CHARACTERISTICS ($V_{DD} = 4.5V$ to $5.5V$; $-40^{\circ}C$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
UART Bit Time	T_T	8.68		104	μs	6
Device Bit Time	T_R	8.68		104	μs	6, 7, 16
Fall Time RXD	t_{FR}	8		20	ns	8,17
Rise Time RXD	t_{RR}	13		27	ns	8,17
Transmit Idle Time	t_{IDLET}	0			μs	9
Receive Idle Time	t_{IDLER}		t_{IDLET}		μs	
Asymmetry	t_{ASYM}			1	μs	10
Arrival Response Time	t_{ARR}	4.4		52	μs	11
Master Reset Time	t_{MR}	104			μs	12
Active Pullup on Time	t_{APUOT}	0.5		2.0	μs	13
Response Time	t_{RESP}	$8.68 + \Delta$		$104 + \Delta$	μs	11, 14

NOTES:

- $V_{PP} - \Delta V_{PROG}$ must be within 11.5V to 12.0V.
- Applies only if a 12.0V supply is connected. If V_{PP} and V_{DD} are tied together, current is less than $1\mu A$.
- Input load is to GND.
- Voltage difference between V_{DD} and 1-W.
- Voltage difference between V_{PP} and 1-W.
- $8.68\mu s$ (115.2kbps), $52\mu s$ (19.2kbps), $17.36\mu s$ (57.6kbps), $104\mu s$ (9.6kbps).
- Nominal values; tolerance = $\pm 5\%$.
- At $V_{CC} = 5.0V$ and 100pF load to GND.
- See Table 7, *Function and Speed Matrix*.
- Independent of baud rate.
- Minimum at 115.2kbps, maximum at 9.6kbps.
- The master reset cycle is complete after t_{MR} is over.
- Minimum value at Overdrive speed; maximum value at standard speed.
- Δ is the time to complete the activity on the 1-Wire bus; values range from 0 (configuration command) up to $5130\mu s$ (alarming presence pulse).
- With standard and flexible speed the total capacitive load of the 1-Wire bus should not exceed 20nF, otherwise the active pullup on threshold V_{IAPO} may not be reached in the available time. With Overdrive speed the capacitive load on the 1-Wire bus must not exceed 1nF.
- Baud rate calibration is valid at a static V_{DD} operating point. Post calibration changes in V_{DD} by more than 5% may cause calibration error to exceed 5%. The DS2480B requires a 1-Wire reset command sent by the host at a data rate of 9600bps for calibration. Data rates of 115200bps or higher during calibration may put the DS2480B in an undefined state, requiring a power-down reset to restore normal operation.
- Not production tested.

Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8+5	21-0041

REVISION DATE	DESCRIPTION	PAGES CHANGED
3/17/99	Initial release	—
10/19/99	Removed preliminary status, deleted V_{PPmin} spec, changed $\Delta V_{PROGMAX}$ to 0.30V	29
7/1/03	Changing the Communication Command Response Bit 5 to Don't Care status.	7
8/20/04	Added references to Application Note 192. Clarification in the second paragraph of the Device Operation section. Removed references to DOS from the search accelerator introduction. Appended to EC table note 16: <i>The DS2480B requires a 1-Wire reset command sent by the host at a data rate of 9600bps for calibration. Data rates of 115200bps or higher during calibration may put the DS2480B in an undefined state, requiring a power-down reset to restore normal operation.</i>	2 3 8 31
5/10	Conversion to lead free, using “standard” instead of “regular” when referring to the slower 1-Wire speed, removal of load sensor (dynamic duration) as a feature, correction in Figures 10, 11a, 11b (filter capacitor moved to the left of the resistor, filter resistor changed from 100 Ω to 62 Ω), correction of minor oversights and style updates. EC table: added <i>Voltage on VPP to Ground</i> to Absolute Maximum Ratings, deleted V_{PP} senspr trip point, changed $I_{WEAKPUMAX}$ from 5.0 to 5.4 mA, changed $I_{ACTPUMIN}$ from 9 to 7 mA.	Various 31
4/15	Updated <i>Benefits and Features</i> section	1