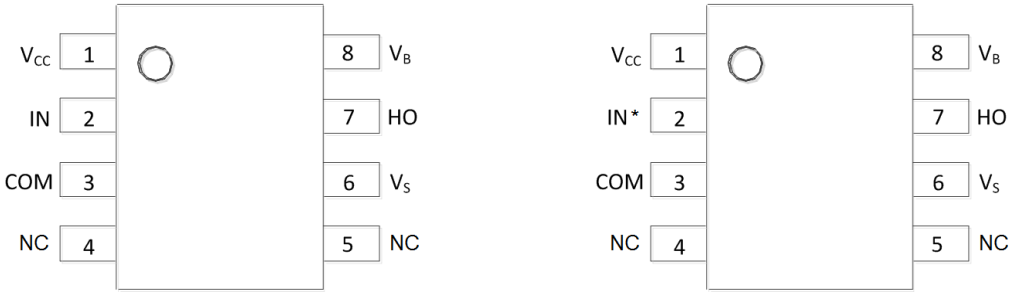
Pin Diagrams



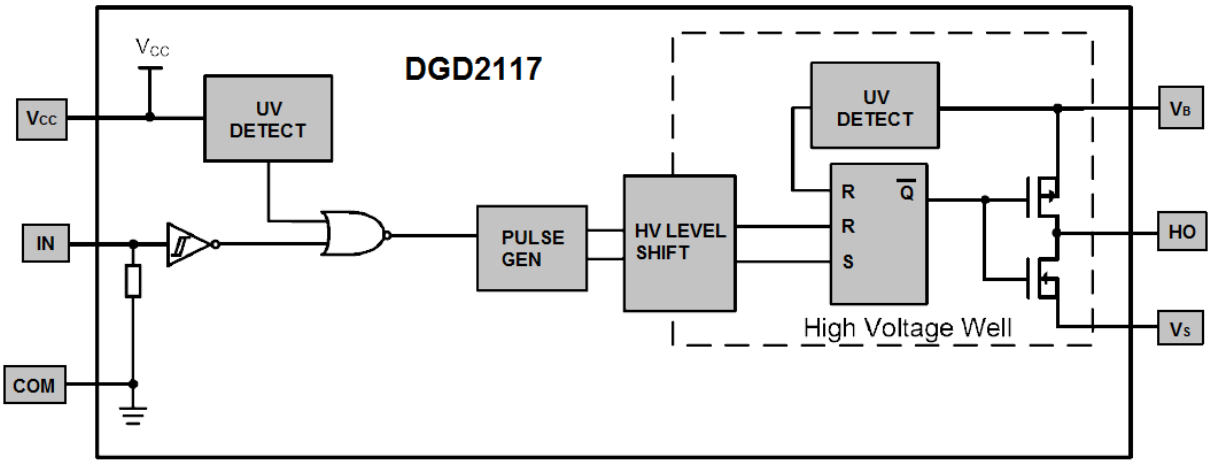
DGD2117 DGD2118

Top View SO-8

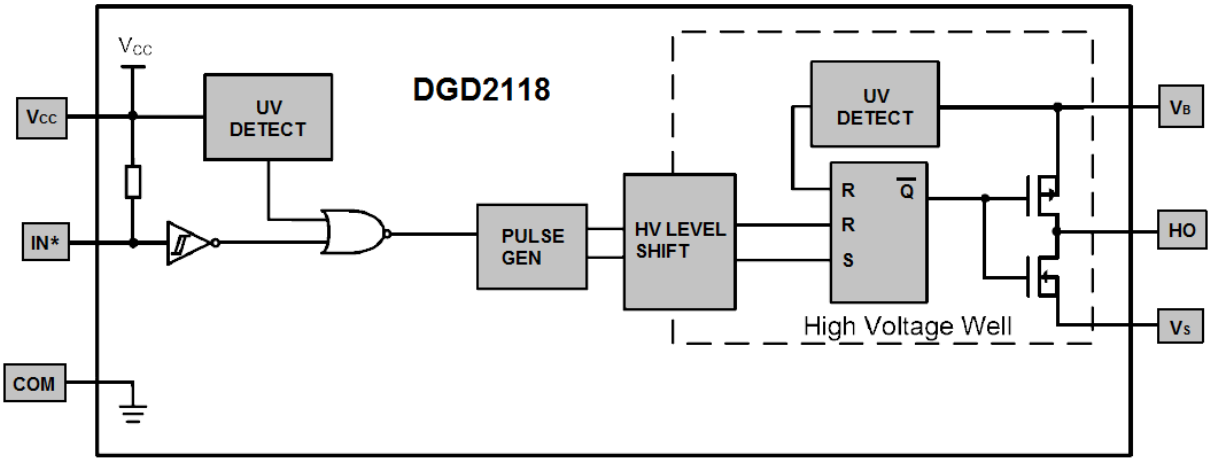
Pin Descriptions

Pin Number	Pin Name	Function
1	V_{CC}	Logic and gate driver supply
2	IN	DGD2117 Logic input for gate driver output (HO), in phase with HO
2	IN*	DGD2118 Logic input for gate driver output (HO), out of phase with HO
3	COM	Logic ground
4, 5	NC	No Connection (No Internal Connection)
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

Functional Block Diagram



Functional Block Diagram (continued)



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V_B	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	V_S	V_B-24 to V_B+0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S-0.3 to V_B+0.3	V
Logic Supply Voltage	V_{CC}	-0.3 to +24	V
Logic Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Allowable Offset Supply Voltage Transient	dV_S / dt	50	V/ns

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P_D	0.625	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	45	°C/W
Operating Temperature	T_J	+150	°C
Lead Temperature (Soldering, 10s)	T_L	+300	
Storage Temperature Range	T_{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	V_B	V_S + 10	V_S + 20	V
High Side Floating Supply Offset Voltage	V_S	(Note 6)	600	V
High Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Low Side and Logic Fixed Supply Voltage	V_{CC}	10	20	V
Logic Input Voltage	V_{IN}	0	V_{CC}	V
Ambient Temperature	T_A	-40	+125	°C

Note: 6. Logic operation for V_S = -5V to +600V.

DC Electrical Characteristics (V_{BIAS} (V_{CC}, V_{BS}) = 15V, @T_A = +25°C, unless otherwise specified.) (Note 7)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Logic "1" (DGD2117) & Logic "0" (DGD2118) Input Voltage (Note 8)		V_{IH}	9.5	—	—	V	—
Logic "0" (DGD2117) & Logic "1" (DGD2118) Input Voltage (Note 8)		V_{IL}	—	—	6.0	V	—
High Level Output Voltage, V_{BIAS} - V_O		V_{OH}	—	0.05	0.2	V	I_O = 2mA
Low Level Output Voltage, V_O		V_{OL}	—	0.02	0.1	V	I_O = 2mA
Offset Supply Leakage Current		I_{LK}	—	—	50	µA	V_B = V_S = 600V
Quiescent V_{BS} Supply Current		I_{BSQ}	—	50	240	µA	V_{IN} = 0V or V_{CC}
Quiescent V_{CC} Supply Current		I_{CCQ}	—	70	340	µA	V_{IN} = 0V or V_{CC}
Logic "1" Input Bias Current	DGD2117	I_{IN+}	—	20	40	µA	V_{IN} = V_{CC}
	DGD2118						V_{IN} = 0V
Logic "0" Input Bias Current	DGD2117	I_{IN-}	—	—	5.0	µA	V_{IN} = 0V
	DGD2118						V_{IN} = V_{CC}
V_{BS} Supply Under-Voltage Positive Going Threshold		V_{BSUV+}	7.6	8.6	9.6	V	—
V_{BS} Supply Under-Voltage Negative Going Threshold		V_{BSUV-}	7.2	8.2	9.2	V	—
V_{CC} Supply Under-Voltage Positive Going Threshold		V_{CCUV+}	7.6	8.6	9.6	V	—
V_{CC} Supply Under-Voltage Negative Going Threshold		V_{CCUV-}	7.2	8.2	9.2	V	—
Output High Short Circuit Pulsed Current		I_{O+}	200	290	—	mA	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10µs
Output Low Short Circuit Pulsed Current		I_{O-}	420	600	—	mA	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10µs

Notes: 7. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to the logic input pins: IN and IN*. The V_O and I_O parameters are referenced to COM and are applicable to the output pin: HO.
8. For optimal operation, it is recommended that the input pulses (IN and IN*) should have a minimum amplitude of 9.5V with a minimum pulse width of 250ns.

AC Electrical Characteristics (V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Turn-On Propagation Delay	t_{ON}	—	125	200	ns	V_S = 0V
Turn-Off Propagation Delay	t_{OFF}	—	105	180	ns	V_S = 600V
Turn-On Rise Time	t_r	—	75	130	ns	—
Turn-Off Fall Time	t_f	—	35	65	ns	—

Timing Waveforms

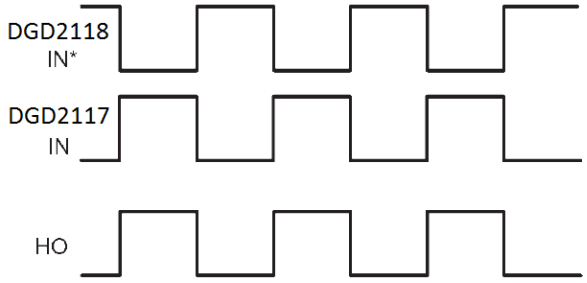


Figure 1. Input / Output Timing Diagram

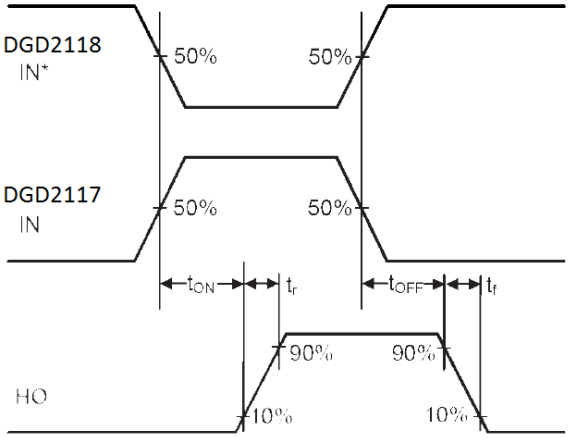


Figure 2. Switching Time Waveform Definitions

Typical Performance Characteristics (V_{CC} = 15V, @T_A = +25°C, unless otherwise specified.)

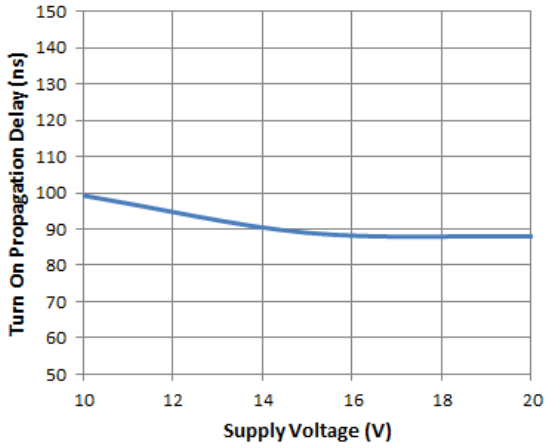


Figure 3. Turn-on Propagation Delay vs. Supply Voltage

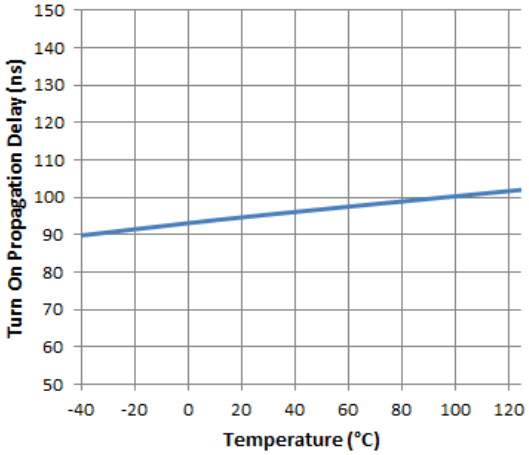


Figure 4. Turn-on Propagation Delay vs. Temperature

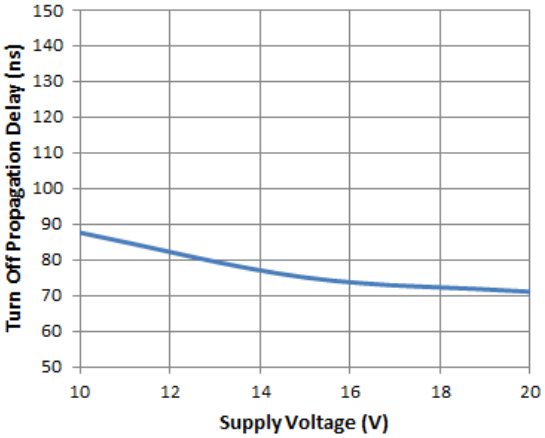


Figure 5. Turn-off Propagation Delay vs. Supply Voltage

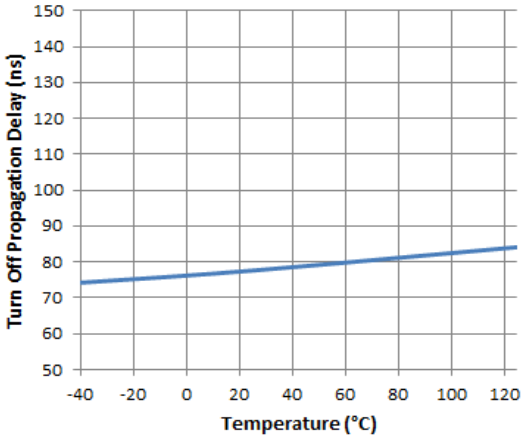


Figure 6. Turn-off Propagation Delay vs. Temperature

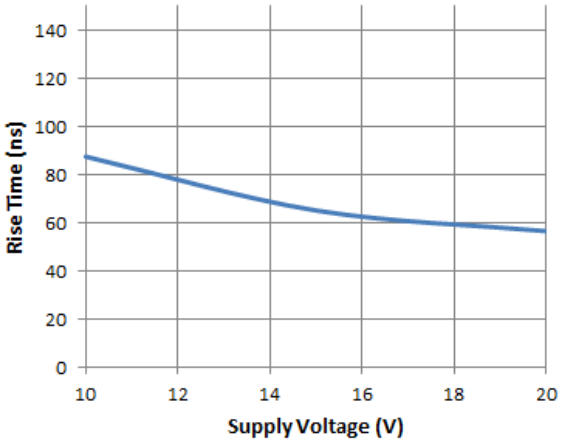


Figure 7. Rise Time vs. Supply Voltage

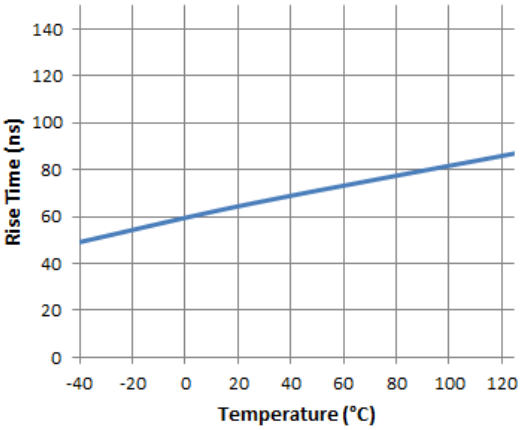


Figure 8. Rise Time vs. Temperature

Typical Performance Characteristics (continued)

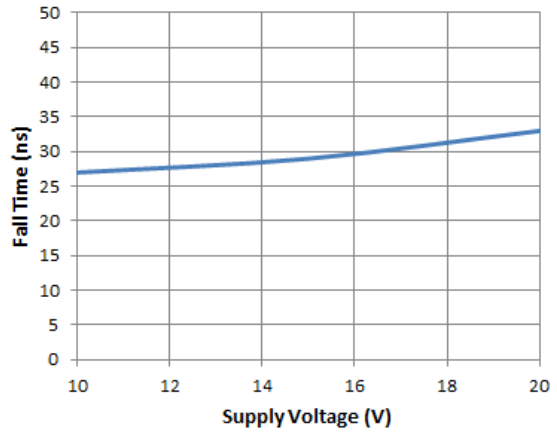


Figure 9. Fall Time vs. Supply Voltage

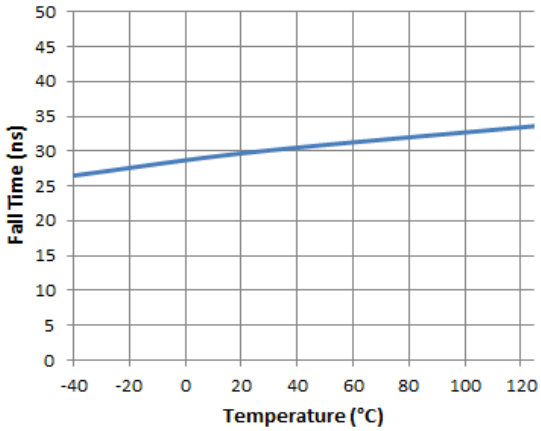


Figure 10. Fall Time vs. Temperature

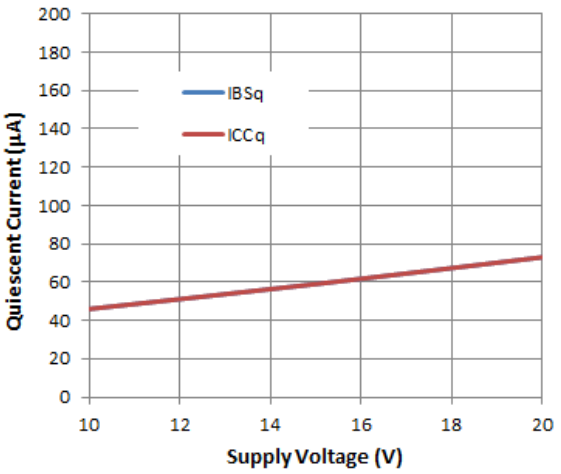


Figure 11. Quiescent Current vs. Supply Voltage

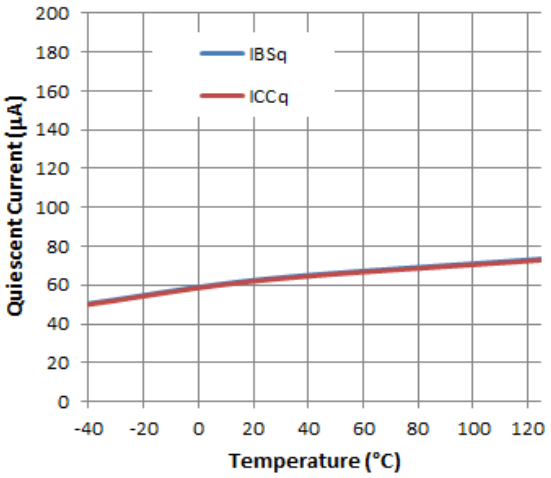


Figure 12. Quiescent Current vs. Temperature

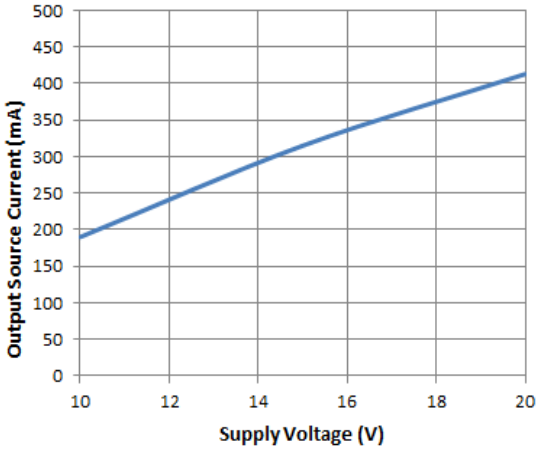


Figure 13. Output Source Current vs. Supply Voltage

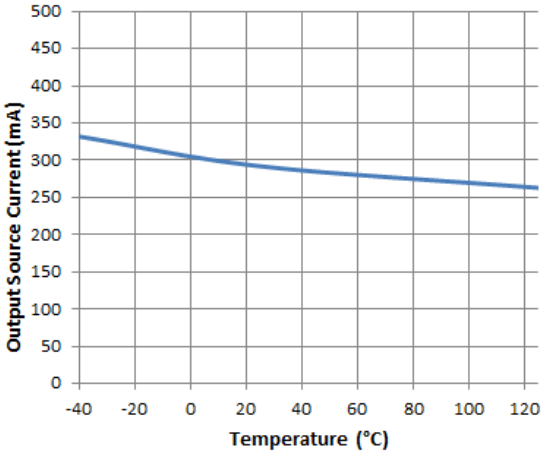


Figure 14. Output Source Current vs. Temperature

Typical Performance Characteristics (continued)

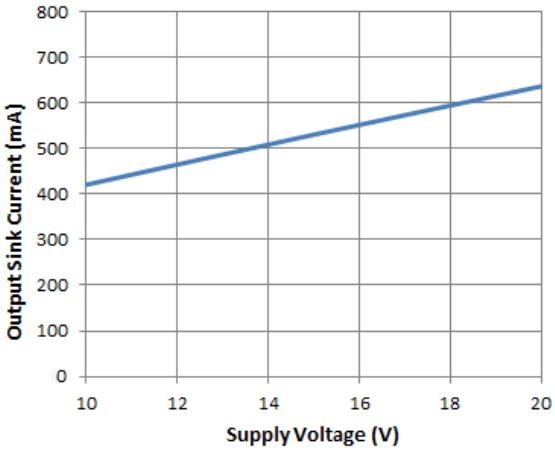


Figure 15. Output Sink Current vs. Supply Voltage

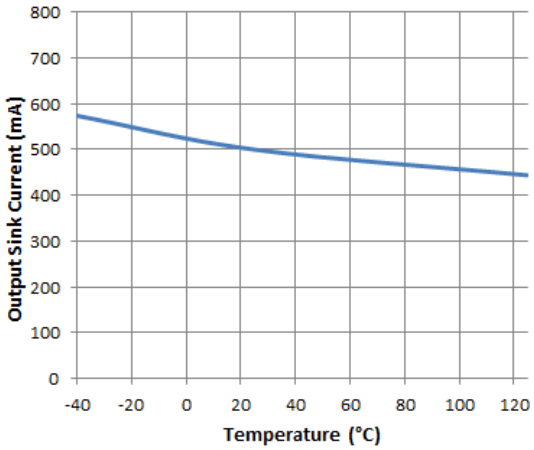


Figure 16. Output Sink Current vs. Temperature

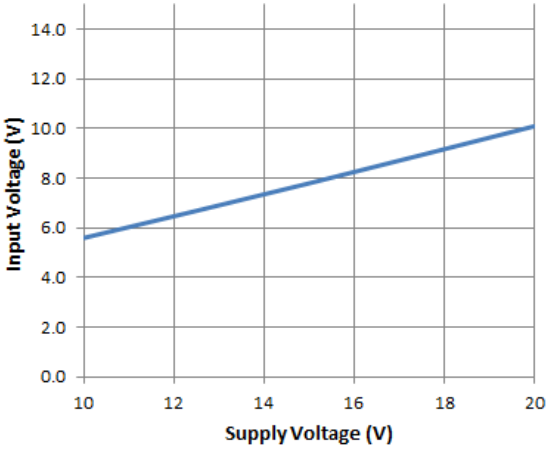


Figure 17. DGD2117 Logic 1 (DGD2118 Logic 0) Input Voltage vs. Supply Voltage

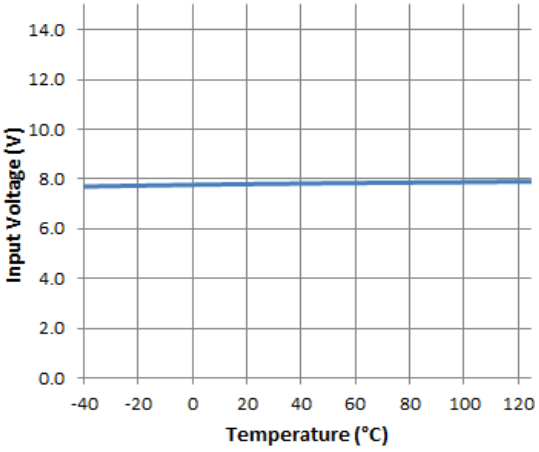


Figure 18. DGD2117 Logic 1 (DGD2118 Logic 0) Input Voltage vs. Temperature

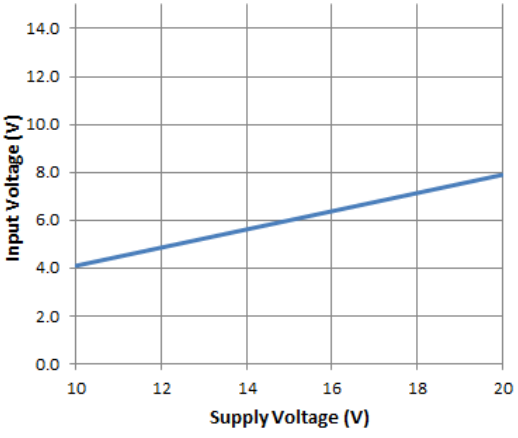


Figure 19. DGD2117 Logic 0 (DGD2118 Logic 1) Input Voltage vs. Supply Voltage

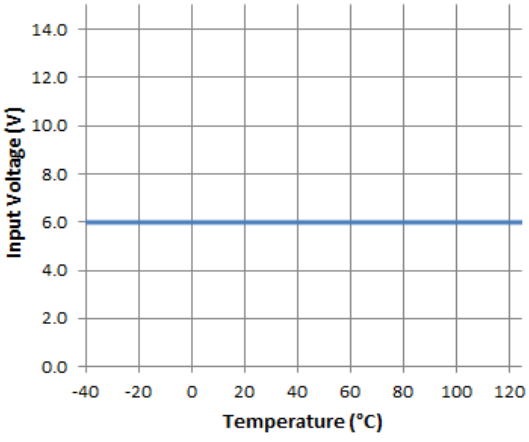


Figure 20. DGD2117 Logic 0 (DGD2118 Logic 1) Input Voltage vs. Temperature

Typical Performance Characteristics (continued)

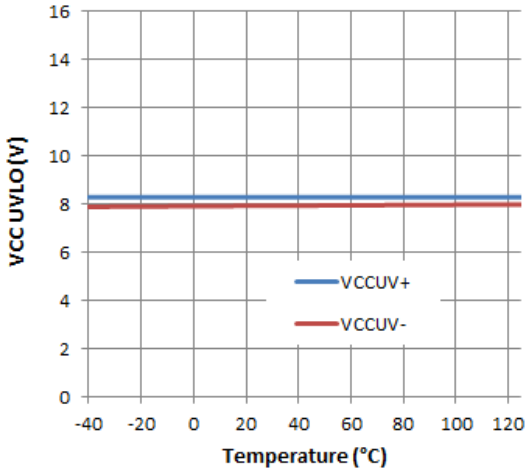


Figure 21. VCC UVLO vs. Temperature

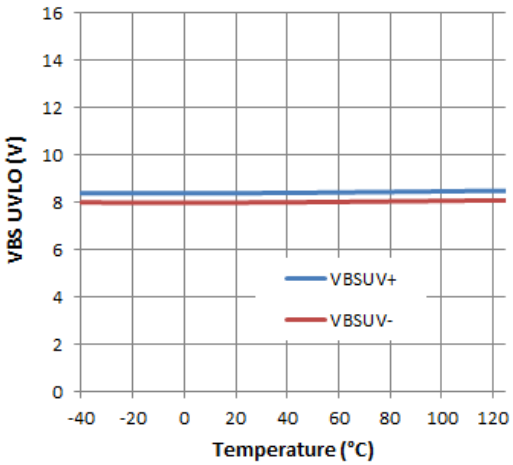


Figure 22. VBS UVLO vs. Temperature

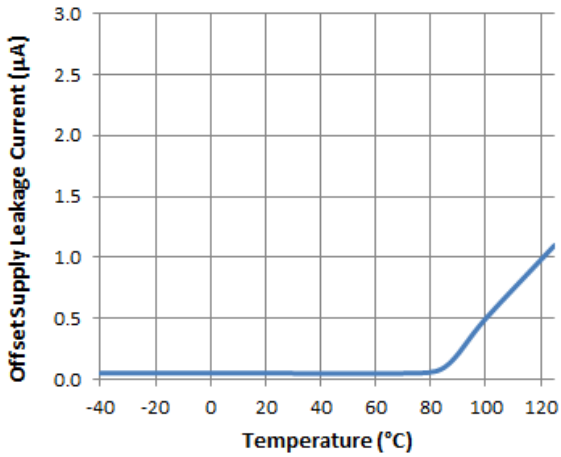
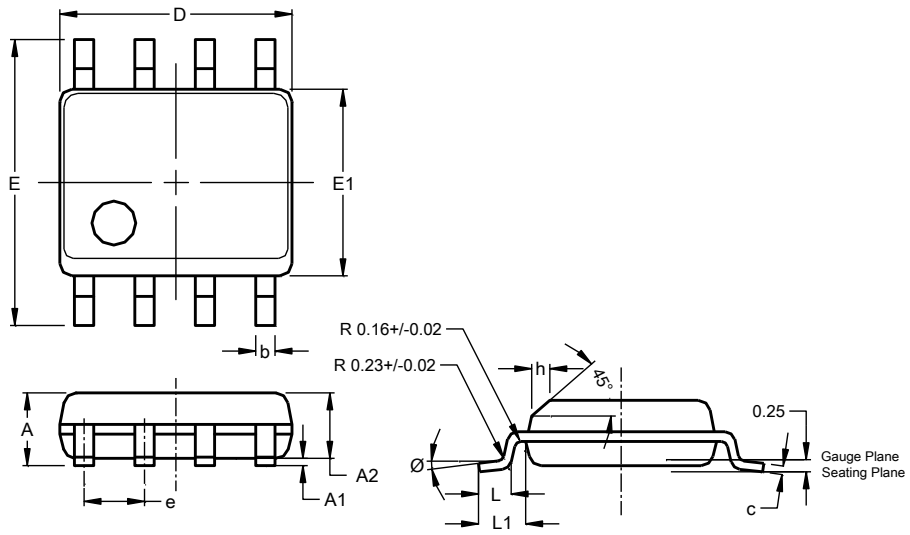


Figure 23. Offset Supply Leakage Current vs. Temperature

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type TH)

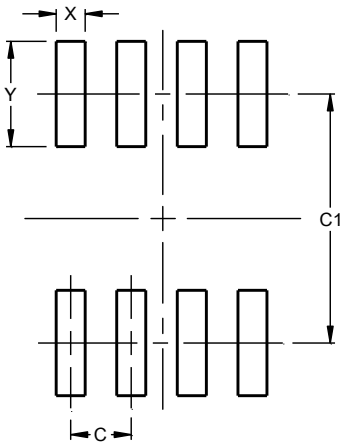


SO-8 (Type TH)			
Dim	**Min**	**Max**	**Typ**
A	1.35	1.75	--
A1	0.10	0.25	--
A2	--	--	1.45
b	0.35	0.51	--
c	0.190	0.248	--
D	4.80	5.00	4.90
E	5.80	6.20	6.00
E1	3.80	4.00	3.90
e	--	--	1.27
h	0.25	0.50	--
L	0.41	1.27	--
L1	--	--	1.04
Ø	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type TH)



Dimensions	Value (in mm)
C	1.27
C1	5.20
X	0.60
Y	2.20

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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