

Improved, SPST/SPDT Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+	44V
GND	25V
VL	(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs V _S , V _D (Note 1)	(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) (Note 1)	30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)	100mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW
CERDIP (derate 8.00mW/°C above +70°C)	640mW

Operating Temperature Ranges

DG41_C_	0°C to +70°C
DG41_D_	-40°C to +85°C
DG41_AK	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS		
SWITCH											
Analog Signal Range	V _S , V _D	(Note 3)				-15		15	V		
Drain-Source On-Resistance	R _{DS(ON)}	V+ = 13.5V, V- = -13.5V, V _D = ±10V, I _S = -10mA		T _A = +25°C	C, D	20		35	Ω		
					A	20		30			
				T _A = T _{MIN} to T _{MAX}							45
On-Resistance Match Between Channels (Note 4)	ΔR _{DS(ON)}	V+ = 15V, V- = -15V, V _D = ±10V, I _S = -10mA		T _A = +25°C				3	Ω		
				T _A = T _{MIN} to T _{MAX}				4			
On-Resistance Flatness (Note 4)	R _{FLAT(ON)}	V+ = 15V, V- = -15V, V _D = ±5V, I _S = -10mA		T _A = +25°C				4	Ω		
				T _A = T _{MIN} to T _{MAX}				6			
Source-Off Leakage Current (Note 5)	I _{S(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ∓15.5V		T _A = +25°C		-0.25		0.25	nA		
				T _A = T _{MIN} to T _{MAX}	C, D		-5			5	
					A		-20			20	
Drain-Off Leakage Current (Note 5)	I _{D(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ∓15.5V		DG417/ DG418	T _A = +25°C		-0.25	0.1	0.25	nA	
					T _A = T _{MIN} to T _{MAX}	C, D		-5			5
						A		-20			20
				DG419	T _A = +25°C		-0.75	-0.1	0.75		
					T _A = T _{MIN} to T _{MAX}	C, D		-10			10
						A		-40			40
Drain-On Leakage Current (Note 5)	I _{D(ON)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ±15.5V		DG417/ DG418	T _A = +25°C		-0.4		0.4	nA	
					T _A = T _{MIN} to T _{MAX}	C, D		-10			10
						A		-40			40
				DG419	T _A = +25°C		-0.75		0.75		
					T _A = T _{MIN} to T _{MAX}	C, D		-10			10
						A		-40			40

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DG417/DG418/DG419

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, VINL = 0.8V, VINH = 2.4V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Logic Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V		-0.5	0.005	0.5	μA
Logic Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V		-0.5	0.005	0.5	μA
DYNAMIC							
Turn-On Time	t _{ON}	DG417/DG418, V _D = ±10V, Figure 2	T _A = +25°C	100	175	ns	
			T _A = T _{MIN} to T _{MAX}	250			
Turn-Off Time	t _{OFF}	DG417/DG418, V _D = ±10V, Figure 2	T _A = +25°C	60	145	ns	
			T _A = T _{MIN} to T _{MAX}	210			
Transition Time	t _{TRANS}	DG419, V _S = ±10V, Figure 3	T _A = +25°C	175		ns	
			T _A = T _{MIN} to T _{MAX}	250			
Break-Before-Make Interval	t _D	DG419, V _{S1} = V _{S2} = ±10V, Figure 4, T _A = +25°C		5	13	ns	
Charge Injection (Note 3)	Q	V _{GEN} = 0V, Figure 5, T _A = +25°C		3	10	pC	
Off-Isolation Rejection Ratio (Note 6)	OIRR	R _L = 500Ω, C _L = 5pF, f = 1MHz, Figure 6, T _A = +25°C		68		dB	
Crosstalk (Note 7)		DG419, R _L = 50Ω, C _L = 5pF, f = 1MHz, Figure 7, T _A = +25°C		85		dB	
Drain Off-Capacitance	C _D (OFF)	V _D = 0V, f = 1MHz, Figure 8, T _A = +25°C		8		pF	
Source Off-Capacitance	C _S (OFF)	V _D = 0V, f = 1MHz, Figure 8, T _A = +25°C		8		pF	
Drain-Source On-Capacitance	C _D (ON) or C _S (ON)	V _S = 0V, f = 1MHz, Figure 9, T _A = +25°C	DG417/DG418	30		pF	
			DG419	35			
SUPPLY							
Positive Supply Current	I ⁺	V ⁺ = 16.5V, V ⁻ = -16.5V, V _{IN} = 0V or 5V	T _A = +25°C	-1	-0.0001	1	μA
			T _A = T _{MIN} to T _{MAX}	-5	5		
Negative Supply Current	I ⁻	V ⁺ = 16.5V, V ⁻ = -16.5V, V _{IN} = 0V or 5V	T _A = +25°C	-1	-0.0001	1	μA
			T _A = T _{MIN} to T _{MAX}	-5	5		
Logic Supply Current	I _L	V ⁺ = 16.5V, V ⁻ = -16.5V, V _{IN} = 0V or 5V	T _A = +25°C	-1	-0.0001	1	μA
			T _A = T _{MIN} to T _{MAX}	-5	5		
Ground Current	I _{GND}	V ⁺ = 16.5V, V ⁻ = -16.5V, V _{IN} = 0V or 5V	T _A = +25°C	-1	-0.0001	1	μA
			T _A = T _{MIN} to T _{MAX}	-5	5		

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ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, VL = 5V, GND = 0V, VINH = 2.4V, VINL = 0.8V, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	VANALOG	(Note 3)	0		12	V
Drain-Source On-Resistance	RDS(ON)	IS = -10mA, VD = 3.8V, V+ = 10.8V		40	100	Ω
DYNAMIC						
Turn-On Time	tON	DG417/DG418, VD = 8V, Figure 2		110		ns
Turn-Off Time	tOFF	DG417/DG418, VD = 8V, Figure 2		40		ns
Break-Before-Make Interval	tD	DG419, RL = 1000Ω, CL = 35pF, Figure 4		60		ns
Charge Injection (Note 3)	Q	CL = 10nF, VGEN = 0V, RGEN = 0V, Figure 5		2	10	pC
SUPPLY						
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, VL = 5.25V, VIN = 0V or 5V		-0.0001		μA
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, VL = 5.25V, VIN = 0V or 5V		-0.0001		μA
Logic Supply Current	IL	All channels on or off, VL = 5.25V, VIN = 0V or 5V		-0.0001		μA
Ground Current	IGND	All channels on or off, VL = 5.25V, VIN = 0V or 5V		-0.0001		μA

Note 2: Typical values are for **design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

Note 5: Leakage parameters IS(OFF), ID(OFF), and ID(ON) are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off-Isolation Rejection Ratio = 20log (VD/VS), VD = output, VS = input to off switch.

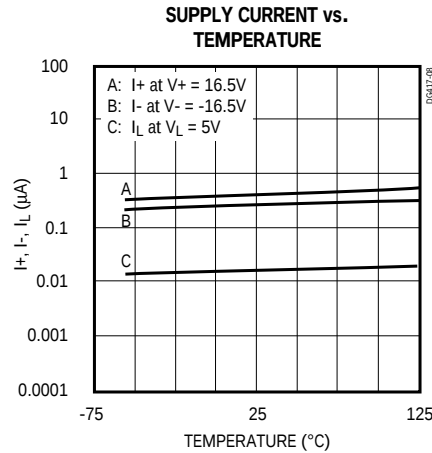
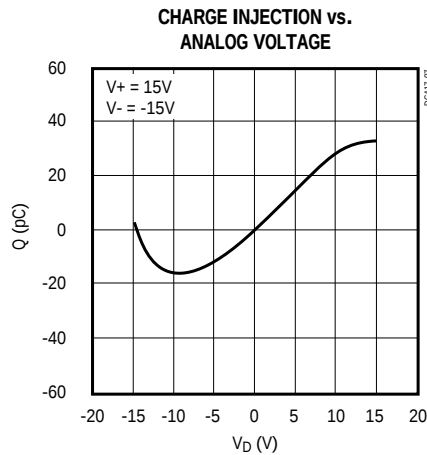
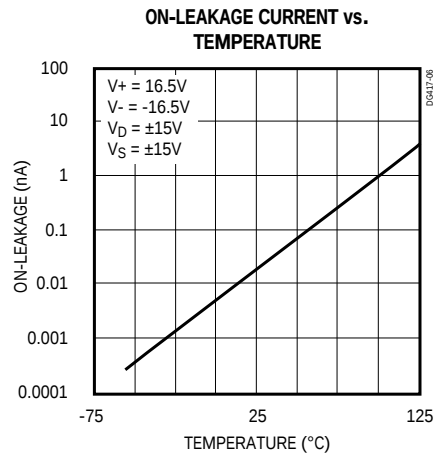
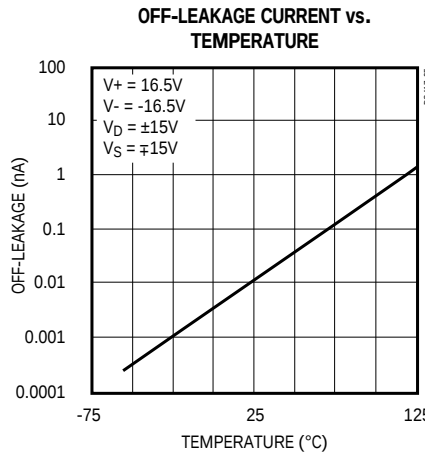
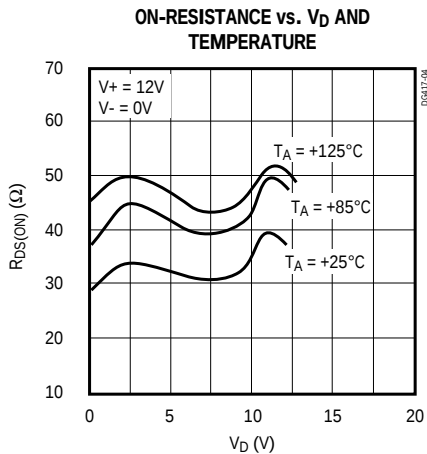
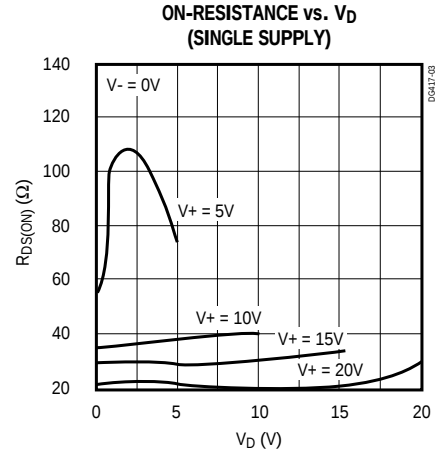
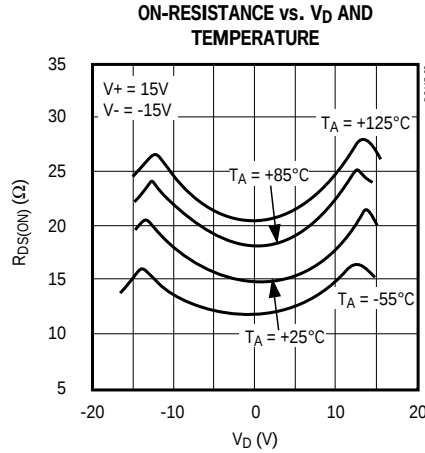
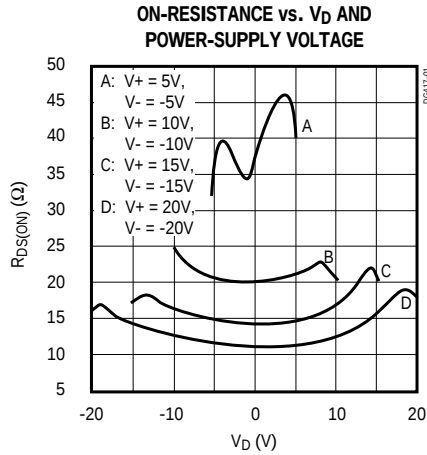
Note 7: Between any two switches.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

DG417/DG418/DG419



Improved, SPST/SPDT Analog Switches

Pin Description

PIN			NAME	FUNCTION
DG417	DG418	DG419		
1	—	—	S	Analog-Switch Source Terminal (normally closed)
—	1	—	S	Analog-Switch Source Terminal (normally open)
—	—	2	S1	Analog-Switch Source Terminal 1 (normally closed)
2	2	—	N.C.	No Internal Connection
3	3	3	GND	Logic Ground
4	4	4	V+	Analog-Signal Positive Supply Input
5	5	5	VL	Logic-Level Positive Supply Input
6	6	6	IN	Logic-Level Input
7	7	7	V-	Analog-Signal Negative Supply Input
8	8	1	D	Analog-Switch Drain Terminal
—	—	8	S2	Analog-Switch Source Terminal 2 (normally open)

Applications Information

Operation with Supply Voltages Other than $\pm 15V$

Using supply voltages other than $\pm 15V$ reduces the analog signal range. The DG417/DG418/DG419 switches operate with $\pm 4.5V$ to $\pm 20V$ bipolar supplies or with a $+10V$ to $+30V$ single supply; connect V^- to $0V$ when operating with a single supply. Also, all device types can operate with unbalanced supplies, such as $+24V$ and $-5V$. VL must be connected to $+5V$ to be TTL compatible, or to V^+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with $\pm 20V$, $\pm 15V$, $\pm 10V$, and $\pm 5V$ supplies. (Switching times increase by a factor of two or more for operation at $\pm 5V$.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V^+ on first, followed by VL , V^- , and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with the supply pins for overvoltage protection (Figure 1).

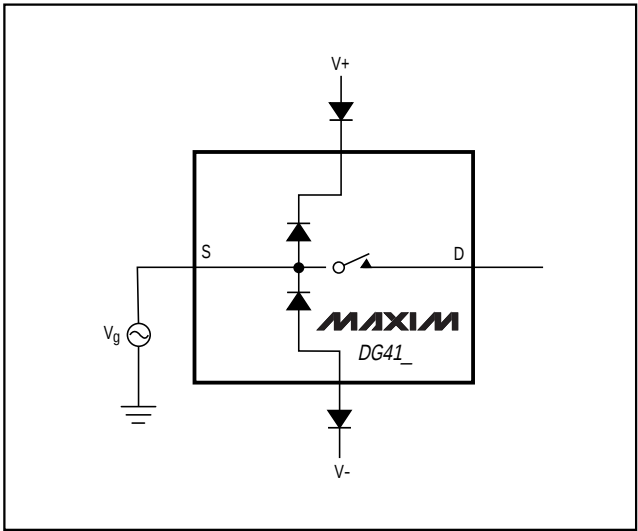


Figure 1. Overvoltage Protection Using External Blocking Diodes

Adding diodes reduces the analog signal range to $1V$ below V^+ and $1V$ above V^- , without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V^+ and V^- should not exceed $+44V$.

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Test Circuits/Timing Diagrams

DG417/DG418/DG419

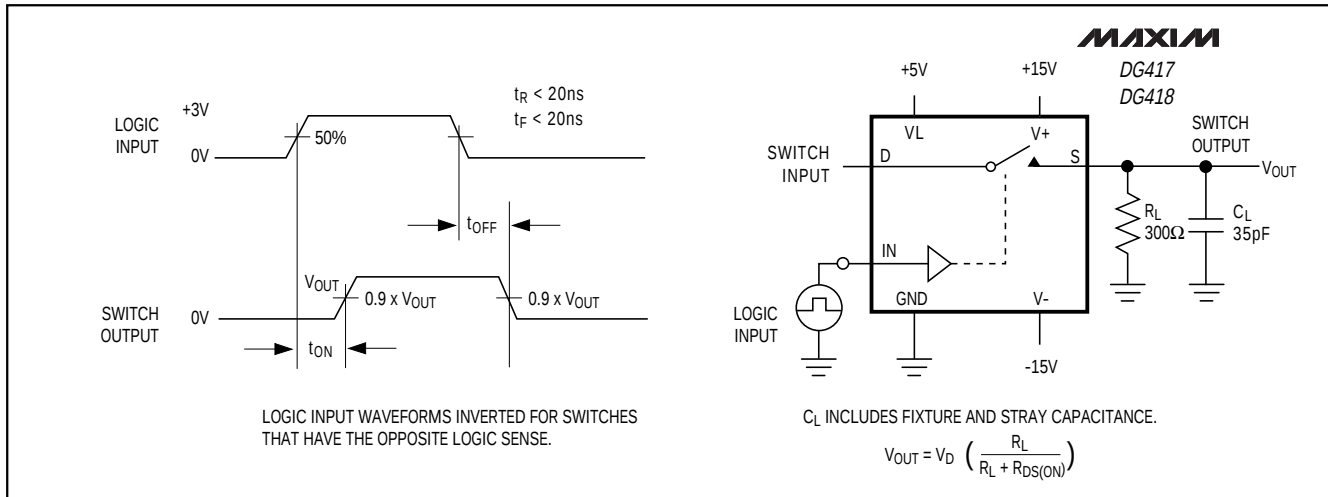


Figure 2. DG417/DG418 Switching Time

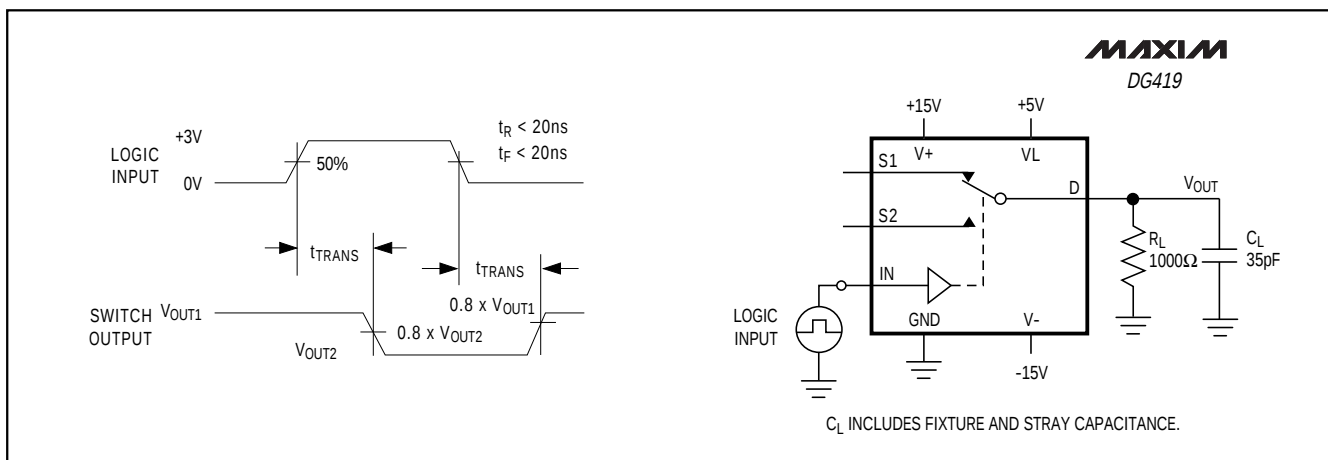


Figure 3. DG419 Transition Time

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Test Circuits/Timing Diagrams (continued)

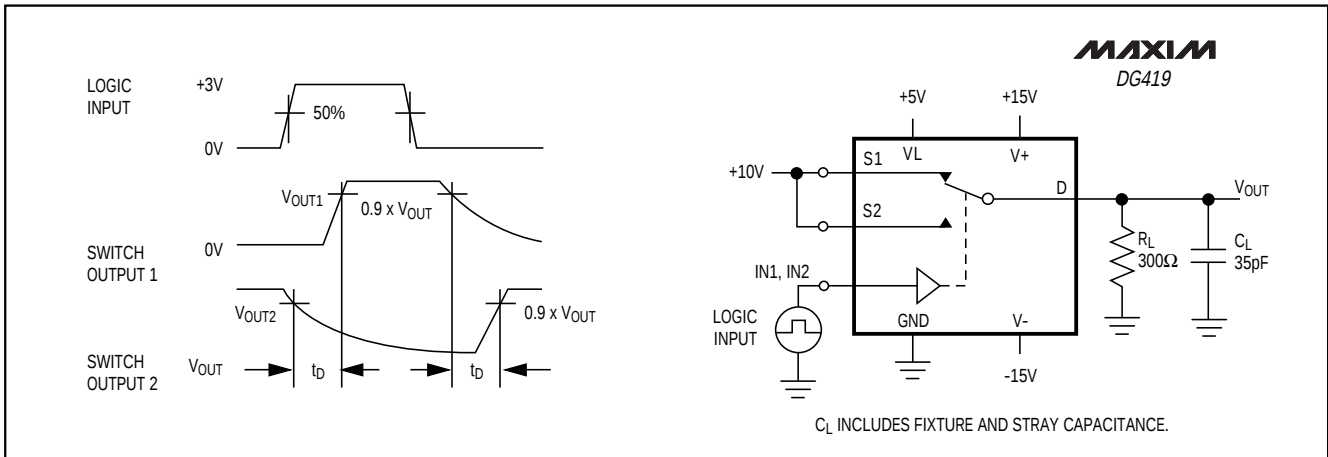


Figure 4. DG419 Break-Before-Make Interval

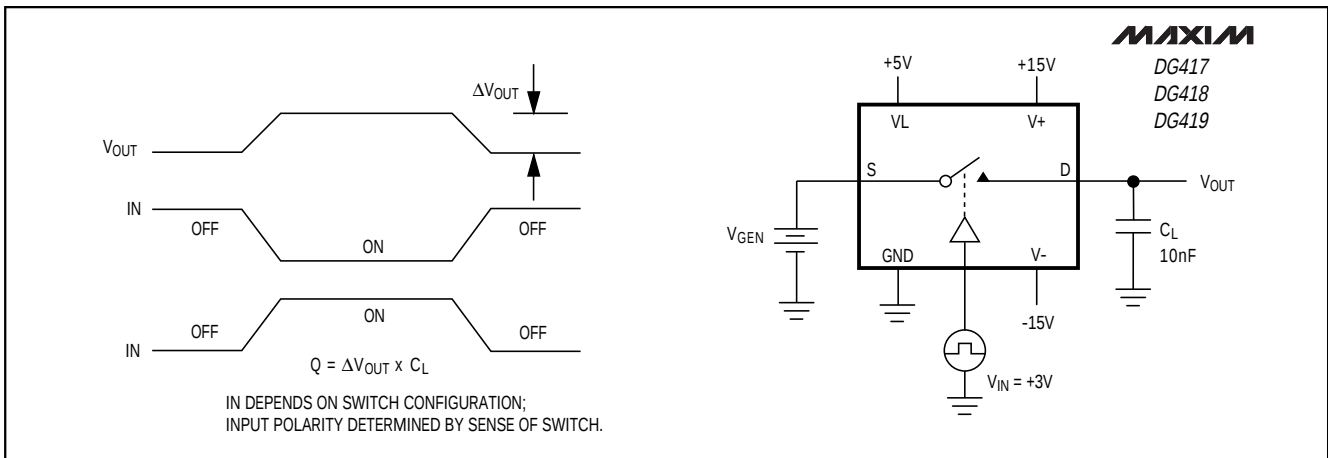


Figure 5. Charge Injection

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Test Circuits/Timing Diagrams (continued)

DG417/DG418/DG419

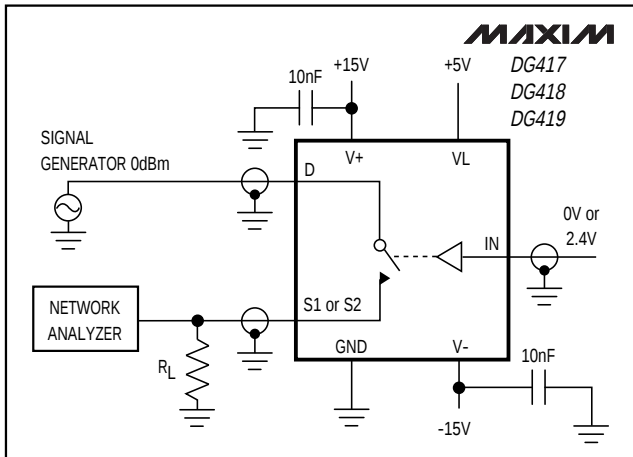


Figure 6. Off-Isolation Rejection Ratio

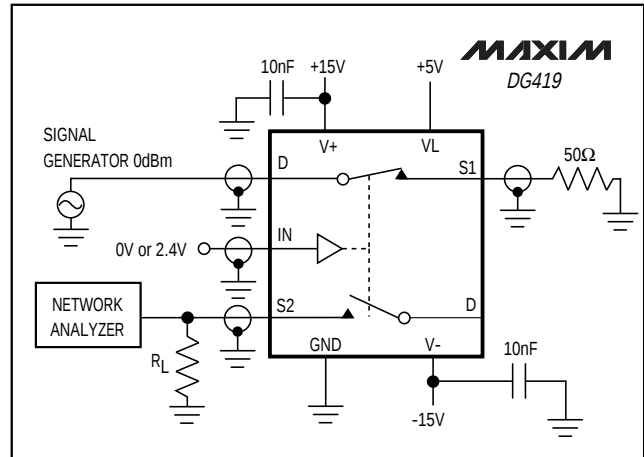


Figure 7. DG419 Crosstalk

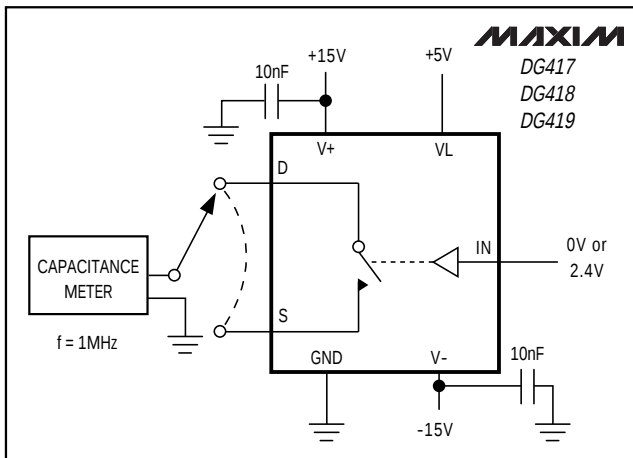


Figure 8. Drain-Source Off-Capacitance

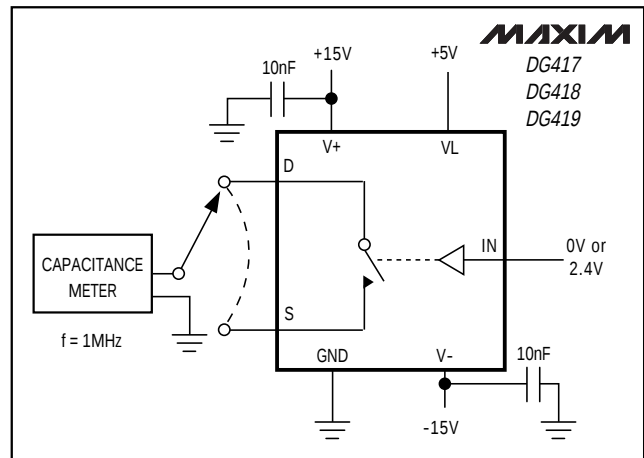


Figure 9. Drain-Source On-Capacitance

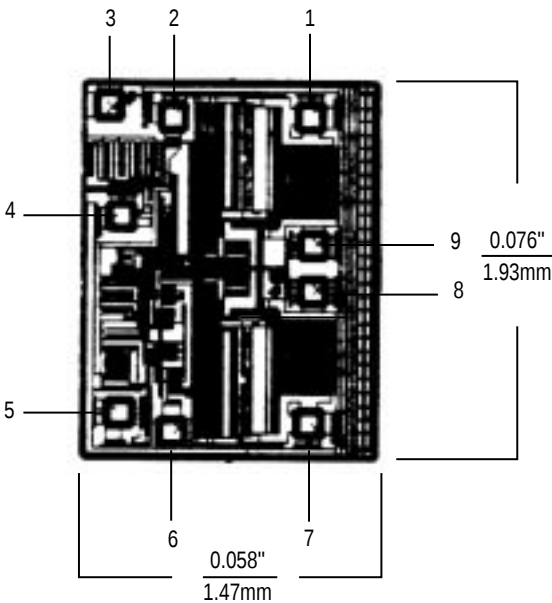
Improved, SPST/SPDT Analog Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
DG417DK	-40°C to +85°C	8 Cerdip
DG417AK	-55°C to +125°C	8 Cerdip**
DG418CJ	0°C to +70°C	8 Plastic DIP
DG418CY	0°C to +70°C	8 SO
DG418C/D	0°C to +70°C	Dice*
DG418DJ	-40°C to +85°C	8 Plastic DIP
DG418DY	-40°C to +85°C	8 SO
DG418DK	-40°C to +85°C	8 Cerdip
DG418AK	-55°C to +125°C	8 Cerdip**
DG419CJ	0°C to +70°C	8 Plastic DIP
DG419CY	0°C to +70°C	8 SO
DG419C/D	0°C to +70°C	Dice*
DG419DJ	-40°C to +85°C	8 Plastic DIP
DG419DY	-40°C to +85°C	8 SO
DG419DK	-40°C to +85°C	8 Cerdip
DG419AK	-55°C to +125°C	8 Cerdip**

* Contact factory for dice specifications.
**Contact factory for availability and processing to MIL-STD-883B.

Chip Topography



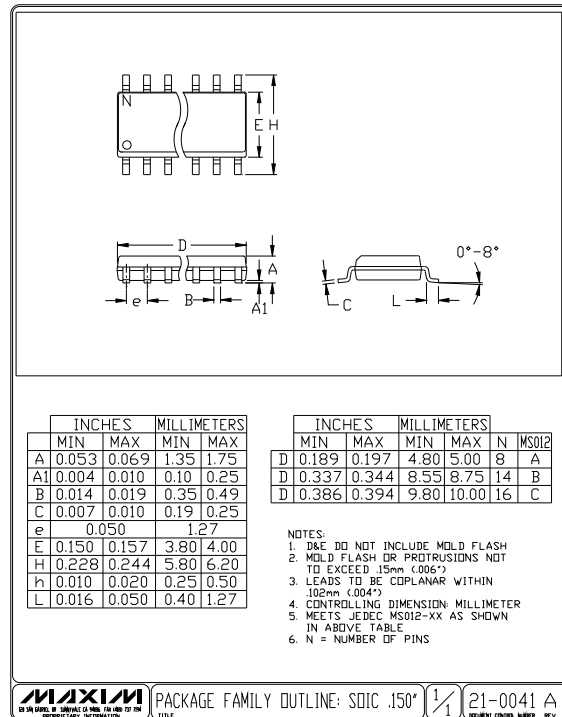
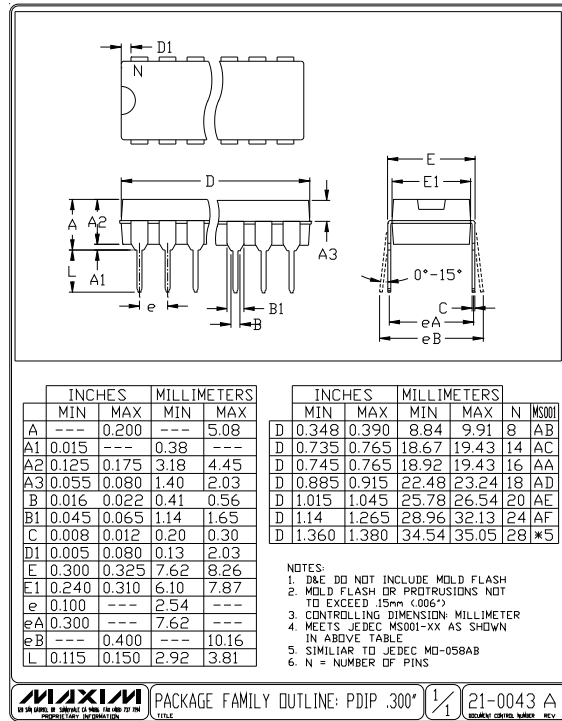
TRANSISTOR COUNT: 32
SUBSTRATE CONNECTED TO V+

DIE PAD	DG417	DG418	DG419
1	D	N.C.	S
2	GND	GND	GND
3	V+	V+	V+
4	VL	VL	VL
5	IN	IN	IN
6	V-	V-	V-
7	N.C.	S	S
8	N.C.	D	D
9	S	N.C.	D

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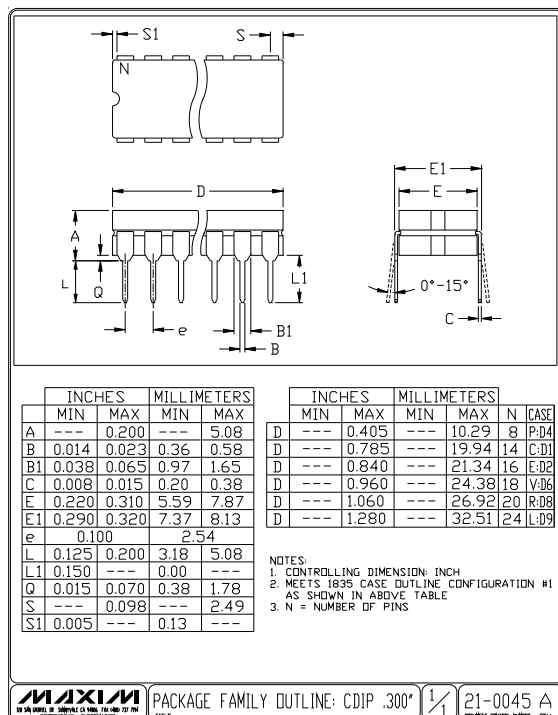
Package Information

DG417/DG418/DG419



Improved, SPST/SPDT Analog Switches

Package Information (continued)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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