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Pin Configuration

Figure 1. 44-pin TSOP II ^[1]

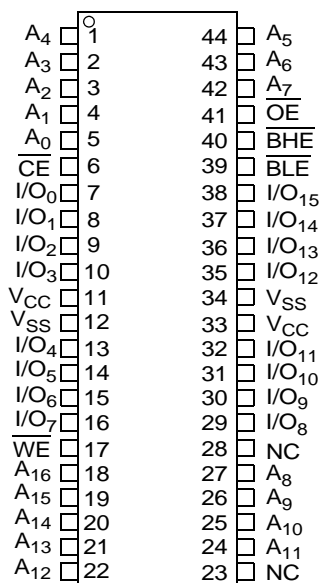
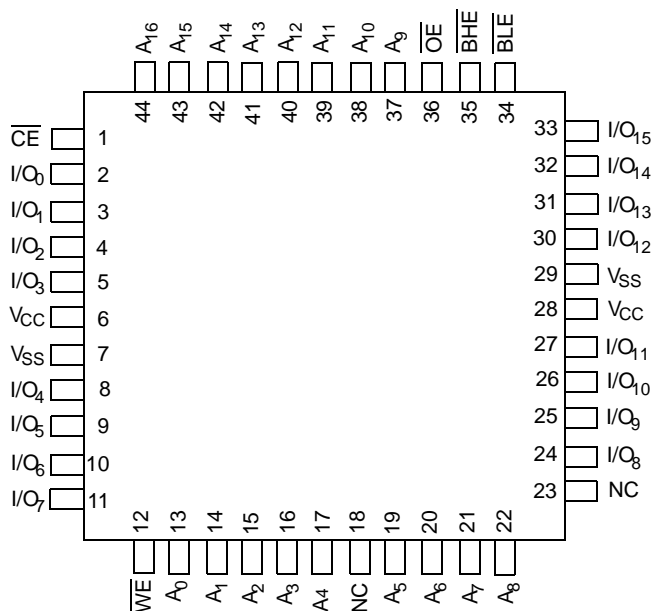


Figure 2. 44-pin TQFP



Note

1. NC pins are not connected on the die.

Selection Guide

Description		-10	-12	Unit
Maximum access time		10	12	ns
Maximum operating current	Industrial	100	95	mA
	Automotive-A	100	–	mA
	Automotive-E	–	120	mA
Maximum CMOS standby current	Industrial	10	10	mA
	Automotive-A	10	–	mA
	Automotive-E	–	15	mA

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{CC} relative to GND^[2] -0.5 V to +4.6 V

DC voltage applied to outputs in High Z state^[2] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage > 2001 V (MIL-STD-883, method 3015)

Latch up current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	-40 °C to +85 °C	3.3 V \pm 10%
Automotive-A	-40 °C to +85 °C	
Automotive -E	-40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		Unit
				Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = −4.0 mA		2.4	–	2.4	–	V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 8.0 mA		–	0.4	–	0.4	V
V _{IH}	Input HIGH voltage			2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage ^[2]			−0.3	0.8	−0.3	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	Industrial	−1	+1	−1	+1	μA
			Automotive-A	−1	+1	–	–	
			Automotive-E	–	–	−20	+20	
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , Output disabled	Industrial	−1	+1	−1	+1	μA
			Automotive-A	−1	+1	–	–	
			Automotive-E	–	–	−20	+20	
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Industrial	–	100	–	95	mA
			Automotive-A	–	100	–	–	
			Automotive-E	–	–	–	120	
I _{SB1}	Automatic CE power down current — TTL Inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Industrial	–	40	–	40	mA
			Automotive-A	–	40	–	–	
			Automotive-E	–	–	–	45	
I _{SB2}	Automatic CE power down current — CMOS inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	Industrial	–	10	–	10	mA
			Automotive-A	–	10	–	–	
			Automotive-E	–	–	–	15	

Note

2. $V_{IL}(\text{min}) = -2.0 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

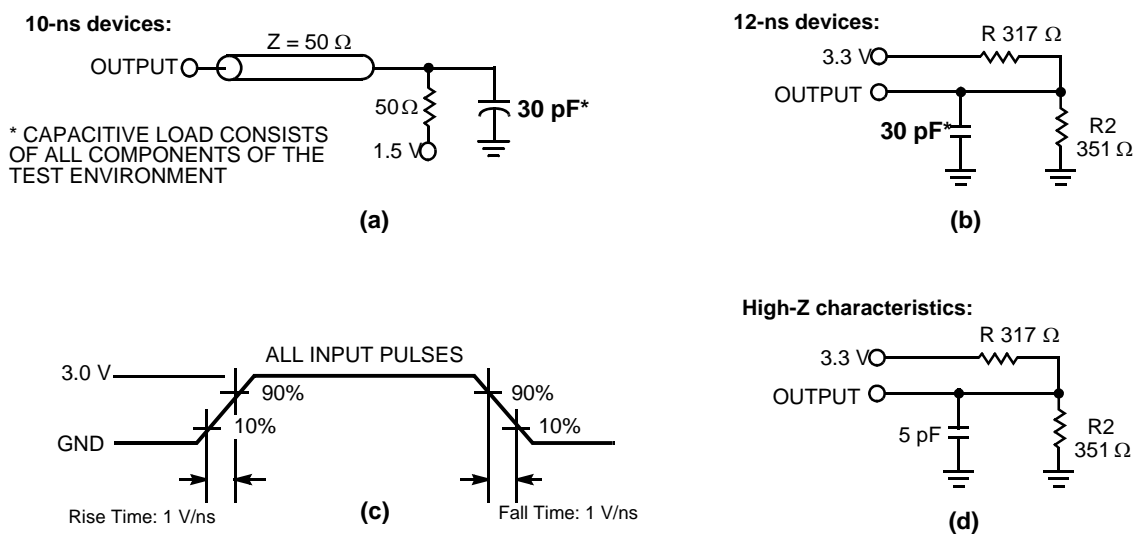
Parameter ^[3]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	44-pin TSOP II	44-pin TQFP	Unit
Θ _{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.56	42.66	°C/W
Θ _{JC}	Thermal resistance (Junction to case)		10.75	14.64	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms ^[4]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description		-10		-12		Unit
			Min	Max	Min	Max	
Read Cycle							
t _{power} ^[6]	V _{CC} (typical) to the first access		1	–	1	–	μs
t _{RC}	Read cycle time		10	–	12	–	ns
t _{AA}	Address to data valid		–	10	–	12	ns
t _{OHA}	Data hold from address change		3	–	3	–	ns
t _{ACE}	CE LOW to data valid		–	10	–	12	ns
t _{DOE}	OE LOW to data valid	Industrial/Automotive-A	–	5	–	6	ns
		Automotive-E	–	–	–	8	
t _{LZOE}	OE LOW to Low Z ^[7]		0	–	0	–	ns
t _{HZOE}	OE HIGH to High Z ^[7, 8]		–	5	–	6	ns
t _{LZCE}	CE LOW to Low Z ^[7]		3	–	3	–	ns
t _{HZCE}	CE HIGH to High Z ^[7, 8]		–	5	–	6	ns
t _{PU}	CE LOW to power up		0	–	0	–	ns
t _{PD}	CE HIGH to power down		–	10	–	12	ns
t _{DBE}	Byte enable to data valid	Industrial/Automotive-A	–	5	–	6	ns
		Automotive-E	–	–	–	8	
t _{LZBE}	Byte enable to Low Z		0	–	0	–	ns
t _{HZBE}	Byte disable to High Z		–	5	–	6	ns
Write Cycle ^[9, 10]							
t _{WC}	Write cycle time		10	–	12	–	ns
t _{SCE}	CE LOW to write end		7	–	8	–	ns
t _{AW}	Address setup to write end		7	–	8	–	ns
t _{HA}	Address hold from write end		0	–	0	–	ns
t _{SA}	Address setup to write start		0	–	0	–	ns
t _{PWE}	WE pulse width		7	–	8	–	ns
t _{SD}	Data setup to write end		5	–	6	–	ns
t _{HD}	Data hold from write end		0	–	0	–	ns
t _{LZWE}	WE HIGH to Low Z ^[7]		3	–	3	–	ns
t _{HZWE}	WE LOW to High Z ^[7, 8]		–	5	–	6	ns
t _{BW}	Byte enable to end of write		7	–	8	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
- At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of [Figure 3 on page 6](#). Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, $\overline{\text{WE}}$ LOW, and $\overline{\text{BHE/BL E}}$ LOW. $\overline{\text{CE}}$, $\overline{\text{WE}}$, and $\overline{\text{BHE/BL E}}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

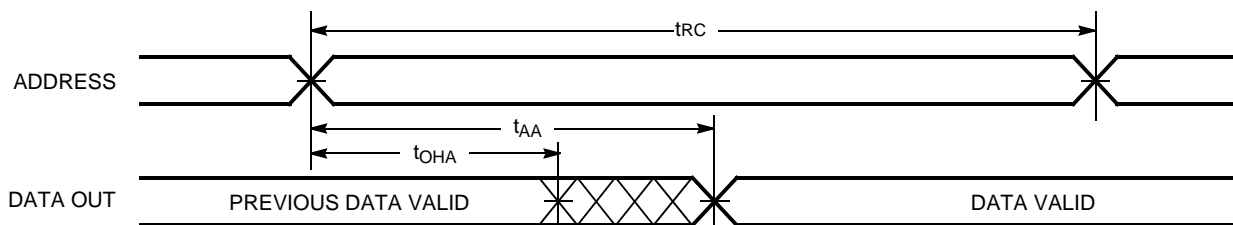
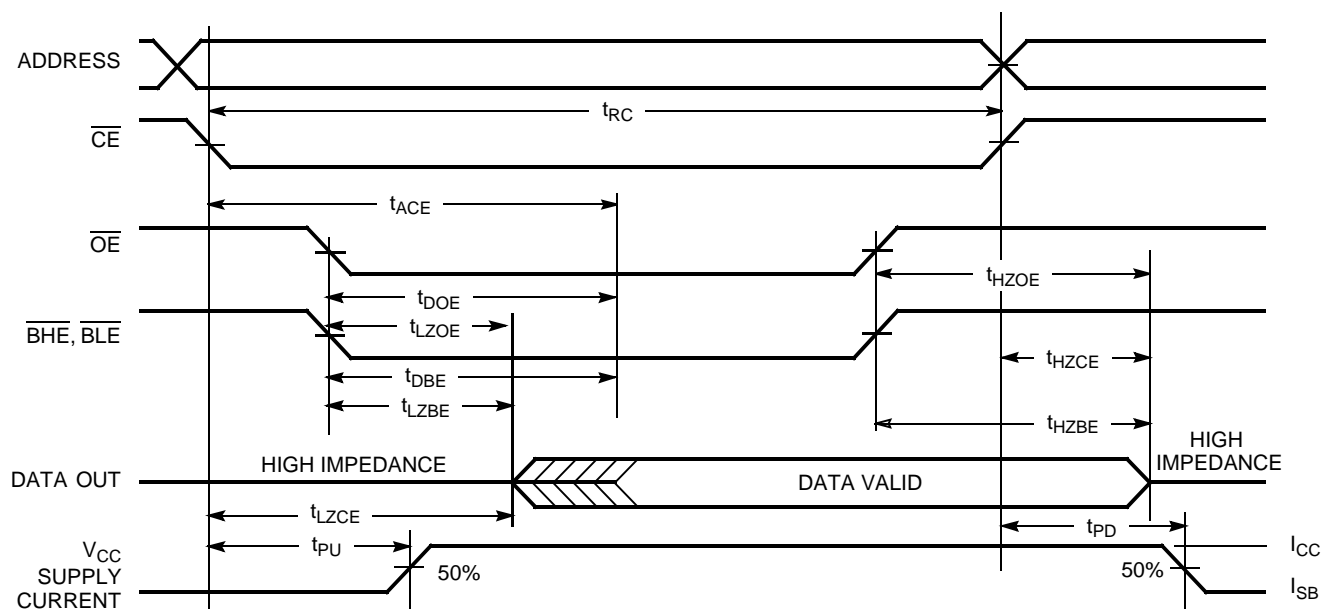


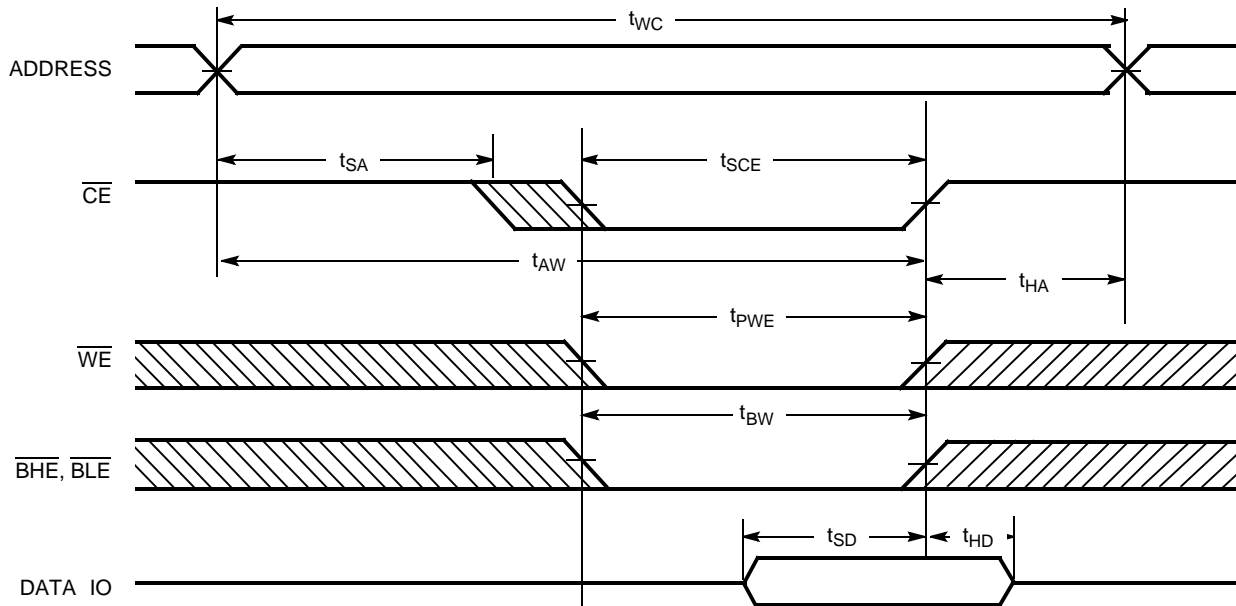
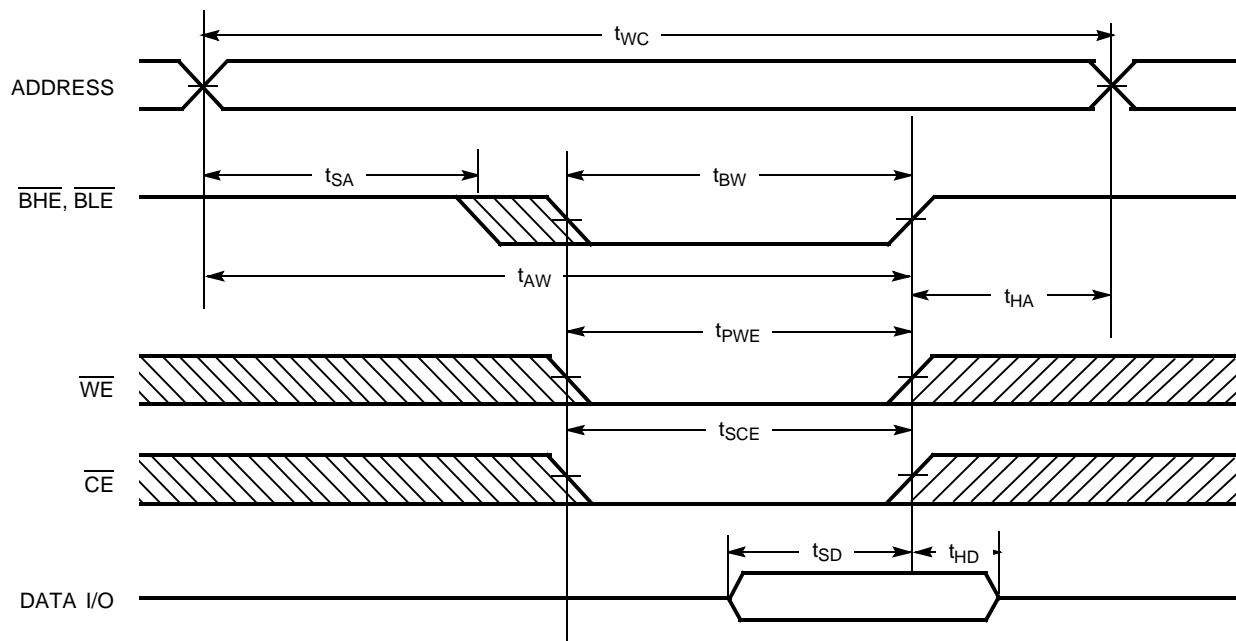
Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]



Notes

11. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and/or \overline{BLE} = V_{IL} .
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

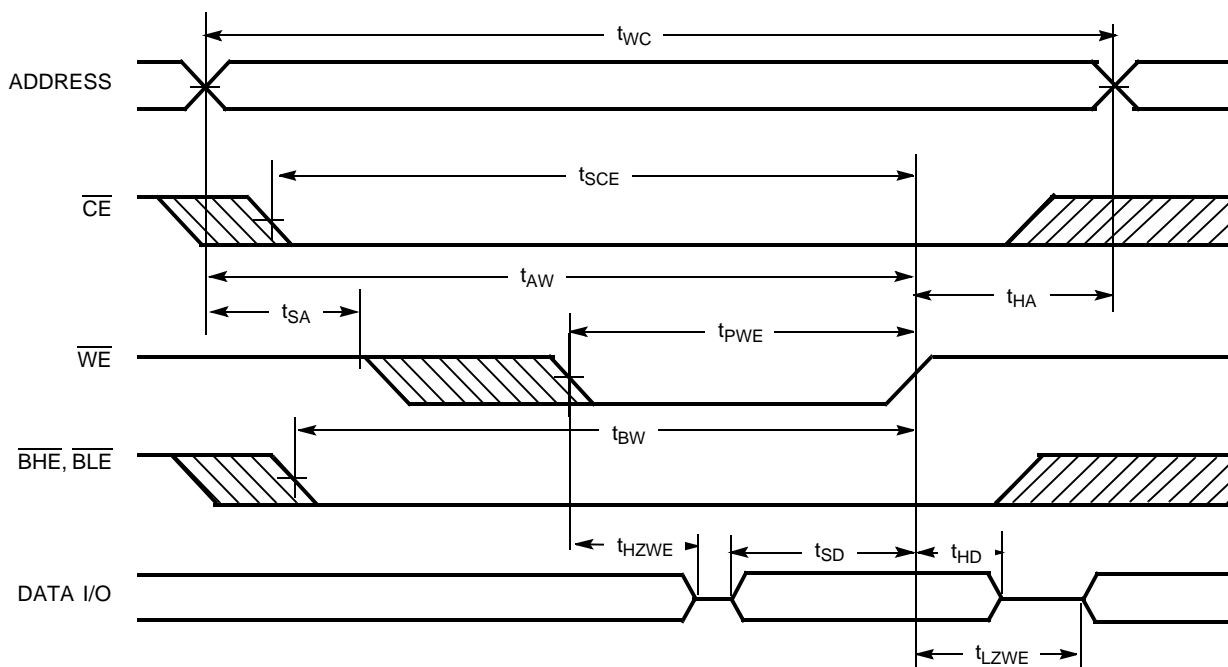
Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [14, 15]

Figure 7. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes

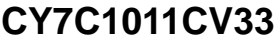
 14. Data I/O is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}}$ = V_{IH} .

 15. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, LOW)

Truth Table

CE	OE	WE	BLE	BHE	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – all bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read – lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read – upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – all bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write – lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write – upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})



Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1011CV33-10ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
12	CY7C1011CV33-12AXI	51-85064	44-pin TQFP (Pb-free)	Industrial
	CY7C1011CV33-12ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

Temperature range: X = A or I or E
A = Automotive-A; I = Industrial; E = Automotive-E

Pb-free

Package Type: XX = ZS or A or BV
ZS = 44-pin TSOP II
A = 44-pin TQFP

Speed grade: XX = 10 ns or 12 ns

V33 = 3.3 V

Process Technology: 150 nm

Bus Width: x 16 bits

Density: 2-Mbit

Fast Asynchronous SRAM family

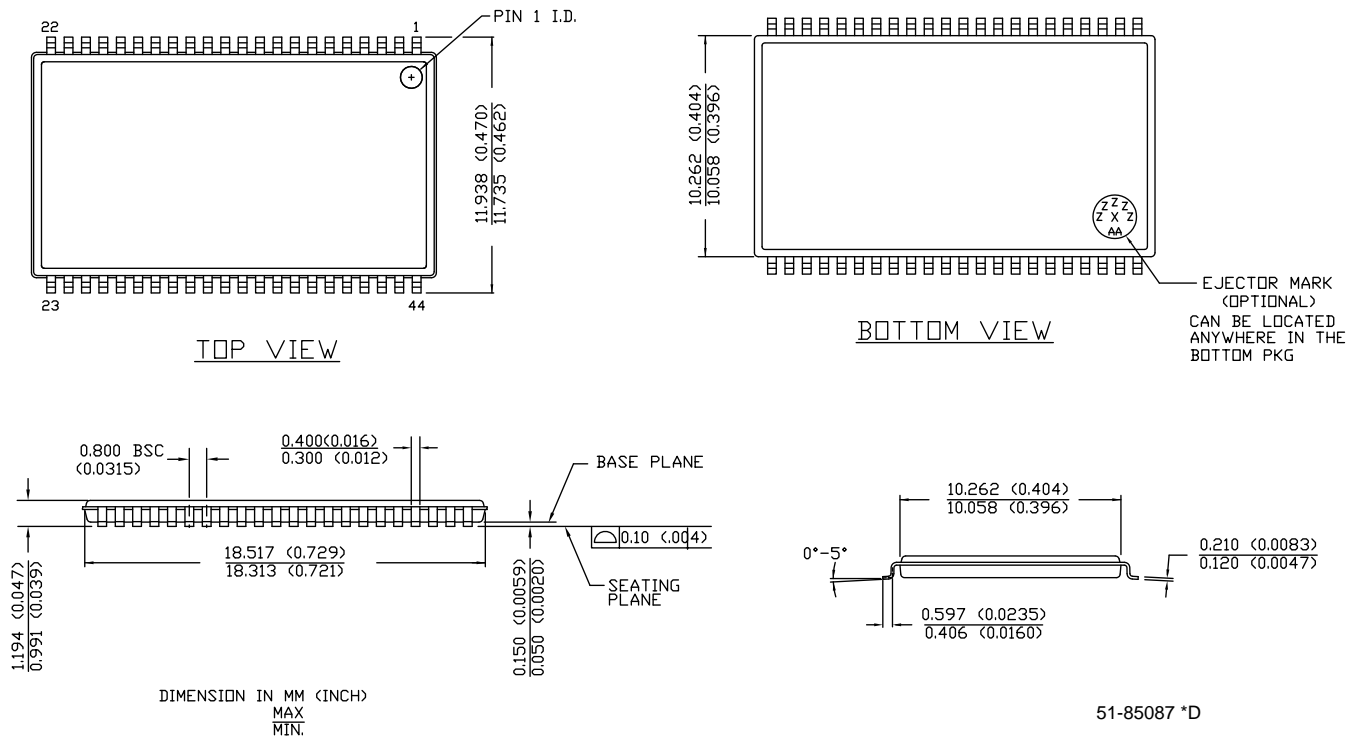
Technology Code: C = CMOS

Marketing Code: 7 = SRAM

Company ID: CY = Cypress

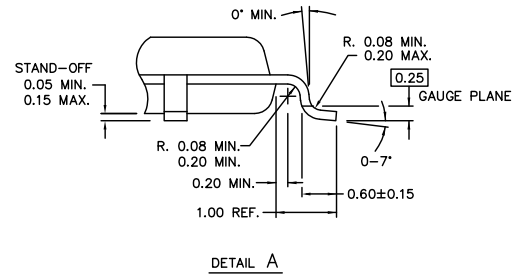
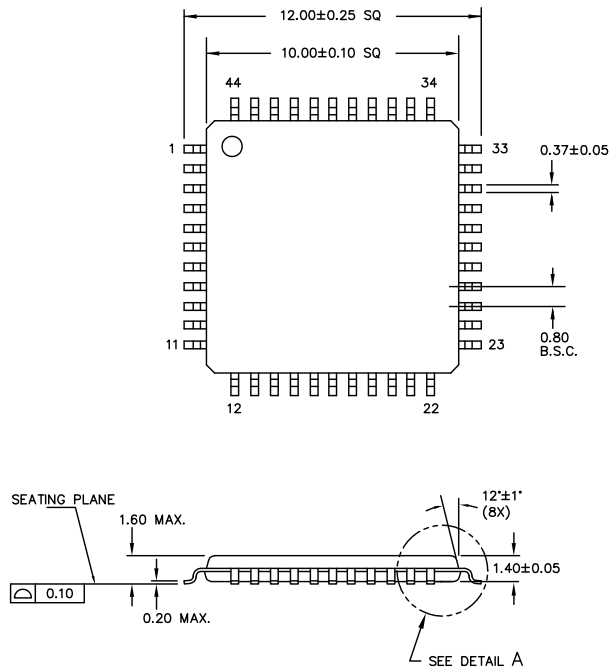
Package Diagrams

Figure 9. 44-pin TSOP Z44-II, 51-85087



Package Diagrams (continued)

Figure 10. 44-pin TQFP (10 × 10 × 1.4 mm) A44S, 51-85064



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *E

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{\text{CE}}$	chip enable
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TQFP	thin quad flat pack
TSOP	thin small outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
%	percent
pF	pico farad
V	volt
W	watt

Document History Page

Document Title: CY7C1011CV33, 2-Mbit (128 K × 16) Static RAM Document Number: 38-05232				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	117132	HGK	07/31/02	New Data Sheet
*A	118057	HGK	08/19/02	Pin configuration for 48-ball FBGA correction
*B	119702	DFP	10/11/02	Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA
*C	386106	PCI	See ECN	Added lead-free parts in Ordering Information Table
*D	498501	NXR	See ECN	Corrected typo in the Logic Block Diagram on page# 1 Included the Maximum Ratings for Static Discharge Voltage and Latch up Current on page# 3 Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*E	522620	VKN	See ECN	Added Thermal Resistance Table
*F	1891366	VKN/AESA	See ECN	Added -10ZSXA part Updated Ordering Information table
*G	2428606	VKN/PYRS	See ECN	Corrected typo in the 44-Pin TSOP and 48-Ball FBGA pinout Removed Commercial parts Removed 15 ns speed bin Removed inactive parts from the Ordering Information table
*H	2664421	VKN/AESA	02/25/09	Added Automotive-E specs for 12 ns speed Updated Ordering Information table
*I	2898399	KA0/AJU	03/24/2010	Updated Package Diagrams
*J	2950666	VKN	06/11/2010	Included "CY7C1011CV33-12BVXE" in Ordering Information Added Contents and Acronyms Updated Sales, Solutions, and Legal Information Added Ordering Code Definitions .
*K	3089939	PRAS	11/13/2010	Removed inactive part from Ordering Information.
*L	3276463	KA0	06/07/2011	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Added Units of Measure . Updated Package Diagrams . Updated in new template.
*M	3591978	TAVA	04/19/2012	Removed all information related to 48-ball VFBGA throughout the document. Updated package diagram revisions.

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