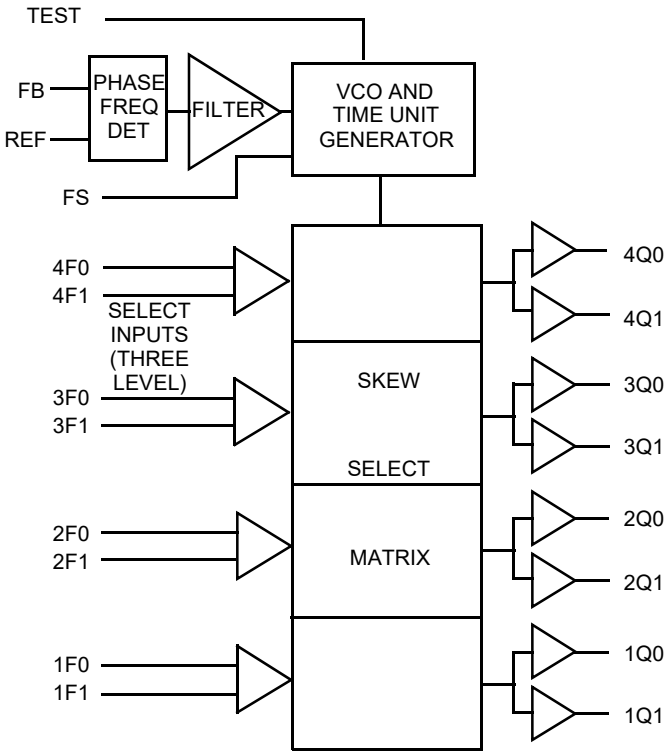
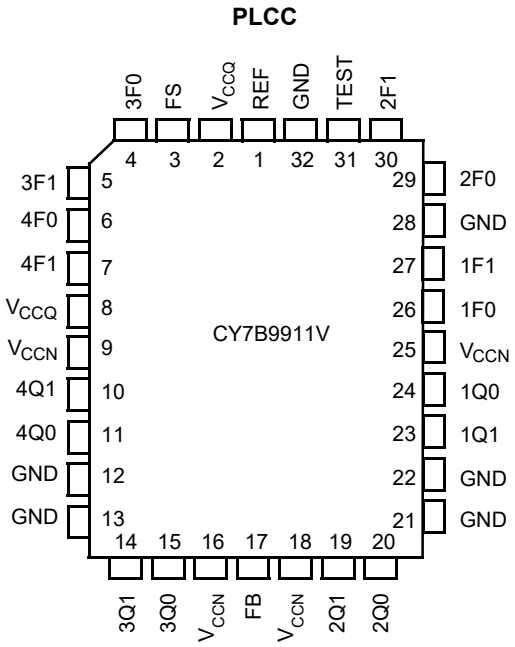
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 32-pin PLCC pinout



Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three level frequency range select. See Table 1 on page 5.
1F0, 1F1	I	Three level function select inputs for output pair 1 (1Q0, 1Q1). See Table 2 on page 5.
2F0, 2F1	I	Three level function select inputs for output pair 2 (2Q0, 2Q1). See Table 2 on page 5.
3F0, 3F1	I	Three level function select inputs for output pair 3 (3Q0, 3Q1). See Table 2 on page 5.
4F0, 4F1	I	Three level function select inputs for output pair 4 (4Q0, 4Q1). See Table 2 on page 5.
TEST	I	Three level select. See Test Mode on page 6 under the Block Diagram Description on page 5.
1Q0, 1Q1	O	Output pair 1. See Table 2 on page 5.
2Q0, 2Q1	O	Output pair 2. See Table 2 on page 5.
3Q0, 3Q1	O	Output pair 3. See Table 2 on page 5.
4Q0, 4Q1	O	Output pair 4. See Table 2 on page 5.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

The Phase Frequency Detector and Filter blocks accept inputs from the Reference Frequency (REF) input and the Feedback (FB) input. They generate correction information to control the frequency of the Voltage Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block. It generates a frequency used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 1.

Table 1. Frequency Range Select and t_U Calculation [1]

FS [2, 3]	f_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) At Which t_U = 1.0 ns
	Min	Max		
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	110	16	62.5

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low skew, high fanout drivers (xQ0, xQ1), and two corresponding three level function select (xF0, xF1) inputs. Table 2 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

Table 2. Programmable Skew Configurations [1]

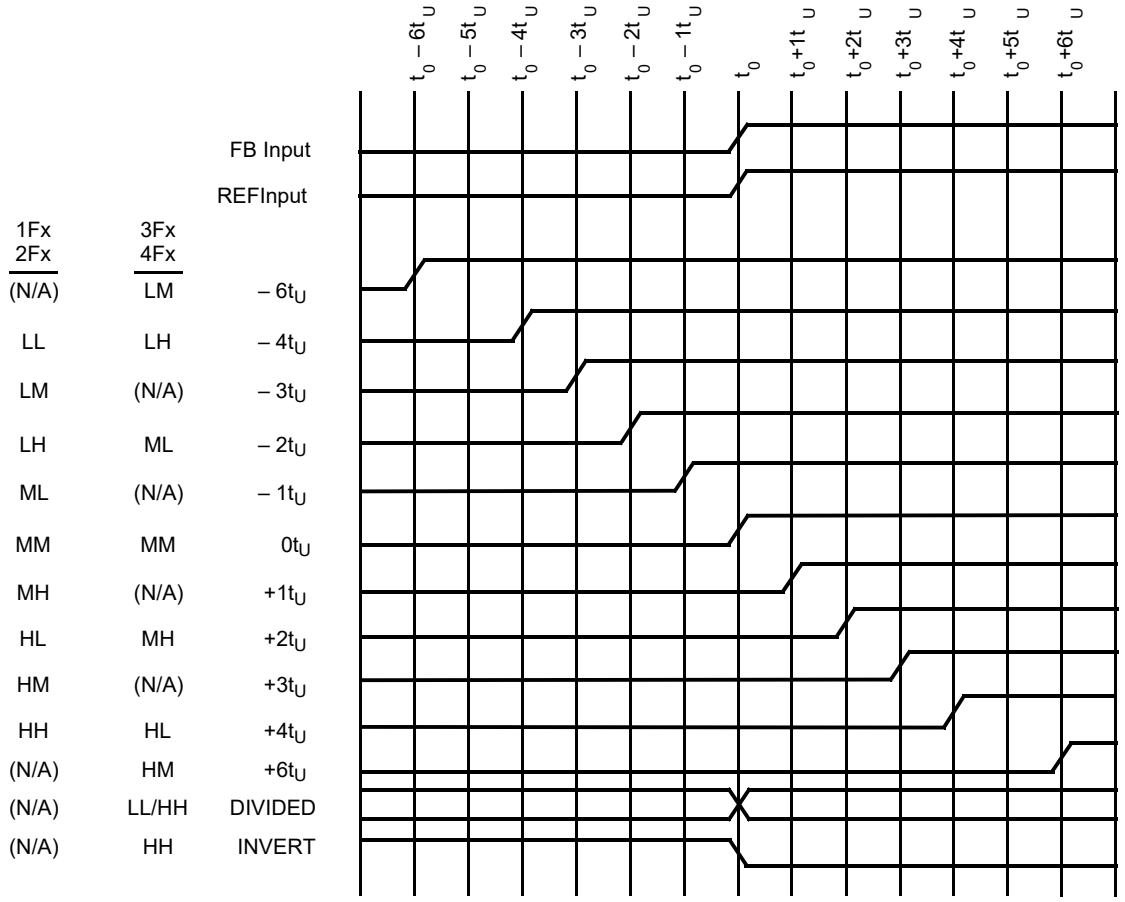
Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram on page 2). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 2.8 V.

Figure 2 shows the typical outputs with FB connected to a zero skew output. [4]

Figure 2. Typical Outputs with FB Connected to a Zero Skew Output



Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, allowing the CY7B9911V to operate as described in Block Diagram Description on page 5. For testing purposes, any of the three level inputs can have a removable jumper to ground or be tied LOW through a 100Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected, and input levels supplied to REF directly control all outputs. Relative output-to-output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW), all outputs function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Note
4. FB connected to an output selected for “zero” skew (that is, xF1 = xF0 = MID).

Operational Mode Descriptions

Figure 3. Zero Skew and Zero Delay Clock Driver

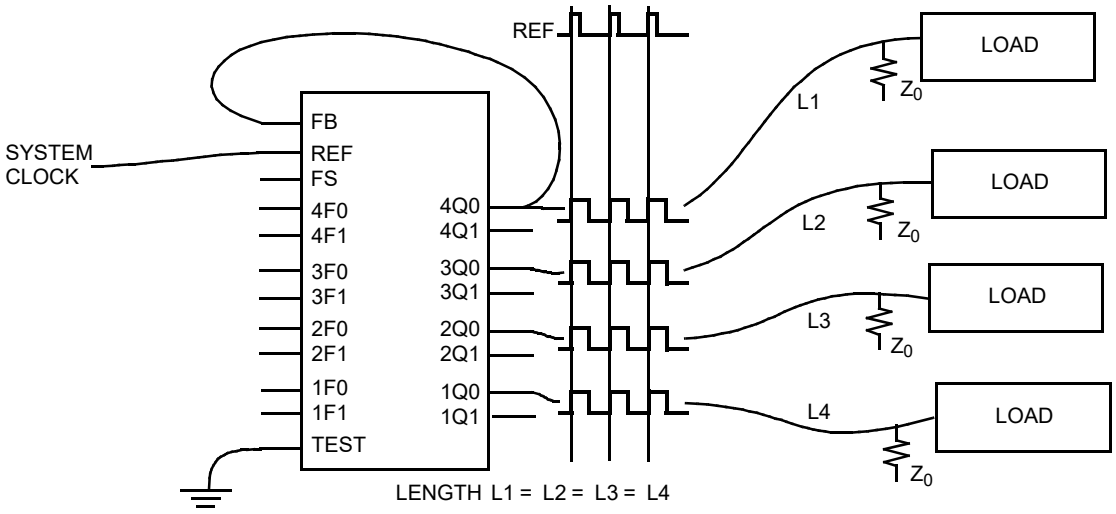


Figure 3 shows the LVPSCB configured as a zero skew clock buffer. In this mode the CY7B9911V is used as the basis for a low skew clock distribution tree. When all the function select inputs (xF0, xF1) are left open, each of the outputs are aligned and drive a terminated transmission line to an independent load. The FB input is tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low skew specification, along with the ability to drive terminated transmission lines (with impedances as low as 50 Ω), enables efficient printed circuit board design.

Figure 4. Programmable Skew Clock Driver

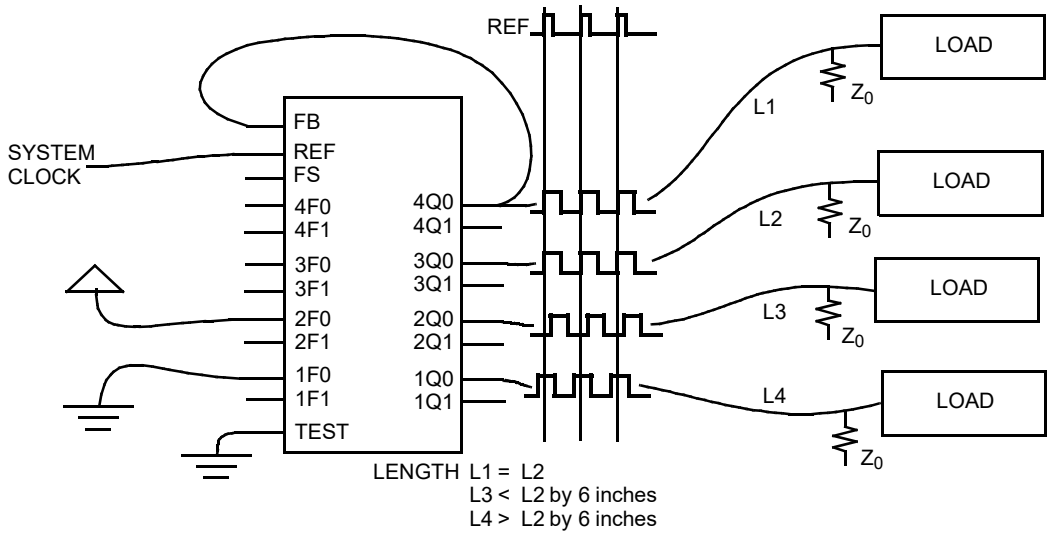


Figure 4 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the LVPSCB is programmed to stagger the timing of its outputs. Each of the four groups of output pairs is programmed to different output timing. Skew timing is adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is sent back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads receive the clock pulse at the same time.

In Figure 4 the FB input is connected to an output with 0 ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to make certain that all outputs have precise phase alignment.

Clock skews are advanced by ±6 time units (tU) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since “Zero Skew”, +tU, and –tU are defined relative to output

groups, and the PLL aligns the rising edges of REF and FB, you can create wider output skews by proper selection of the xFn inputs. For example, a +10 tU between REF and 3Qx is achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at –4 tU and 3Qx skews to +6 tU, a total of +10 tU skew is realized). Many other configurations are realized by skewing both the outputs used as the FB input and skewing the other outputs.

Figure 5. Inverted Output Connections

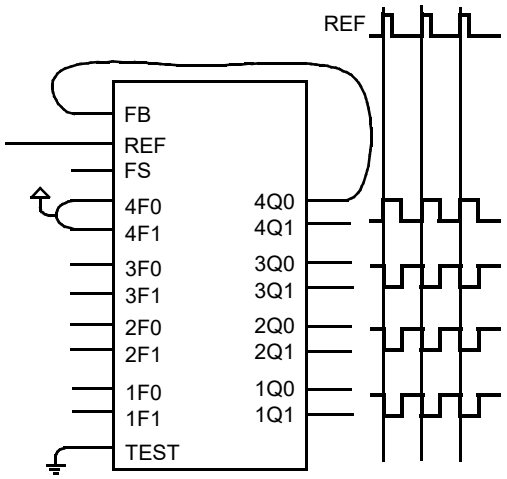


Figure 5 shows an example of the invert function of the LVPSCB. In this example, the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied HIGH, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the “inverted” outputs with respect to the REF input. By selecting the output connected to FB, you can have two inverted and six non-inverted outputs or six inverted and two non-inverted outputs. The correct configuration is determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs are also skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 6. Frequency Multiplier with Skew Connections

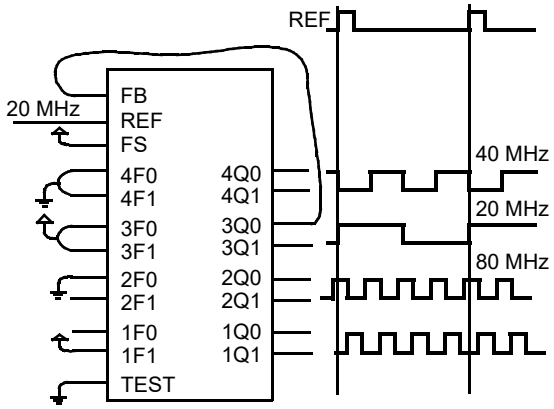


Figure 6 shows the LVPSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is sent back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz, while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, that results in a 40 MHz waveform at these outputs. Note that the 20 and 40 MHz clocks fall simultaneously and are out of phase on their rising edge. This enables the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80 MHz operation because that is the frequency of the fastest output.

Figure 7. Frequency Divider Connections

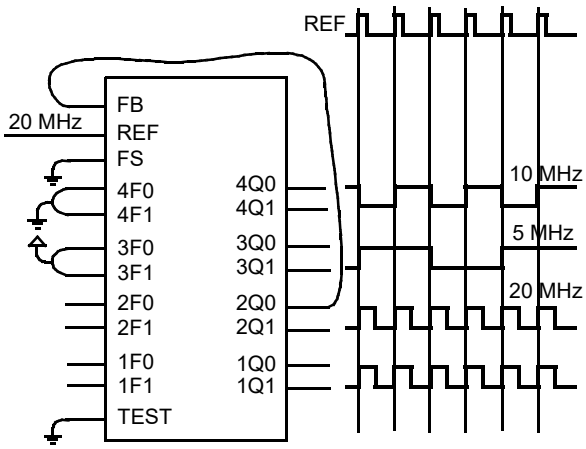


Figure 7 shows the LVPSCB in a clock divider application. 2Q0 is sent back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This enables use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15 to 30 MHz range, since the highest frequency output is running at 20 MHz.

Figure 8 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output enables the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function enables each of the two subsystems to clock 180 degrees out of phase, but still is aligned within the skew specification.

The divided outputs offer a zero delay divider for portions of the system that divide the clock by either two or four, and still remain within a narrow skew of the “1X” clock. Without this feature, an external divider is added, and the propagation delay of the divider adds to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the LVPSCB to multiply the clock rate at the REF input by either two or four. This mode enables the designer to distribute a low frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low skew characteristics of the clock driver. The LVPSCB performs all of the functions described in this section at the same time. It can multiply by two and four or divide by two (and four) at the same time. This shifts its outputs over a wide range or maintain zero skew between selected outputs.

Figure 8. Multi-Function Clock Driver

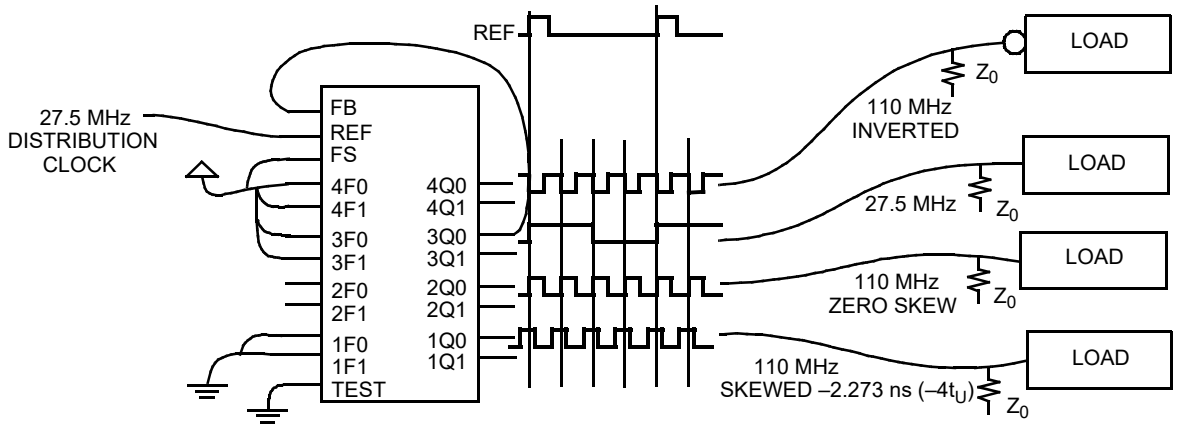


Figure 9. Board-to-Board Clock Distribution

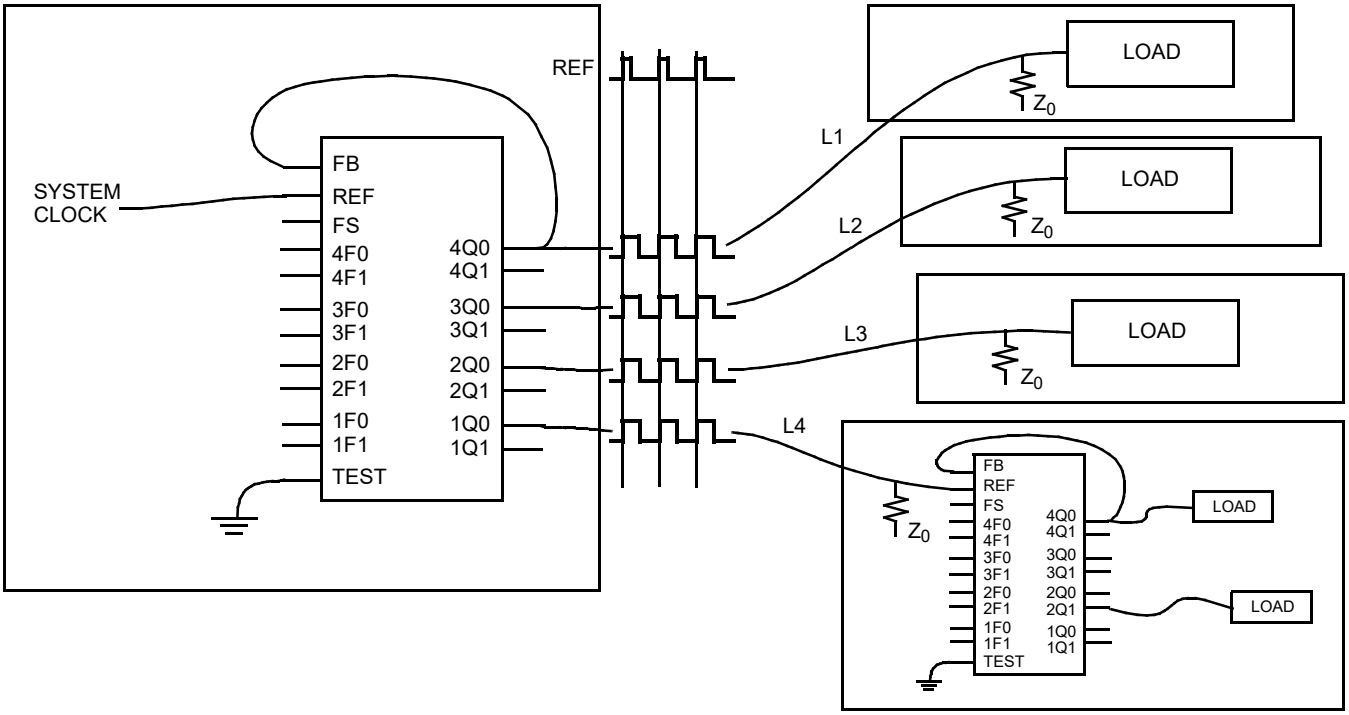


Figure 9 shows the CY7B9911V connected in series to construct a zero skew clock distribution tree between boards. Delays of the downstream clock buffers are programmed to compensate for the wire length (that is, select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero delay clock tree. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in a series.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential .....–0.5 V to +7.0 V

DC Input Voltage .....–0.5 V to +7.0 V

Output Current into Outputs (LOW) ..... 64 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter [5]	Description	Test Conditions		CY7B9911V		Unit
				Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –18 mA		2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 35 mA		–	0.45	V
V_{IH}	Input HIGH Voltage (REF and FB inputs only)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)			–0.5	0.8	V
V_{IHH}	Three Level Input HIGH Voltage (Test, FS, xFn) [5]	Min ≤ V_{CC} ≤ Max		0.87 × V_{CC}	V_{CC}	V
V_{IMM}	Three Level Input MID Voltage (Test, FS, xFn) [5]	Min ≤ V_{CC} ≤ Max		0.47 × V_{CC}	0.53 × V_{CC}	V
V_{ILL}	Three Level Input LOW Voltage (Test, FS, xFn) [5]	Min ≤ V_{CC} ≤ Max		0.0	0.13 × V_{CC}	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max		–	20	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V		–20	–	µA
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}		–	200	µA
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = V_{CC}/2		–50	50	µA
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		–	–200	µA
I_{OS}	Short Circuit Current [7]	V_{CC} = MAX, V_{OUT} = GND (25 °C only)		–	–200	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max, All Input Selects Open	Commercial	–	95	mA
			Military / Industrial	–	100	
I_{CCN}	Output Buffer Current per Output Pair [8]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA Input Selects Open, f_{MAX}		–	19	mA
PD	Power Dissipation per Output Pair [9]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA Input Selects Open, f_{MAX}		–	104	mW

Notes

5. For more information see Group A subgroup testing information.
6. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
7. CY7B9911V must be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
8. Total output current per output pair is approximated by the following expression that includes device current plus load current:
   CY7B9911V: ICCN = [(4 + 0.11F) + [[((835 –3F)/Z) + (.0022FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F × C
9. Total power dissipation per output pair is approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   PD = [(22 + 0.61F) + [[(1550 + 2.7F)/Z) + (.0125FC)]N] x 1.1. (See note 8 for variable definition.)

Capacitance

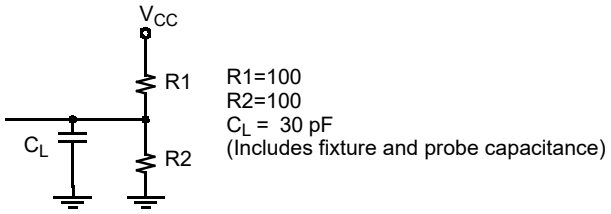
Parameter [10, 11]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF

Thermal Resistance

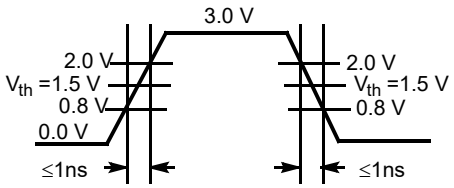
Parameter [11]	Description	Test Conditions	32-pin PLCC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	44	°C/W
Θ_{JC}	Thermal resistance (junction to case)		26	°C/W

AC Test Loads and Waveforms

Figure 10. AC Test Loads and Waveforms



TTL AC Test Load



TTL Input Test Waveform

Notes
10. Applies to REF and FB inputs only.
11. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

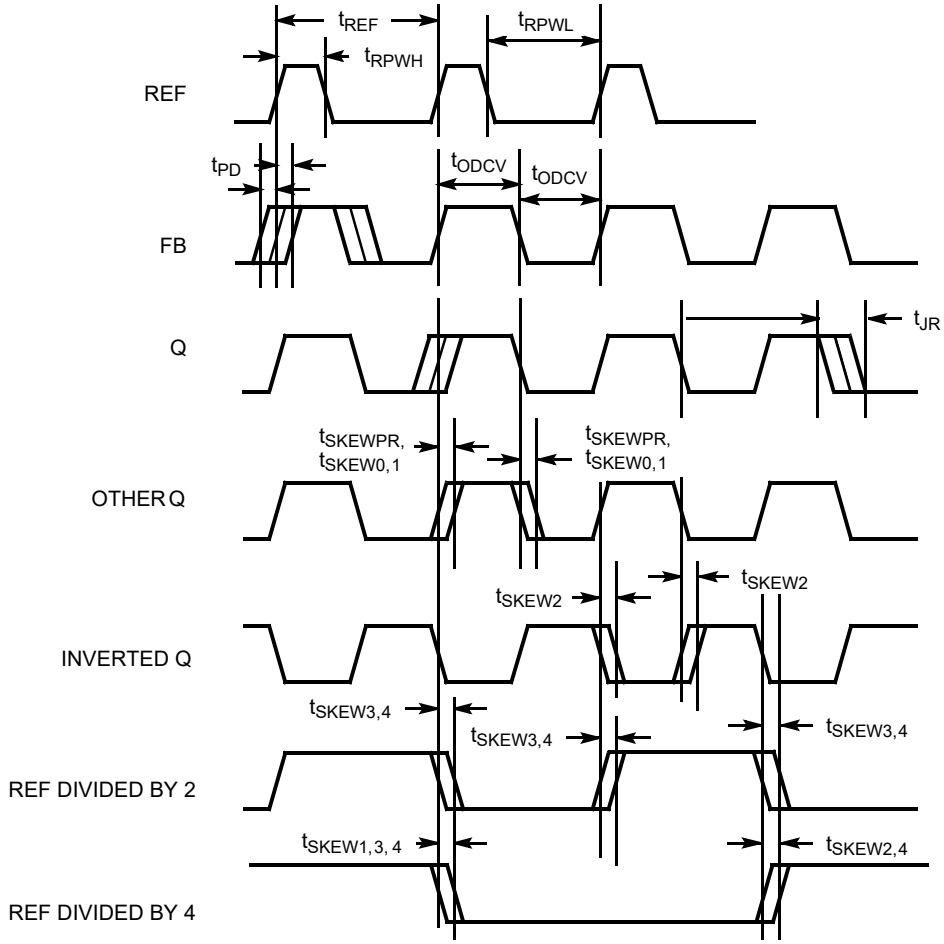
Over the Operating Range

Parameter [12, 13]	Description		CY7B9911V-5			Unit
			Min	Typ	Max	
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW [12, 14]	15	–	30	MHz
		FS = MID [12, 14]	25	–	50	
		FS = HIGH [12,14, 15]	40	–	110	
t_{RPWH}	REF Pulse Width HIGH measured at 1/2*V_{CCQ} threshold.		3.65	–	–	ns
t_{RPWL}	REF Pulse Width LOW measured at 1/2*V_{CCQ} threshold.		3.65	–	–	ns
t_U	Programmable Skew Unit		See Table 1			
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) [16, 17]		–	0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [16, 18]		–	0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [16, 19]		–	0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[16, 19]		–	0.5	1.0	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[16, 19]		–	0.5	0.7	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[16, 19]		–	0.5	1.0	ns
t_{DEV}	Device-to-Device Skew[20, 21]		–	–	1.25	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[22]		–1.0	0.0	+1.0	ns
t_{PWH}	Output HIGH Time Deviation from 50%[23]		–	–	2.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[23]		–	–	3	ns
t_{ORISE}	Output Rise Time[23, 24]		0.15	1.0	1.5	ns
t_{OFALL}	Output Fall Time[23, 24]		0.15	1.0	1.5	ns
t_{LOCK}	PLL Lock Time[25]		–	–	0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[20]	–	–	25	ps
		Peak-to-Peak[20]	–	–	200	ps

Notes

12. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs is f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs is $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication using a divided output as the FB input.
13. Test measurement levels for the CY7B9911V are TTL levels (1.5 V to 1.5 V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the Figure 10 on page 11 unless otherwise specified.
14. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
15. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 2.8 V.
16. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same tU delay is selected when all are loaded with 30 pF and terminated with 50Ω to VCC/2 (CY7B9911V).
17. tSKEWPR is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for 0tU.
18. tSKEW0 is defined as the skew between outputs when they are selected for 0tU. Other outputs are divided or inverted but not shifted.
19. There are three classes of outputs: Nominal (multiple of tU delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
20. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
21. tDEV is the output-to-output skew between any two devices operating under the same conditions (VCC ambient temperature, air flow, and so on.)
22. tODCV is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in tSKEW2 and tSKEW4 specifications.
23. Specified with outputs loaded with 30 pF. Devices are terminated through 50Ω to VCC/2. tPWH is measured at 2.0 V. tPWL is measured at 0.8 V.
24. tORISE and tOFALL measured between 0.8 V and 2.0 V.
25. tLOCK is the time that is required before synchronization is achieved. This specification is valid only after VCC is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until tPD is within specified limits.
26. CL=0 pF. For CL=30 pF, tSKEW0=0.35 ns.

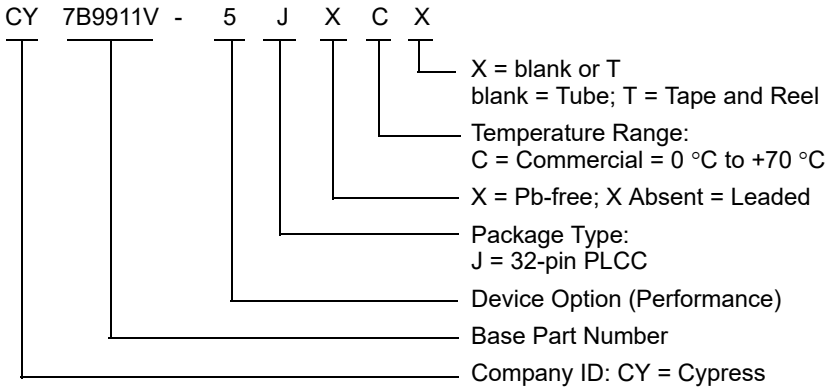
AC Timing Diagrams



Ordering Information

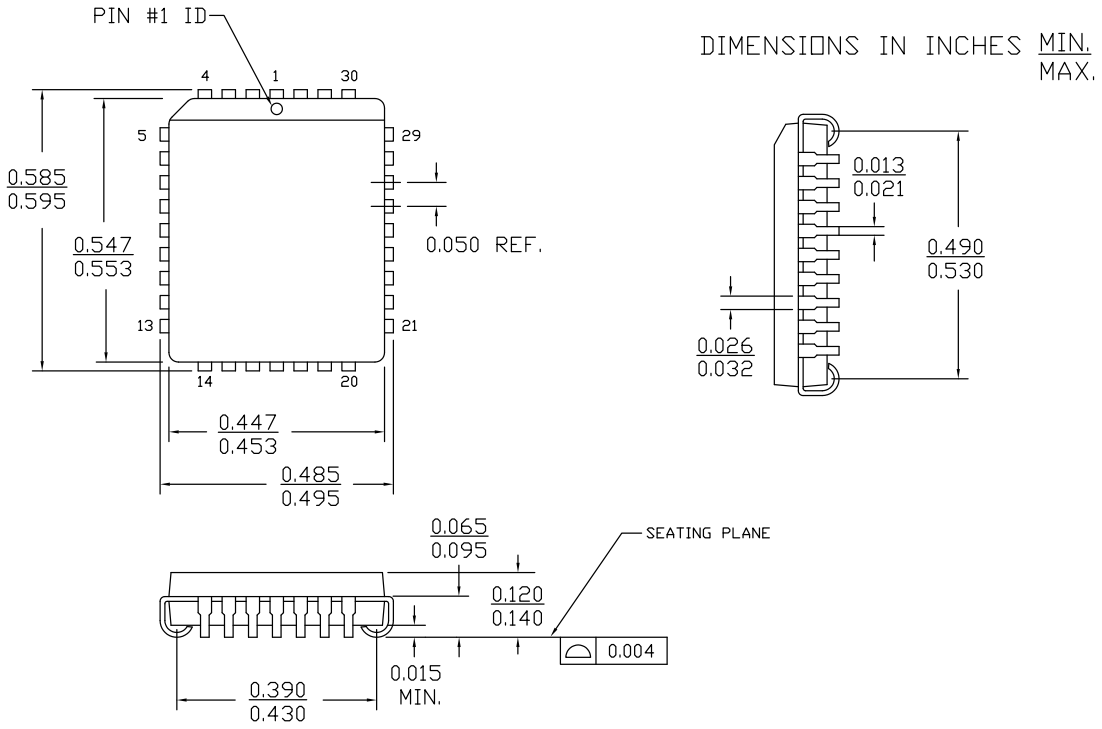
Ordering Code	Package Type	Operating Range
CY7B9911V-5JC	32-pin PLCC	Commercial
CY7B9911V-5JCT	32-Pin PLCC – Tape and Reel	Commercial
Pb-free		
CY7B9911V-5JXC	32-pin PLCC	Commercial
CY7B9911V-5JXCT	32-pin PLCC – Tape and Reel	Commercial

Ordering Code Definitions



Package Diagram

Figure 11. 32-pin PLCC (0.453 × 0.553 Inches) Package Outline, 51-85002



51-85002 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
FB	Feedback
LVPSCB	Low-Voltage Programmable Skew Clock Buffer
LVTTL	Low-Voltage Transistor-Transistor Logic
OE	Output Enable
PLL	Phase-Locked Loop
PLCC	Plastic Leaded Chip Carrier
RF	Reference Frequency
RMS	Root Mean Square
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY7B9911V, 3.3 V RoboClock+™, High-Speed, Low-Voltage, Programmable Skew Clock Buffer Document Number: 38-07408				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	114350	DSG	03/20/2002	Changed specification number from 38-00765 to 38-07408.
*A	299713	RGL	12/14/2004	Updated Switching Characteristics: Added 100 ps as typical value for t_{JR} parameter corresponding to “Peak”. Updated Ordering Information: Updated part numbers.
*B	404630	RGL	10/31/2005	Updated Ordering Information: No change in part numbers. Added “(Pure Sn)” next to Lead-free.
*C	1199925	KVM / AESA	06/29/2007	Updated Ordering Information: No change in part numbers. Replaced “Lead-free (Pure Sn)” with “Pb-Free”. Added Note “Parts not recommended for the new design.” and referred the same note in CY7B9911V-7JC, CY7B9911V-7JCT, CY7B9911V-7JXC, CY7B9911V-7JXCT. Updated to new template.
*D	1286064	AESA	07/18/2007	Change status from Preliminary to Final.
*E	2894960	KVM	03/18/2010	Updated Switching Characteristics: Removed 7 ns speed bin related information. Added 5 ns speed bin related information. Updated Ordering Information: Updated part numbers. Removed Note “Parts not recommended for the new design.” and its reference. Updated Package Diagram: spec 51-85002 – Changed revision from *B to *C.
*F	3218954	BASH	04/07/2011	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*G	4345036	XHT	04/14/2014	Updated Package Diagram: spec 51-85002 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*H	4570105	XHT	01/16/2015	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85002 – Changed revision from *D to *E.
*I	4635424	TAVA	01/22/2015	Updated Switching Characteristics: Changed minimum value of t_{RPWH} parameter from 5 ns to 3.65 ns. Changed minimum value of t_{RPWL} parameter from 5 ns to 3.65 ns.
*J	4719592	XHT	04/15/2015	Updated Electrical Characteristics: Changed maximum value of V_{IH} parameter from “V_{CC}” to “V_{CC} + 0.5”. Completing Sunset Review.
*K	5245116	PSR	04/27/2016	Updated Electrical Characteristics: Updated Note 8 (Replaced “FC = F < C” with “FC = F × C”). Added Thermal Resistance. Updated to new template.
*L	6134828	XHT	04/12/2018	Updated to new template. Completing Sunset Review.

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