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**Description**

The AUIRS2336S are high voltage, high speed, power MOSFET and IGBT gate drivers with three high-side and three low-side referenced output channels for 3-phase applications. This IC is designed to be used with low-cost bootstrap power supplies. Proprietary HVIC and latch immune CMOS technologies have been implemented in a rugged monolithic structure. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3 V logic). A current trip function which terminates all six outputs can be derived from an external current sense resistor. Enable functionality is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that a fault (e.g., over-current, over-temperature, or undervoltage shutdown event) has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Shoot-through protection circuitry and a minimum deadtime circuitry have been integrated into this IC. Propagation delays are matched to simplify the HVIC's use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high-side configuration, which operate up to 600 V.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Automotive (per AEC-Q100 <sup>††</sup> )
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
<b>Moisture Sensitivity Level</b>		MSL3 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (200V) (per AEC-Q100-003)
	Human Body Model	Class H1C (1500V) (per AEC-Q100-002)
	Charged Device Model	Class C4 (1000V) (per AEC-Q100-011)
<b>IC Latch-Up Test</b>		Class II Level A (per AEC-Q100-004)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Voltage clamps are included between  $V_{CC}$  & COM (25 V),  $V_{CC}$  &  $V_{SS}$  (20 V), and  $V_B$  &  $V_S$  (20 V).

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low side supply voltage	-0.3	20 <sup>†</sup>	V
$V_{IN}$	Logic input voltage (HIN, LIN, ITRIP, EN)	$V_{SS}-0.3$	$V_{SS}+5.2$	
$V_{RCIN}$	RCIN input voltage	$V_{SS}-0.3$	$V_{CC}+0.3$	
$V_B$	High-side floating well supply voltage	-0.3	620 <sup>†</sup>	
$V_S$	High-side floating well supply return voltage	$V_B-20^{\dagger}$	$V_B+0.3$	
$V_{HO}$	Floating gate drive output voltage	$V_S-0.3$	$V_B+0.3$	
$V_{LO}$	Low-side output voltage	COM-0.3	$V_{CC}+0.3$	
$V_{FLT}$	Fault output voltage	$V_{SS}-0.3$	$V_{CC}+0.3$	
COM	Power ground	$V_{CC}-25$	$V_{CC}+0.3$	
$dV_S/dt$	Allowable $V_S$ offset supply transient relative to $V_{SS}$	—	50	V/ns
$PW_{HIN}$	High-side input pulse width	500	—	ns
$P_D$	Package power dissipation @ $T_A \leq +25^{\circ}\text{C}$	—	1.6	W
$R_{thJA}$	Thermal resistance, junction to ambient	—	78	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction temperature	—	150	$^{\circ}\text{C}$
$T_S$	Storage temperature	-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are tested at 25 V. An internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless otherwise stated in the table. The offset rating is tested with supplies of  $(V_{CC}-COM) = (V_B-V_S) = 15\text{ V}$ .

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low-side supply voltage	10	20	V
$V_{IN}$	HIN, LIN, & EN input voltage	$V_{SS}$	$V_{SS}+5$	
$V_B$	High-side floating well supply voltage	$V_S+10$	$V_S+20$	
$V_S$	High-side floating well supply offset voltage <sup>†</sup>	COM-8	600	
$V_S(t)$	Transient high-side floating supply voltage <sup>††</sup>	-50	600	
$V_{HO}$	Floating gate drive output voltage	$V_S$	$V_B$	
$V_{LO}$	Low-side output voltage	COM	$V_{CC}$	
COM	Power ground	-5	5	
$V_{FLT}$	FAULT output voltage	$V_{SS}$	$V_{CC}$	
$V_{RCIN}$	RCIN input voltage	$V_{SS}$	$V_{CC}$	
$V_{ITRIP}$	ITRIP input voltage	$V_{SS}$	$V_{SS}+5$	
$T_A$	Ambient temperature	-40	125	°C

† Logic operation for  $V_S$  of -8 V to 600 V. Logic state held for  $V_S$  of -8 V to  $-V_{BS}$ .

†† Operational for transient negative  $V_S$  of  $V_{SS} - 50\text{ V}$  with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

### Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $(V_{CC}-COM) = (V_B-V_S) = 15\text{ V}$ . The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels. The  $V_O$  and  $I_O$  parameters are referenced to respective  $V_S$  and COM and are applicable to the respective output leads HO or LO. The  $V_{CCUV}$  parameters are referenced to  $V_{SS}$ . The  $V_{BSUV}$  parameters are referenced to  $V_S$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V <sub>CCUV+</sub>	V <sub>CC</sub> supply undervoltage positive going threshold	8	8.9	9.8	V	NA
V <sub>CCUV-</sub>	V <sub>CC</sub> supply undervoltage negative going threshold	7.4	8.2	9		
V <sub>CCUVHY</sub>	V <sub>CC</sub> supply undervoltage hysteresis	0.3	0.7	—		
V <sub>BSUV+</sub>	V <sub>BS</sub> supply undervoltage positive going threshold	8	8.9	9.8		
V <sub>BSUV-</sub>	V <sub>BS</sub> supply undervoltage negative going threshold	7.4	8.2	9		
V <sub>BSUVHY</sub>	V <sub>BS</sub> supply undervoltage hysteresis	0.3	0.7	—		
I <sub>LK</sub>	High-side floating well offset supply leakage	—	—	50	μA	V <sub>B</sub> = V <sub>S</sub> = 600 V
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> supply current	—	70	120		All inputs are in the off state
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> supply current	—	2	3	mA	
V <sub>OH</sub>	High level output voltage drop, V <sub>BIAS</sub> -V <sub>O</sub>	—	0.90	1.5	V	I <sub>O</sub> = 20 mA
V <sub>OL</sub>	Low level output voltage drop, V <sub>O</sub>	—	0.40	0.6	V	
I <sub>O+</sub>	Output high short circuit pulsed current	75	200	—	mA	V <sub>O</sub> =0 V, V <sub>IN</sub> =0 V, PW ≤ 10 μs
I <sub>O-</sub>	Output low short circuit pulsed current	150	350	—		V <sub>O</sub> =15 V, V <sub>IN</sub> =5 V, PW ≤ 10 μs
V <sub>IH</sub>	Logic “0” input voltage	2.5	—	—	V	NA
	Logic “1” input voltage					
V <sub>IL</sub>	Logic “1” input voltage	—	—	0.8		
	Logic “0” input voltage					
V <sub>IN,CLAMP</sub>	Input voltage clamp (HIN, LIN, ITRIP and EN)	4.8	5.2	5.65		I <sub>IN</sub> = 100 μA
I <sub>HIN+</sub>	Input bias current (HO = High)	—	150	200	μA	V <sub>IN</sub> = 0 V
I <sub>HIN-</sub>	Input bias current (HO = Low)	—	110	150		V <sub>IN</sub> = 4 V
I <sub>LIN+</sub>	Input bias current (LO = High)	—	150	200		V <sub>IN</sub> = 0 V
I <sub>LIN-</sub>	Input bias current (LO = Low)	—	110	150		V <sub>IN</sub> = 4 V
V <sub>RCIN,TH</sub>	RCIN positive going threshold	—	8	—	V	NA
V <sub>RCIN,HY</sub>	RCIN hysteresis	—	3	—		
I <sub>RCIN</sub>	RCIN input bias current	—	—	1	μA	V <sub>RCIN</sub> = 0 V or 15 V
R <sub>ON RCIN</sub>	RCIN low on resistance	—	50	100	Ω	I = 1.5 mA

**Static Electrical Characteristics (continued)**

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55	V	NA
$V_{IT,TH-}$	ITRIP negative going threshold	—	0.4	—		
$V_{IT,HYS}$	ITRIP hysteresis	—	0.07	—		
$I_{ITRIP+}$	“High” ITRIP input bias current	—	5	20	$\mu A$	$V_{IN} = 4\text{ V}$
$I_{ITRIP-}$	“Low” ITRIP input bias current	—	—	1		$V_{IN} = 0\text{ V}$
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5	V	NA
$V_{EN,TH-}$	Enable negative going threshold	0.8	—	—		
$I_{EN+}$	“High” enable input bias current	—	5	20	$\mu A$	$V_{IN} = 4\text{ V}$
$I_{EN-}$	“Low” enable input bias current	—	—	1		$V_{IN} = 0\text{ V}$
$R_{ON,FLT}$	FAULT low on resistance	—	50	100	$\Omega$	$I = 1.5\text{ mA}$

### Dynamic Electrical Characteristics

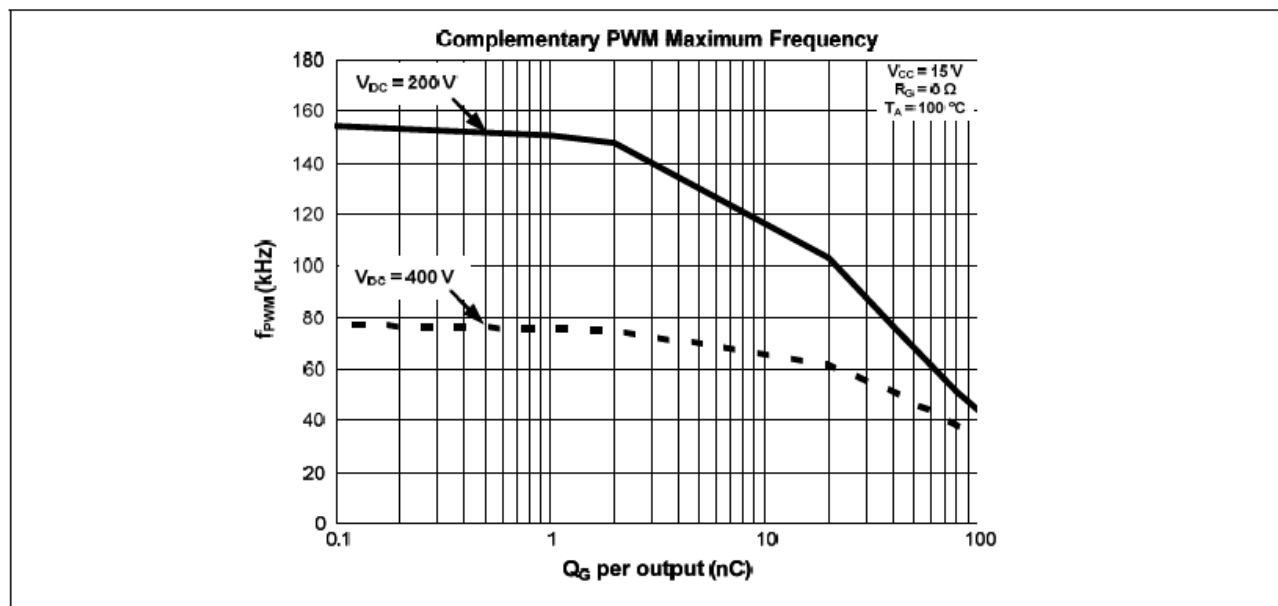
Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{CC} = V_B = 15\text{ V}$ ,  $V_S = V_{SS} = \text{COM}$ ,  $T_A = 25^{\circ}\text{C}$ , and  $C_L = 1000\text{ pF}$ . The dynamic electrical characteristics are measured using the test definitions shown in Figure .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{ON}$	Turn-on propagation delay	400	530	750	ns	$V_{IN} = 0\text{ V} \text{ \& } 5\text{ V}$
$t_{OFF}$	Turn-off propagation delay	400	530	750		
$t_R$	Turn-on rise time	—	125	320		
$t_F$	Turn-off fall time	—	50	120		
$t_{FIL,IN}$	Input filter time <sup>†</sup> ( $H_{IN}$ , $L_{IN}$ , $I_{TRIP}$ )	200	350	510		
$t_{EN}$	Enable low to output shutdown propagation delay	350	460	650	ms	$V_{IN}, V_{EN} = 0\text{ V} \text{ or } 5\text{ V}$
$t_{FILTER,EN}$	Enable input filter time	100	200	—		NA
$t_{FLTCLR}$	FAULT clear time RCIN: $R = 2\text{ M}\Omega$ , $C = 1\text{ nF}$	1	1.65	2.5		$V_{IN} = 0\text{ V} \text{ or } 5\text{ V}$ $V_{ITRIP} = 0\text{ V}$
$t_{ITRIP}$	ITRIP to output shutdown propagation delay	500	750	1200	ns	$V_{ITRIP} = 5\text{ V}$
$t_{BL}$	ITRIP blanking time	—	400	—		$V_{IN} = 0\text{ V} \text{ or } 5\text{ V}$ $V_{ITRIP} = 5\text{ V}$
$t_{FLT}$	ITRIP to FAULT propagation delay	400	600	950		$V_{IN} = 0\text{ V} \text{ \& } 5\text{ V}$ without external deadtime
DT	Deadtime	190	275	420		$V_{IN} = 0\text{ V} \text{ \& } 5\text{ V}$ with external deadtime larger than DT
MDT	DT matching <sup>††</sup>	—	—	100		PW input=10 $\mu\text{s}$
MT	Delay matching time ( $t_{ON}$ , $t_{OFF}$ ) <sup>††</sup>	—	—	50		
PM	Pulse width distortion <sup>†††</sup>	—	—	100		

† The minimum width of the input pulse is recommended to exceed 500 ns to ensure the filtering time of the input filter is exceeded.

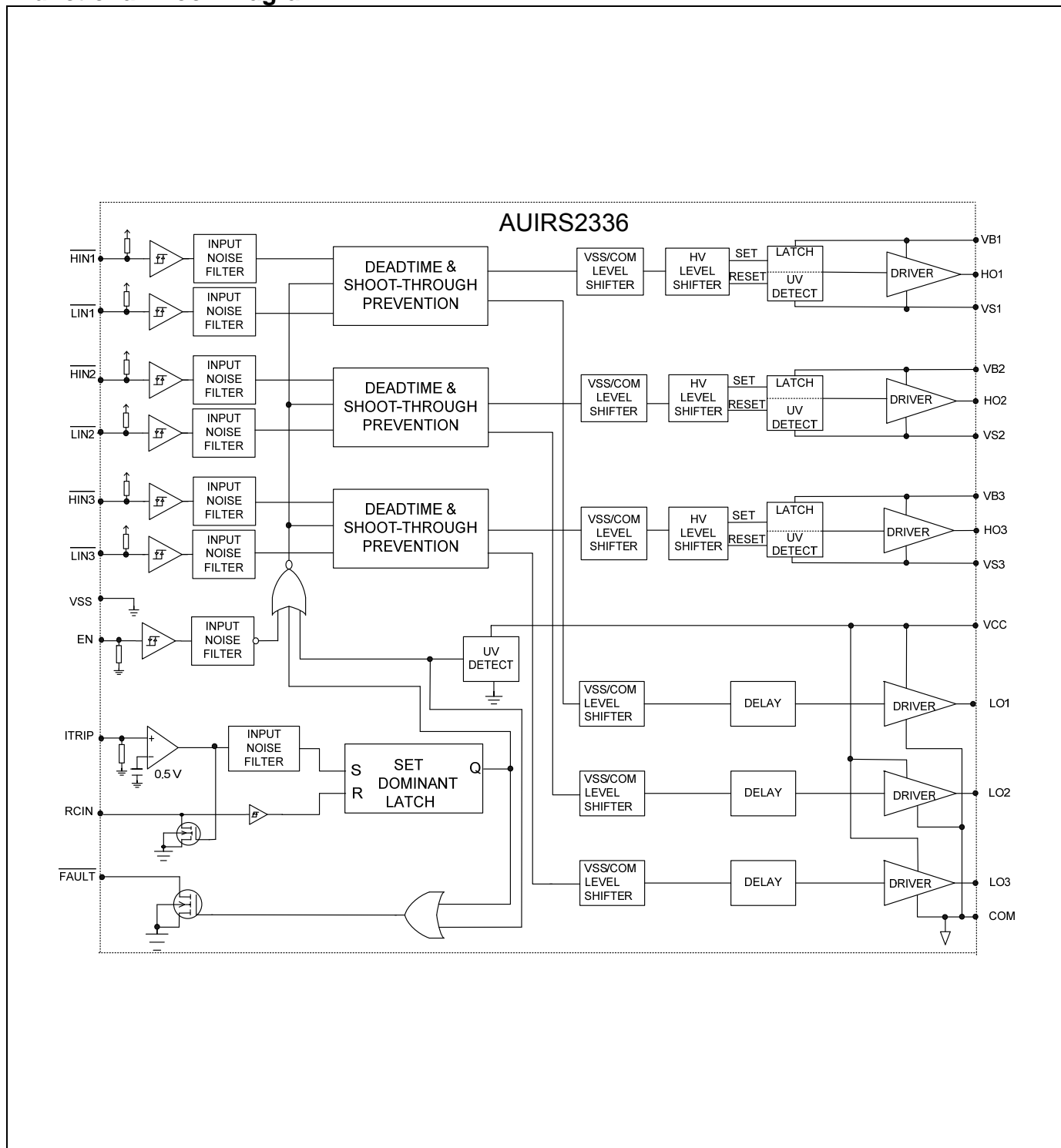
†† This parameter applies to all of the channels. Please see the application section for more details.

††† PM is defined as  $PW_{IN} - PW_{OUT}$ .

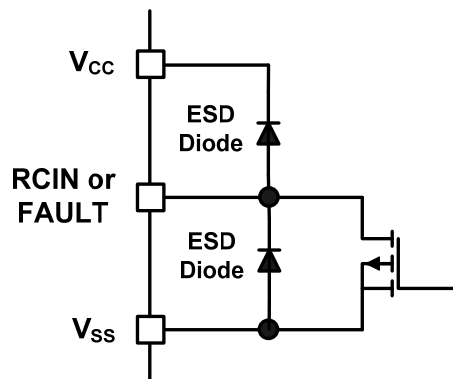
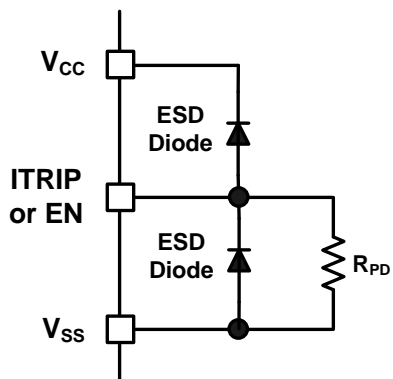
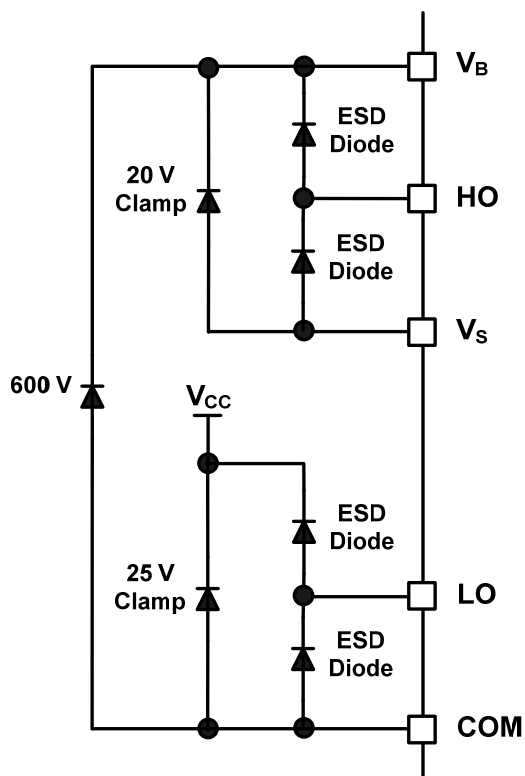
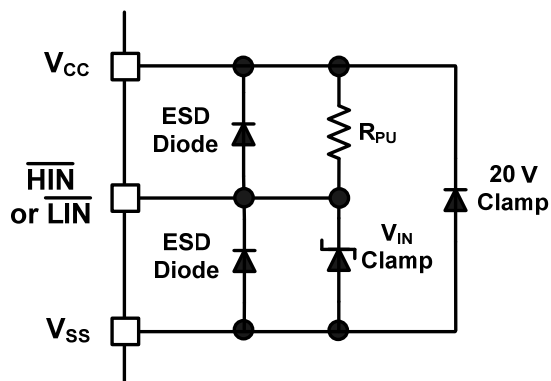




**Functional Block Diagram:**



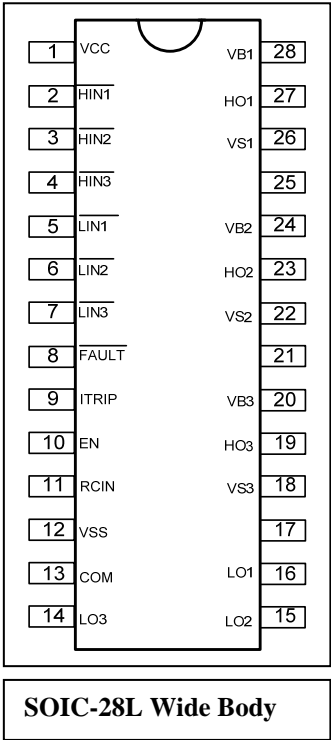
**Input/Output Pin Equivalent Circuit Diagrams:**



**Lead Definitions:**

Symbol	Description
VCC	Low-side supply voltage
VSS	Logic ground
VB1	High-side gate drive floating supply (phase 1)
VB2	High-side gate drive floating supply (phase 2)
VB3	High-side gate drive floating supply (phase 3)
VS1	High voltage floating supply return (phase 1)
VS2	High voltage floating supply return (phase 2)
VS3	High voltage floating supply return (phase 3)
HIN1/N	Logic inputs for high-side gate driver outputs (phase 1); input is out-of-phase with output
HIN2/N	Logic inputs for high-side gate driver outputs (phase 2); input is out-of-phase with output
HIN3/N	Logic inputs for high-side gate driver outputs (phase 3); input is out-of-phase with output
LIN1/N	Logic inputs for low-side gate driver outputs (phase 1); input is out-of-phase with output
LIN2/N	Logic inputs for low-side gate driver outputs (phase 2); input is out-of-phase with output
LIN3/N	Logic inputs for low-side gate driver outputs (phase 3); input is out-of-phase with output
HO1	High-side driver outputs (phase 1)
HO2	High-side driver outputs (phase 2)
HO3	High-side driver outputs (phase 3)
LO1	Low-side driver outputs (phase 1)
LO2	Low-side driver outputs (phase 2)
LO3	Low-side driver outputs (phase 3)
COM	Low-side gate drive return
FAULT/N	Indicates over-current, over-temperature (ITRIP), or low-side undervoltage lockout has occurred. This pin has negative logic and an open-drain output. The use of over-current and over-temperature protection requires the use of external components.
EN	Logic input to shutdown functionality. Logic functions when EN is high (i.e., positive logic). No effect on FAULT and not latched.
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time $t_{FLTCLR}$ , then automatically becomes inactive (open-drain high impedance).
RCIN	An external RC network input used to define the FAULT CLEAR delay ( $t_{FLTCLR}$ ) approximately equal to $R \cdot C$ . When $RCIN > 8\text{ V}$ , the FAULT pin goes back into an open-drain high-impedance state.

**Lead Assignments**



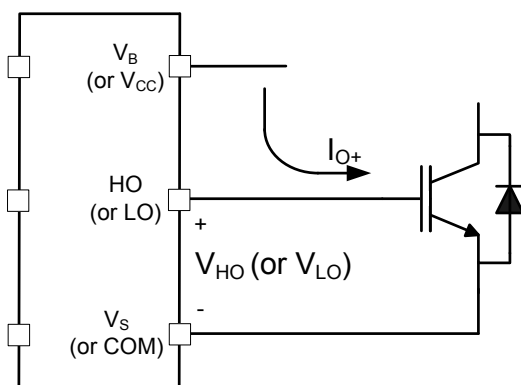
## Application Information and Additional Details

Information regarding the following topics are included as subsections within this section of the datasheet.

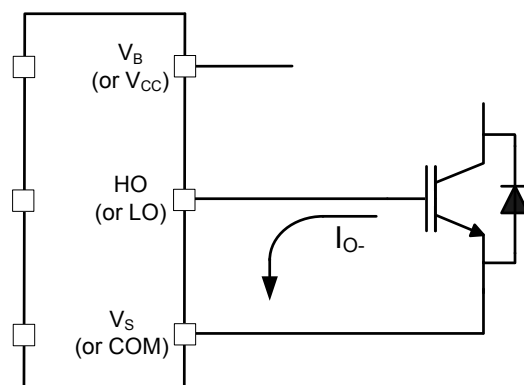
- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Deadtime
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Shoot-Through Protection
- Enable Input
- Fault Reporting and Programmable Fault Clear Timer
- Over-Current Protection
- Over-Temperature Shutdown Protection
- Truth Table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced Input Filter
- Short-Pulse / Noise Rejection
- Bootstrap Power Supply Design
- Separate Logic and Power Grounds
- Tolerant to Negative  $V_S$  Transients
- PCB Layout Tips
- Additional Documentation

### IGBT/MOSFET Gate Drive

The AUIRS2336S HVICs are designed to drive up to six MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as  $I_O$ . The voltage that drives the gate of the external power switch is defined as  $V_{HO}$  for the high-side power switch and  $V_{LO}$  for the low-side power switch; this parameter is sometimes generically called  $V_{OUT}$  and in this case does not differentiate between the high-side or low-side output voltage.



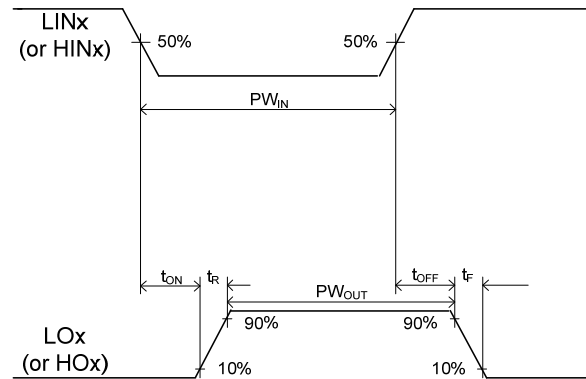
**Figure 1: HVIC sourcing current**



**Figure 2: HVIC sinking current**

### Switching and Timing Relationships

The relationship between the input and output signals of the AUIRS2336S is illustrated below in Figures 3. From these figures, we can see the definitions of several timing parameters (i.e.,  $PW_{IN}$ ,  $PW_{OUT}$ ,  $t_{ON}$ ,  $t_{OFF}$ ,  $t_R$ , and  $t_F$ ) associated with this device.



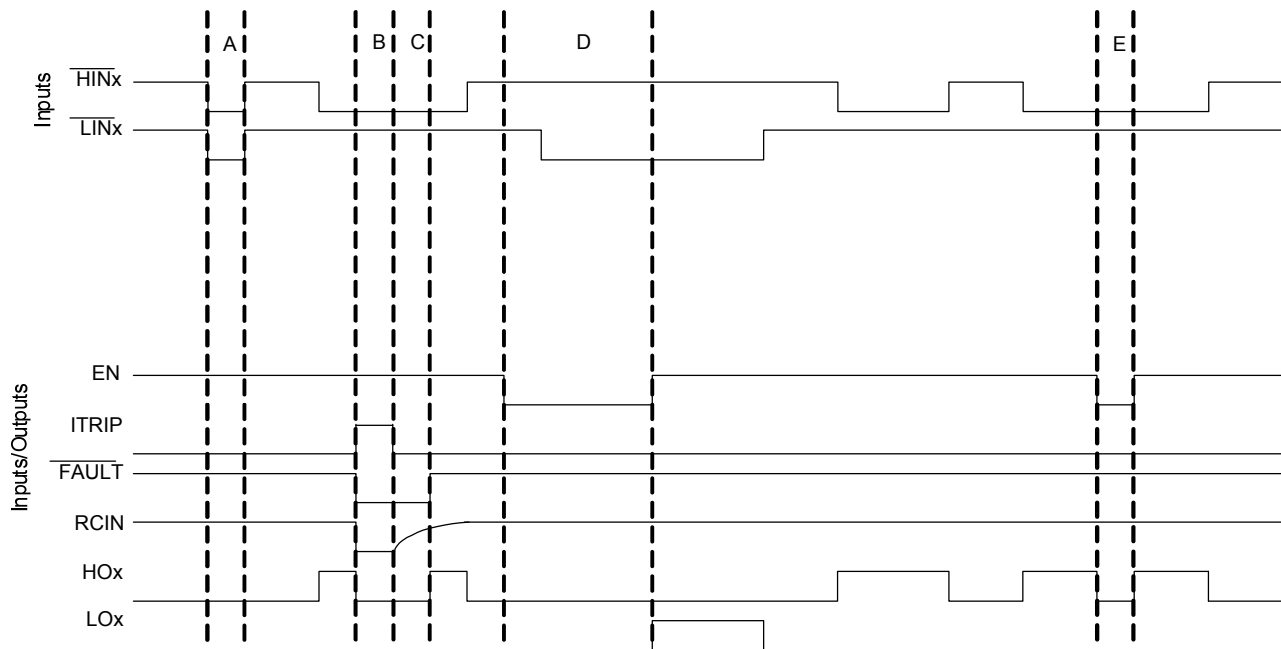
**Figure 3: Switching time waveforms**

The following two figures illustrate the timing relationships of some of the functionality of the AUIRS2336S; this functionality is described in further detail later in this document.

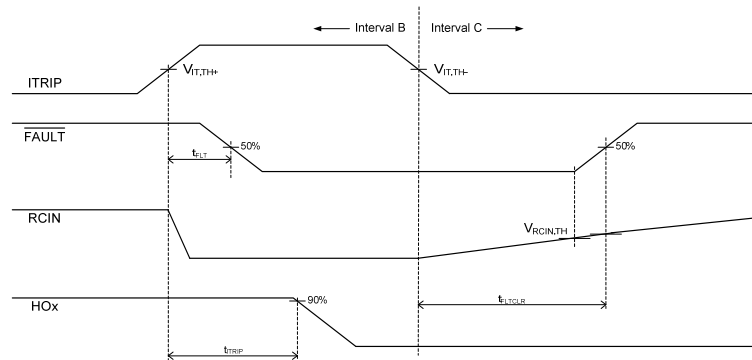
During interval A of Figure 5, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the high- and low-side output are held in the off state.

Interval B of Figures 5 and 6 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to  $V_{RCIN,TH}$  (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 5, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx) being held in the low state until the enable pin is pulled high.



**Figure 5: Input/output timing diagram for AUIRS2336S**

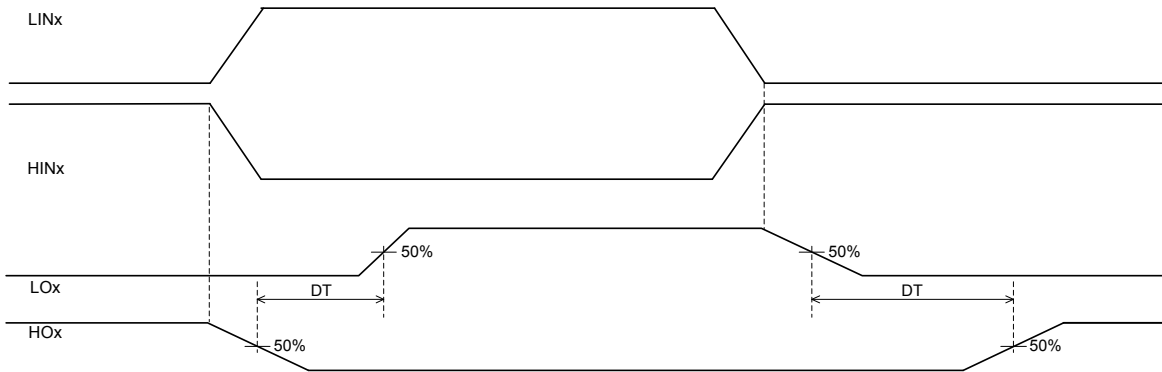


**Figure 6: Detailed view of B & C intervals**

## Deadtime

This HVIC features integrated deadtime protection circuitry. The deadtime for this ICs is fixed; other ICs within IR's HVIC portfolio feature programmable deadtime for greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 7 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of the AUIRS2336S is matched with respect to the high- and low-side outputs of a given channel; additionally, the deadtimes of each of the three channels are matched. Figure 7 defines the two deadtime parameters (i.e.,  $DT_1$  and  $DT_2$ ) of a specific channel; the deadtime matching parameter (MDT) associated with the AUIRS2336S specifies the maximum difference between  $DT_1$  and  $DT_2$ . The MDT parameter also applies when comparing the DT of one channel of the AUIRS2336S to that of another.



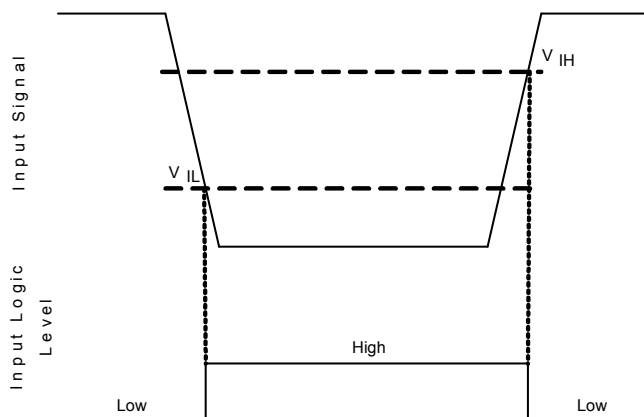
**Figure 7: Illustration of deadtime**

### Matched Propagation Delays

The AUIRS2336S is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e.,  $t_{ON}$ ,  $t_{OFF}$ ) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). Additionally, the propagation delay for each low-side channel is matched when compared to the other low-side channels and the propagation delays of the high-side channels are matched with each other; the MT specification applies as well. The propagation turn-on delay ( $t_{ON}$ ) of the AUIRS2336S is matched to the propagation turn-on delay ( $t_{OFF}$ ).

### Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The AUIRS2336S has been designed to be compatible with 3.3 V and 5 V logic-level signals. It features an integrated 5.2 V Zener clamp on the HIN, LIN, ITRIP, and EN pins; Figure 8 illustrates an input signal, its input threshold values, and the logic state of the IC as a result of the input signal.



**Figure 8: HIN & LIN input thresholds**



## Undervoltage Lockout Protection

This IC provides undervoltage lockout protection on both the  $V_{CC}$  (logic and low-side circuitry) power supply and the  $V_{BS}$  (high-side circuitry) power supply. Figure 9 is used to illustrate this concept;  $V_{CC}$  (or  $V_{BS}$ ) is plotted over time and as the waveform crosses the UVLO threshold ( $V_{CCUV+/-}$  or  $V_{BSUV+/-}$ ) the undervoltage protection is enabled or disabled.

Upon power-up, should the  $V_{CC}$  voltage fail to reach the  $V_{CCUV+}$  threshold, the IC will not turn-on. Additionally, if the  $V_{CC}$  voltage decreases below the  $V_{CCUV-}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the  $V_{BS}$  voltage fail to reach the  $V_{BSUV}$  threshold, the IC will not turn-on the high-side gate drive output. Additionally, if the  $V_{BS}$  voltage decreases below the  $V_{BSUV}$  threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

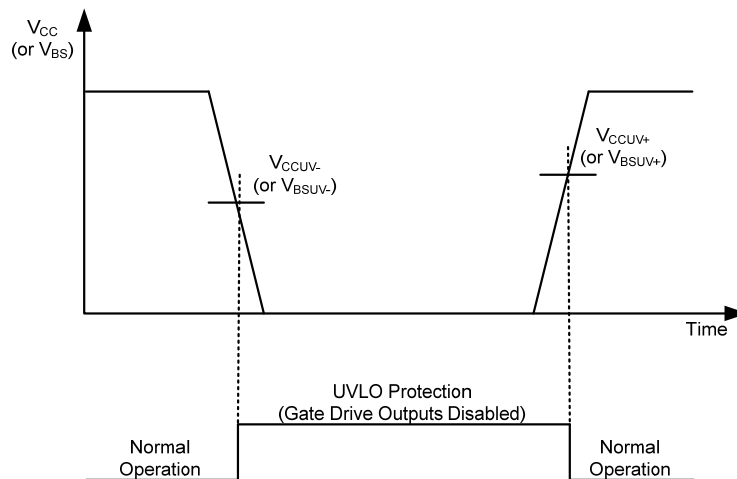


Figure 9: UVLO protection

## Shoot-Through Protection

The AUIRS2336S is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 10 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. Table 1 illustrates the input/output relationship of the devices in the form of a truth table.

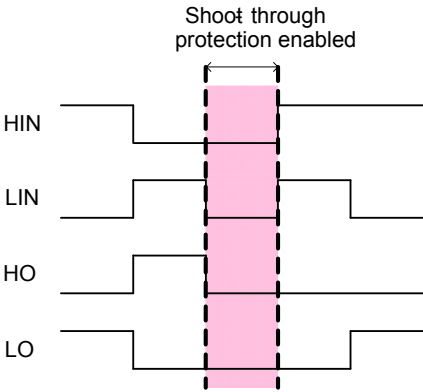


Figure 10: Illustration of shoot-through protection circuitry

HIN	LIN	HO	LO
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

Table 1: Input/output truth table

Enable Input

The AUIRS2336S is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state. The enable circuitry of the AUIRS2336S features an input filter; the minimum input duration is specified by  $t_{\text{FILTER,EN}}$ . Please refer to the EN pin parameters  $V_{\text{EN,TH+}}$ ,  $V_{\text{EN,TH-}}$ , and  $I_{\text{EN}}$  for the details of its use. Table 2 gives a summary of this pin’s functionality and Figure 11 illustrates the outputs’ response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled*
Enable input low	Outputs disabled

Table 2: Enable functionality truth table  
(\*assumes no other fault condition)

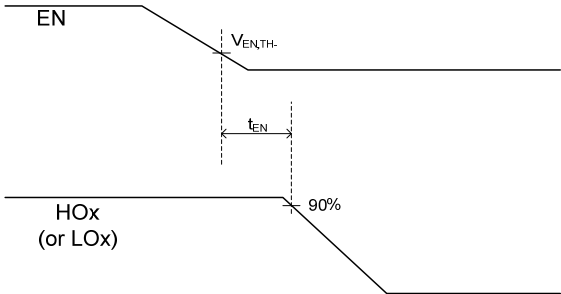


Figure 11: Output enable timing waveform

## Fault Reporting and Programmable Fault Clear Timer

The AUIRS2336S provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the FAULT pin. The first is an undervoltage condition of  $V_{CC}$  and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to  $V_{SS}$ . The fault clear timer is activated only if ITRIP pin recognizes a fault: in this case the fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to  $V_{CC}$ .

The length of the fault clear time period ( $t_{FLTCLR}$ ) is determined by exponential charging characteristics of the capacitor where the time constant is set by  $R_{RCIN}$  and  $C_{RCIN}$ . In Figure 12 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to  $V_{SS}$ , and once the fault has been removed, the fault clear timer begins. Figure 13 shows that  $R_{RCIN}$  is connected between the  $V_{CC}$  and the RCIN pin, while  $C_{RCIN}$  is placed between the RCIN and  $V_{SS}$  pins.

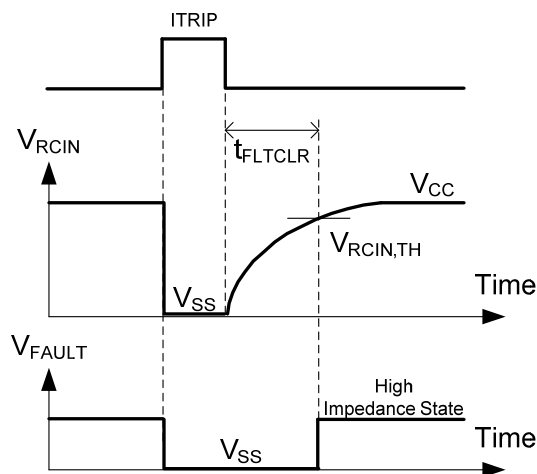


Figure 12: RCIN and FAULT pin waveforms

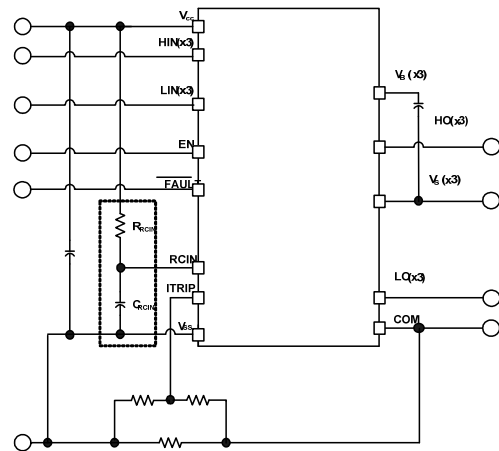


Figure 13: Programming the fault clear timer

The design guidelines for this network are shown in Table 3.

$C_{RCIN}$	$\leq 1 \text{ nF}$
	Ceramic
$R_{RCIN}$	$0.5 \text{ M}\Omega \text{ to } 2 \text{ M}\Omega$
	$\gg R_{ON,RCIN}$

Table 3: Design guidelines

The length of the fault clear time period can be determined by using the formula below.

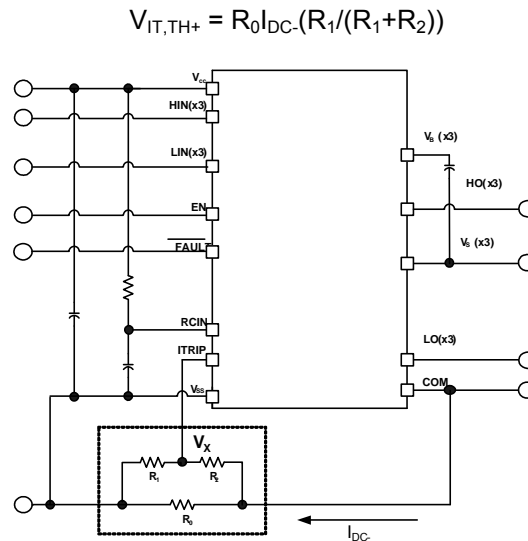
$$V_C(t) = V_i(1 - e^{-t/RC})$$

$$t_{FLTCLR} = -(R_{RCIN}C_{RCIN})\ln(1 - V_{RCIN,TH}/V_{CC})$$

### Over-Current Protection

The AUIRS2336S is equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to  $V_{SS}$ .

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e.,  $R_0$ ,  $R_1$ , and  $R_2$ ) connected to ITRIP as shown in Figure 14, and the ITRIP threshold ( $V_{IT,TH+}$ ). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select  $R_0$ ,  $R_1$ , and  $R_2$  such that the voltage at node  $V_X$  reaches the over-current threshold ( $V_{IT,TH+}$ ) at that current level.



**Figure 14: Programming the over-current protection**

For example, a typical value for resistor  $R_0$  could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

### Over-Temperature Shutdown Protection

The ITRIP input of the AUIRS2336S can also be used to detect over-temperature events in the system and initiate a shutdown of the HVIC (and power switches) at that time. In order to use this functionality, the circuit designer will need to design the resistor network as shown in Figure 15 and select the maximum allowable temperature.

This network consists of a thermistor and two standard resistors  $R_3$  and  $R_4$ . As the temperature changes, the resistance of the thermistor will change; this will result in a change of voltage at node  $V_X$ . The resistor values should be selected such the voltage  $V_X$  should reach the threshold voltage ( $V_{IT,TH+}$ ) of the ITRIP functionality by the time that the maximum allowable temperature is reached. The voltage of the ITRIP pin should not be allowed to exceed 5 V.

When using both the over-current protection and over-temperature protection with the ITRIP input, OR-ing diodes (e.g., DL4148) can be used. This network is shown in Figure 16; the OR-ing diodes have been labeled  $D_1$  and  $D_2$ .

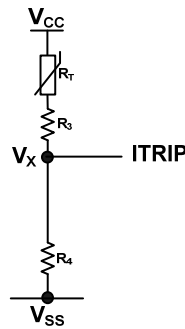


Figure 15: Programming over-temperature protection

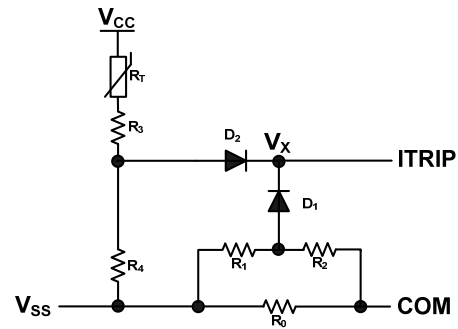


Figure 16: Using over-current protection and over-temperature protection

### Truth Table: Undervoltage lockout, ITRIP, and ENABLE

Table 4 provides the truth table for the AUIRS2336S. The first line shows that the UVLO for  $V_{CC}$  has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled.  $V_{CCUV}$  is not latched in this case and when  $V_{CC}$  is greater than  $V_{CCUV}$ , the FAULT output returns to the high impedance state.

The second case shows that the UVLO for  $V_{BS}$  has been tripped and that the high-side gate drive outputs have been disabled. After  $V_{BS}$  exceeds the  $V_{BSUV}$  threshold, HO will stay low until the HVIC input receives a new falling transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin. In the last case, the HVIC has received a command through the EN input to shutdown; as a result, the gate drive outputs have been disabled.

	VCC	VBS	ITRIP	EN	RCIN	FAULT	LO	HO
UVLO $V_{CC}$	$<V_{CCUV}$	—	—	—	High	0	0	0
UVLO $V_{BS}$	15 V	$<V_{BSUV}$	0 V	5 V	High	High impedance	LIN	0
Normal operation	15 V	15 V	0 V	5 V	High	High impedance	LIN	HIN
ITRIP fault	15 V	15 V	$>V_{ITRIP}$	5 V	Low	0	0	0
EN command	15 V	15 V	0 V	0 V	High	High impedance	0	0

Table 4: UVLO, ITRIP, EN, RCIN, & FAULT truth table

### Advanced Input Filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN, LIN, and EN inputs. The working principle of the new filter is shown in Figures 17 and 18.

Figure 17 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer than  $t_{FIL,IN}$ ; the resulting output is approximately the difference between the input signal and  $t_{FIL,IN}$ . The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer than  $t_{FIL,IN}$ ; the resulting output is approximately the difference between the input signal and  $t_{FIL,IN}$ .

Figure 18 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer than  $t_{FIL,IN}$ ; the resulting output is

approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer than  $t_{FIL,IN}$ ; the resulting output is approximately the same duration as the input signal.

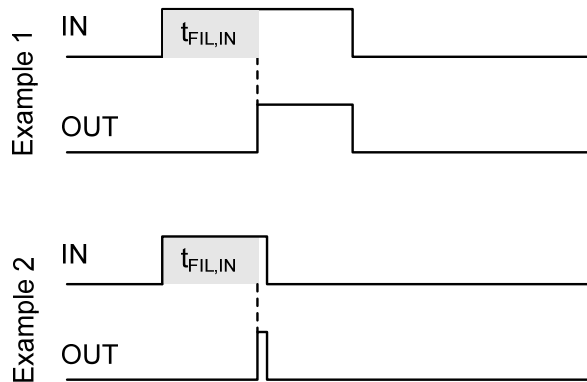


Figure 17: Typical input filter

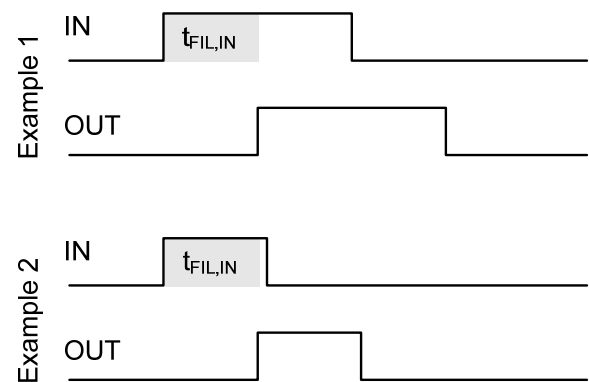


Figure 18: Advanced input filter

### Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than  $t_{FIL,IN}$ , the output will not change states. Example 1 of Figure 19 shows the output in the high state with input positive noise spikes of durations less than  $t_{FIL,IN}$ ; the output does not change states. Example 2 of Figure 19 shows the output in the low state with input negative noise spikes of durations less than  $t_{FIL,IN}$ ; the output does not change states.

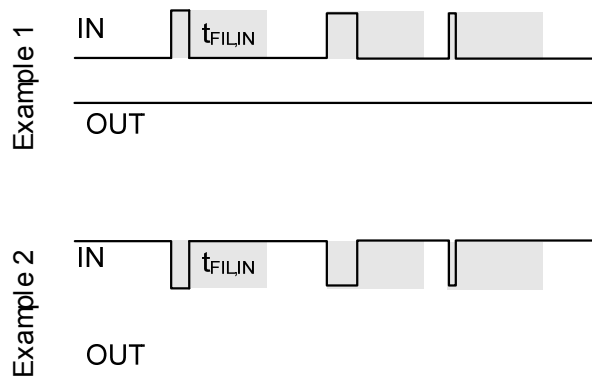


Figure 19: Noise rejecting input filters

Figures 20 and 21 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 20; the left side illustrates the narrow pulse ON (short negative pulse) characteristic while the left shows the narrow pulse OFF (short positive pulse) characteristic. The x-axis of Figure 20 shows the duration of  $PW_{IN}$ , while the y-axis shows the resulting  $PW_{OUT}$  duration. It can be seen that for a  $PW_{IN}$  duration less than  $t_{FIL,IN}$ , that the resulting  $PW_{OUT}$  duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the  $PW_{IN}$  duration exceed  $t_{FIL,IN}$ , that the  $PW_{OUT}$  durations mimic the  $PW_{IN}$  durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be  $\geq 500$  ns.

The difference between the  $PW_{OUT}$  and  $PW_{IN}$  signals of both the narrow ON and narrow OFF cases is shown in Figure 21; the careful reader will note the scale of the y-axis. The x-axis of Figure 21 shows the duration of  $PW_{IN}$ , while the y-axis shows the resulting  $PW_{OUT}-PW_{IN}$  duration. This data illustrates the performance and near symmetry of this input filter.

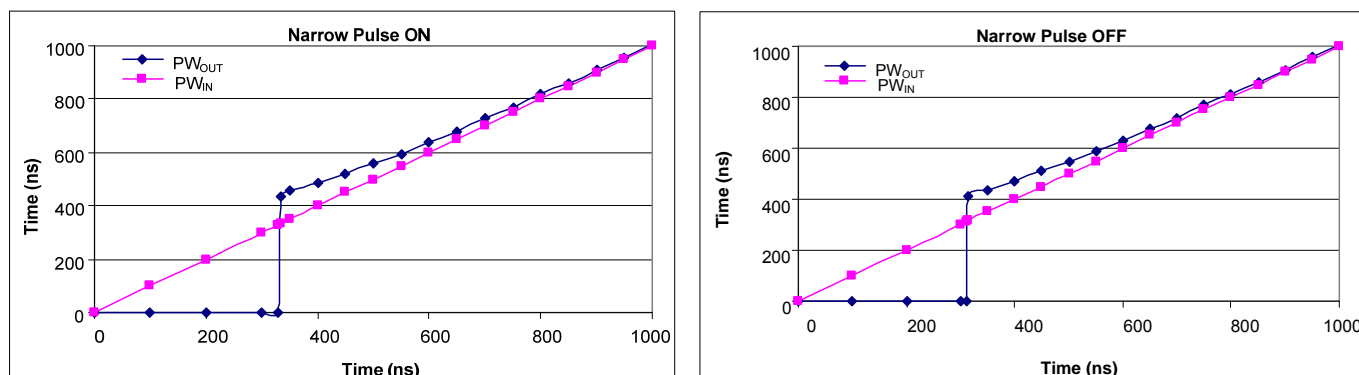


Figure 20: input filter characteristic

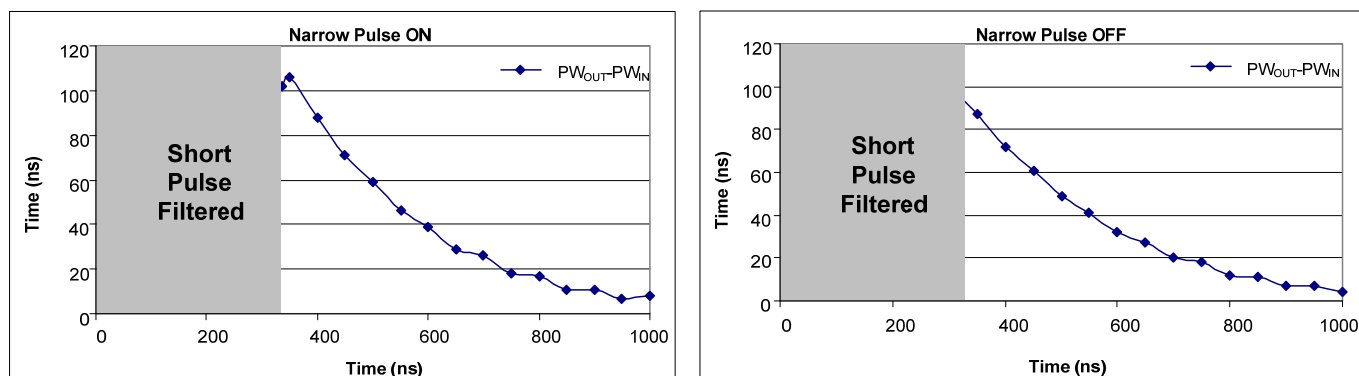
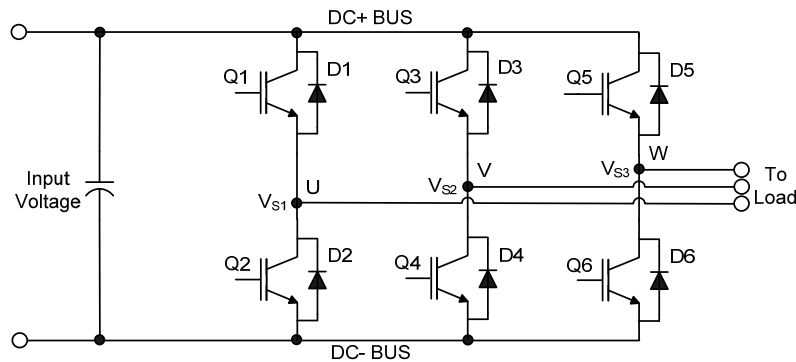


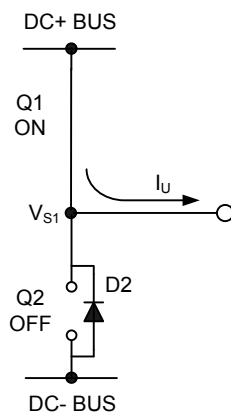
Figure 21: Difference between the input pulse and the output pulse



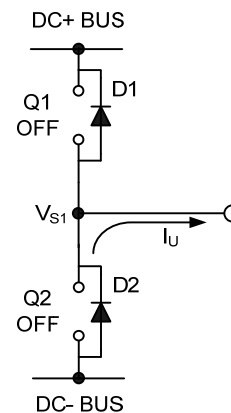




**Figure 25: Three phase inverter**

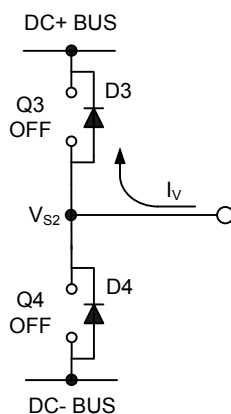


**Figure 26: Q1 conducting**

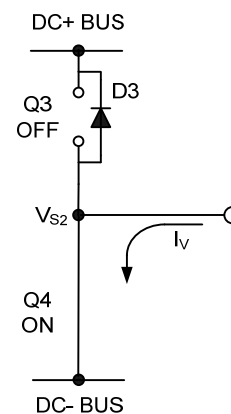


**Figure 27: D2 conducting**

Also when the V phase current flows from the inductive load back to the inverter (see Figures 28 and 29), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node,  $V_{S2}$ , swings from the positive DC bus voltage to the negative DC bus voltage.



**Figure 28: D3 conducting**

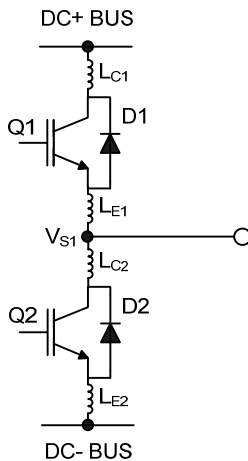


**Figure 29: Q4 conducting**

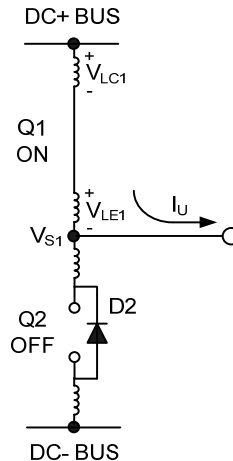
However, in a real inverter circuit, the  $V_S$  voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative  $V_S$  transient”.

The circuit shown in Figure 30 depicts one leg of the three phase inverter; Figures 31 and 32 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in  $L_C$  and  $L_E$  for each IGBT. When the high-side switch is on,

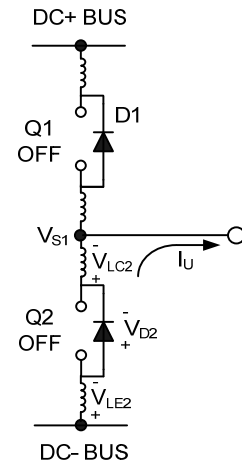
$V_{S1}$  is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to  $V_{S1}$  (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between  $V_{S1}$  and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the  $V_S$  pin).



**Figure 30: Parasitic Elements**



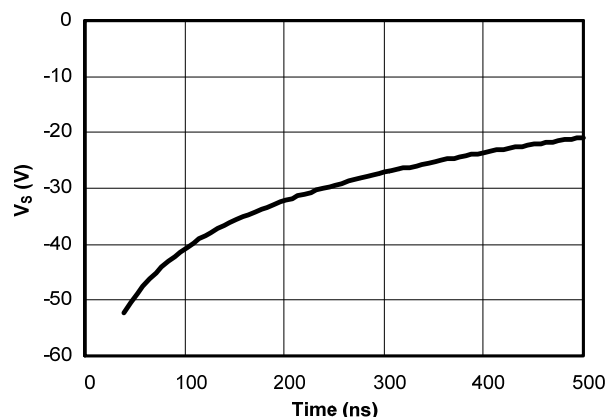
**Figure 31:  $V_S$  positive**



**Figure 32:  $V_S$  negative**

In a typical motor drive system,  $dV/dt$  is typically designed to be in the range of 3-5 V/ns. The negative  $V_S$  transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when  $di/dt$  is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. The AUIRS2336S has been seen to withstand large negative  $V_S$  transient conditions on the order of -50 V for a period of 50 ns. An illustration of the AUIRS2336S performance can be seen in Figure 33. This experiment was conducted using various loads to create this condition; the curve shown in this figure illustrates the successful operation of the AUIRS2336S under these stressful conditions. In case of  $-V_S$  transients greater than -20 V for a period of time greater than 100 ns, the HVIC is designed to hold the high-side outputs in the off state for 4.5  $\mu$ s in order to ensure that the high- and low-side power switches are not on at the same time.



**Figure 33: Negative  $V_S$  transient results for an International Rectifier HVIC**

Even though the AUIRS2336S has been shown able to handle these large negative  $V_S$  transient conditions, it is highly recommended that the circuit designer always limit the negative  $V_S$  transients as much as possible by careful PCB layout and component use.

## PCB Layout Tips

**Distance between high and low voltage components:** It's strongly recommended to place the components tied to the floating voltage pins ( $V_B$  and  $V_S$ ) near the respective high voltage portions of the device.

**Ground Plane:** In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

**Gate Drive Loops:** Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 34). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

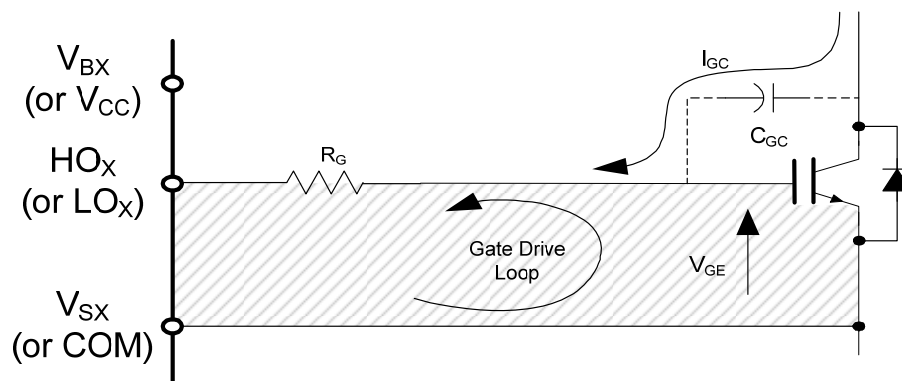


Figure 34: Antenna Loops

**Supply Capacitor:** It is recommended to place a bypass capacitor ( $C_{IN}$ ) between the  $V_{CC}$  and  $V_{SS}$  pins. This connection is shown in Figure 35. A ceramic 1  $\mu$ F ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

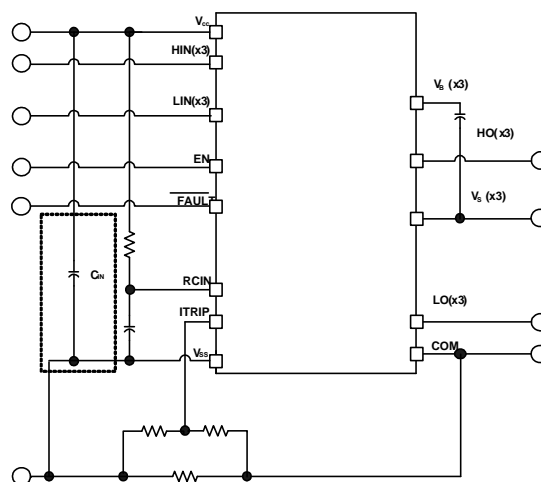
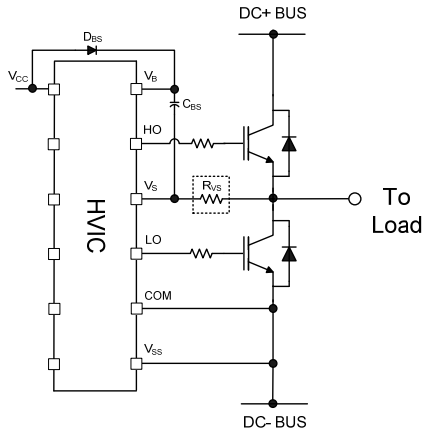
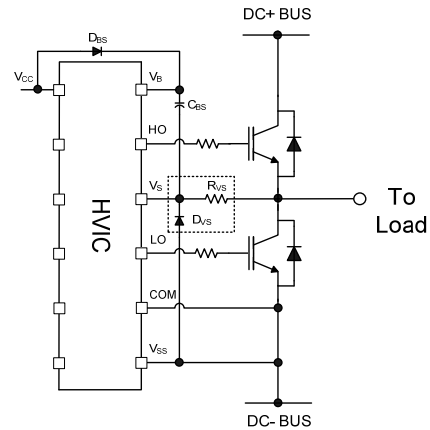


Figure 35: Supply capacitor

**Routing and Placement:** Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative  $V_S$  spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5  $\Omega$  or less) between the  $V_S$  pin and the switch node (see Figure 36), and in some cases using a clamping diode between  $V_{SS}$  and  $V_S$  (see Figure 37). See DT04-4 at [www.irf.com](http://www.irf.com) for more detailed information.



**Figure 36:  $V_S$  resistor**



**Figure 37:  $V_S$  clamping diode**

### Additional Documentation

Several technical documents related to the use of HVICs are available at [www.irf.com](http://www.irf.com); use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages

AN-1123: Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

DT04-4: Using Monolithic High Voltage Gate Drivers

AN-978: HV Floating MOS-Gate Driver ICs

## Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2336S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

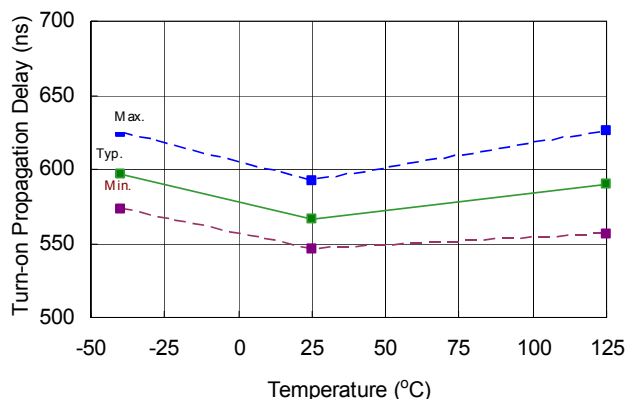


Figure 38:  $t_{ON}$  vs. temperature

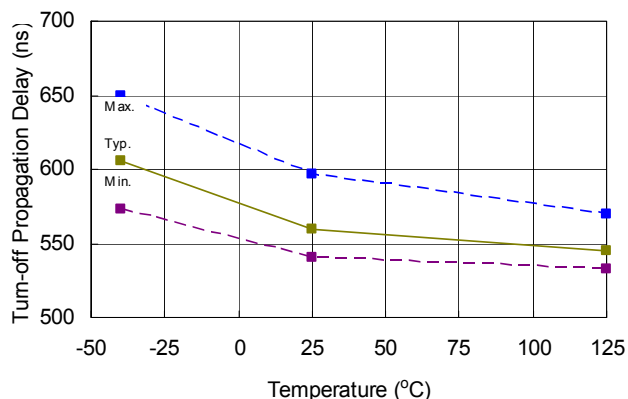


Figure 39:  $t_{OFF}$  vs. temperature

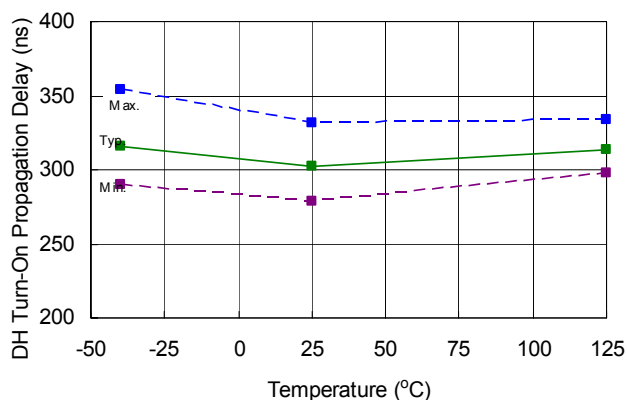


Figure 40: DT vs. temperature

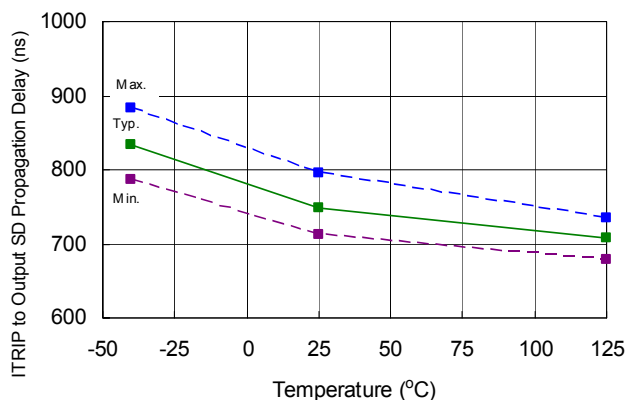


Figure 41:  $t_{ITRIP}$  vs. temperature

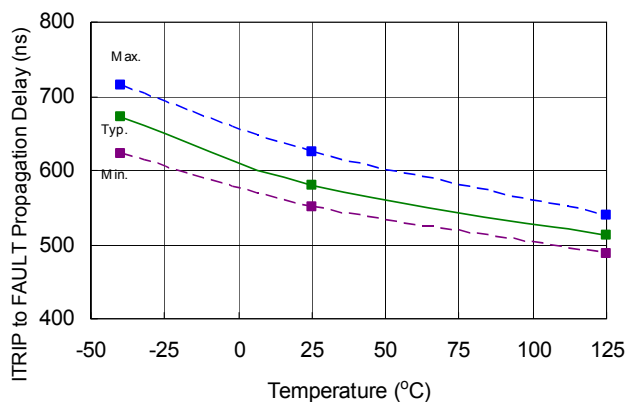


Figure 42:  $t_{FLT}$  vs. temperature

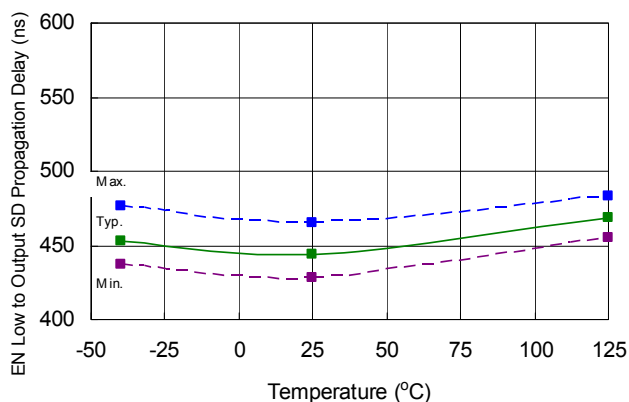


Figure 43:  $t_{EN}$  vs. temperature

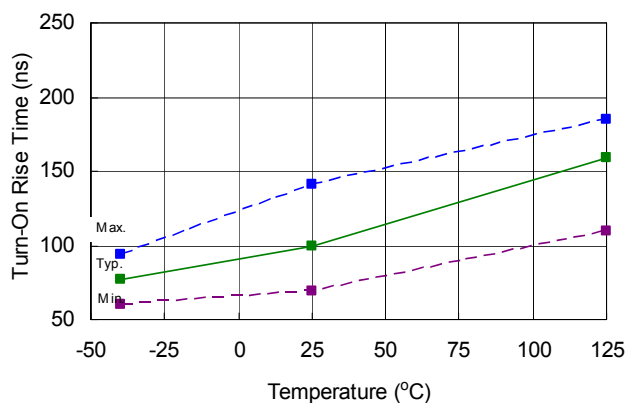


Figure 44:  $T_r$  vs. temperature

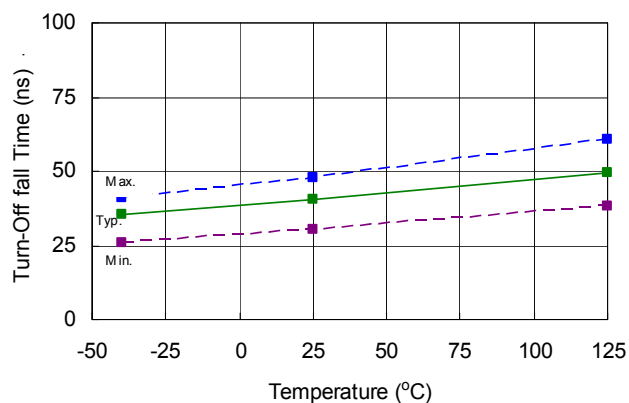


Figure 45:  $T_f$  vs. temperature

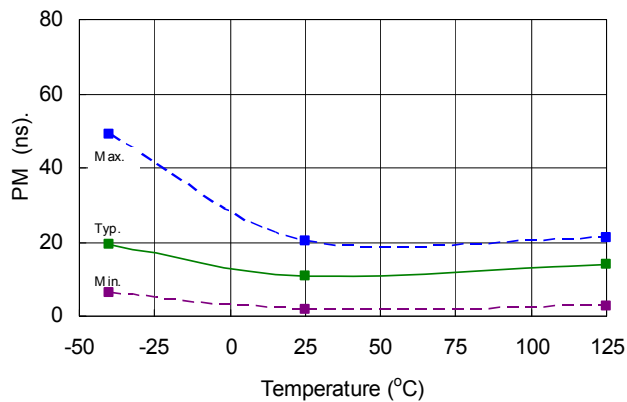


Figure 46:  $PM$  vs. temperature

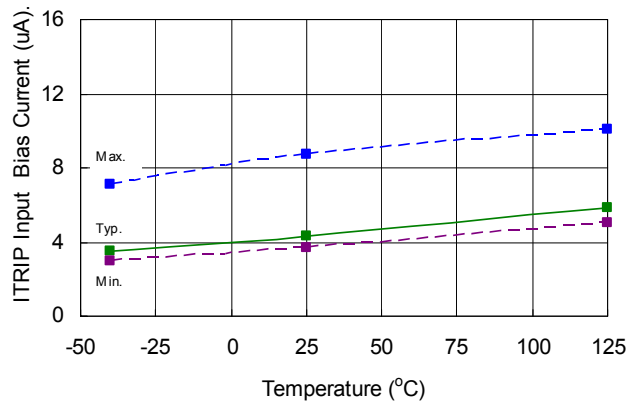


Figure 47:  $I_{ITRIP+}$  vs. temperature

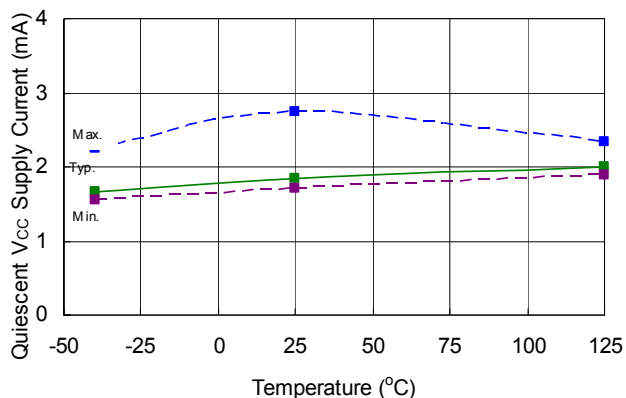


Figure 48:  $I_{QCC}$  vs. temperature

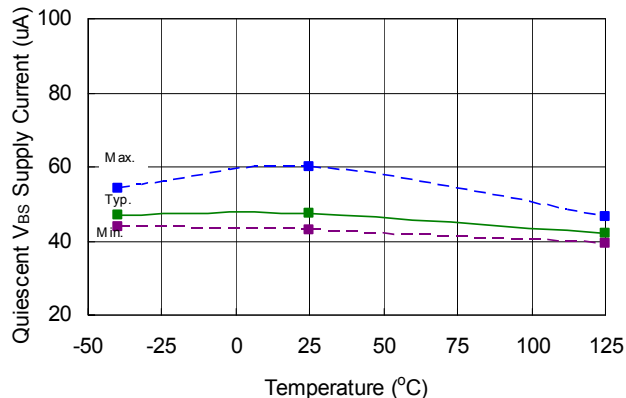


Figure 49:  $I_{QBS}$  vs. temperature

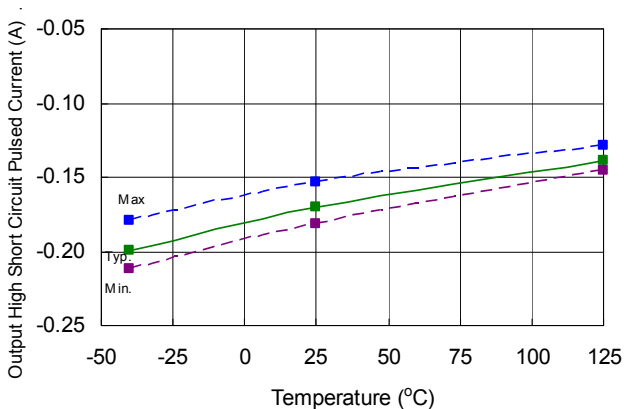


Figure 50:  $I_{O+}$  vs. temperature

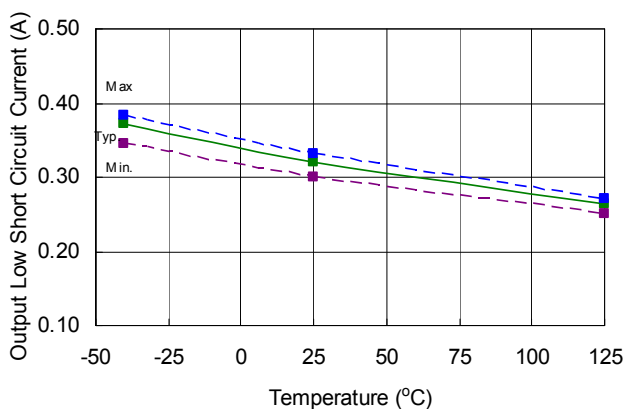


Figure 51:  $I_{O-}$  vs. temperature

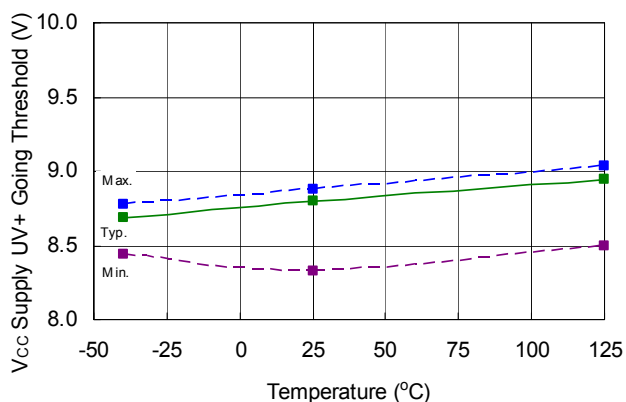


Figure 52:  $V_{CCUV+}$  vs. temperature

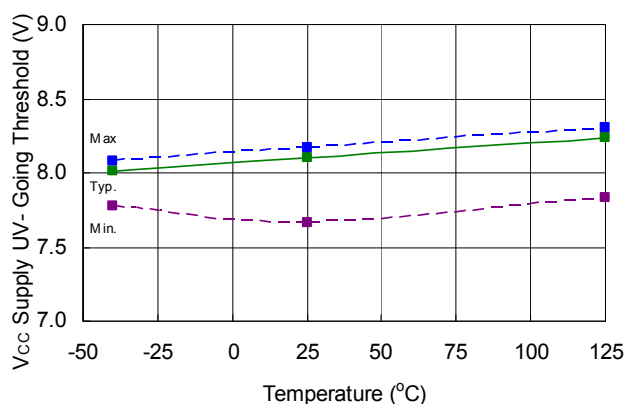


Figure 53:  $V_{CCUV-}$  vs. temperature

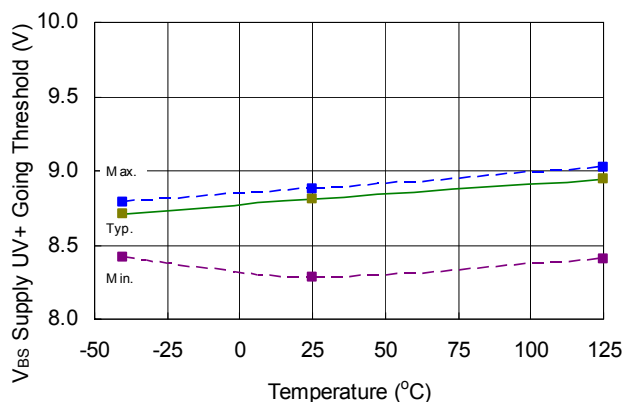


Figure 54:  $V_{BSUV+}$  vs. temperature

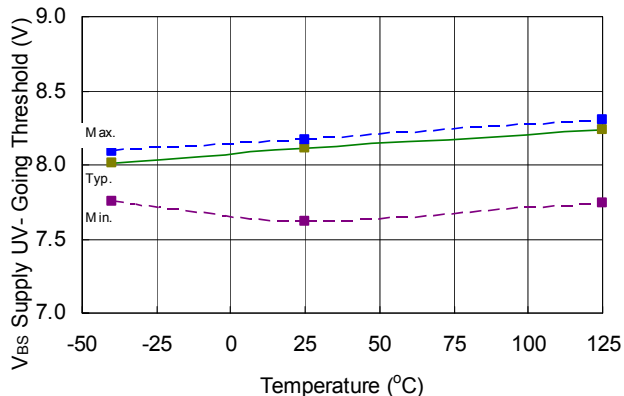


Figure 55:  $V_{BSUV-}$  vs. temperature

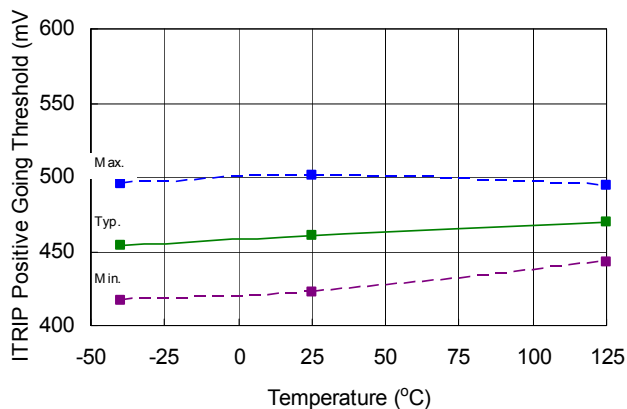


Figure 56:  $V_{IT,TH+}$  vs. temperature

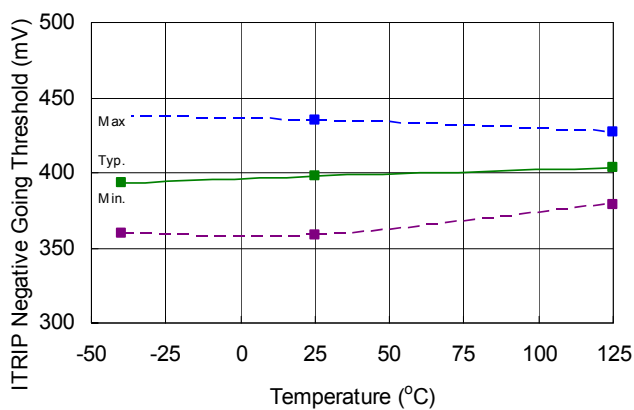


Figure 57:  $V_{IT,TH-}$  vs. temperature

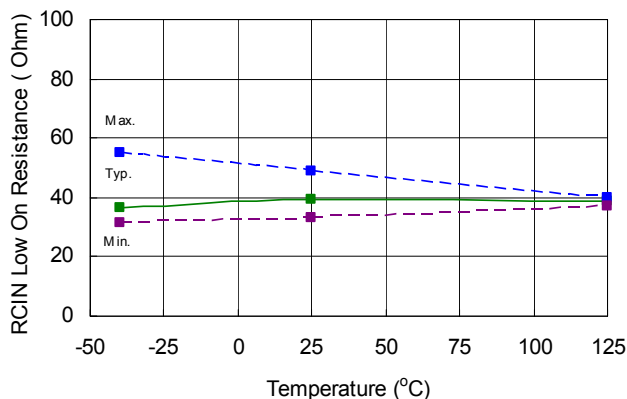


Figure 58:  $R_{ON,RCIN}$  vs. temperature

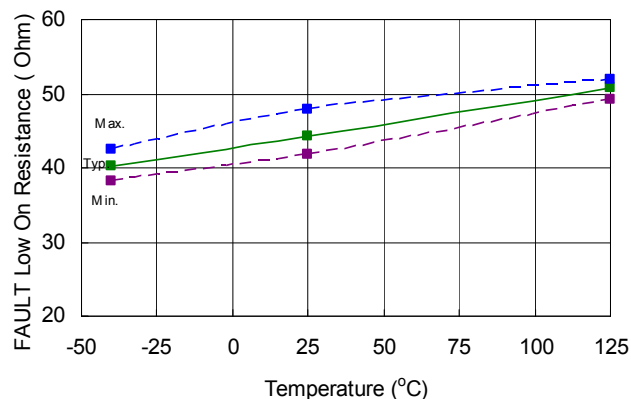
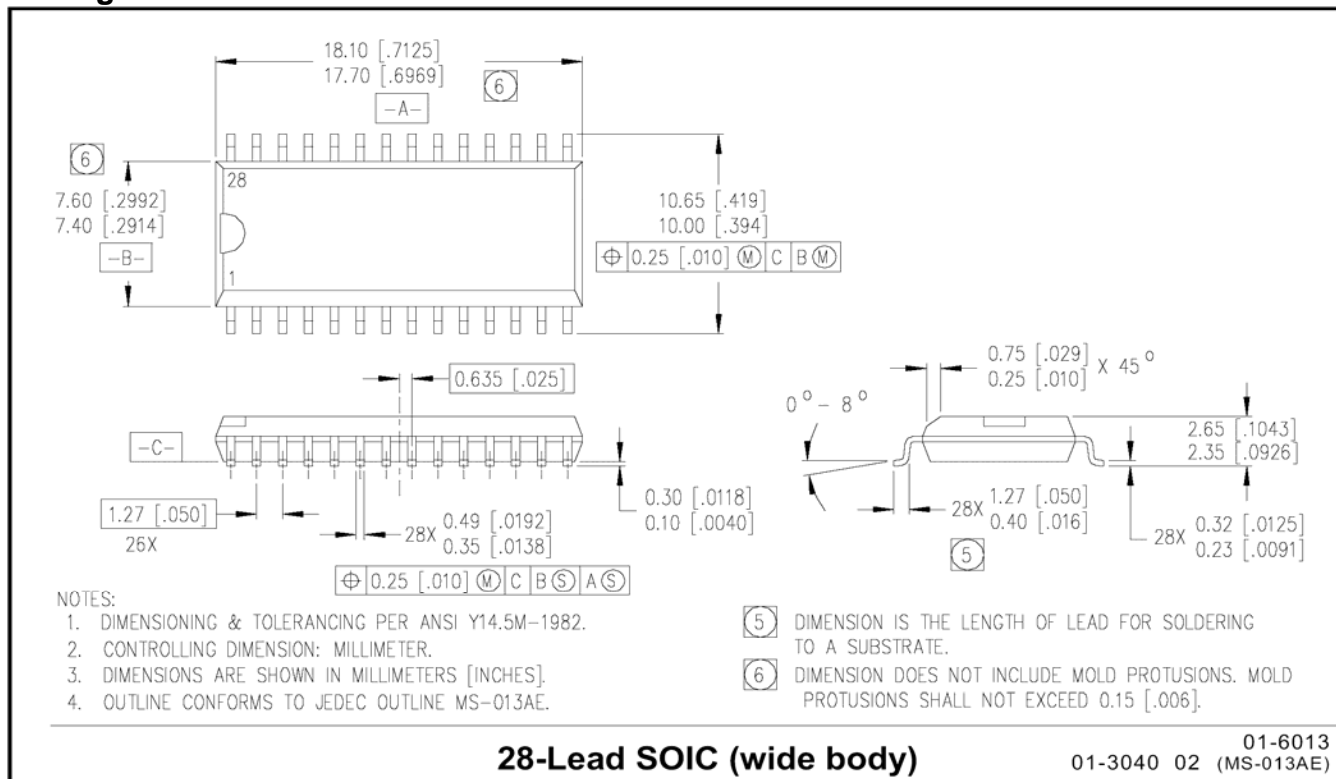


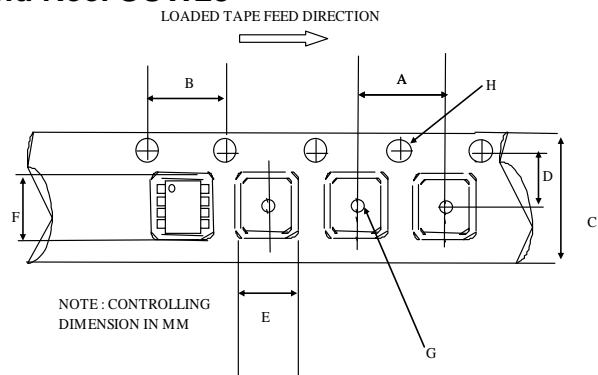
Figure 59:  $R_{ON,FLT}$  vs. temperature



**Package Details: SOIC28W**

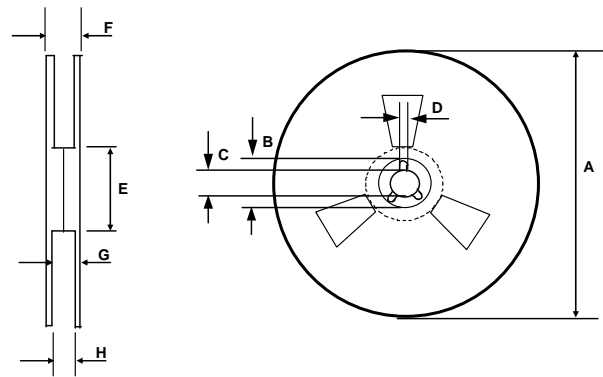


**Package Details: Tape and Reel SOW28**



CARRIER TAPE DIMENSION FOR 28SOICW

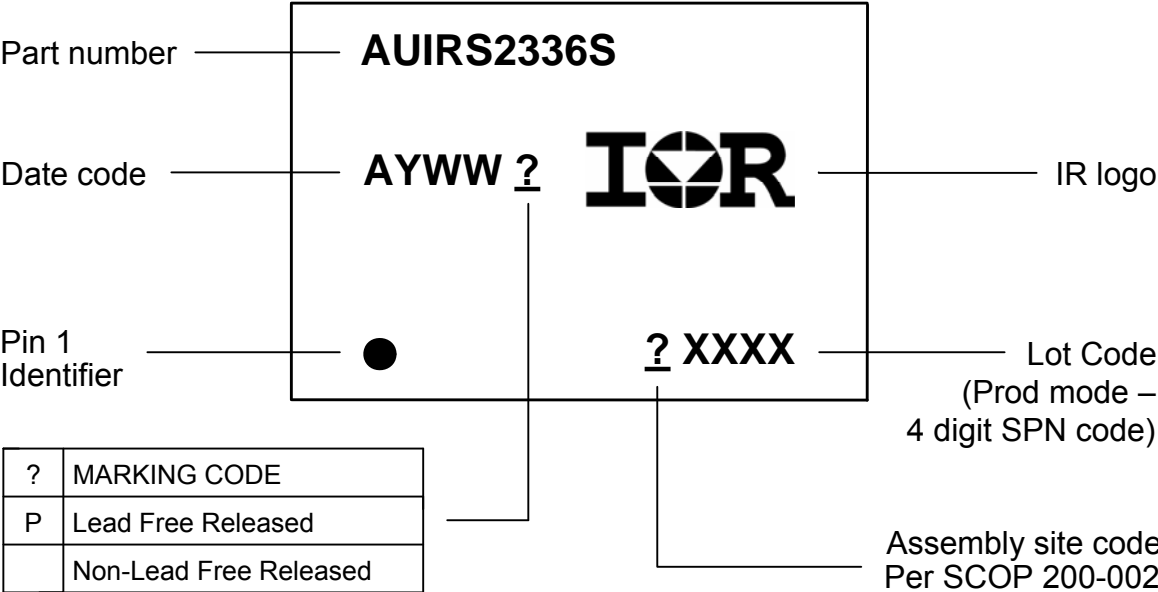
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
	SOIC28W	Tube/Bulk	25	AUIRS2336S
		Tape and Reel	1000	AUIRS2336STR

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