The AT43301 consists of a Serial Interface Engine, a Hub Repeater, and a Hub Controller.

The Serial Interface Engine's tasks are:

- Manage the USB communication protocol
- USB signaling detection/generation
- Clock/data separation, data encoding/decoding, CRC generation/checking
- Data serialization/deserialization

The Hub Repeater is responsible for:

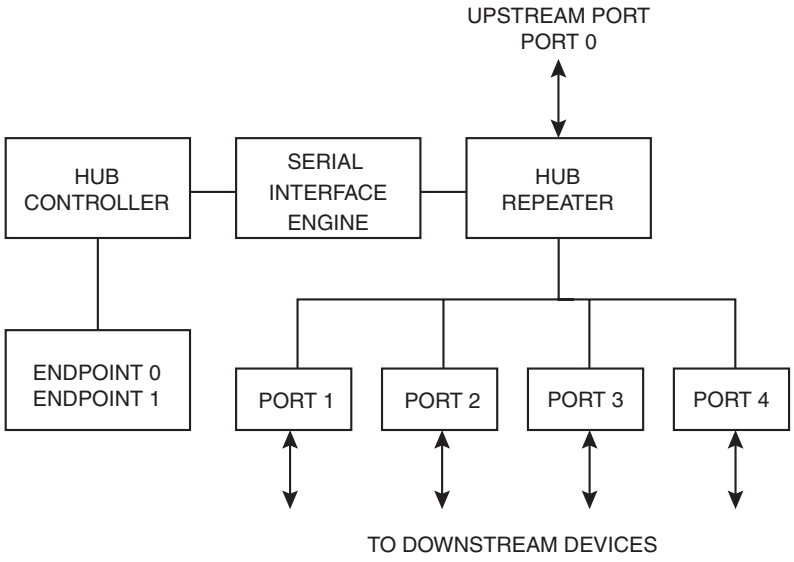
- Providing upstream connectivity between the selected device and the host
- Managing connectivity setup and tear-down
- Handling bus fault detection and recovery
- Detecting connect/disconnect on each port

The Hub Controller is responsible for:

- Hub enumeration
- Providing configuration information to the Host
- Providing status of each port to the Host
- Controlling each port per host command
- Managing port power supply

1.1 Block Diagram

Figure 1-2. AT43301 Block Diagram



Note: This document assumes that the reader is familiar with the Universal Serial Bus and therefore only describes the unique features of the AT43301 controller. For detailed information about the USB and its operation, the reader should refer to the Universal Serial Bus Specification Version 1.1, September 23, 1998.

1.2 Pin Assignment

Type:

I = Input,

IS = Input, Schmitt Trigger

O = Output

OD = Output, open drain

B = Bi-directional

V = Power supply, ground

Table 1-1. 24-lead SOIC AT43301-SC Pin Assignment

Pin Number	Signal	Type
1	VCC	V
2	VSS	V
3	CEXT1	O
4	OSC1	I
5	OSC2	O
6	LFT	I
7	$\overline{\text{STAT}}$	O
8	$\overline{\text{PWR}}$	O
9	$\overline{\text{OVC}}$	IS
10	LPSTAT	IS
11	$\overline{\text{TEST}}$	I
12	SELF/$\overline{\text{BUS}}$	IS
13	VSS	V
14	DM0	B
15	DP0	B
16	DM1	B
17	DP1	B
18	DM2	B
19	DP2	B
20	DM3	B
21	DP3	B
22	DM4	B
23	DP4	B
24	NC	-

Table 1-2. 32-lead AT43301-AC Pin Assignment

Pin Number	Signal	Type
1	NC	–
2	DM4	B
3	DP4	B
4	48	I
5	VCC	V
6	VSS	V
7	CEXT	O
8	NC	–
9	VSS	V
10	OSC1	I
11	OSC2	O
12	LFT	I
13	$\overline{\text{STAT}}$	O
14	$\overline{\text{PWR}}$	O
15	NC	–
16	$\overline{\text{OVC}}$	IS
17	LPSTAT	IS
18	$\overline{\text{TEST}}$	I
19	SELF/$\overline{\text{BUS}}$	IS
20	$\overline{\text{NC}}$	–
21	$\overline{\text{VSS}}$	V
22	DM0	B
23	DP0	B
24	NC	–
25	NC	–
26	DM1	B
27	DP1	B
28	DM2	B
29	DP2	B
30	DM3	B
31	DP3	B
32	NC	–

Table 1-3. Signal Descriptions

CEXT1	O	External Capacitor. For proper operation of the on-chip regulator, a 0.27 µF capacitor must be connected to CEXT1.
DP0	B	Upstream Plus USB I/O. This pin should be connected to the CEXT1 pin through an external 1.5 kΩ pull-up resistor. DP0 and DM0 form the differential signal pin pairs connected to the USB host controller or an upstream Hub.
DM0	B	Upstream Minus USB I/O.
DP[1:4]	B	Port Plus USB I/O. This pin should be connected to VSS through an external 15 kΩ resistor. DP[1:4] and DM[1:4] are the differential signal pin pairs to connect downstream USB devices.
DM[1:4]	B	Port Minus USB I/O. This pin should be connected to VSS through an external 15 kΩ resistor.
LFT	I	PLL Filter. For proper operation of the PLL, this pin should be connected through a 2.2 nF capacitor in parallel with a 100Ω resistor in series with a 10 nF capacitor to ground (VSS).
LPSTAT	I	Local Power Status. Schmitt Trigger input pin that is used in the self-powered mode to indicate the condition of the local power supply. This pin should be connected to the local power supply through a 100 kΩ resistor.
48	I	48 MHz Select, 32-lead LQFP only. This pin sets the clock input to the AT43301-AC. If it is tied low, a 48 MHz clock must be input to OSC1. If it is tied high (to CEXT1 or to 5V through a 47 kΩ resistor), a 6 MHz crystal must be connected between OSC1 and OSC2, or a 6 MHz clock input to OSC1.
OSC1	I	Oscillator Input. Input to the inverting 6 MHz oscillator amplifier.
OSC2	O	Oscillator Output. Output of the inverting oscillator amplifier.
$\overline{\text{OVC}}$	I	Port Overcurrent. This is the Schmitt Trigger input signal used to indicate to the AT43301 that there is a power supply problem with the ports. If $\overline{\text{OVC}}$ is asserted, the AT43301 will de-assert $\overline{\text{PWR}}$ and report the status to the USB Host.
$\overline{\text{PWR}}$	O	Power Switch. This is an output signal to enable or disable the external port power switch for the port power supply. $\overline{\text{PWR}}$ is de-asserted when an overcurrent is detected at OVC.
SELF/$\overline{\text{BUS}}$	I	Power Mode. Schmitt Trigger input pin to set power mode of hub. If high, the AT43301 works in the self-powered mode. If low, the bus-powered mode.
$\overline{\text{STAT}}$	O	Status. Output pin which is asserted by the AT43301 whenever it is enumerated. $\overline{\text{STAT}}$ is de-asserted when the hub enters the suspend state. An LED in series with a resistor can be connected to this pin to provide visual feedback to the user.
$\overline{\text{TEST}}$	I	Test. This pin has an internal pull up and should be left unconnected in the normal operating mode.
VCC	V	5V Power Supply from the USB.
VSS	V	Ground.
NC	-	No Connect. This pin should be left unconnected.

2. Functional Description

2.1 Summary

The Atmel AT43301 USB hub controller chip contains various features that makes it the ideal solution for very low-cost USB hubs. These features are: on-chip regulator, low-frequency oscillator, bus or self-powered operation, ganged port power switching and global overcurrent protection. Such a hub can be a stand-alone hub used with portable computers to allow convenient connectivity to standard desktop peripheral devices. Alternatively, the hub can be added to an existing non-USB peripheral such a keyboard. The AT43301 provides 4 downstream USB ports and can operate in a self-powered or bus-powered mode.

2.2 USB Ports

The AT43301's upstream port, Port0, is a full speed port. A 1.5 kΩ pull-up resistor to the 3.3V regulator output, CEXT, is required for proper operation. The downstream ports support both full-speed as well as low-speed devices. 15 kΩ pull down resistors are required at their inputs.

Full speed signal requirements demand controlled rise/fall times and impedance matching of the USB ports. To meet these requirements, 22Ω resistors must be inserted in series between the USB data pins and the USB connectors.

2.3 Hub Repeater

The Hub Repeater is responsible for port connectivity setup and teardown. It also supports exception handling such as bus fault detection and recovery, and connect/disconnect detection. Port0 is the root port and is connected to the root hub or an upstream hub. When a packet is received at Port0, the AT43301 propagates it to all the enabled downstream ports. Conversely, a packet from a downstream port is transmitted from Port0.

The AT43301 supports downstream port data signaling at both 1.5 Mb/s and 12 Mb/s. Devices attached to the downstream ports are determined to be either full speed or low speed depending which data line (DP or DM) is pulled high. If a port is enumerated as low speed, its output buffers operate at a slew rate of 75-300 ns, and the AT43301 will not propagate any traffic to that port unless it is prefaced with a preamble PID. Low speed data following the preamble PID is propagated to both low- and full-speed devices. The AT43301 will enable low-speed drivers within four full-speed bit times of the last bit of a preamble PID, and will disable them at the end of an EOP. The upstream traffic from all ports is propagated by Port0 using the full speed 4-20ns slew rate drivers.

All the AT43301 ports independently drive and monitor their DP and DM pins so that they are able to detect and generate the 'J', 'K', and SE0 bus signaling states. Each hub port has single-ended and differential receivers on its DP and DM lines. The ports' I/O buffers comply with the voltage levels and drive requirements as specified in the USB Specifications Rev 1.0.

The Hub Repeater implements a frame timer which is timed by the 12 MHz USB clock and gets reset every time an SOF token is received from the host.

2.4 Serial Interface Engine

The Serial Interface Engine handles the USB communication protocol. It performs the USB clock/data separation, the NRZI data encoding/decoding, bit stuffing, CRC generation and checking, USB packet ID decoding and generation, and data serialization and de-serialization.

The on-chip phase locked loop generates the high frequency clock for the clock/data separation circuit.

2.5 Power Management

A hub is allowed to draw up to 500 mA of power from the host or upstream hub. The AT43301's itself and its external circuitry typically consume about 24 mA. Therefore, in the bus-powered mode, 100 mA is available for each of the hub's downstream devices. In the self-powered mode, an external power supply is required which must be capable of supplying 500 mA per port. The power supplied to the ports is monitored and controlled by the AT43301.

The AT43301 reports overcurrent on a global basis. The overcurrent signal, which needs to be detected by an external device, is read through the $\overline{OVC}$ pin. A logic low at $\overline{OVC}$ is interpreted as an overcurrent condition. This could be caused by an overload, or a short circuit, and causes the AT43301 to set the Over-Current Indicator bit of the Hub Status Field, wHubStatus, as well as the Over-Current Indicator Change bit of the Hub Change Field, wHubChange. At the same time, power to the ports is switched off by de-asserting $\overline{PWR}$.

An external device is needed to perform the actual switching of the ports' power under control of the AT43301. Any type of suitable switch or device is acceptable. However, the switch should have a low-voltage drop across it even when the port absorbs full power. In its simplest form, this switch can be a high side MOSFET switch. The advantage of using a MOSFET switch is its very low-voltage drop.

The power control pin, $\overline{PWR}$, is asserted only when a SetPortFeature[PORT-POWER] request is received from the host. $\overline{PWR}$ is de-asserted under the following conditions:

1. Power up
2. Reset and initialization
3. Overcurrent condition
4. Requested by the host though a ClearPortFeature[PORT_POWER] for ALL the ports

2.5.1 Self-powered Mode

In the self-powered mode, power to the downstream ports must be supplied by an external power supply. This power supply must be capable of supplying 500 mA per port or 2A total with good voltage tolerance and regulation. At full hub operating power, that is all downstream ports drawing 500 mA each, the minimum voltage at the downstream port connector must be 4.75V.

The USB specification requires that the voltage drop at the power switch and board traces be no more than 100 mV. A good conservative maximum drop at the power switch itself should be no more than 75 mV. Careful design and selection of the power switch and PC board layout is required to meet the specifications. When using a MOSFET switch, its resistance must be 40 mΩ or less under worst case conditions. A suitable MOSFET switch for an AT43301 based hub is an integrated highside MOSFET switch such as the Micrel MIC2505.

2.5.2 Bus-Powered Mode

In the bus-powered mode all the power for the hub itself as well as the downstream ports is supplied by the root hub or upstream hub through the USB. Only 100 mA is available for each of the hub's downstream devices and therefore only low-power devices are supported.

The power switch works exactly like the self-powered mode, except that the allowable switch resistance is higher: 140 mΩ or less under the worst case condition. An example of a suitable high side switch for a bus-powered hub is the Micrel MIC2525.

The diagrams of Figure 2-1 and Figure 2-2 show examples of the power supply and power management scheme in the self-powered mode and bus-powered mode using an integrated switch with built-in overcurrent protection.

Figure 2-1. Bus-powered Hub

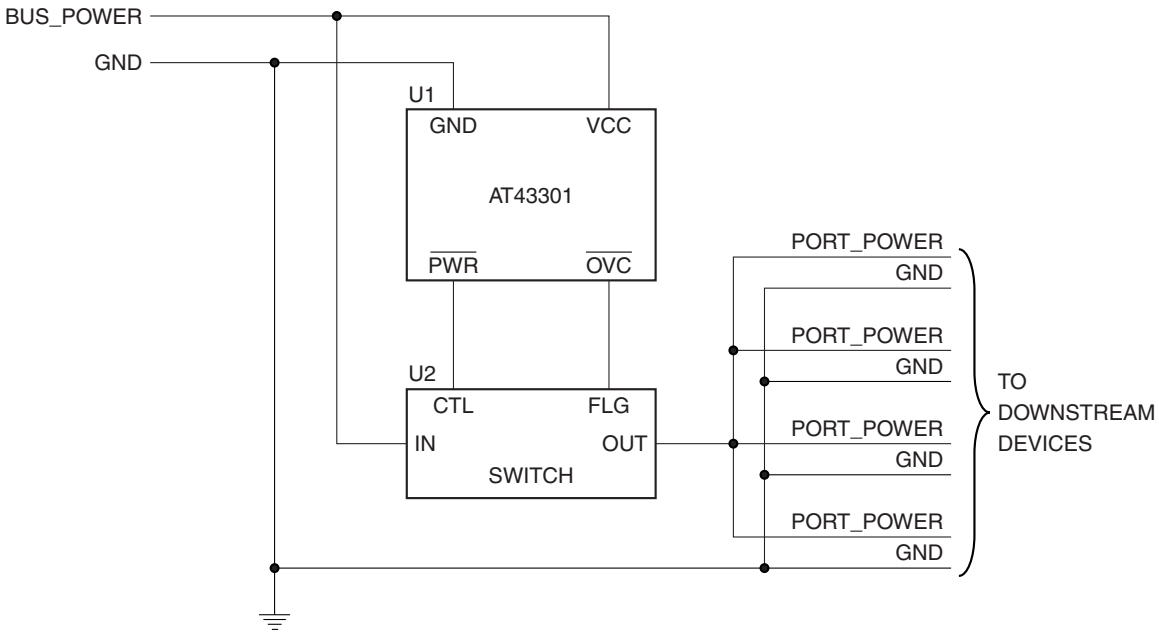
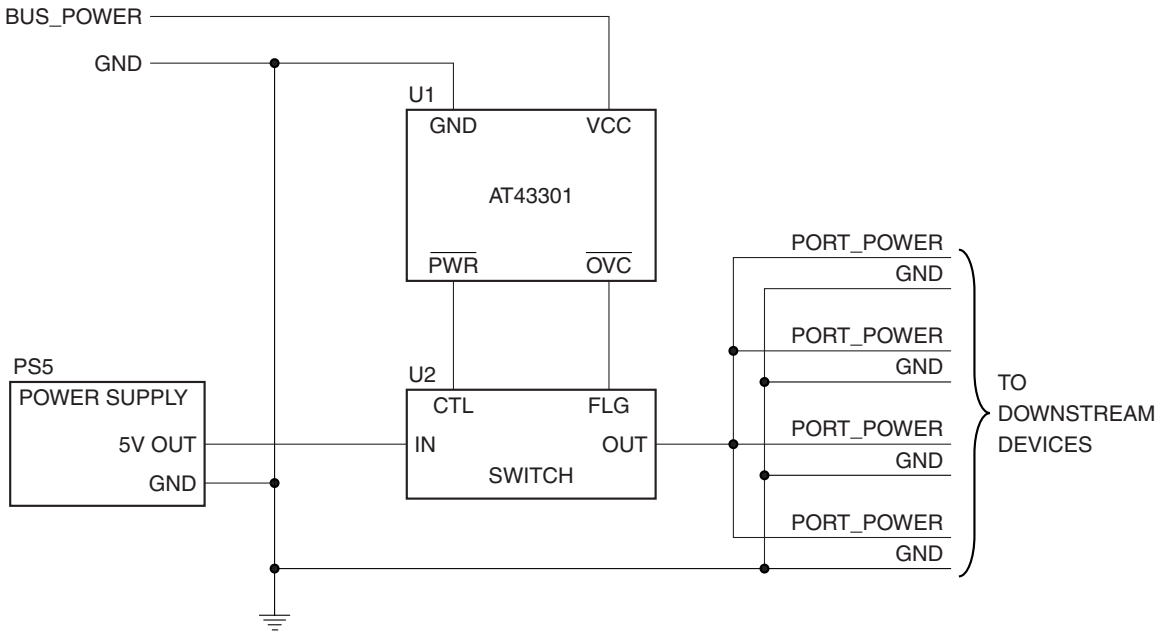


Figure 2-2. Self-powered Hub



2.6 Hub Controller

The Hub Controller of the AT43301 provides the mechanism for the host to enumerate the hub and the AT43301 to provide the host with its configuration information. It also provides a mechanism for the host to monitor and control the downstream ports.

The Hub Controller supports two endpoints, Endpoint0 and Endpoint1.

The Hub Controller maintains a status register, Controller Status Register, which reflects the AT43301's current settings. At power up, all bits in this register will be set to 0's.

Table 2-1. Controller Status Register

Bit	Function	Value	Description
0	Hub configuration status	0 1	Set to 0 or 1 by a Set_Configuration Request Hub is not currently configured Hub is currently configured
1	Hub remote wakeup status	0 1	Set to 0 or 1 by ClearFeature or SetFeature request. Default value is 0. Hub is currently not enabled to request remote wakeup Hub is currently enabled to request remote wakeup
2	Endpoint0 STALL status	0 1	Endpoint0 is not stalled Endpoint0 is stalled
3	Endpoint1 STALL status	0 1	Endpoint1 is not stalled Endpoint1 is stalled

2.6.1 Endpoint 0

Endpoint 0 is the AT43301's default endpoint used for enumeration of the hub and exchange of configuration information and requests between the host and the AT43301. Endpoint 0 supports control transfers.

The Hub Controller supports the following descriptors through Endpoint 0: Device Descriptor, Configuration Descriptor, Interface Descriptor, Endpoint Descriptor, and Hub Descriptor. These descriptors are described in detail elsewhere in this document. Standard USB Device Requests and class-specific Hub Requests are also supported through Endpoint 0. There is no endpoint descriptor for Endpoint0.

2.6.2 Endpoint 1

Endpoint1 is used by the Hub Controller to send status change information to the host. This endpoint supports interrupt transfers.

The Hub Controller samples the changes at the end of every frame at time marker EOF2 in preparation for a potential data transfer in the subsequent frame. The sampled information is stored in a byte wide register, the Status Change Register, using a bitmap scheme.

Each bit in the Status Change Register corresponds to one port as shown below:

Table 2-2. Status Change Register

Bit	Function	Value	Meaning
0	Hub status change	0 1	No change in status Change in status detected
1	Port1 status change	0 1	No change in status Change in status detected
2	Port2 status change	0 1	No change in status Change in status detected
3	Port3 status change	0 1	No change in status Change in status detected
4	Port4 status change	0 1	No change in status Change in status detected
5-7	Reserved	000	Default values

An IN Token packet from the host to Endpoint 1 indicates a request for port change status. If the hub has not detected any change on its ports, or any changes in itself, then all bits in this register will be 0 and the Hub Controller will return a NAK to requests on Endpoint1. If any of bits 0-4 is 1, the Hub Controller will transfer the whole byte. The Hub Controller will continue to report a status change when polled until that particular change has been removed by a ClearPortFeature request from the Host. No status change will be reported by Endpoint 1 until the AT43301 has been enumerated and configured by the host.

2.7 Oscillator and Phase-Locked-Loop

All the clock signals required to run the AT43301 are derived from an on-chip oscillator. To reduce EMI and power dissipation in the system, the AT43301 is designed to operate with a 6 MHz crystal. An on-chip PLL generates the high frequency for the clock/data separator of the Serial Interface Engine. In the suspended state, the oscillator circuitry is turned off. To assure quick startup, a crystal with a high Q, or low ESR, should be used. To meet the USB hub frequency accuracy and stability requirements for hubs, the crystal should have an accuracy and stability of better than 100 ppm. Even though the oscillator circuit would work with a ceramic resonator, its use is not recommended because a resonator would not have the frequency accuracy and stability.

A 6 MHz parallel resonance quartz crystal with a load capacitance of approximately 10 pF is recommended. The oscillator is a special low-power design and in most cases no external capacitors and resistors are necessary. If the crystal requires a higher value capacitance, external capacitors can be added to the two terminals of the crystal and ground to meet the required value. If the crystal used cannot tolerate the drive levels of the oscillator, a series resistor between OSC2 and the crystal pin is recommended.

The clock can also be externally sourced. In this case, connect the clock source to the OSC1 pin, while leaving OSC2 pin floating. The switching level at the OSC1 pin can be as low as 0.47V (see “Electrical Specification” on page 12) and a CMOS device is required to drive this pin to maintain good noise margins at the low switching level. The 32-lead AT43301-AC can also be driven by a 48 MHz external clock instead. In this case, connect the 48N pin to ground.

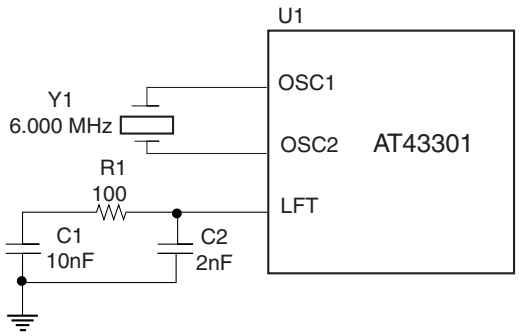
For proper operation of the PLL, an external RC filter consisting of a series RC network of 100Ω and 10 nF in parallel with a 2 nF capacitor must be connected from the LFT pin to V_{SS}.

2.8 Status Pin

The status pin, $\overline{STAT}$, is provided to allow feedback to the user. If an LED and a series resistor is connected between $\overline{STAT}$ and VCC, the LED will light when the hub is enumerated. During an overcurrent condition, the LED will blink. It will continue to blink until the host turns off the power to the ports or until the hub is re-enumerated.

The I/O pins of the AT43301 should not be directly connected to voltages less than VSS or more than the voltage at the CEXT pins. If it is necessary to violate this rule, insert a series resistor between the I/O pin and the source of the external signal source that limits the current into the I/O pin to less than 0.2 mA. Under no circumstance should the external voltage exceed 5.5V. To do so will put the chip under excessive stress.

Figure 2-3. External Oscillator and PLL Circuit



2.9 Power Supply

The AT43301 is powered from the USB bus, but has an internal voltage regulator to supply the 3.3V operating power to its circuitry. For proper operation, an external high quality, low ESR, 0.27 µF, or larger, capacitor should be connected to the output of the regulator, CEXT1 and ground. The CEXT1 pin can also be used to supply the voltage to the 1.5 kΩ pull up resistor at Port 0's DP pin.

To provide the best operating condition for the AT43301, careful consideration of the power supply connections are recommended. Use short, low impedance connections to all power supply lines: V_{CC} and V_{SS}. Use sufficient decoupling capacitance to reduce noise: 0.1 µF of high quality ceramic capacitor soldered as close as possible to the VCC and VSS package pins are recommended.

The AT43301 can also operate directly off a 3.3V power supply. In this case, leave the VCC pin floating and connect the 3.3V power to CEXT1.

3. Electrical Specification

3.1 Absolute Maximum Ratings*

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC5}	5V Power Supply			5.5	V
V_I	DC Input Voltage		-0.3V	V_{CEXT} + 0.3 4.6 max	V
V_O	DC Output Voltage		-0.3	V_{CEXT} + 0.3 4.6 max	V
T_O	Operating Temperature		-40	+125	°C
T_S	Storage Temperature		-65	+150	°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 DC Characteristics

The values shown in this table are valid for T_A = 0°C to 85°C, V_{CC} = 4.4V to 5.25V, unless otherwise noted.

Table 3-1. Power Supply

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	5V Power Supply		4.4	5.25	V
I_{CC}	5V Supply Current			24	mA
I_{CCS}	Suspended Device Current			150	µA

Table 3-2. USB Signals: DPx, DMx

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input Level High (driven)		2.0		V
V_{IHZ}	Input Level High (floating)		2.7	3.6	V
V_{IL}	Input Level Low			0.8	V
V_{DI}	Differential Input Sensitivity	DPx and DMx	0.2		V
V_{CM}	Differential Common Mode Range		0.8	2.5	V
V_{OL1}	Static Output Low	R_L of 1.5 kΩ to 3.6V		0.3	V
V_{OH1}	Static Output High	R_L of 15 kΩ to GND	2.8	3.6	V
V_{CRS}	Output Signal Crossover		1.3	2.0	V
C_{IN}	Input Capacitance			20	pF

Table 3-3. $\overline{PWR}$, $\overline{STAT}$, $\overline{OVC}$

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL2}	Output Low Level, $\overline{PWR}$, $\overline{STAT}$	I_{OL} = 4 mA		0.5	V
C_{OUT}	Output Capacitance	1 MHz		10	pF
V_{IL3}	Input Low Level			$0.3V_{CEXT}$	V
V_{IH3}	Input High Level		$0.7V_{CEXT}$		V
C_{OUT}	Output Capacitance	1 MHz		10	pF
V_{OH2}	Output High Level, $\overline{PWR}$	I_{OH} = 4 mA	V_{CEXT} - 0.5		V

Table 3-4. Oscillator Signals: OSC1, OSC2

Symbol	Parameter	Condition	Min	Max	Unit
V_{LH}	OSC1 Switching Level		0.47	1.20	V
V_{HL}	OSC1 Switching Level		0.67	1.44	V
C_{X1}	Input Capacitance, OSC1			17	pF
C_{X2}	Output Capacitance, OSC2			17	pF
C_{12}	OSC1/2 Capacitance			1	pF
tsu	Start-up Time	6 MHz, fundamental		2	ms
D_L	Drive Level	V_{CC} = 3.3V, 6 MHz crystal, 100Ω equiv series resistor		150	µW

Note: OSC2 must not be used to drive other circuitry.

3.3 AC Characteristics

Table 3-5. DPx, DMx Driver Characteristics, Full Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	C_L = 50 pF	4	20	ns
t_F	Fall Time	C_L = 50 pF	4	20	ns
t_{RFM}	t_R/t_F Matching		90	110	%
Z_{DRV}	Driver Output Resistance[1]	Steady state drive	28	44	Ω

Note: 1. With external 22Ω series resistor.

Table 3-6. DPx, DMx Source Timings, Full Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{DRATE}	Full Speed Data Rate[1]	Average bit rate	11.97	12.03	Mb/s
t_{FRAME}	Frame Interval[1]		0.9995	1.0005	ms
t_{RFI}	Consecutive Frame Interval Jitter[1]	No clock adjustment		42.0	ns
t_{RFIADJ}	Consecutive Frame Interval Jitter[1]	With clock adjustment		126.0	ns
	Source Diff Driver Jitter				
t_{DJ1}	To Next Transition		-3.5	3.5	ns
t_{DJ2}	For Paired Transitions		-4.0	4.0	ns
t_{FDEOP}	Source Jitter for Differential Transition to SEO Transitions		-2.0	5.0	ns
	Recvr Data Jitter Tolerance				
t_{JR1}	To Next Transition		-18.5	18.5	ns
t_{JR2}	For Paired Transitions		-9.0	9.0	ns
t_{FEOPT}	Source SEO interval of EOP		160.0	175.0	ns
t_{FEOPR}	Receiver SEO interval of EOP		82.0		ns
t_{FST}	Width of SEO interval during differential transition			14.0	ns

Note: 1. With 6.000 MHz, 100 ppm crystal.

Table 3-7. DPx, DMx Driver Characteristics, Low-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise time	C_L = 200 - 600 pF	75.0	300.0	ns
t_F	Fall time	C_L = 200 - 600 pF	75.0	300.0	ns
t_{RFM}	t_R/t_F matching		80.0	125.0	%

Table 3-8. DPx, DMx Hub Timings, High-Speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{HDD2}	Hub Differential Data Delay without Cable			44.0	ns
	Hub Diff Driver Jitter				
t_{HDJ1}	To Next Transition		-3.0	3.0	ns
t_{HDJ2}	For Paired Transitions		-1.0	1.0	ns
t_{FSOP}	Data Bit Width Distortion after SOP		-5.0	5.0	ns
t_{FEOPD}	Hub EOP Delay Relative to t_{HDD}		0	15.0	ns
t_{FHESK}	Hub EOP Output Width Skew		-15.0	15.0	ns

Table 3-9. DPx, DMx Hub Timings, Low-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{LHDD}	Hub Differential Data Delay			300.0	ns
	Downstr Hub Diff Driver Jitter				
t_{LHDJ1}	To Next Transition, downst		-45.0	45.0	ns
t_{LHDJ2}	For Paired Transitions, downst		-15.0	15.0	ns
t_{LUHJ1}	To Next Transition, upstr		-45.0	45.0	ns
t_{LUHJ2}	For Paired Transitions, upstr		-45.0	45.0	ns
t_{SOP}	Data Bit Width Distortion after SOP		-60.0	60.0	ns
t_{LEOPD}	Hub EOP Delay Relative to t_{HDD}		0	200.0	ns
t_{LHESK}	Hub EOP Output Width Skew		-300.0	300.0	ns

Table 3-10. Hub Event Timings

Symbol	Parameter	Condition	Min	Max	Unit
t_{DCNN}	Time to Detect a Downstream Port Connect Event				
	Awake Hub		2.5	2000.0	µs
	Suspended Hub		2.5	12000.0	µs
t_{DDIS}	Time to Detect a Disconnect Event on Downstream Port				
	Awake Hub		2.5	2.5	µs
	Suspended Hub		2.5	10000.0	µs
t_{URSM}	Time from Detecting Downstream Resume to Rebroadcast			100.0	µs
t_{DRST}	Duration of Driving Reset to a Downstream Device	Only for a SetPortFeature (PORT_RESET) request	10.0	20.0	ms
t_{URLK}	Time to Detect a Long K from Upstream		2.5	100.0	µs
t_{URLSEO}	Time to Detect a Long SEO from Upstream		2.5	10000.0	µs
t_{URPSEO}	Duration of repeating SEO Upstream			23	FS bit time

4. Timing Waveforms

Figure 4-1. Data Signal Rise and Fall Time

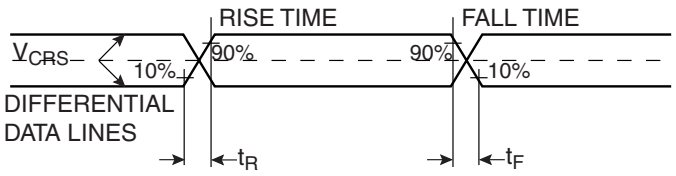


Figure 4-2. Full-speed Load

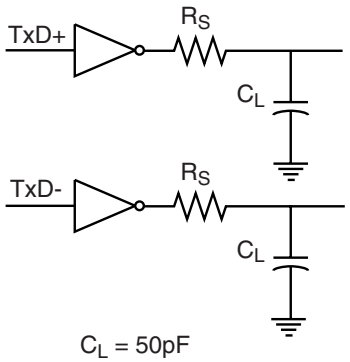


Figure 4-3. Low-speed Downstream Port Load

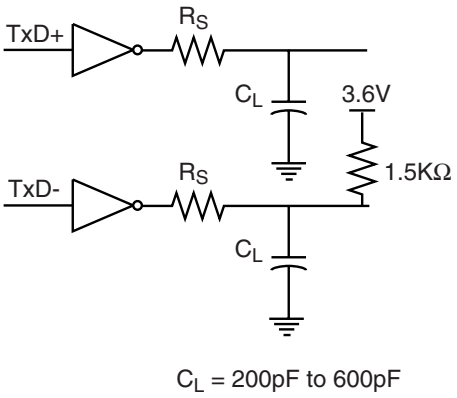


Figure 4-4. Differential Data Jitter

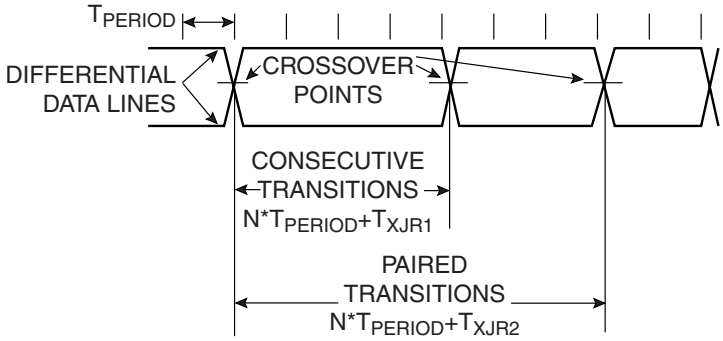


Figure 4-5. Differential-to-EOP Transition Skew and EOP Width

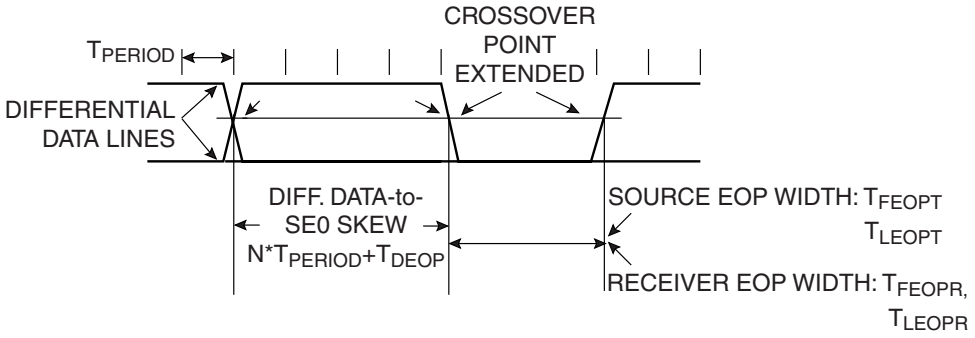


Figure 4-6. Receiver Jitter Tolerance

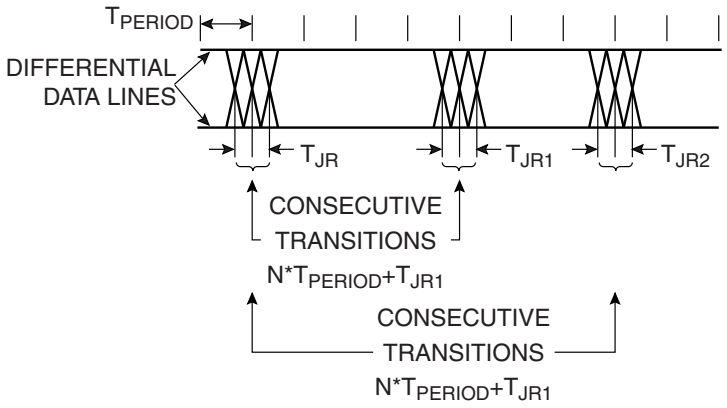
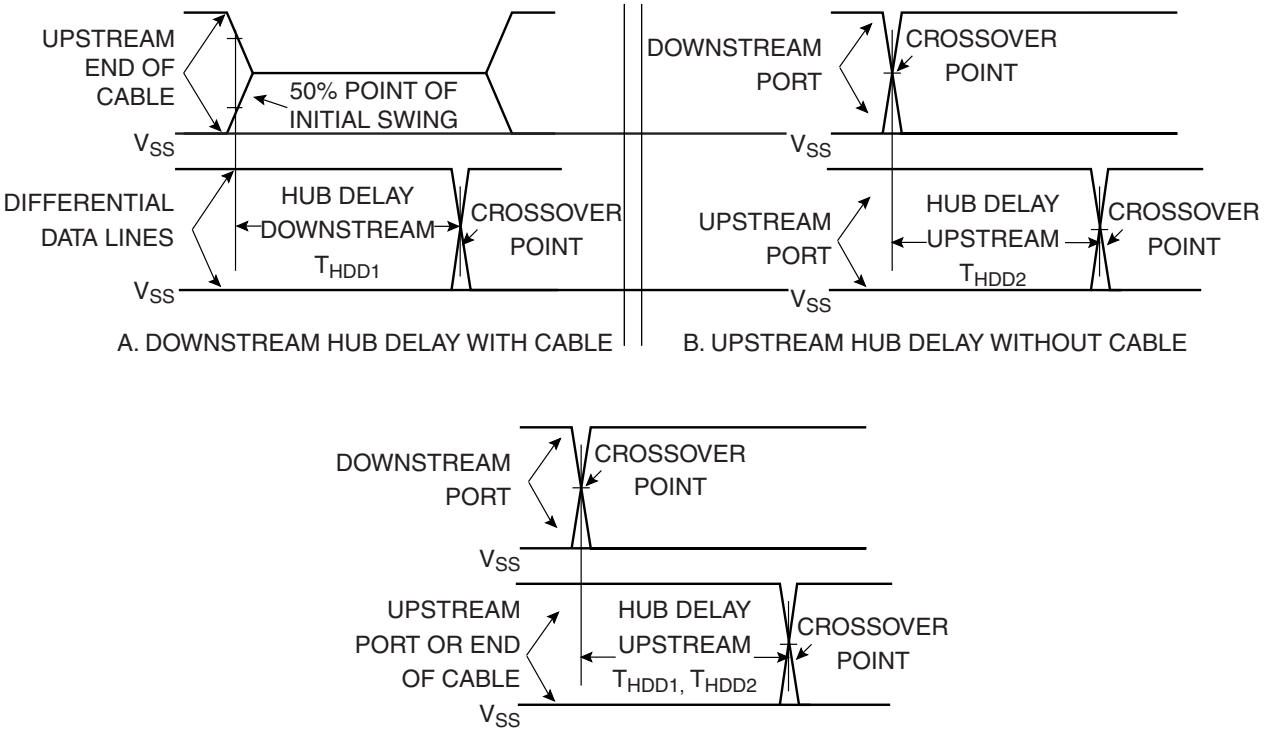


Figure 4-7. Hub Differential Delay, Differential Jitter, and SOP Distortion



Hub Differential Jitter:

$T_{HDJ1} = T_{HDDX}(J) - T_{HDDX}(K)$ or $T_{HDDX}(K) - T_{HDDX}(J)$ Consecutive Transitions

$T_{HDJ2} = T_{HDDX}(J) - T_{HDDX}(J)$ or $T_{HDDX}(K) - T_{HDDX}(K)$ Paired Transitions

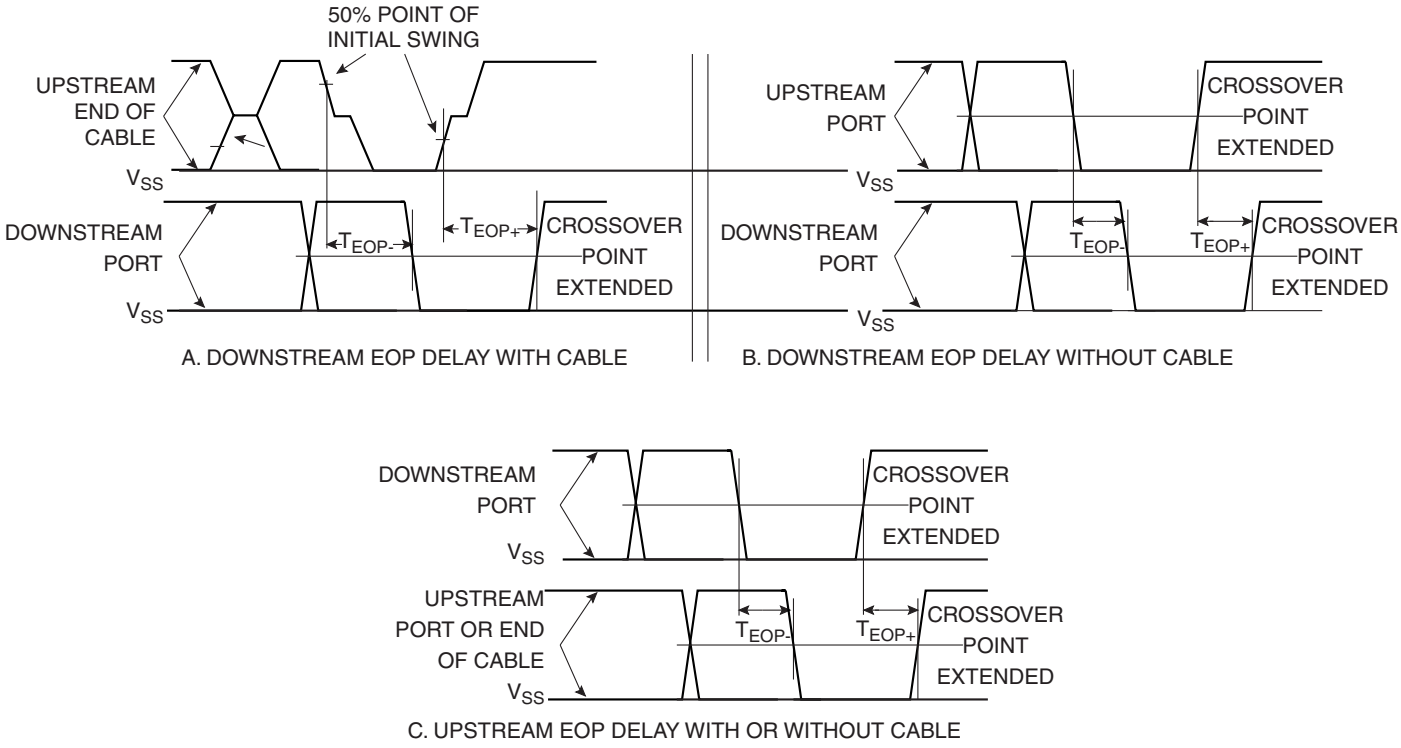
Bit After Sop Width Distortion (Same as Data Jitter for Sop and Next J Transition):

$T_{SOP} = T_{HDDX}(NEXTJ) - T_{HDDX}(SOP)$

Low-speed timings are determined in the same way for:

T_{LHDD}, T_{LDHJ1}, T_{LDJH2}, T_{LUHJ1}, T_{LUJH2}, and T_{LSOP}

Figure 4-8. Hub EOP Delay and EOP Skew



EOP Delay:

$T_{EOPD} = T_{EOP} - T_{HDDX}$

EOP Skew:

$T_{HESK} = T_{EOP+} - T_{EOP-}$

Low-speed timings are determined in the same way for:

T_{LEOPD} and T_{LHESK}

5. Schematic Diagrams

The following pages show schematic diagrams of an AT43301 based bus-powered hub and self-powered hub.

Figure 5-1. Bus-powered Hub

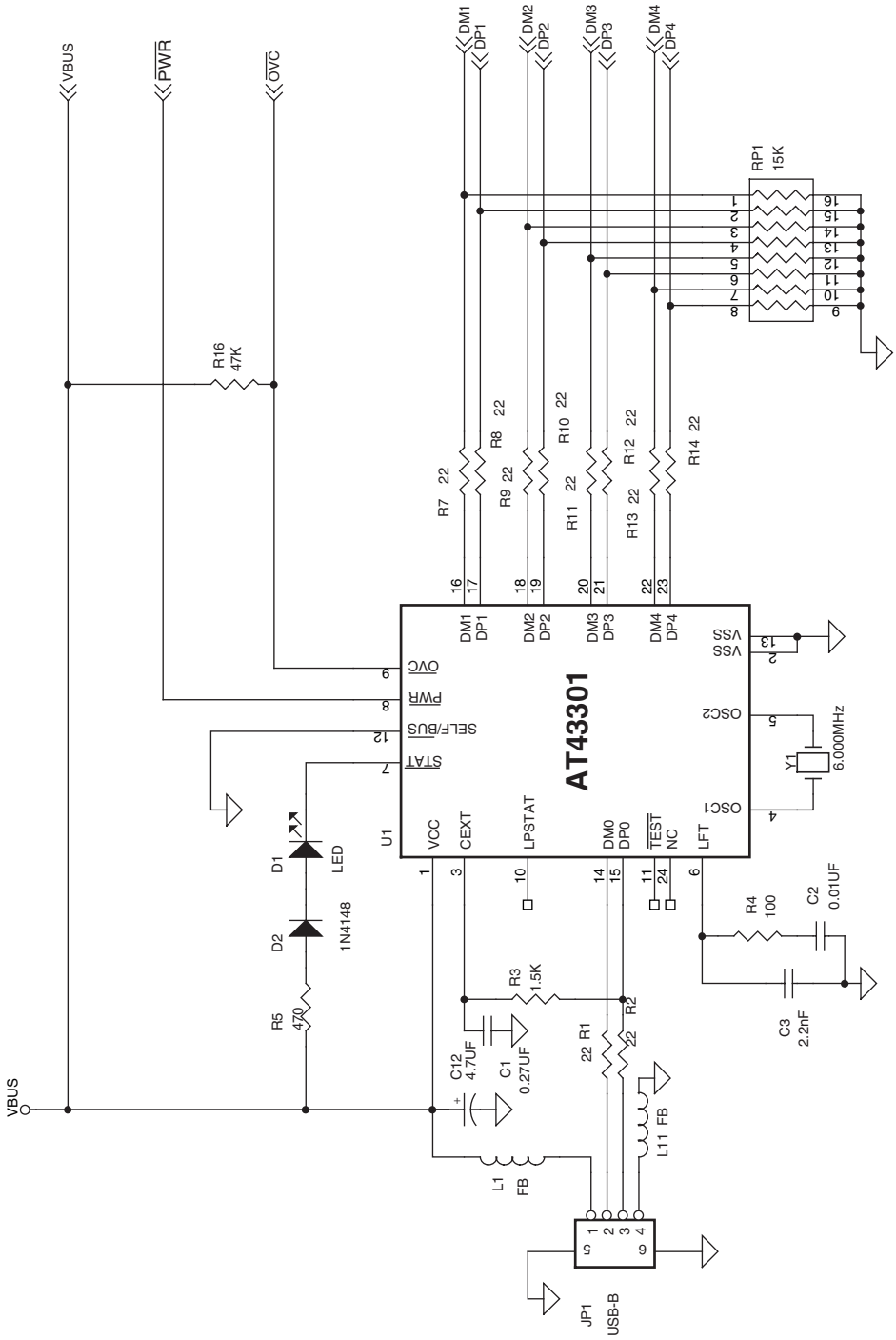


Figure 5-2. Bus-powered Hub

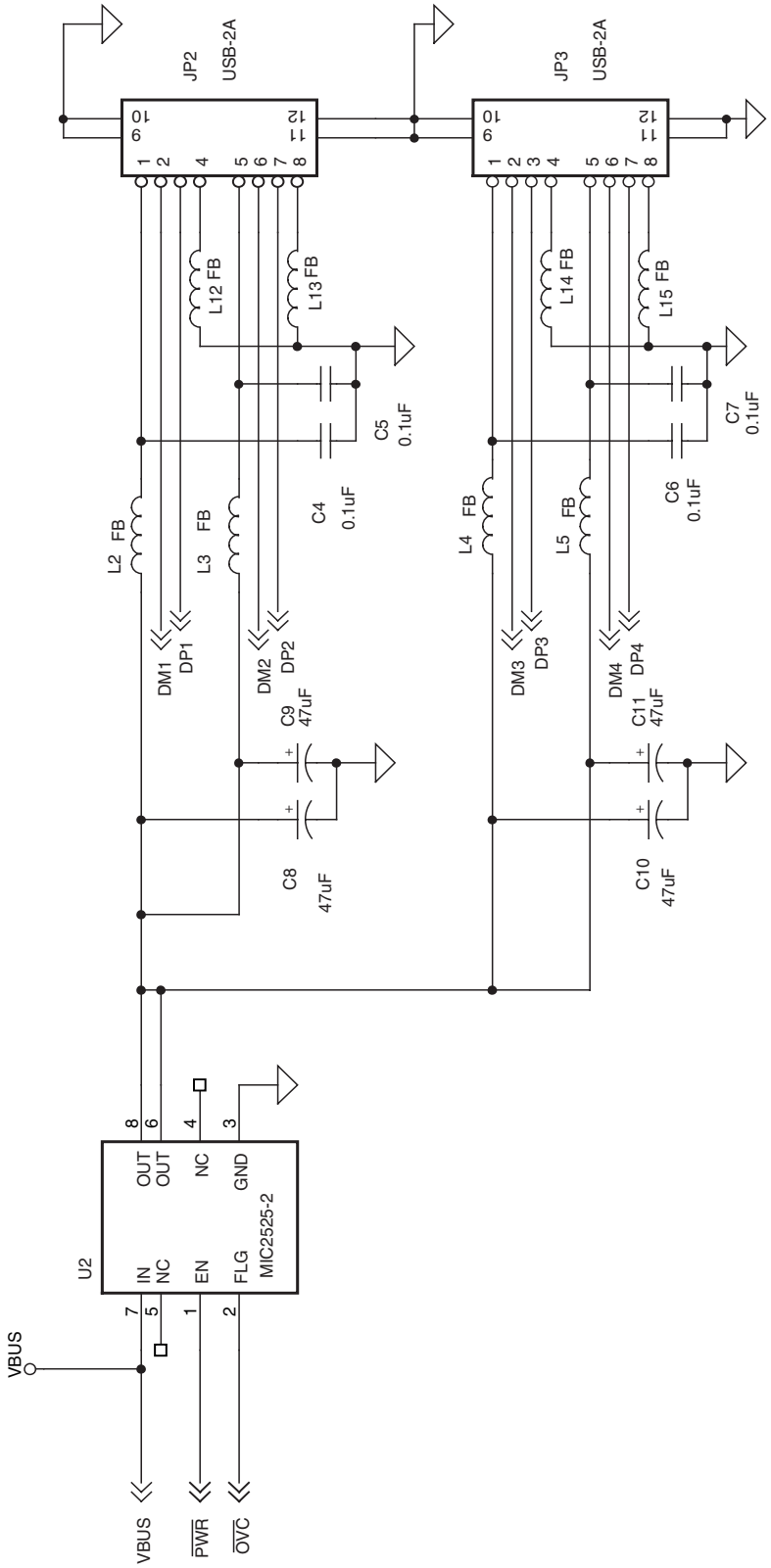


Figure 5-3. Self-powered Hub

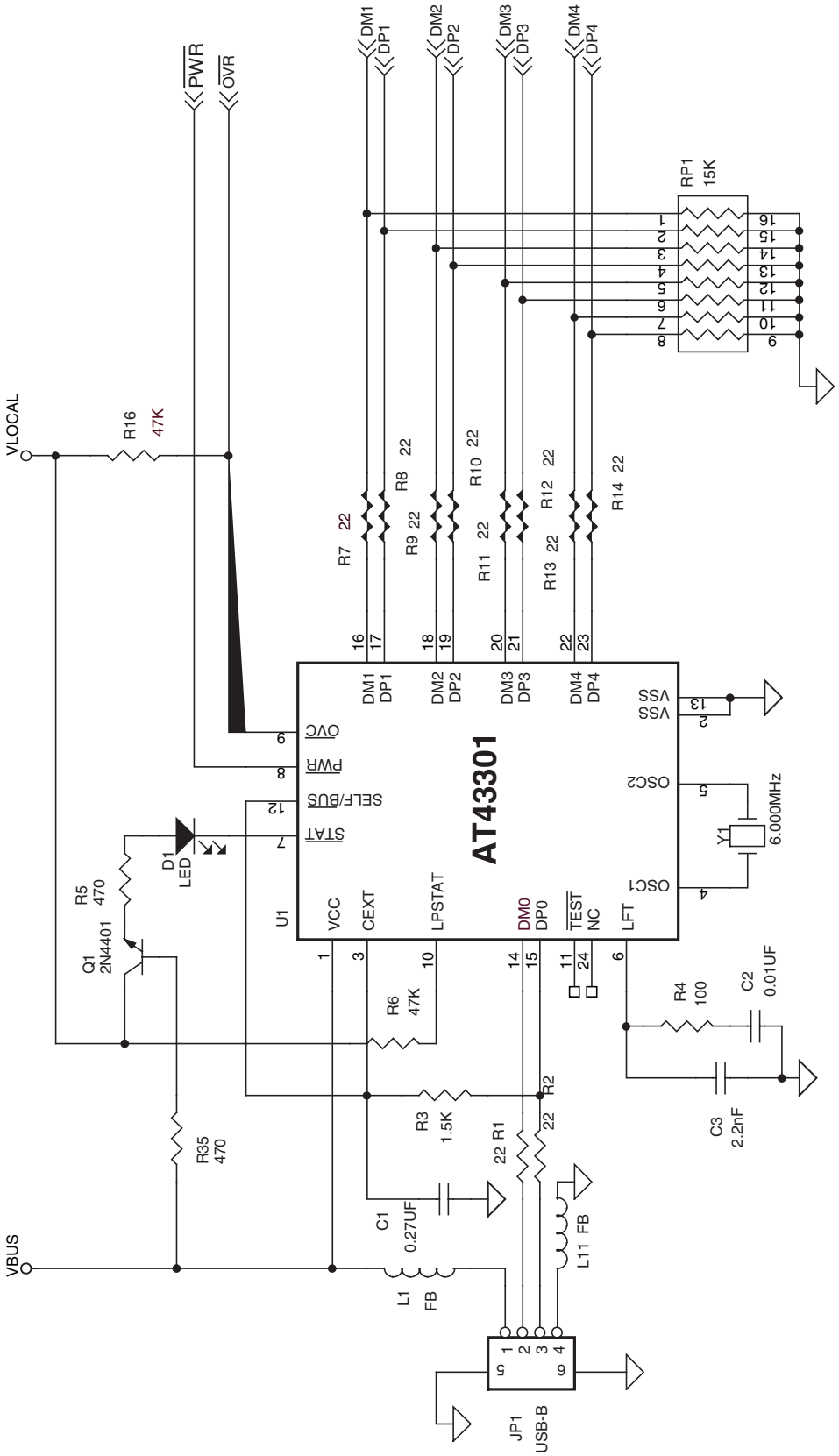
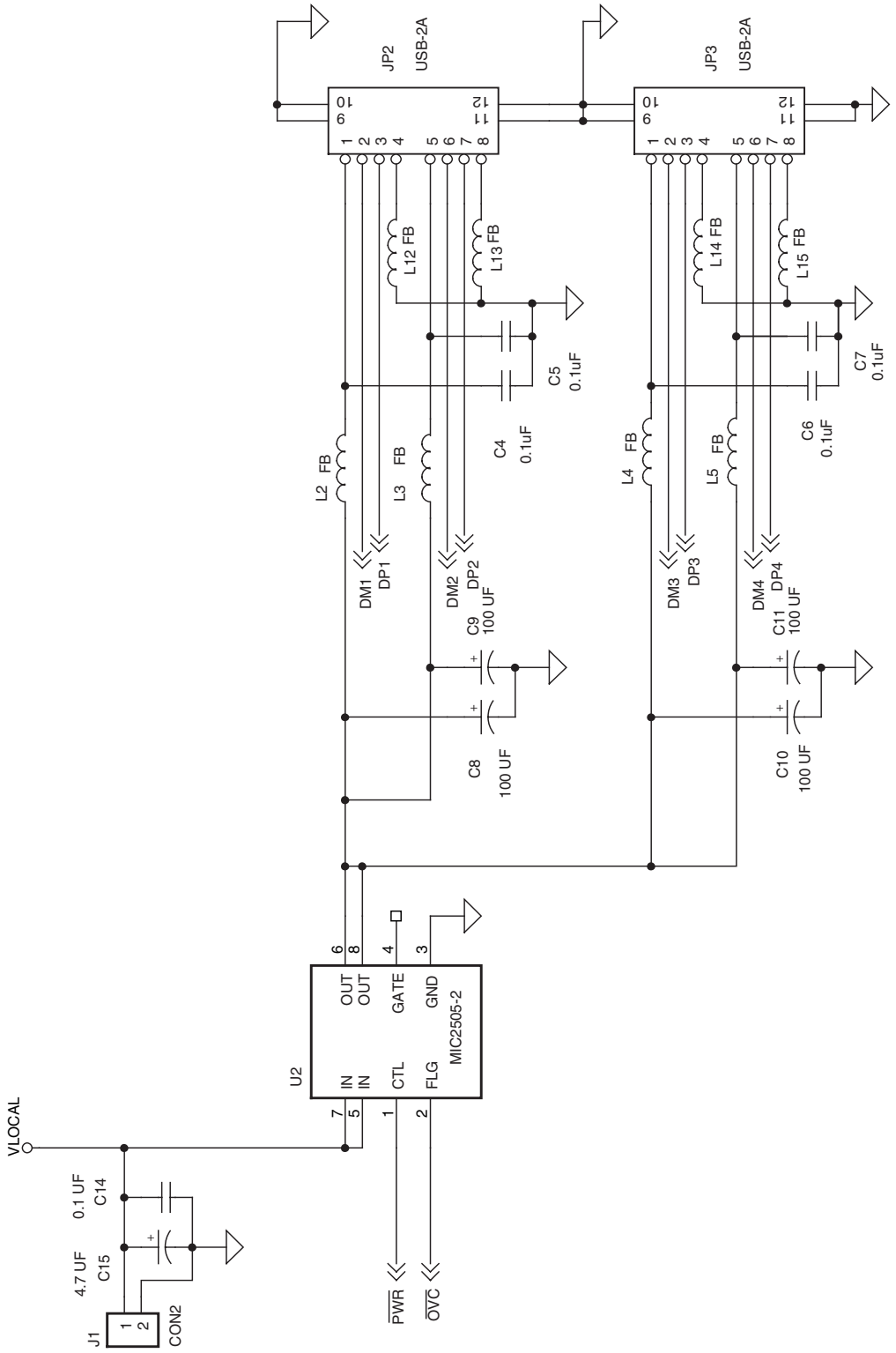


Figure 5-4. Self-powered Hub



6. Ordering Information

6.1 AT43301 Standard Package Options

Ordering Code	Package	Operation Range
AT43301-SC	24S – SOIC	Commercial (0°C to 70°C)
AT43301-AC	32AA – LQFP	Commercial (0°C to 70°C)

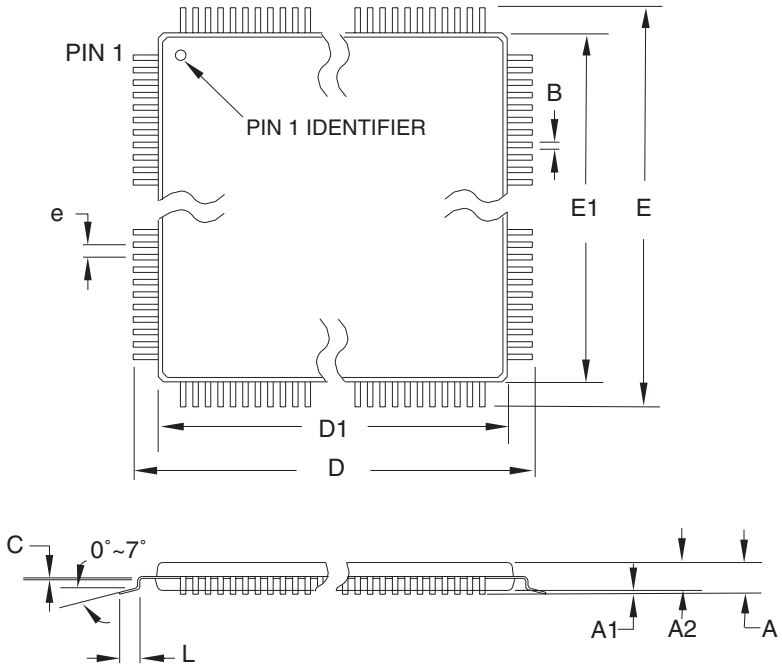
6.2 AT43301 Green Package Options (Pb/Halide-free/RoHS Compliant)

Ordering Code	Package	Operation Range
AT43301-AU	32AA – LQFP	Industrial (-40°C to 85°C)
AT43301-SU	24S – SOIC	Industrial (-40°C to 85°C)

Package Type	
24S	24-lead (0.300 in. body) Plastic Gull Wing Small Outline Package (SOIC)
32AA	32-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)

7. Packaging Information

7.1 32AA – LQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

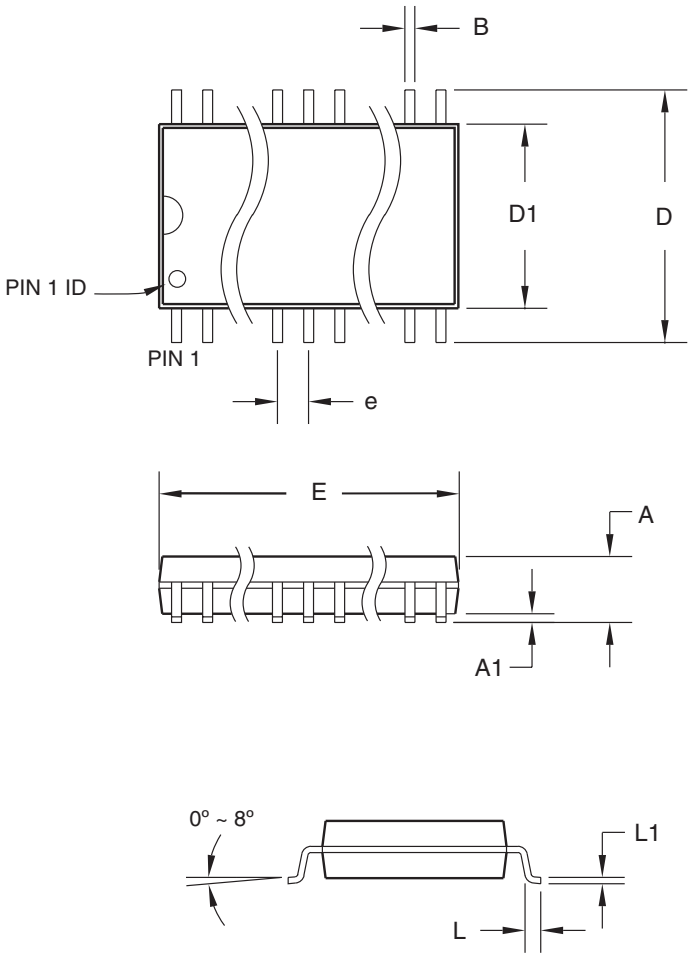
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation BBA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32AA,** 32-lead, 7 x 7 mm Body Size, 1.4 mm Body Thickness, 0.8 mm Lead Pitch, Low Profile Plastic Quad Flat Package (LQFP)	32AA	B

7.2 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	2.65	
A1	0.10	–	0.30	
D	10.00	–	10.65	
D1	7.40	–	7.60	
E	15.20	–	15.60	
B	0.33	–	0.51	
L	0.40	–	1.27	
L1	0.23	–	0.32	
e	1.27 BSC			

06/17/2002

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**24S**, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC)	24S	B

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