

Applications

The AS5035 is suitable for:

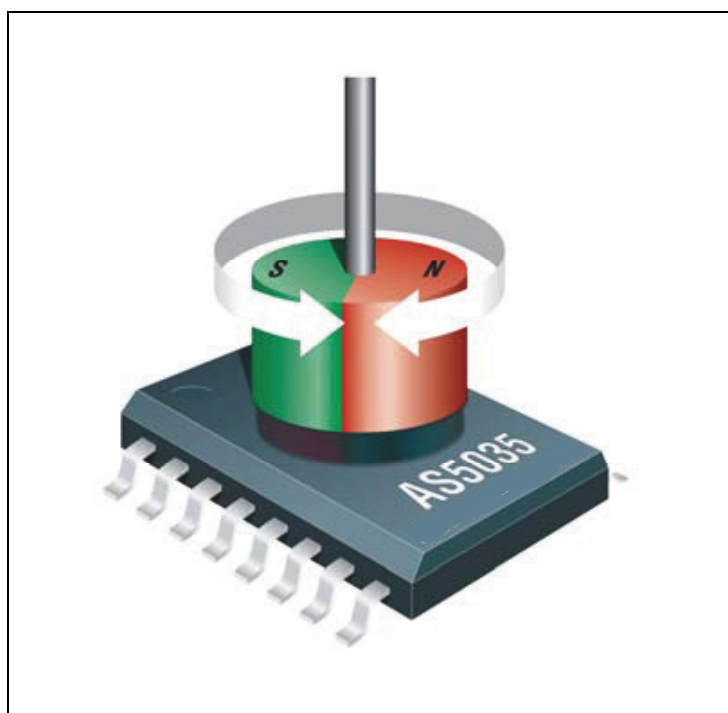
Industrial applications:

- Robotics
- Replacement of optical position sensors
- Flow meters
- Man-machine interface

Automotive application:

- Power seat position sensing
- Power mirror position sensing

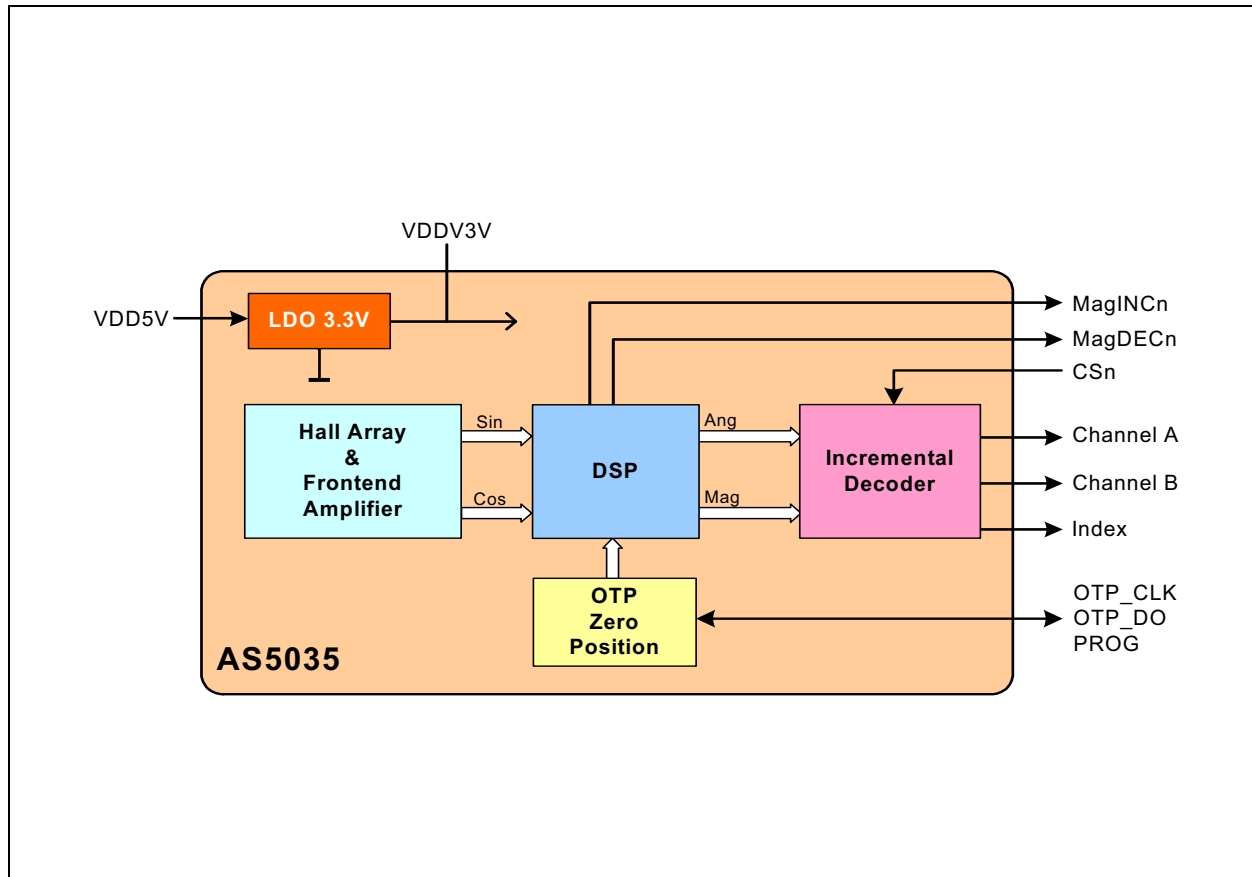
Figure 2:
Typical Arrangement of AS5035 and Magnet



Block Diagram

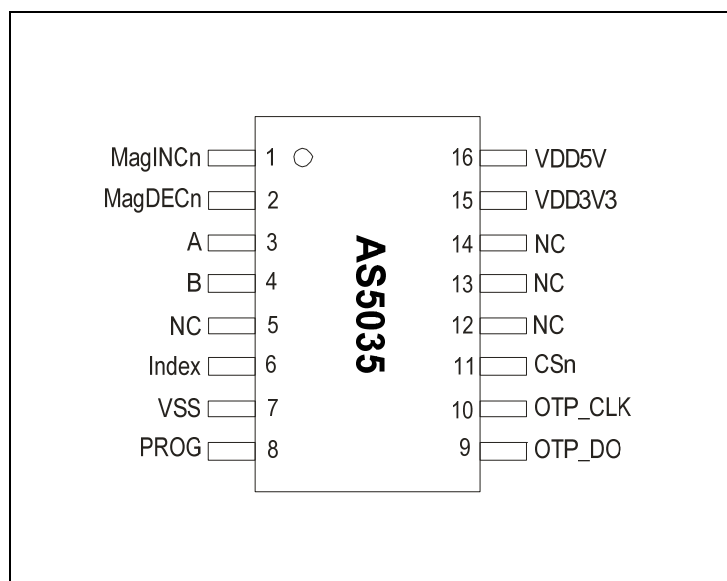
The functional blocks of this device are shown below:

Figure 3:
AS5035 Block Diagram



Pin Assignment

Figure 4:
AS5035 Pin Configuration SSOP16



Pin Description

Figure 5:
Pin Description

Pin # SSOP16	Pin Name	Type	Description
1	MagInc	DO_OD	Mag. Field Indicator
2	MagDec	DO_OD	Mag. Field Indicator
3	A	DO	Quadrature Channel A
4	B	DO	Quadrature Channel B
5	N.C.	Test	Must be left open
6	Index	DO	Incremental Index Output
7	VSS	Supply	Supply Ground
8	Prog	DI, pd	OTP Programming Input. Internal pull-down resistor (~74kΩ). Should be connected to VSS if not used
9	OTP_DO	DO_T	Data Output for Zero Position Programming
10	OTP_CLK	DI, ST	Clock Input for Zero Position Programming; Schmitt-Trigger input. Should be connected to VSS if not used

Pin # SSOP16	Pin Name	Type	Description
11	CSn	DI_ST, pu	Enable Outputs A,B,I (see Output Current). Connect to VSS for normal operation
12	N.C.	Test	Must be left open
13	N.C.	Test	Must be left open
14	N.C.	Test	Must be left open
15	VDD3V3	Supply	3V Regulator Output
16	VDD5V	Supply	5V Positive Supply Input

DO_OD: Digital output, open drain

DO: Digital push/pull output

DI: Digital input

ST: Schmitt-Trigger input

pu: Internal pull-up resistor

pd: Internal pull-down resistor

Test: Pin is used for factory testing, must be left unconnected

Unused Pins

Pins # 5, 8, 12, 13 and 14 are for factory testing and must be left unconnected

Pins# 8, 9 and 10 are used for OTP Zero Position Programming only. In normal operation, they can be left open or connected to VSS (pins 8 and 10 only)

Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
VDD5V	DC supply voltage at pin VDD5V	-0.3	7	V	
VDD3V3	DC supply voltage at pin VDD3V3		5	V	
V _{in}	Input pin voltage	-0.3	VDD5V +0.3	V	
I _{scr}	Input current (latchup immunity)	-100	100	mA	JEDEC 78
ESD	Electrostatic discharge	± 2		kV	MIL 883 E method 3015
T _{strg}	Storage temperature	-55	125	°C	Min: – 67°F; Max: 257°F
T _{Body}	Body temperature (Lead-free package)		260	°C	t=20s to 40s, IPC/JEDEC J-Std-020C Lead finish 100% Sn “matte tin”
RH _{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor life time of 168h

Figure 7:
Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
T_{amb}	Ambient temperature	-40		125	°C	-40°F to 257°F
I_{supp}	Supply current		16	25	mA	
VDD5V	Supply voltage at pin VDD5V	4.5	5.0	5.5	V	5V operation
VDD3V3	Voltage regulator output voltage at pin VDD3V3	3.0	3.3	3.6	V	
VDD5V	Supply voltage at pin VDD5V	3.0	3.3	3.6	V	3.3V operation (pin VDD5V and VDD3V3 connected)
VDD3V3	Supply voltage at pin VDD3V3	3.0	3.3	3.6	V	

DC Characteristics for Digital Inputs and Outputs

Figure 8:
CMOS Schmitt-Trigger Inputs: OTP_CLK, CSn (CSn = Internal Pull-Up)

Symbol	Parameter	Min	Max	Units	Note
V_{IH}	High level input voltage	$0.7 * VDD5V$		V	Normal operation
V_{IL}	Low level input voltage		$0.3 * VDD5V$	V	
$V_{Ion} - V_{loff}$	Schmitt-Trigger hysteresis	1		V	
I_{LEAK}	Input leakage current	-1	1	μA	CLK only
I_{iL}	Pull-up low level input current	-30	-100	μA	CSn only, VDD5V: 5.0V

Figure 9:
CMOS Output Open Drain: MagINCn, MagDECn

Symbol	Parameter	Min	Max	Units	Note
V_{OL}	Low level output voltage		$VSS + 0.4$	V	
I_O	Output current		4 2	mA	VDD5V: 4.5V VDD5V: 3V
I_{OZ}	Open drain leakage current		1	μA	

Figure 10:
CMOS Outputs: A, B, Index, OTP_DO

Symbol	Parameter	Min	Max	Units	Note
V_{OH}	High level output voltage	$V_{DD5V}-0.5$		V	
V_{OL}	Low level output voltage		$V_{SS}+0.4$	V	
I_O	Output current		4 2	mA mA	V_{DD5V} : 4.5V V_{DD5V} : 3V

Magnetic Input Specification

Two-pole cylindrical diametrically magnetized source.

Figure 11:
Magnetic Input Specification

Symbol	Parameter	Min	Typ	Max	Units	Note
d_{mag}	Diameter	4	6		mm	
t_{mag}	Thickness	2.5			mm	Recommended magnet Ø 6mm x 2.5mm for cylindrical magnets
B_{pk}	Magnetic input field amplitude	45		75	mT	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm
B_{off}	Magnetic offset			± 10	mT	Constant magnetic stray field
	Field non-linearity			5	%	Including offset gradient
f_{mag_inc}	Input frequency (rotational speed of magnet)			500	Hz	Incremental mode: no missing pulses at rotational speeds of up to 30000 rpm
B_{tc}	Magnetic field temperature drift		- 0.035		%/K	Samarium Cobalt ReComa28
Disp	Displacement radius			0.25	mm	Max. offset between defined device center and magnet axis (see Figure 23)

Electrical System Specifications

Figure 12:
Electrical System Specification

Symbol	Parameter	Min	Typ	Max	Units	Note
LSB	Resolution		1.406		deg	Degrees / step
RES				8 64	bit ppr	Channel A and B
$t_{w,Index}$	Index bit width		1.406		deg	= 1 LSB (see Figure 27)
INL_{opt}	Integral non-linearity (optimum)			± 0.5	deg	Maximum error with respect to the best line fit. Centered magnet placement without calibration, $T_{amb} = 25^{\circ}C$
INL_{temp}	Integral non-linearity (optimum)			± 0.9	deg	Maximum error with respect to the best line fit. Centered magnet placement without calibration, $T_{amb} = -40^{\circ}C$ to $125^{\circ}C$
INL	Integral non-linearity			± 1.4	deg	Best line fit = $(Err_{max} - Err_{min}) / 2$ Over displacement tolerance with 6mm diameter magnet, without calibration $T_{amb} = -40^{\circ}C$ to $125^{\circ}C$
DNL	Differential non-linearity			± 0.176	deg	No missing codes
TN	Transition noise			0.06	Deg rms	rms = 1 sigma (see Transition Noise)
Hyst	Hysteresis		0.704		deg	
V_{on} V_{off}	Power-on reset thresholds ON voltage; 300mV typ. hysteresis OFF voltage; 300mV typ. hysteresis	1,37 1.08	2.2 1.9	2.9 2.6	V V	DC supply voltage 3.3V (VDD3V3) DC supply voltage 3.3V (VDD3V3)

Timing Characteristics

Figure 13:
Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Note
t_{PwrUp}	Power-up time			50	ms	Until internal offset compensation is finished
$t_{Incremental}$ outputs valid	Incremental outputs valid after power-up			500	ns	If CSn is high during power up: = Time after t_{PwrUp} from first falling edge of CSn to valid incremental outputs.
						If CSn is low during power up: Incremental outputs are valid as soon as t_{PwrUp} is expired
	System propagation delay			192	μ s	Calculation over two samples
f_s	Sampling rate	9.5	10	10.5	kHz	Internal sampling rate

Incremental Output Signal Tolerances

See [Figure 27](#).

Programming Conditions

Operating conditions: $T_{amb} = -40^{\circ}\text{C}$ to 125°C ,

VDD5V = 3.0-3.6V (3V operation)

VDD5V = 4.5-5.5V (5V operation) unless otherwise noted.

Figure 14:
Programming Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
$t_{\text{Prog enable}}$	Programming enable time	2			μs	Time between rising edge at Prog pin and rising edge of CSn
$t_{\text{Data in}}$	Write data start	2			μs	
$t_{\text{Data in valid}}$	Write data valid	250			ns	Write data at the rising edge of CLK _{PROG}
$t_{\text{Load PROG}}$	Load programming data	3			μs	
t_{PrgR}	Rise time of V_{PROG} before CLK _{PROG}	0			μs	
t_{PrgH}	Hold time of V_{PROG} after CLK _{PROG}	0		5	μs	
CLK _{PROG}	Write data – programming CLK _{PROG}			250	kHz	
t_{PROG}	CLK pulse width	1.8	2	2.2	μs	During programming; 16 clock cycles
$t_{\text{PROG finished}}$	Hold time of V_{PROG} after programming	2			μs	Programmed data is available after next Power-ON
V_{PROG}	Programming voltage	7.3	7.4	7.5	V	Must be switched OFF after zapping
V_{ProgOFF}	Programming voltage OFF level	0		1	V	Line must be discharged to this level
I_{PROG}	Programming current			130	mA	During programming

Connecting the AS5035

Power Supply

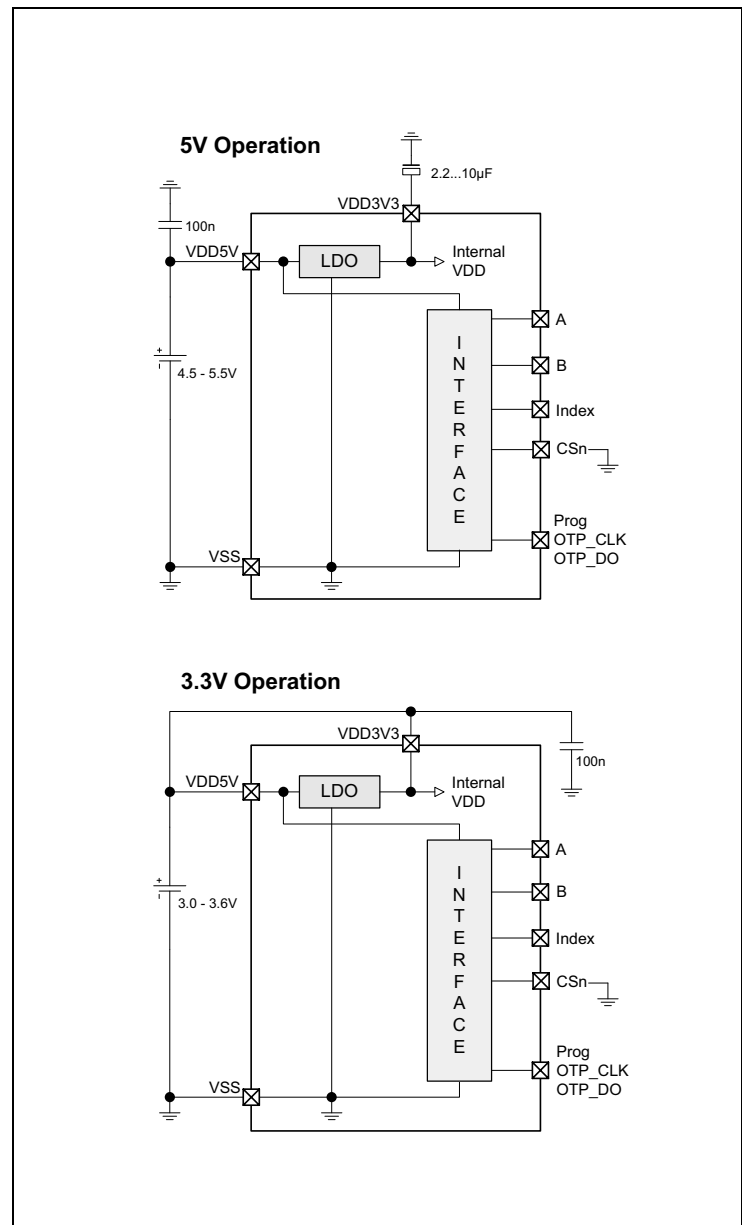
5.0V Operation

Connect a 4.5V to 5.5V power supply to pin VDD5V only. Add a 1 μ F to 10 μ F buffer capacitor to pin VDD3V3.

3.3V Operation

Connect a 3.0V to 3.6 V power supply to both pins VDD5V and VDD3V3. If necessary, add a 100nF ceramic buffer capacitor to pin VDD3V3.

Figure 15:
Connections for 5V/3.3V Supply Voltages



Logic High and Low Levels

VDD5V will be either 3.0 - 3.6V or 4.5 - 5.5V, depending on configuration.

In either case, the logic levels on output pins A, B and Index will be

$$V_{out\ high} = VDD5V - 0.5V,$$

$$V_{out\ low} = VSS + 0.4V.$$

The logic level on the CSn input pin will be

$$V_{in\ high} = VDD5V * 0.7,$$

$$V_{in\ low} = VDD5V * 0.3$$

Output Current

The available maximum output current on pins A, B and Index to maintain the V_{out} high and V_{out} low levels is

2mA (sink and source) at VDD5V = 3.0V

4mA (sink and source) at VDD5V = 4.5V

Chip Select Pin CSn

Without Power-Up Diagnostic Feature

For standalone operation without microcontroller, pin CSn should be connected to VSS permanently. The incremental outputs will be available, as soon as the internal offset compensation is finished (within <50ms).

With Power-Up Diagnostic Feature

A diagnostic feature is available to detect a temporary loss of power or initial power-up of the AS5035:

If the CSn pin is high or left open (internal pull up resistor ~50kΩ) during power-up, the incremental outputs will remain in high state: A = B = Index = High.

This state indicates a power-up or temporary loss of power, as in normal operation A, B and Index will never be high at the same time. When Index is high, both A and B are low.

To clear this state and enable the incremental outputs, CSn must be pulled low. The incremental outputs will remain enabled if CSn returns to high afterwards.

MagInc and MagDec Indicators

These two pins are open-drain outputs with a maximum driving capability of 2mA @ 3.0V and 4mA @ 4.5V.

MagINC, (**M**agnitude **I**ncrease) turns ON, when the magnet is pushed towards the IC, thus when the magnetic field strength is increasing.

MagDEC, (**M**agnitude **D**ecrease) turns ON, when the magnet is pulled away from the IC, thus when the magnetic field strength is decreasing.

If both outputs are low, they indicate that the magnetic field out of the allowed range:

Figure 16:
Magnetic Field Strength Diagnostic Outputs

MagINC	MagDEC	Description
OFF	OFF	No distance change. Magnetic Input Field OK
OFF	ON	Distance increase (Magnet pulled away from IC)
ON	OFF	Distance decrease (Magnet pushed towards IC)
ON	ON	Magnetic Input Field invalid – out of range: either too large (magnet too close) or too small (missing magnet or magnet too far away)

Note(s):

1. OFF = open-drain output transistor is OFF. Using a pull-up resistor, the output is high.
2. ON = open-drain output transistor is ON. Using a pull-up resistor, the output is low.

Both outputs MagInc and MagDec may be tied together, using one common pull-up resistor. In this case, the output will be high only when the magnetic field is in range. It will be low when either the magnet is moving in Z-axis or when the magnetic field is out of range.

Incremental Outputs

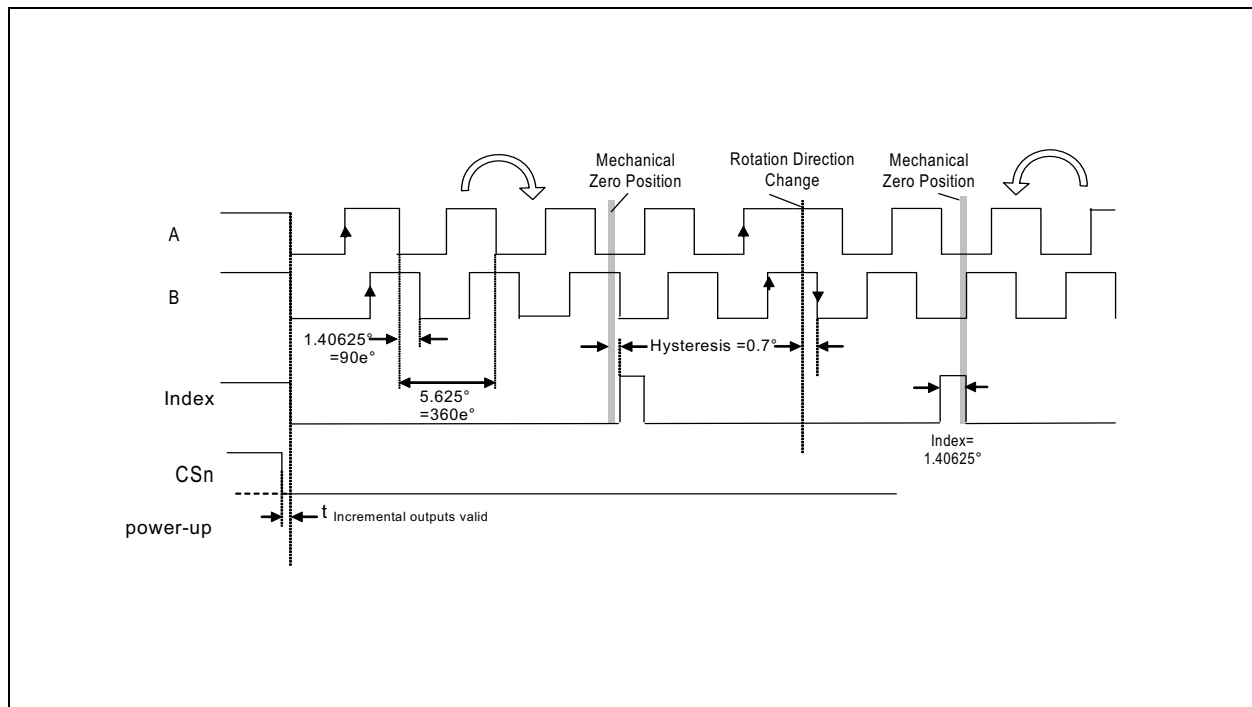
A,B and Index

The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view, magnet placed above or below the device) with 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation. The Index pulse has a width of $1\text{LSB} = 1.4^\circ$

Hysteresis

To avoid flickering of the incremental outputs at a stationary mechanical position, a hysteresis of 0.7° is introduced. When the direction of rotation is reversed, the incremental outputs will not change state unless the movement in the opposite direction is larger than the hysteresis. This leads to the effect that the A,B and Index pulse positions will be shifted by 0.7° when the rotational direction is reversed. This shift is cancelled again with the next reversal of direction so that the A,B and Index pulses appear always at the same position for a given rotational direction no matter how often the rotational direction is reversed (see Figure 17).

Figure 17:
Incremental Quadrature Outputs



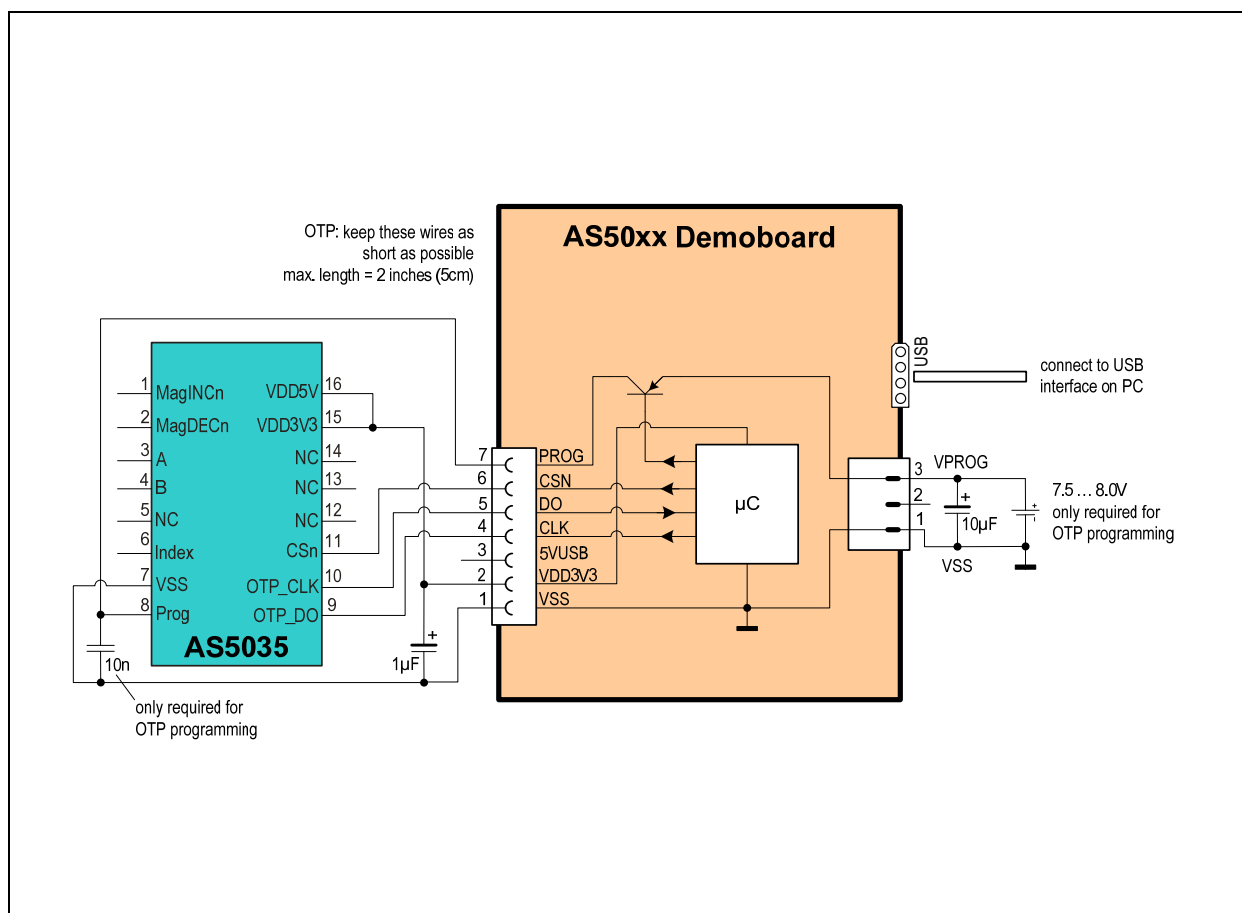
Zero Position Programming

Zero Position Programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new index position.

For Zero Position Programming, the magnet is turned to the mechanical zero position (e.g. the "OFF"-position of a rotary switch) and an automatic zero position programming is applied.

The zero position is programmed to an accuracy of $\pm 0.35^\circ$.

Figure 18:
Hardware Connection of AS5035 to AS50xx Demoboard for Zero Position Programming



OTP Programming Timing

OTP programming requires access to the factory settings register of the AS5035. Improper or accidental modification of the factory settings may render the chip unusable. Therefore the Zero Position and CCW programming is recommended only with **ams** proprietary hardware and software.

Note(s): During the programming process, the transitions in the programming current may cause high voltage spikes generated by the inductance of the connection cable. To avoid these spikes and possible damage to the IC, the connection wires, especially the signals Prog and VSS must be kept as short as possible. The maximum wire length between the VPROG switching transistor and pin Prog (see [Figure 18](#)) should not exceed 50mm (2 inches). To suppress eventual voltage spikes, a 10nF ceramic capacitor should be connected close to pins Prog and VSS. This capacitor is only required for programming, it is not required for normal operation.

The clock timing t_{clk} must be selected at a proper rate to ensure that the signal Prog is stable at the rising edge of CLK (see [Figure 19](#)). Additionally, the programming supply voltage should be buffered with a 10 μ F capacitor mounted close to the switching transistor. This capacitor aids in providing peak currents during programming.

The specified programming voltage at pin Prog is 7.3 – 7.5V (see [Programming Conditions](#)). To compensate for the voltage drop across the VPROG switching transistor, the applied programming voltage may be set slightly higher (7.5 -8.0V).

CCW Bit Programming

The absolute angular output value, by default, increases with clockwise rotation of the magnet (top view). Setting the CCW-bit (see [Figure 19](#)) allows for reversing the indicated direction, e.g. when the magnet is placed underneath the IC:

CCW = 0 – angular value increases clockwise;

CCW = 1 – angular value increases counterclockwise.

Note(s): Further information on the required hardware and software for Zero Position programming of the AS5035 can be found in the “AS5035” section of the **ams** website:

www.ams.com/AS5035

Figure 19:
Programming Access – Write Data

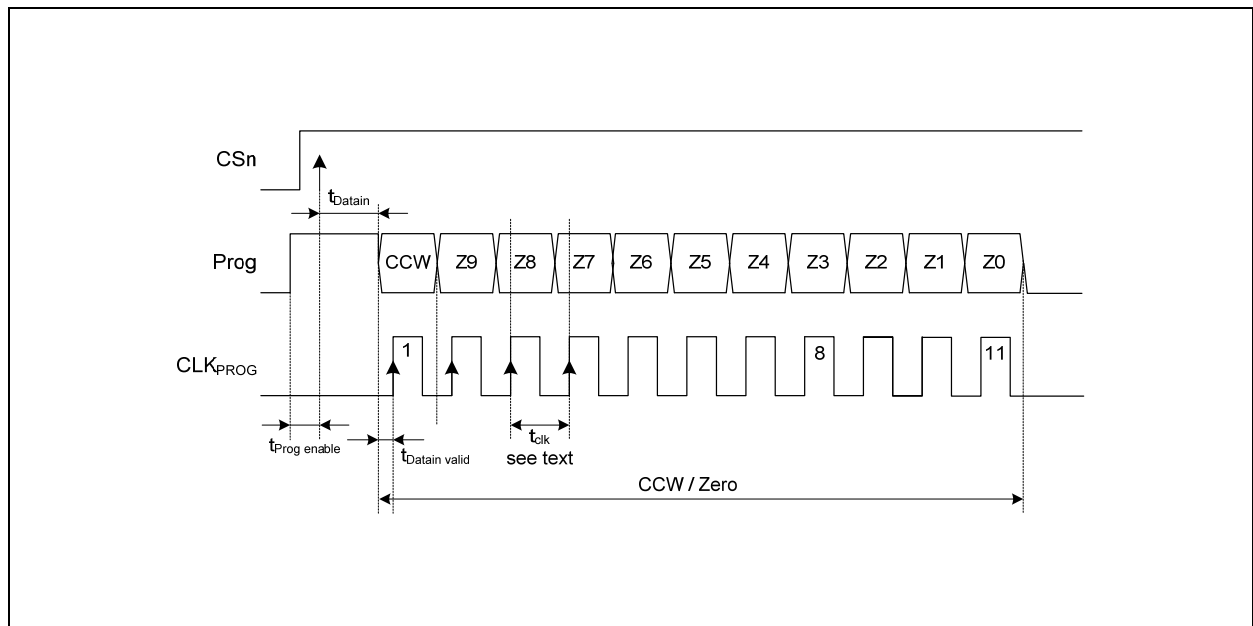
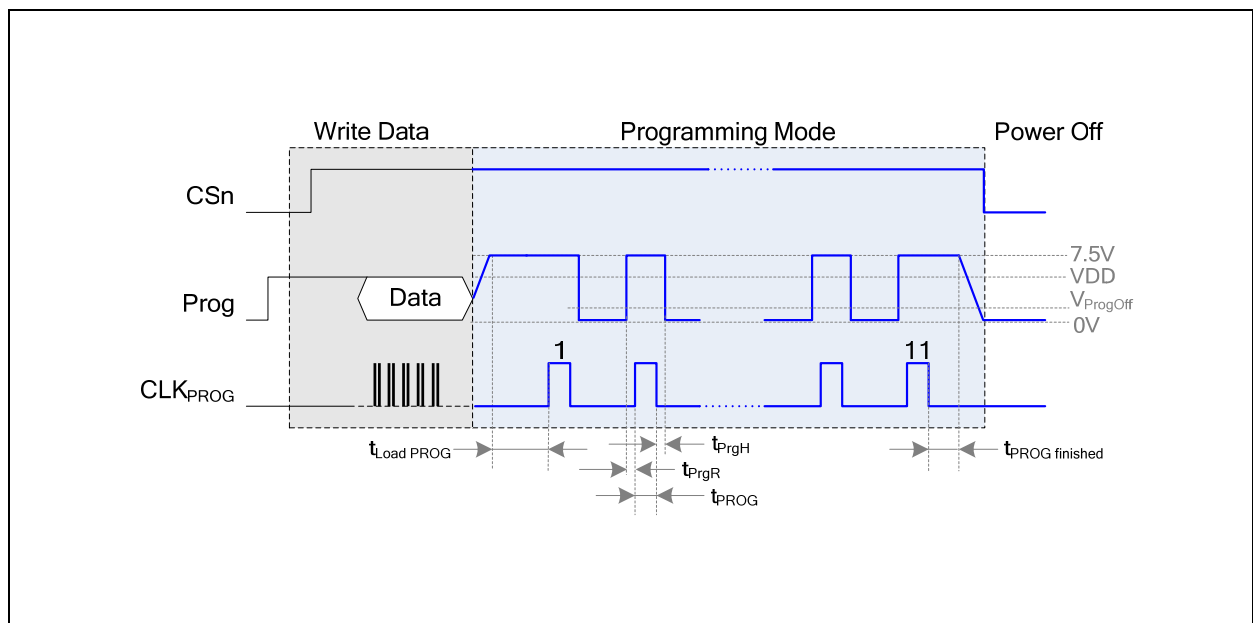
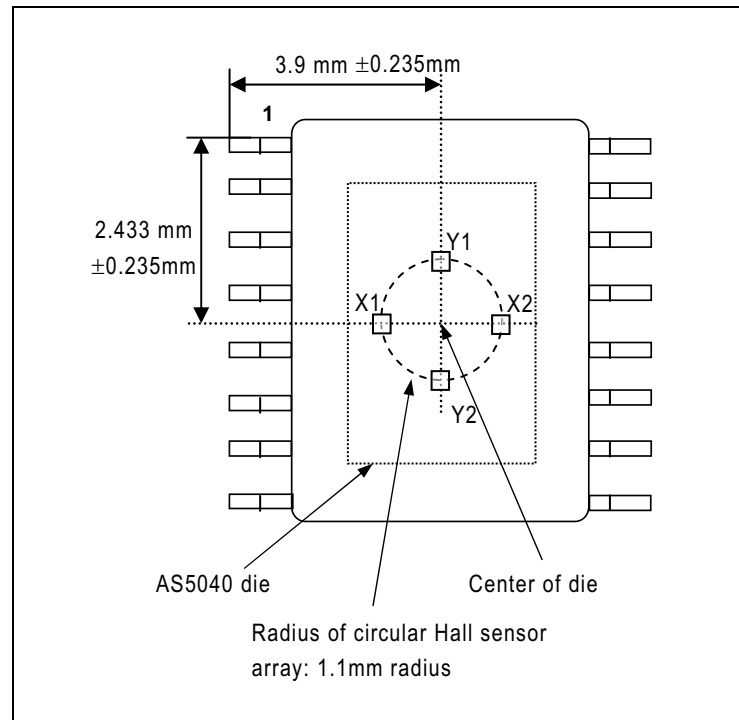


Figure 20:
Complete Programming Sequence



Simulation Modelling

Figure 21:
Arrangement of Hall Sensor Array on Chip (Principle)



With reference to [Figure 21](#), a diametrically magnetized permanent magnet is placed above or below the surface of the AS5035. The chip uses an array of Hall sensors to sample the vertical vector of a magnetic field distributed across the device package surface. The area of magnetic sensitivity is a circular locus of 1.1mm radius with respect to the center of the die. The Hall sensors in the area of magnetic sensitivity are grouped and configured such that orthogonally related components of the magnetic fields are sampled differentially.

The differential signal Y1-Y2 will give a sine vector of the magnetic field. The differential signal X1-X2 will give an orthogonally related cosine vector of the magnetic field.

The angular displacement (Θ) of the magnetic source with reference to the Hall sensor array may then be modelled by:

$$\Theta = \arctan \left(\frac{Y1 - Y2}{X1 - X2} \right) \pm 0.5^\circ$$

The $\pm 0.5^\circ$ angular error assumes a magnet optimally aligned over the center of the die and is a result of gain mismatch errors of the AS5035. Placement tolerances of the die within the package are $\pm 0.235\text{mm}$ in X and Y direction, using a reference point of the edge of pin #1 ([Figure 23](#)).

In order to neglect the influence of external disturbing magnetic fields, a robust differential sampling and ratiometric calculation algorithm has been implemented. The differential sampling of the sine and cosine vectors removes any common mode error due to DC components introduced by the magnetic source itself or external disturbing magnetic fields. A ratiometric division of the sine and cosine vectors removes the need for an accurate absolute magnitude of the magnetic field and thus accurate Z-axis alignment of the magnetic source.

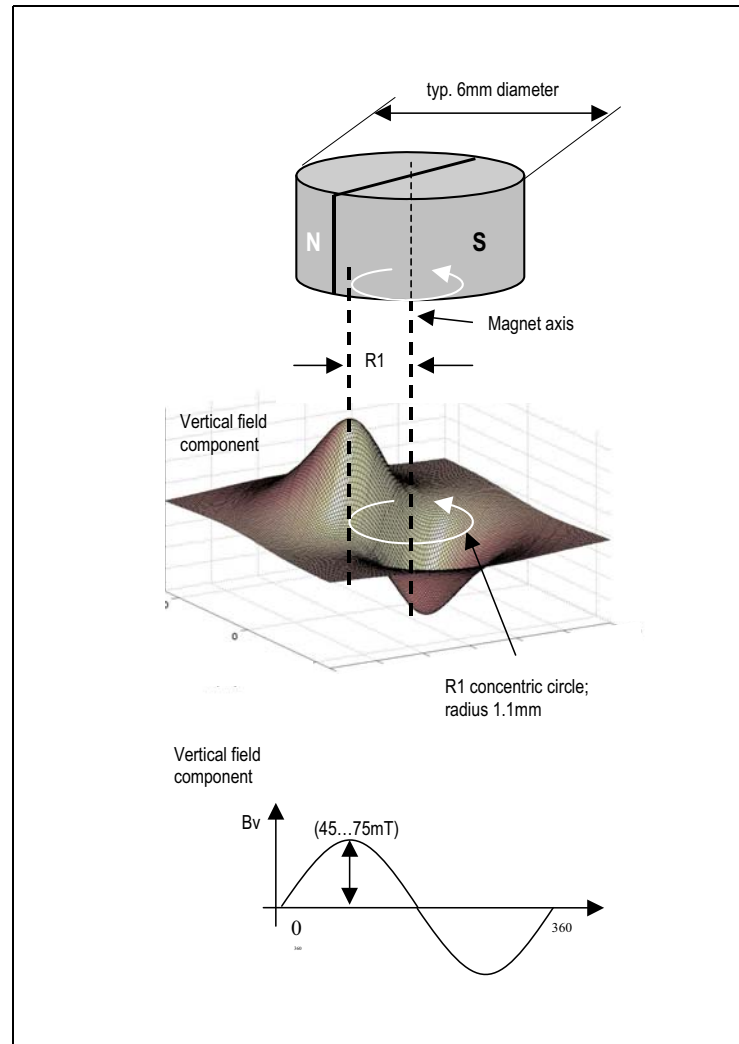
The recommended differential input range of the magnetic field strength ($B(X1-X2), B(Y1-Y2)$) is $\pm 75\text{mT}$ at the surface of the die. In addition to this range, an additional offset of $\pm 5\text{mT}$, caused by unwanted external stray fields is allowed.

The chip will continue to operate, but with degraded output linearity, if the signal field strength is outside the recommended range. Too strong magnetic fields will introduce errors due to saturation effects in the internal preamplifiers. Too weak magnetic fields will introduce errors due to noise becoming more dominant.

Choosing the Proper Magnet

Typically the magnet should be 6mm in diameter and $\geq 2.5\text{mm}$ in height. Magnetic materials such as rare earth AlNiCo, SmCo5 or NdFeB are recommended.

Figure 22:
Typical Magnet and Magnetic Field Distribution

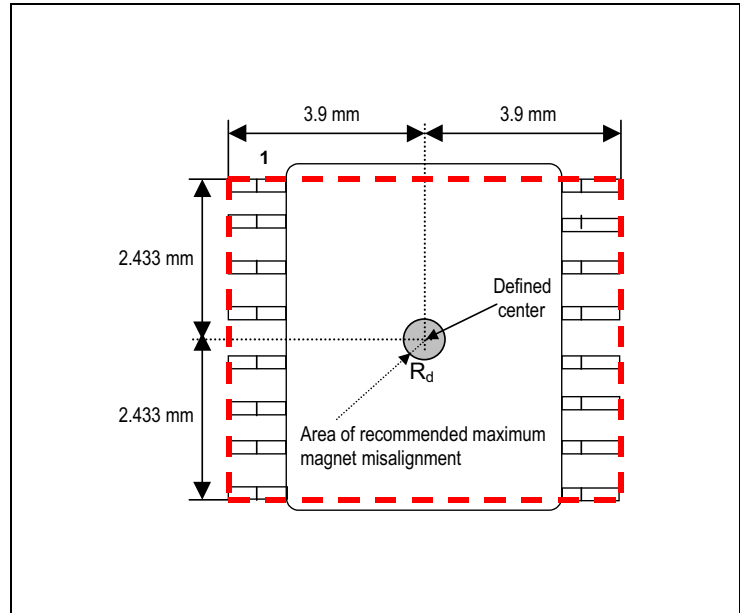


The magnet's field strength perpendicular to the die surface should be verified using a gauss-meter. The magnetic field B_v at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of $\pm 45\text{mT}$ to $\pm 75\text{mT}$. (see [Figure 22](#)).

Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 23:

Figure 23:
Defined IC Center and Magnet Displacement Radius



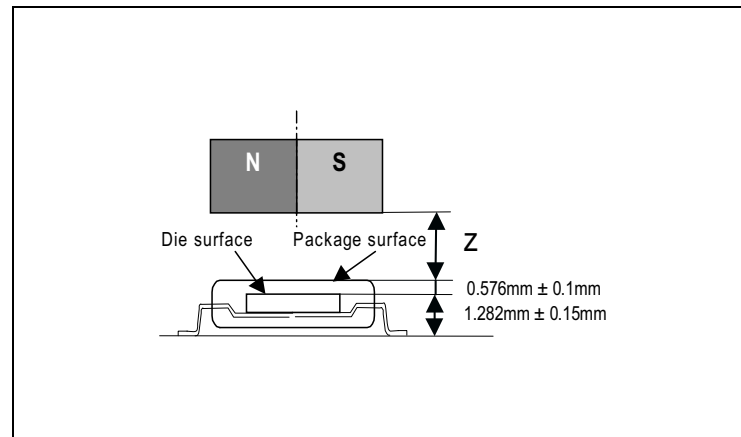
Magnet Placement:

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm from the defined center of the IC with reference to the edge of pin #1 (see Figure 23). This radius includes the placement tolerance of the chip within the SSOP-16 package ($\pm 0.235\text{mm}$). The displacement radius R_d is 0.485mm with reference to the center of the chip.

The vertical distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 22). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.8mm with the recommended magnet (6mm x 3mm). Larger gaps are possible, as long as the required magnetic field strength stays within the defined limits.

A magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by MagINCn (pin 1) and MagDECn (pin 2), see [MagInc and MagDec Indicators](#).

Figure 24:
Vertical Placement of the Magnet



Angular Output Tolerances

Accuracy

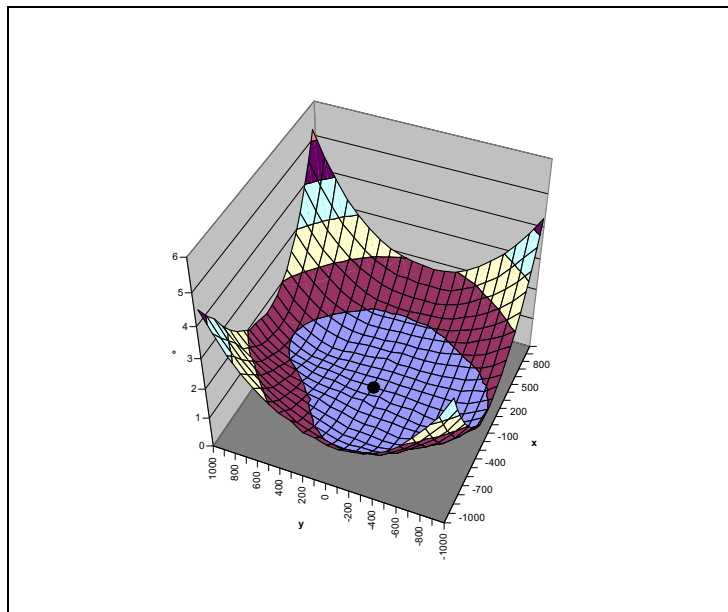
Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- The non-linearity of the analog-digital converters,
- Internal gain and mismatch errors,
- Non-linearity due to misalignment of the magnet

As a sum of all these errors, the accuracy with centered magnet = $(Err_{max} - Err_{min})/2$ is specified as better than ± 0.5 degrees @ 25°C (see [Figure 26](#)).

Misalignment of the magnet further reduces the accuracy. [Figure 26](#) shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ± 1 mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

Figure 25:
Example of Linearity Error Over XY Misalignment



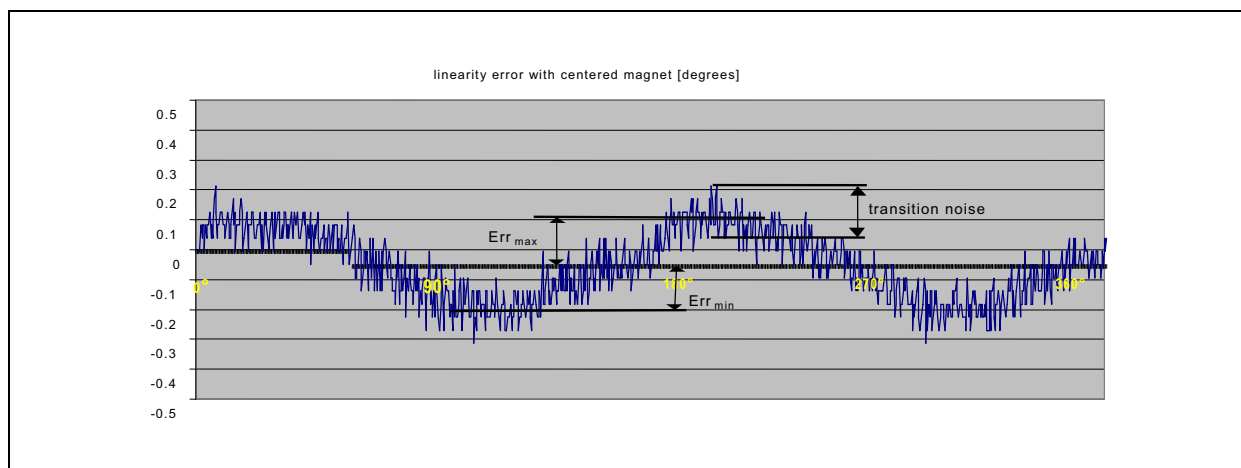
For each misalignment step, the measurement as shown in Figure 14 is repeated and the accuracy $(Err_{max} - Err_{min})/2$ (e.g. 0.25° in Figure 26) is entered as the Z-axis in the 3D-graph.

The maximum non-linearity error on this example is better than ± 1 degree (inner circle) over a misalignment radius of ~ 0.7 mm. For volume production, the placement tolerance of the IC within the package (± 0.235 mm) must also be taken into account.

The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25 mm is specified better than ± 1.4 degrees.

The magnet used for these measurements was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6 mm diameter and 2.5 mm in height.

Figure 26:
Example of Linearity Error Over 360°



Transition Noise

Transition noise is defined as the jitter in the transition between two steps.

Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved.

This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)¹.

This is the repeatability of an indicated angle at a given mechanical position.

The transition noise influences the period, width and phase shift of the output signals A, B and Index:

Figure 27:
Incremental Signal Tolerances with Transition Noise

Parameter	Tolerance (1 σ) (rms)	Tolerance (3 σ) (peak)
Index Pulse width	1.406° ± 0.06°	1.406° ± 0.18°
A,B Pulse width	2.813° ± 0.06°	2.813° ± 0.18°
Period	5.625° ± 0.06°	5.625° ± 0.18°
A-B Phase shift	90e° ± 1.9e°	90e° ± 5.7e°

e° = electrical degrees (see [Figure 17](#))

The algorithm used to generate the incremental outputs guarantees no missing or additional pulses even at high speeds (up to 30000 rpm and higher).

High Speed Operation

Sampling Rate

The AS5035 samples the angular value at a rate of 10k samples per second. Consequently, the incremental outputs are updated each 100 μ s.

At a stationary position of the magnet, this sampling rate creates no additional error.

Incremental position sensors are usually required to produce no missing pulses up to several thousand rpm's.

Therefore, the AS5035 has a built-in interpolator, which ensures that there are no missing pulses at the incremental outputs for rotational speeds of up to 10000rpm.

1. Statistically, 1 sigma represents 68.27% of readings, 3 sigma represents 99.73% of readings.

Output Delays

Due to the sampling rate of 10kHz, there will be a delay of up to 100µs between the time that the sample is taken until it is converted and available as angular data.

A rotating magnet will therefore cause an angular error caused by the output delay.

This error increases linearly with speed:

$$e_{\text{sampling}} = \text{rpm} * 6E^{-4}$$

At low speeds this error is small (e.g. $\leq 0.06^\circ$ at 100 rpm).

At speeds over 586 rpm, the error approaches 1LSB (0.35°). The maximum error caused by the sampling rate of the ADCs is 0/100µs. It has a peak of 1LSB = 0.35° at 586 rpm.

At higher speeds this error is reduced again due to interpolation and the output delay remains at 200µs as the DSP requires two sampling periods ($2 \times 100\mu\text{s}$) to synthesize and redistribute any missing pulses.

Temperature

Magnetic Temperature Coefficient

One of the major benefits of the AS5035 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5035 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5035 operates with magnetic field strengths from $\pm 45\text{mT}$ to $\pm 75\text{mT}$.

Example:

A NdFeB magnet has a field strength of 75mT @ -40°C and a temperature coefficient of -0.12% per Kelvin. The temperature change is from -40°C to $125^\circ\text{C} = 165\text{K}$.

The magnetic field change is: $165 \times -0.12\% = -19.8\%$, which corresponds to 75mT at -40°C and 60mT at 125°C .

The AS5035 can compensate for this temperature related field strength change automatically, no user adjustment is required.

Accuracy over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is $\leq \pm 0.5^\circ$ at room temperature, it may increase to $\leq \pm 0.9^\circ$ due to increasing noise at high temperatures.

Timing Tolerance over Temperature

The internal RC oscillator is factory trimmed to $\pm 5\%$. Over temperature, this tolerance may increase to $\pm 10\%$. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation.

Failure Diagnostics

The AS5035 also offers several diagnostic and failure detection features:

Magnetic Field Strength Diagnosis

Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned ON (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs is low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

Power Supply Failure Detection

MagINCn and MagDECn Pins

These are open drain outputs and require external pullup resistors. In normal operation, these pins are high ohmic and the outputs are high (see [Figure 16](#)). In a failure case, either when the magnetic field is out of range or the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5035, the pull-up resistors ($>10k\Omega$) must be connected to the positive supply at pin 16 (VDD5V).

Incremental Outputs

In normal operation, pins A(#3), B(#4) and Index (#6) will never be high at the same time, as Index is only high when A=B=low. However, after a power-on-reset, if VDD is powered up or restarts after a power supply interruption, all three outputs will remain in high state until pin CSn is pulled low (see [With Power-Up Diagnostic Feature](#)).

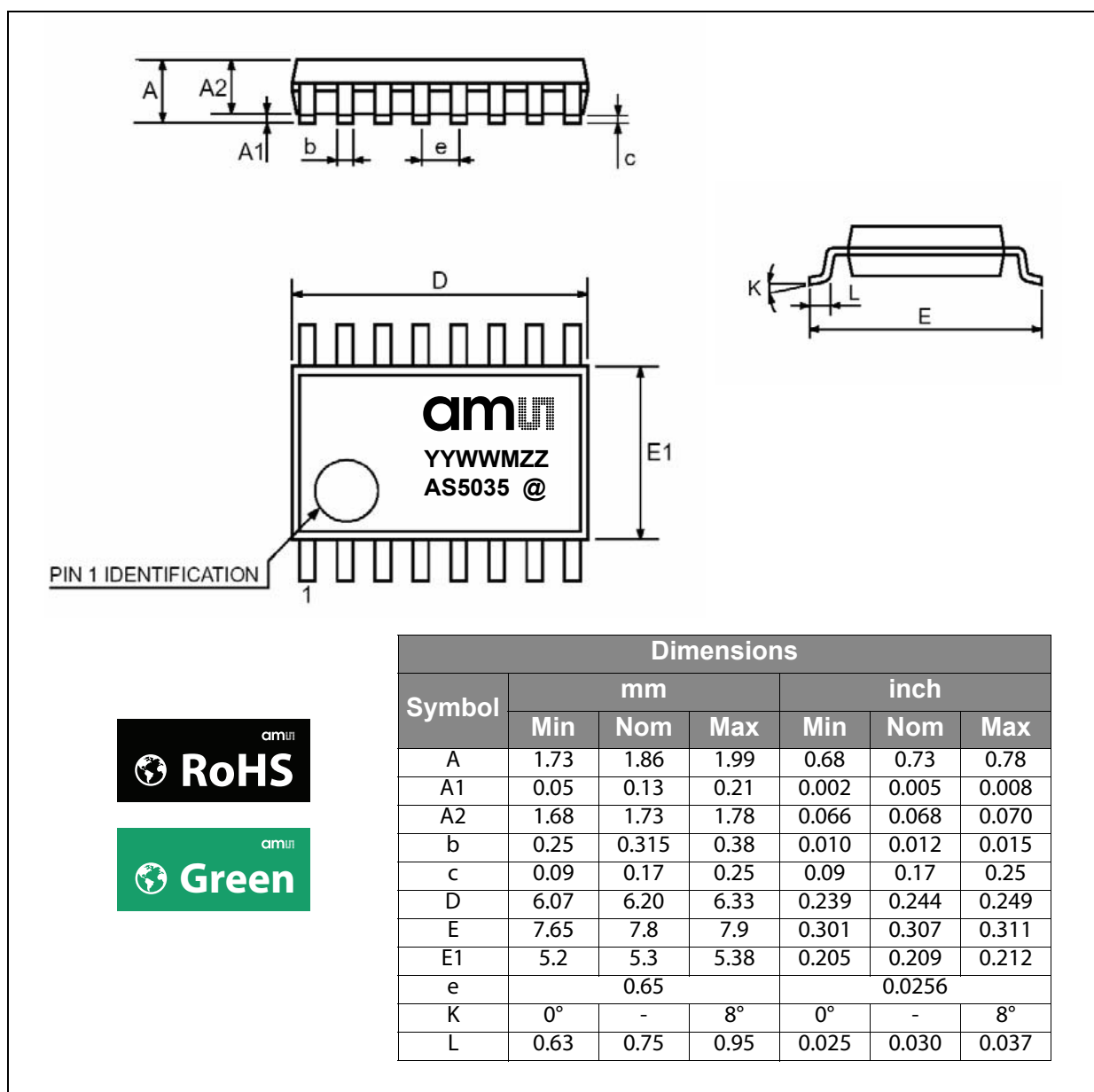
If CSn is already tied to VSS during power-up, the incremental outputs will all be high until the internal offset compensation is finished (within t_{PwrUp}).

Another way to detect a power supply loss is by connecting pull-up resistors to the A,B and Index pins at the receiving side (μC , control unit, etc.). If the negative power line to the sensor is interrupted, all three outputs will be pulled high by the external pull-up resistors. This unique state again indicates a failure as it does not occur in normal operation.

Package Drawings & Markings

The device is available in a 16-Lead Shrink Small Outline package SSOP-16.

Figure 28:
AS5035 Package Drawings and Dimensions



Note(s):

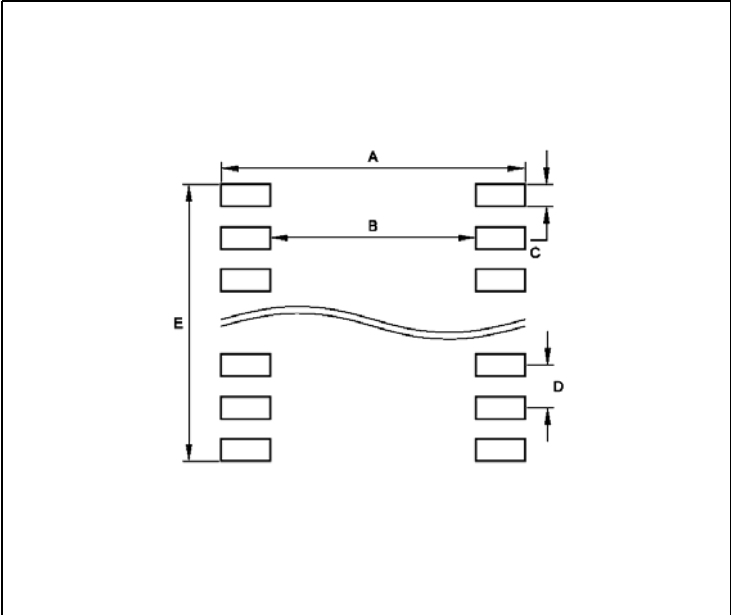
1. JEDEC Package Outline Standard: MO - 150 AC.
2. Thermal Resistance $R_{th(j-a)}$: typ. 151 K/W in still air, soldered on PCB.
3. IC's marked with a white dot or the letters "ES" denote Engineering Samples.

Figure 29:
Marking: YYWWMZZ@

YY	WW	M	ZZ	@
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Traceability code	Sublot Identifier

Recommended PCB Footprint

Figure 30:
PCB Footprint



Recommended Footprint Data		
Symbol	mm	inch
A	9.02	0.355
B	6.16	0.242
C	0.46	0.018
D	0.65	0.025
E	5.01	0.197

Ordering & Contact Information

The devices are available as the standard products shown in [Figure 31](#).

Figure 31:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5035-ASST	SSOP-16	AS5035	Tape & Reel	1 reel = 2000 devices

Not Recommended for New Designs!

ams AG is discontinuing production of this device. Final lifetime buy order must be placed by DECEMBER 31, 2017.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 2-01 (2016-Sep-21) to current revision 2-02 (2017-Jun-23)	Page
Update of document status	
Update of Ordering Information section by adding NRND statement	30

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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