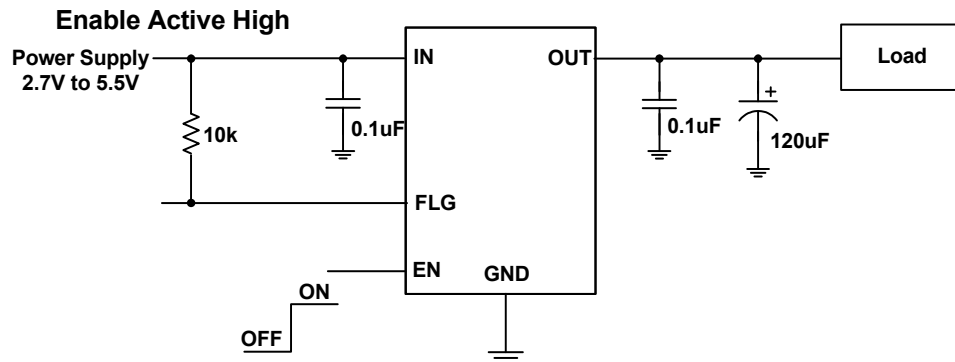


Typical Applications Circuit



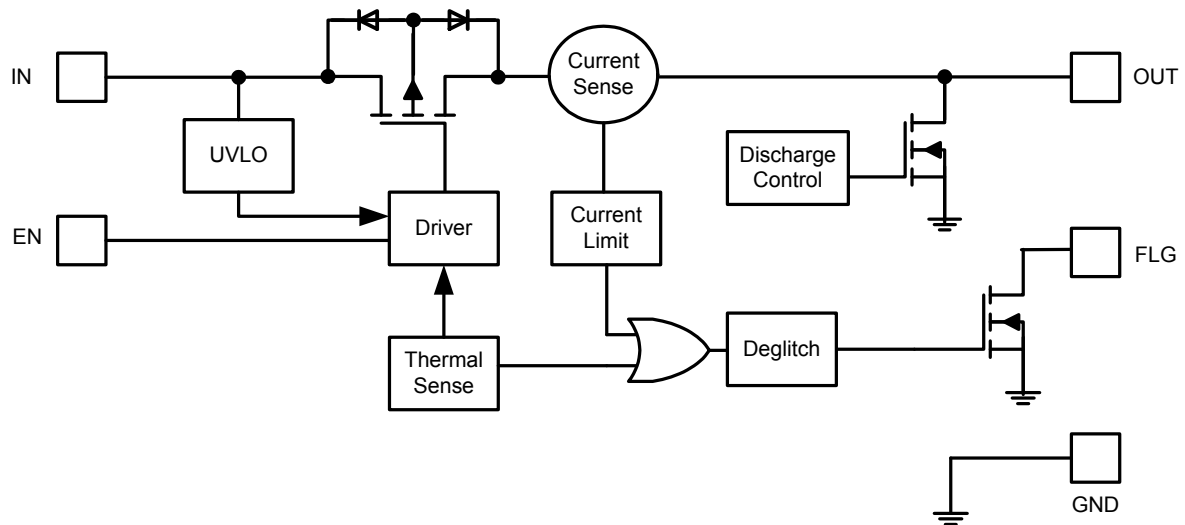
Available Options

Part Number	Channel	Enable Pin (EN)	Recommended Maximum Continuous Load Current (A)	Typical Output Latch-Off Current Limit (A)	Package
AP2401	1	Active Low	2	2.5	SO-8 MSOP-8 MSOP-8EP U-DFN3030-8 U-DFN2020-6
AP2411	1	Active High			

Pin Descriptions

Pin Name	Pin Number			Function
	SO-8, MSOP-8	MSOP-8EP, U-DFN3030-8	U-DFN2020-6	
GND	1	1	2	Ground
IN	2, 3	2, 3	1	Voltage Input Pin. Connect a 0.1uF or larger ceramic capacitor from IN to GND as close as possible. (all IN pins must be tied together externally)
EN	4	4	3	Enable Input. Active low (AP2401) or active high (AP2411).
FLG	5	5	4	Over-temperature and over-current fault reporting with 7ms deglitch; active low open-drain output. FLG is disabled for 7ms after turn-on.
OUT	6, 7	6, 7	5	Voltage Output Pin (all OUT pins must be tied together externally)
NC	8	8	6	No Internal Connection. Recommend tie to OUT pins.
Exposed Pad	—	Exposed Pad	Exposed Pad	Exposed pad. It should be externally connected to GND plane and thermal mass for enhanced thermal impedance. Exposed pad should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	4	kV
ESD MM	Machine Model ESD Protection	300	V
V _{IN}	Input Voltage (Note 4)	-0.3 to 6.5	V
V _{OUT}	Output Voltage (Note 4)	-0.3 to V _{IN} + 0.3 or 6.5	V
V _{EN} , V _{FLG}	Enable Voltage (Note 4)	-0.3 to V _{IN} + 0.3 or 6.5	V
I _{LOAD}	Maximum Continuous Load Current	Internal Limited	A
T _{J(MAX)}	Maximum Junction Temperature	150	°C
T _{ST}	Storage Temperature Range (Note 4)	-65 to +150	°C

- Notes:
4. All voltages referred to GND pin. Maximums are the lower of V_{IN} + 0.3 and 6.5V
 5. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C).

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V _{IN}	Input voltage	2.7	5.5	V
I _{OUT}	Output Current	0	2	A
V _{IL}	EN Input Logic Low Voltage	0	0.8	V
V _{IH}	EN Input Logic High Voltage	2	V _{IN}	V
T _A	Operating Ambient Temperature	-40	+85	°C

Electrical Characteristics (@T_A = +25°C, V_{IN} = +5.0V, C_{IN} = 0.1μF, C_L = 1μF, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 5)	Min	Typ	Max	Unit
V _{UVLO}	Input UVLO	V _{IN} rising	1.6	2.0	2.4	V
ΔV _{UVLO}	Input UVLO Hysteresis	V _{IN} decreasing		50		mV
I _{SHDN}	Input Shutdown Current	Disabled, OUT = open		0.1	1	μA
I _Q	Input Quiescent Current	Enabled, OUT = open		60	100	μA
I _{LEAK}	Input Leakage Current	Disabled, OUT grounded		0.1	1	μA
I _{REV}	Reverse Leakage Current	Disabled, V _{IN} = 0V, V _{OUT} = 5V, I _{REV} at V _{IN}		0.01	1	μA
R _{DS(ON)}	Switch on-resistance	V _{IN} = 5V, I _{OUT} = 2.0A		70	84	mΩ
		T _A = +25°C				
		-40°C ≤ T _A ≤ +85°C			105	
		V _{IN} = 3.3V, I _{OUT} = 2.0A		90	108	
I _{LIMIT}	Over-Load Current Limit (Note 6)	V _{IN} = 5V, V _{OUT} = 4.5V			135	A
		-40°C ≤ T _A ≤ +85°C	2.05	2.5	2.85	
I _{Trig}	Current limiting trigger threshold	Output Current Slew rate (< 100A/s)		2.5		A
I _{SHORT}	Short-Circuit Current Limit	Enabled into short circuit	2.1	2.75	3.3	A
T _{SHORT}	Short-circuit Response Time	V _{OUT} = 0V to I _{OUT} = I _{LIMIT} (OUT shorted to ground)		2		μs
V _{IL}	EN Input Logic Low Voltage	V _{IN} = 2.7V to 5.5V			0.8	V
V _{IH}	EN Input Logic High Voltage	V _{IN} = 2.7V to 5.5V	2			V
I _{LEAK-EN}	EN Input leakage	V _{IN} = 5V, V _{EN} = 0V and 5.5V		0.01	1	μA
I _{LEAK-O}	Output leakage current	Disabled, V _{OUT} = 0V		0.5	1	μA
T _{D(ON)}	Output turn-on delay time	C _L = 1μF, R _{LOAD} = 5Ω		0.1		ms
T _R	Output turn-on rise time	C _L = 1μF, R _{LOAD} = 5Ω		0.6	1.5	ms
T _{D(OFF)}	Output turn-off delay time	C _L = 1μF, R _{LOAD} = 5Ω		0.1		ms
T _F	Output turn-off fall time	C _L = 1μF, R _{LOAD} = 5Ω		0.05	0.1	ms
R _{FLG}	FLG output FET on-resistance	I _{FLG} = 10mA		20	40	Ω
I _{FOH}	FLG Off Current	V _{FLG} = 5V		0.01	1	μA
T _{BLANK}	FLG blanking and latch off time	Assertion or deassertion due to overcurrent and over-temperature condition	4	7	15	ms
T _{DIS}	Discharge time	C _L = 1μF, V _{IN} = 5V, disabled to V _{OUT} < 0.5V		0.6		ms
R _{DIS}	Discharge resistance (Note 7)	V _{IN} = 5V, disabled, I _{OUT} = 1mA		100		Ω
T _{SHDN}	Thermal Shutdown Threshold	Enabled		140		°C
T _{HYS}	Thermal Shutdown Hysteresis			20		°C
θ _{JA}	Thermal Resistance Junction-to-Ambient	SO-8 (Note 8)		96		°C/W
		MSOP-8 (Note 8)		130		°C/W
		MSOP-8EP (Note 9)		92		°C/W
		U-DFN3030-8 (Note 9)		84		°C/W
		U-DFN2020-6 (Note 10)		90		°C/W

- Notes:
- Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
 - The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when V_{IN} < V_{UVLO}). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.
 - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
 - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
 - Device mounted on 1"x1" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground.

Typical Performance Characteristics

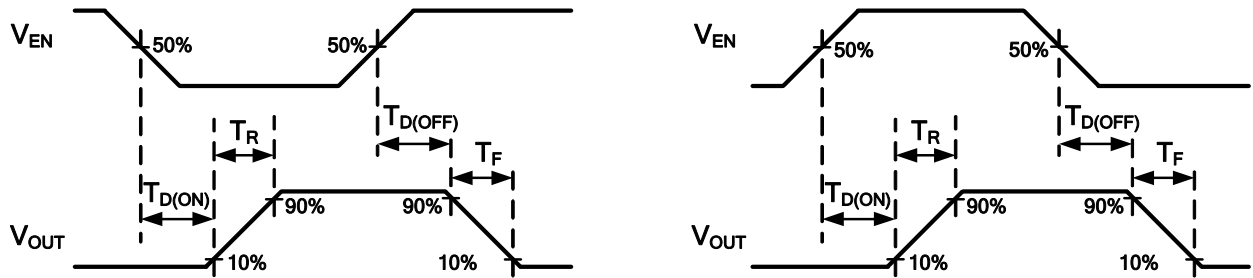
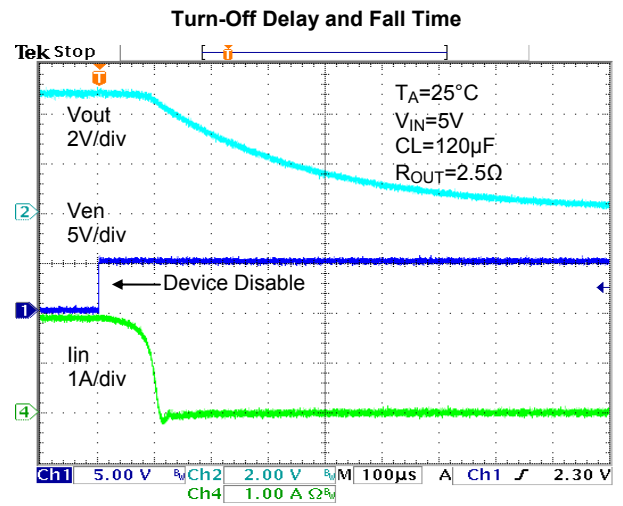
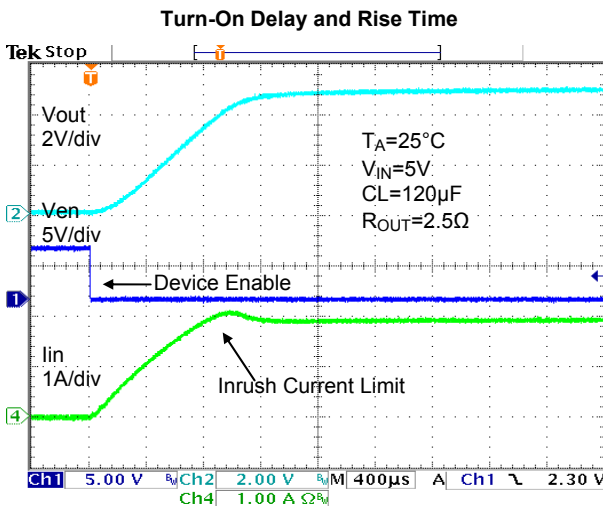
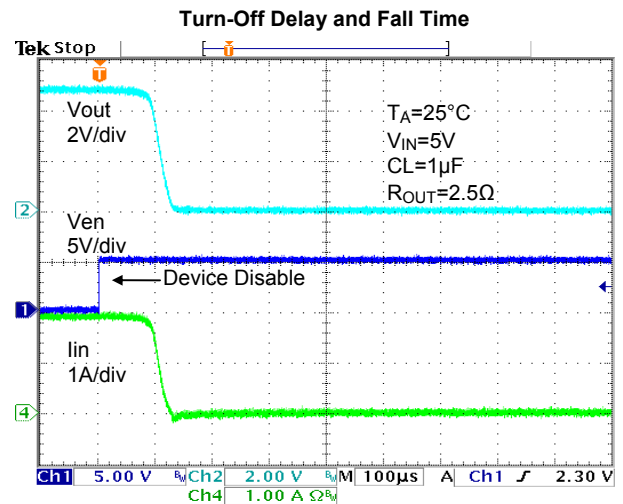
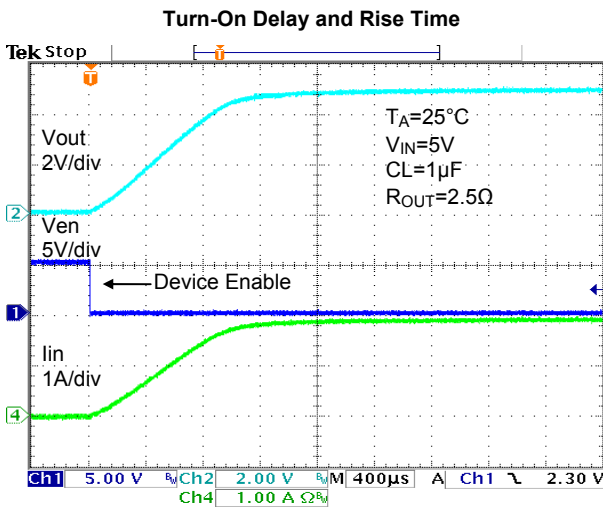
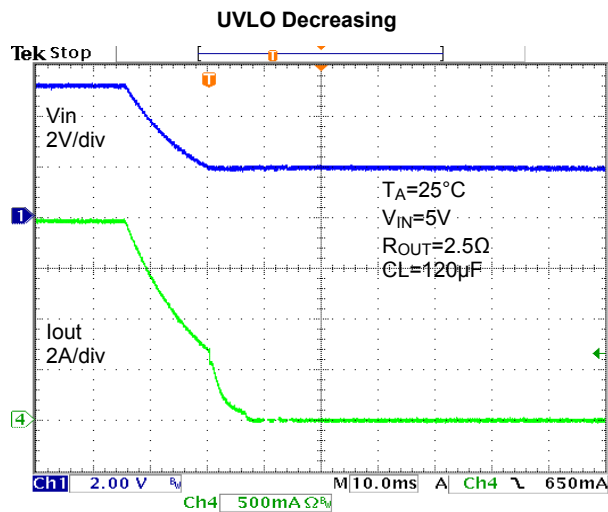
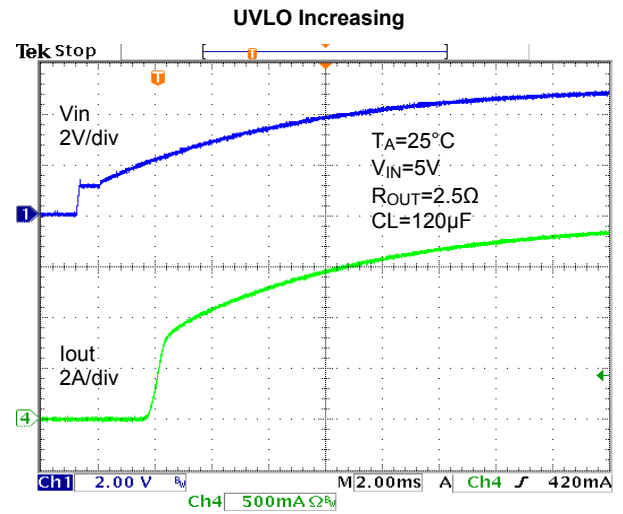
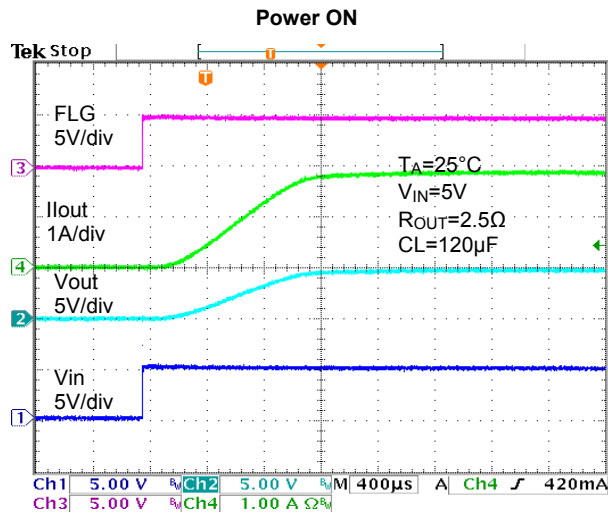


Figure 1 Voltage Waveforms: AP2401 (left), AP2411 (right)

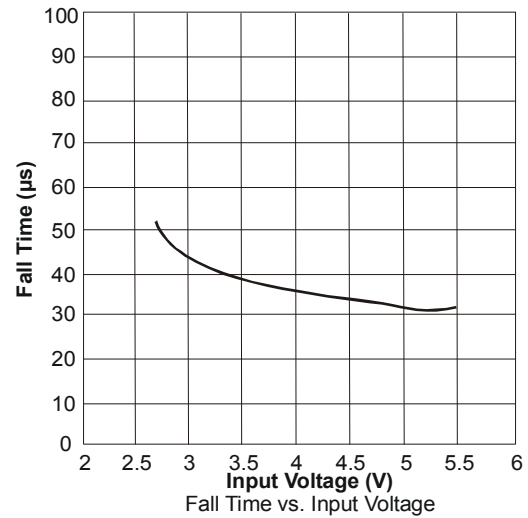
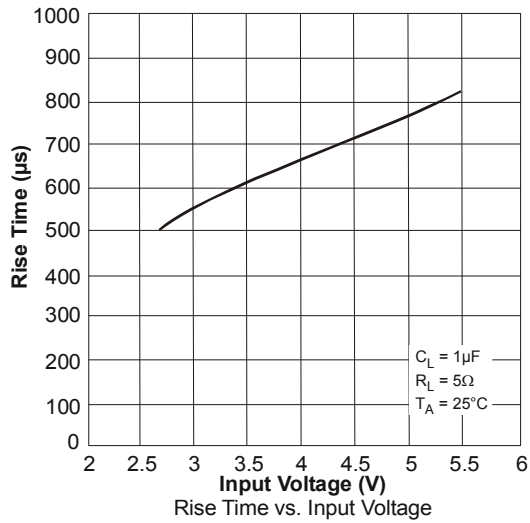
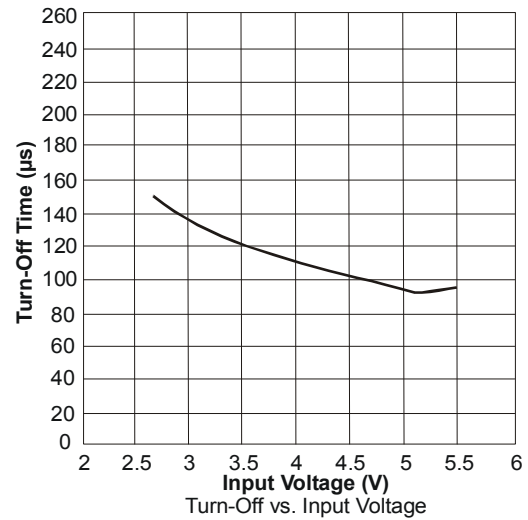
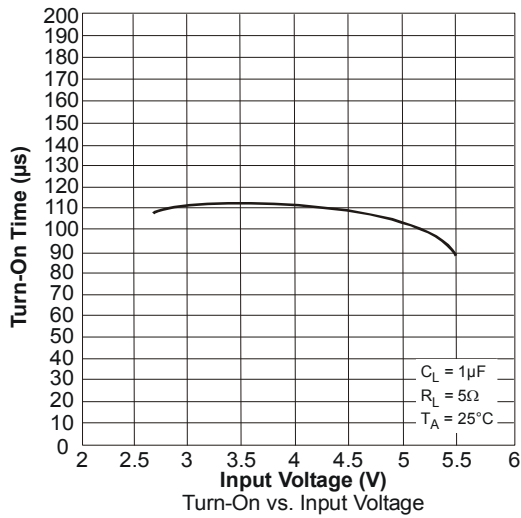
All Enable Plots are for Enable Active Low



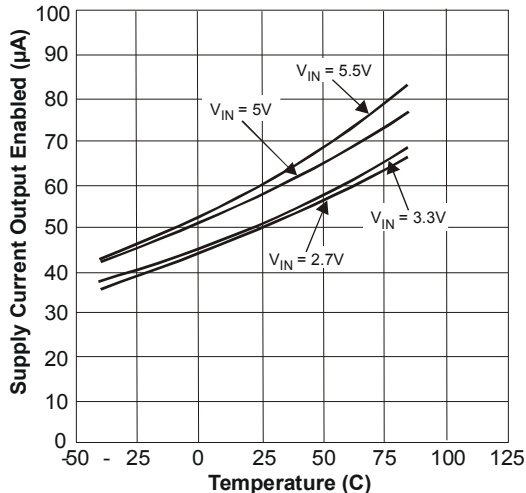
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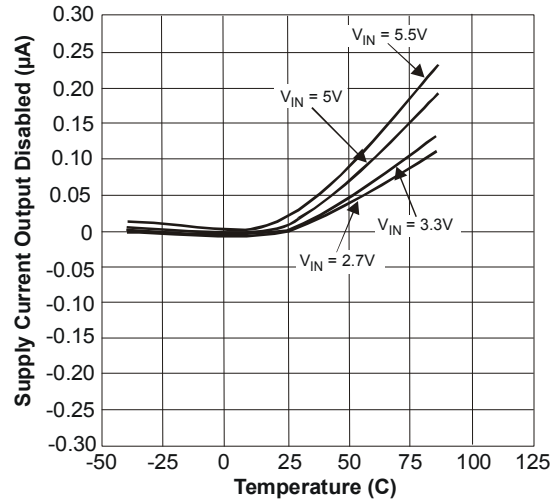
Typical Performance Characteristics (cont.)



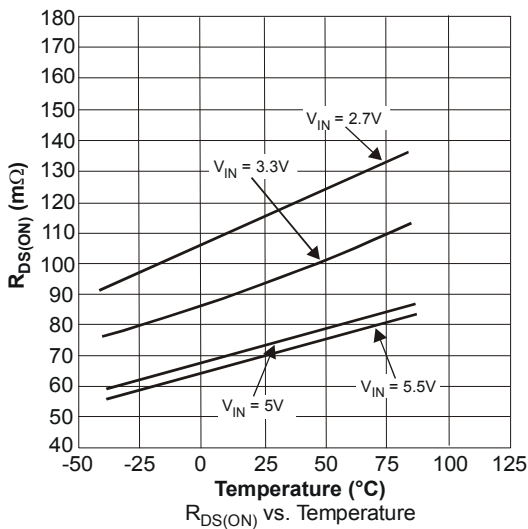
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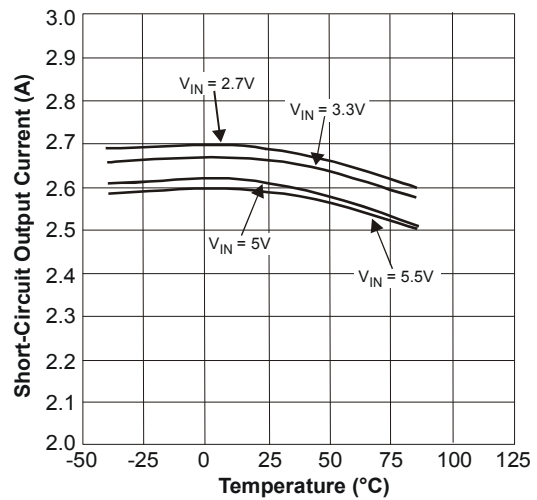
Supply Current, Output Enabled vs. Temperature



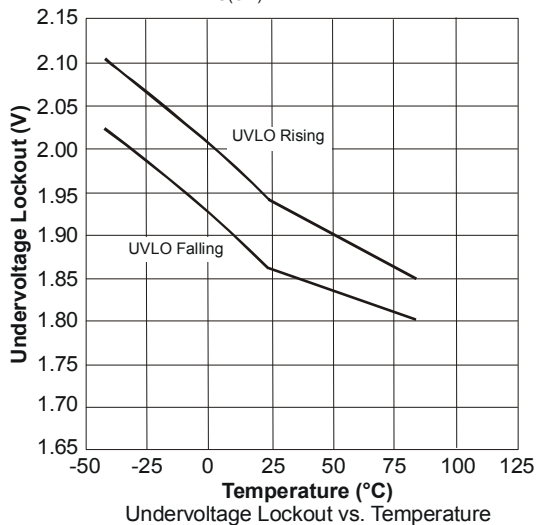
Supply Current, Output Disabled vs. Temperature



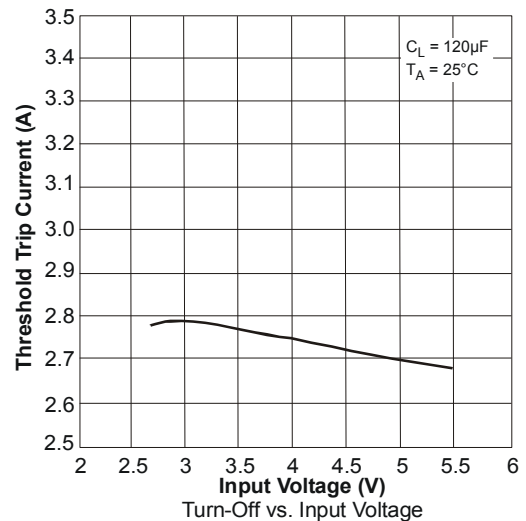
$R_{\text{DS(ON)}}$ vs. Temperature



Short-Circuit, Output Current vs. Temperature



Undervoltage Lockout vs. Temperature



Turn-Off vs. Input Voltage

Application Information

Power Supply Considerations

A 0.1µF to 2.2µF X7R or X5R ceramic bypass capacitor placed between IN and GND, close to the device, is recommended. When an external power supply is used, or an additional ferrite bead is added to the input, high inrush current may cause voltage spikes higher than the device maximum input rating during short circuit condition. In this case a 2.2µF or bigger capacitor is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.1µF to 1.0µF ceramic capacitor improves the immunity of the device to short circuit transients.

Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the devices will limit the current until the overload condition is removed or the internal deglitch time (7-ms typical) is reached and the device is turned off. The device will remain latched off even overload condition is removed until power is cycled or the device enable is toggled.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before VIN has been applied. The AP2401/AP2411 senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT} , and turns off after deglitch time(7-ms typical).

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT} current for deglitch time period (7-ms typical), and then turned off.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIP}) is reached or until the thermal limit of the device is exceeded. The AP2401/AP2411 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and output current is clamped at I_{LIMIT} for deglitch time period (7-ms typical), and then turned off.

FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout.

When that happens, the FLG will remain low and the switch will be latched off until the fault condition is removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2401/AP2411 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature°C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2401/AP2411 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an over-current condition, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately +25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown occurs with 7-ms deglitch.

When the FLG is asserted, the switch will be latched off until the temperature drops to 20°C below the thermal shutdown threshold and the power or EN pin is cycled.

Application Information (cont.)

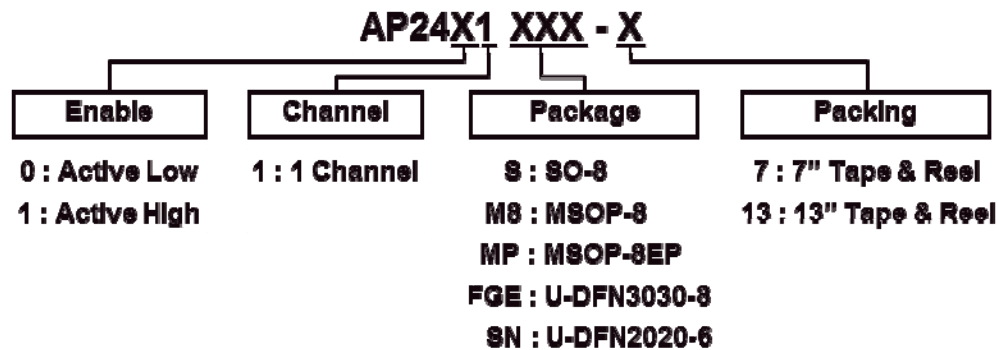
Under-Voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Discharge Function

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the N-MOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

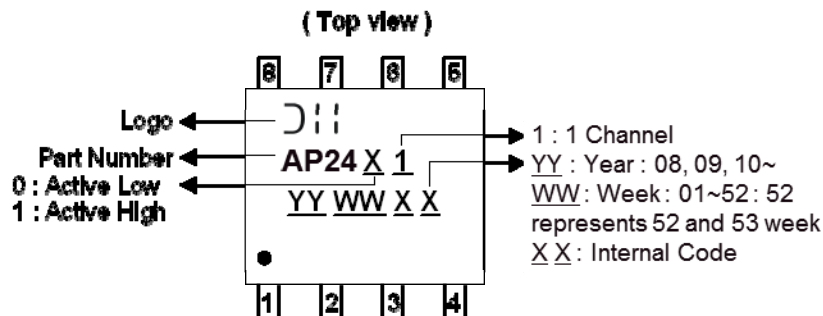
Ordering Information



Part Number	Status	Package Code	Packaging	7"/13" Tape and Reel	
				Quantity	Part Number Suffix
AP24X1S-13	New Product	S	SO-8	2500/Tape & Reel	-13
AP24X1M8-13	New Product	M8	MSOP-8	2500/Tape & Reel	-13
AP24X1MP-13	New Product	MP	MSOP-8EP	2500/Tape & Reel	-13
AP24X1FGE-7	New Product	FGE	U-DFN3030-8	3000/Tape & Reel	-7
AP24X1SN-7	Preview	SN	U-DFN2020-6	3000/Tape & Reel	-7

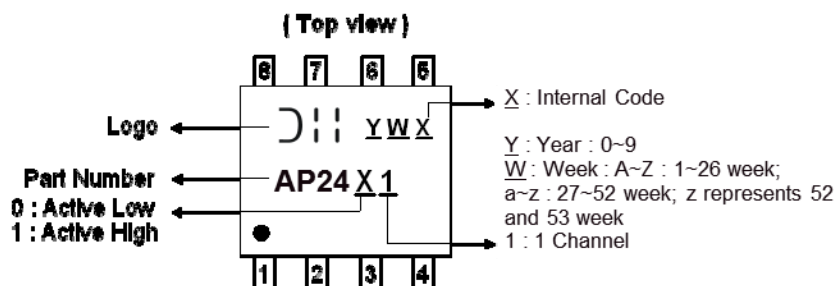
Marking Information

(1) SO-8

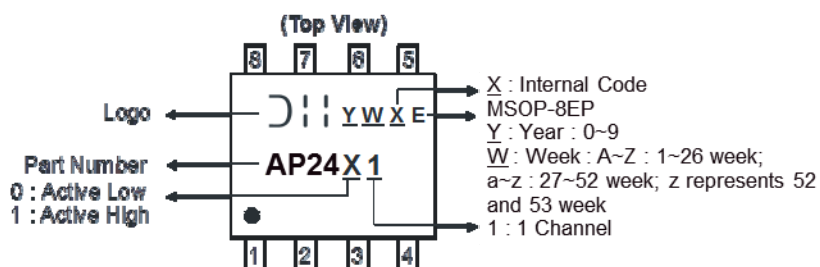


Marking Information (cont.)

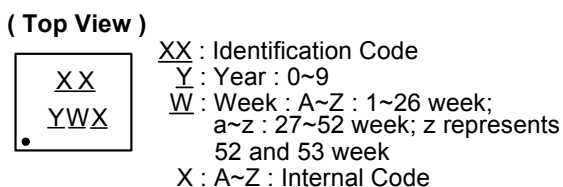
(2) MSOP-8



(3) MSOP-8EP

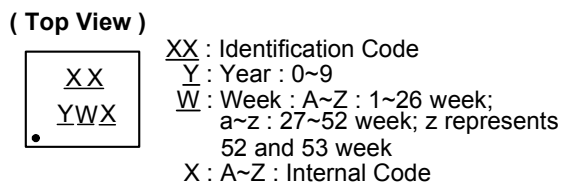


(4) U-DFN3030-8



Part Number	Package	Identification Code
AP2401FGE-7	U-DFN3030-8	BD
AP2411FGE-7	U-DFN3030-8	BF

(5) U-DFN2020-6

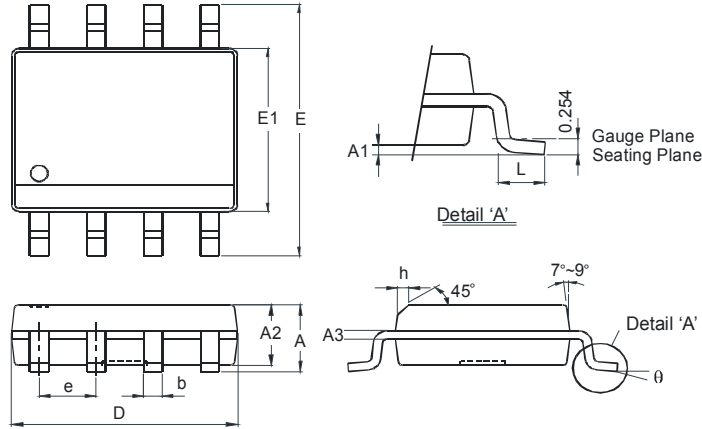


Part Number	Package	Identification Code
AP2401SN-7	U-DFN2020-6	DD
AP2411SN-7	U-DFN2020-6	DF

Package Outline Dimensions (All dimensions in mm.)

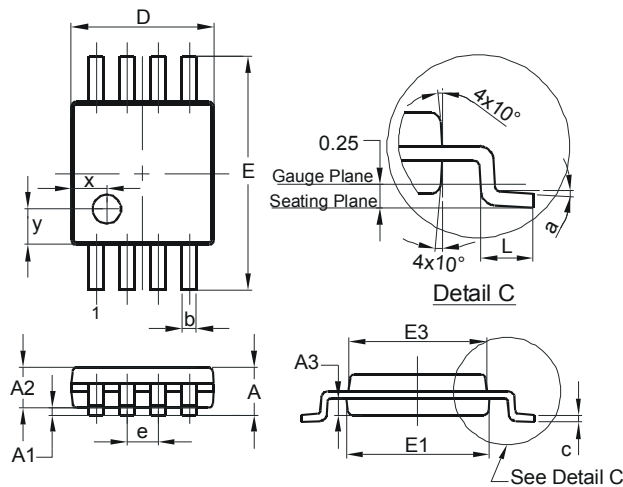
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

1. Package type: SO-8



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

2. Package type: MSOP-8

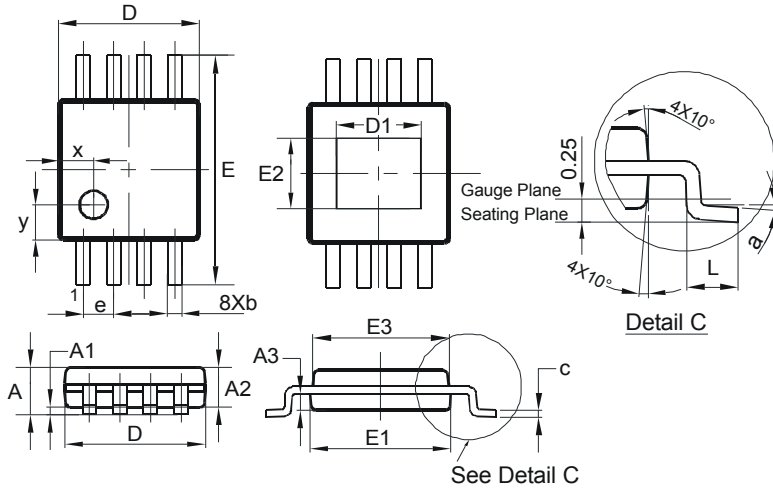


MSOP-8			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

Package Outline Dimensions (cont.) (All dimensions in mm.)

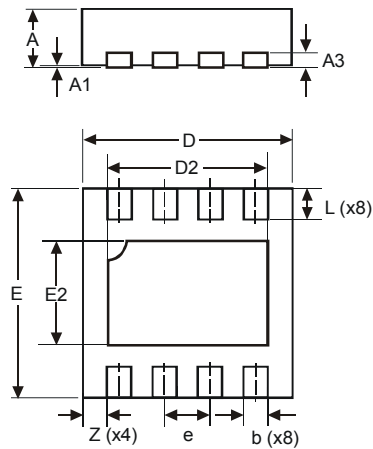
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

3. Package type: MSOP-8EP



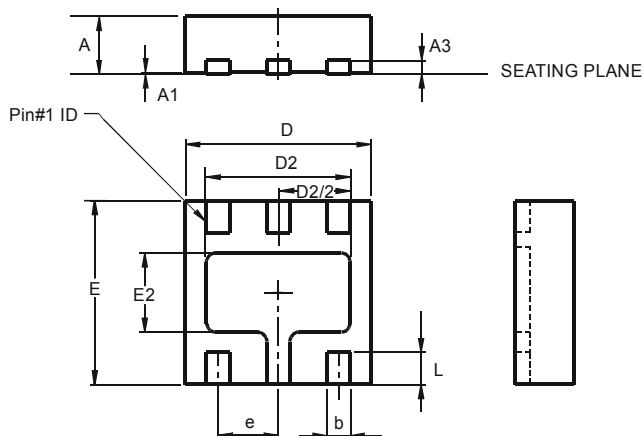
MSOP-8EP			
Dim	Min	Max	Typ
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
D1	1.60	2.00	1.80
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E2	1.30	1.70	1.50
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

4. Package type: U-DFN3030-8 Type E



U-DFN3030-8 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	2.95	3.05	3.00
D2	2.15	2.35	2.25
E	2.95	3.05	3.00
e	-	-	0.65
E2	1.40	1.60	1.50
L	0.30	0.60	0.45
Z	-	-	0.40
All Dimensions in mm			

5. Package type: U-DFN2020-6

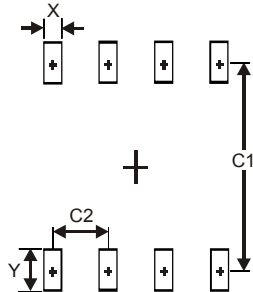


U-DFN2020-6			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	1.45	1.65	1.55
e	-	-	0.65
E	1.95	2.075	2.00
E2	0.76	0.96	0.86
L	0.30	0.40	0.35
All Dimensions in mm			

Suggested Pad Layout

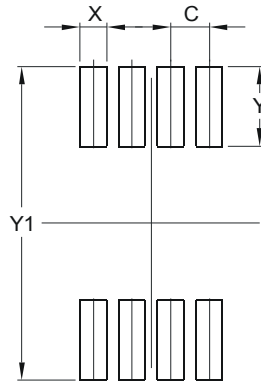
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) Package type: SO-8



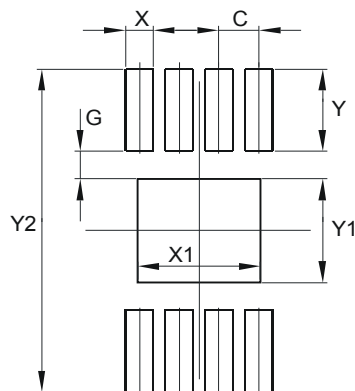
Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

(2) Package type: MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

(3) Package type: MSOP-8EP

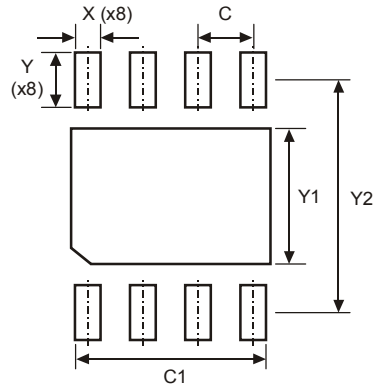


Dimensions	Value (in mm)
C	0.650
G	0.450
X	0.450
X1	2.000
Y	1.350
Y1	1.700
Y2	5.300

Suggested Pad Layout (cont.)

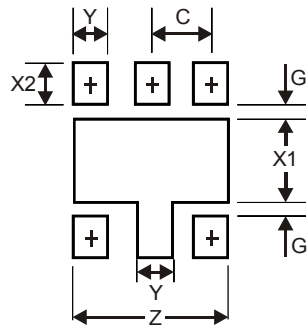
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(4) Package type: U-DFN3030-8 Type E



Dimensions	Value (in mm)
C	0.65
C1	2.35
X	0.30
Y	0.65
Y1	1.60
Y2	2.75

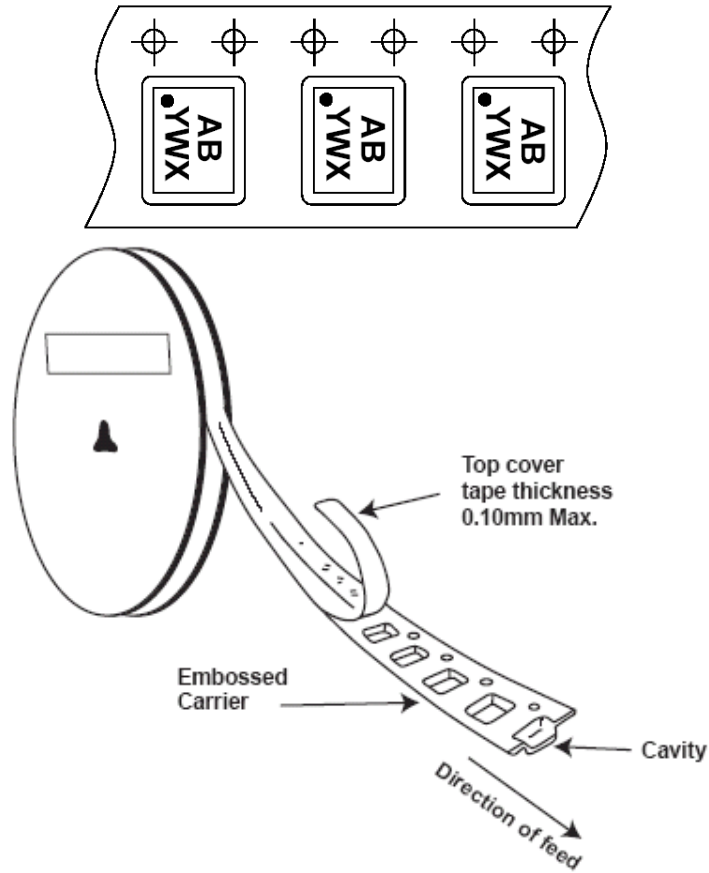
(5) Package type: U-DFN2020-6



Dimensions	Value (in mm)
Z	1.67
G	0.15
X1	0.90
X2	0.45
Y	0.37
C	0.65

Taping Orientation (Note 11)

For U-DFN2020-6 and U-DFN3030-8 Type E



Note: 11. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

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