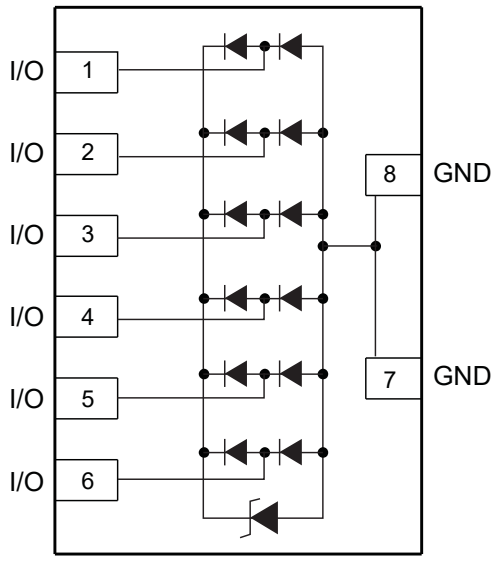
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8806DI-03	-40 °C to +85 °C	3.3 mm x 1.3 mm x 0.55 mm 8-lead	Green Product
AOZ8806DI-05			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



8-Lead Package
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	AOZ8806DI-03	AOZ8806DI-05
Storage Temperature (T_S)	-65 °C to +150 °C	
ESD Rating per IEC61000-4-2, contact(1)	±15 kV	
ESD Rating per IEC61000-4-2, air(1)	±15 kV	
ESD Rating per Human Body Model(2)	±24 kV	

Notes:

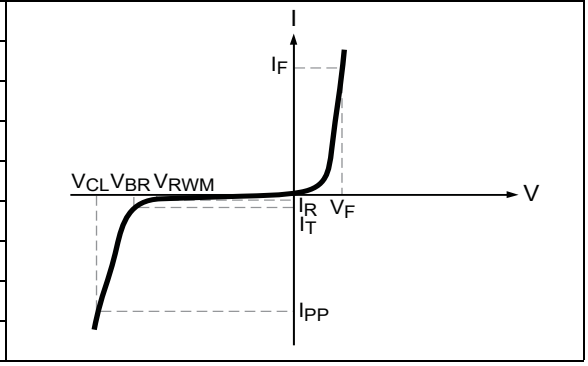
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40 °C to +125 °C

Electrical Characteristics

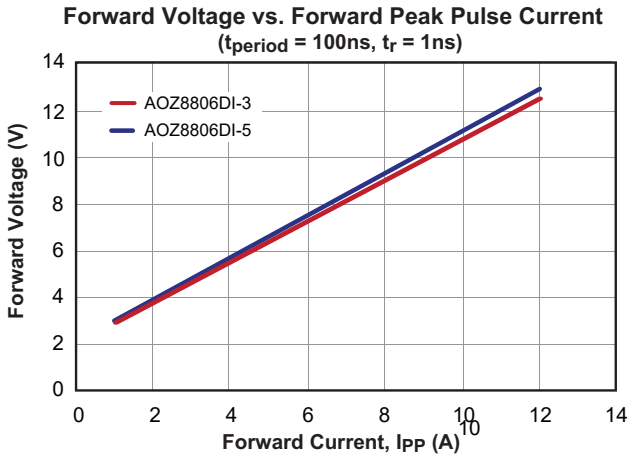
T_A = 25°C unless otherwise specified.

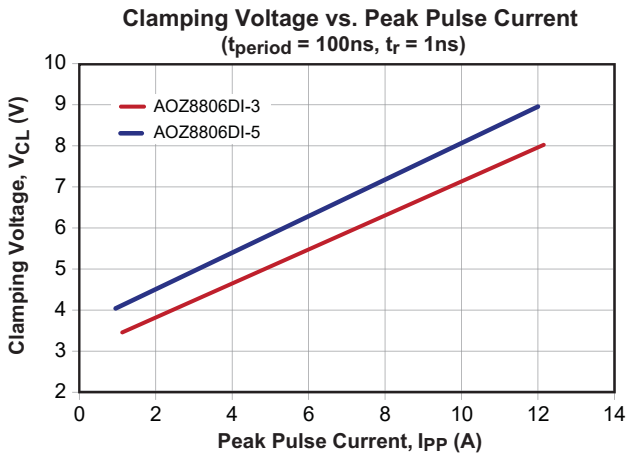
Symbol	Parameter	Diagram
I_{PP}	Maximum Reverse Peak Pulse Current	
V_{CL}	Clamping Voltage @ I_{PP} (IEC61000-4-5 8/20 µs pulse)	
V_{RWM}	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current	
V_{BR}	Breakdown Voltage	
I_T	Test Current	
V_F	Forward Voltage @ I_F	
P_{pk}	Peak Power Dissipation (IEC61000-4-5 8/20 µs pulse)	
C_J	Max. Capacitance @ V_R = 0 and f = 1 MHz	

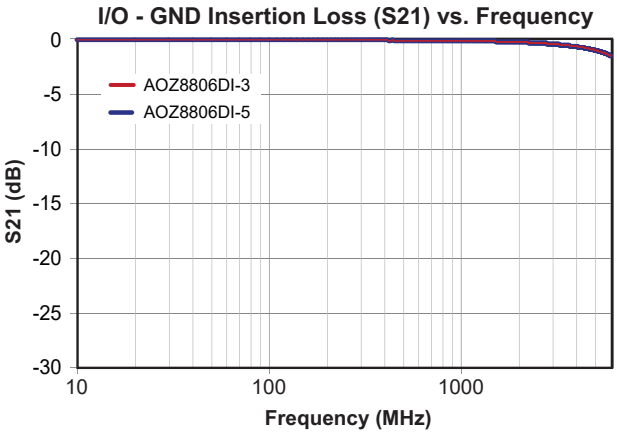
Device	Device Marking	V_{RWM} (V) Max.	V_{BR} (V) Min. I_T = 100 µA	I_R (µA) Max.	V_F (V) Typ.	V_{CL} Max.(3) I_{PP} = 4 A	P_{pk}(3)	C_J (pF) Typ.	C_J (pF) Max.
AOZ8806DI-03	AE	3.3	3.5	1.0	0.85	8.0	32	0.6	0.75
AOZ8806DI-05	AB	5.0	6.0	1.0	0.85	9.0	36	0.6	0.75

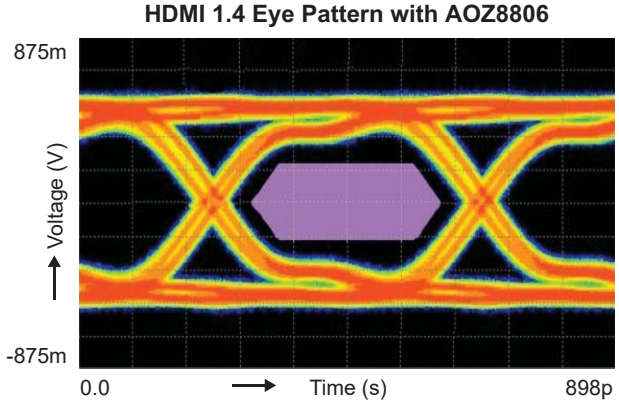
Notes:
3. These specifications are guaranteed by design and characterization.

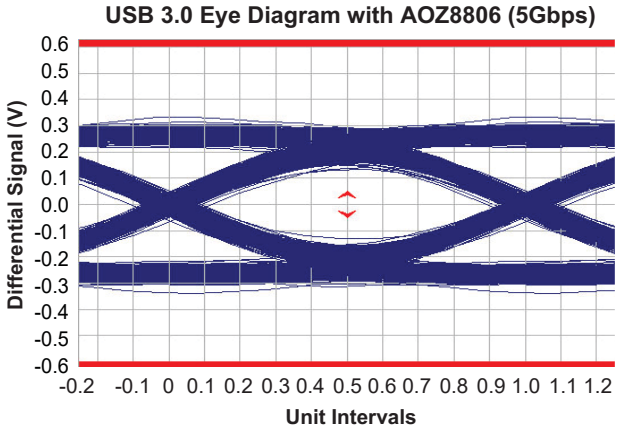
Typical Performance Characteristics

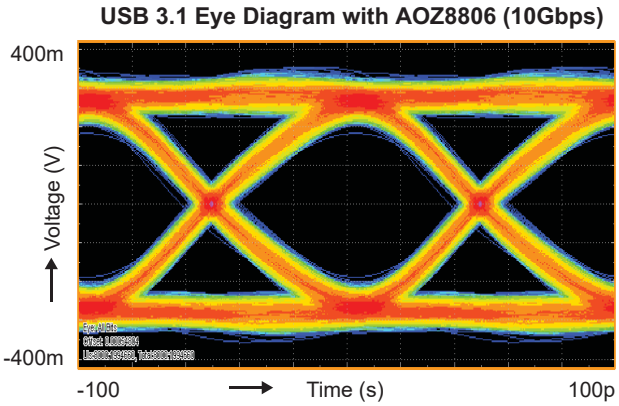












High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8806DI devices should be located as close as possible to the noise source. The AOZ8806DI device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8806DI devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8806DI device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce.

The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8806DI ultra-low capacitance TVS is designed to protect six high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8806DI is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8806DI is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI) or USB 3.0 design without having to divert the signal lines that may add more parasitic inductance.

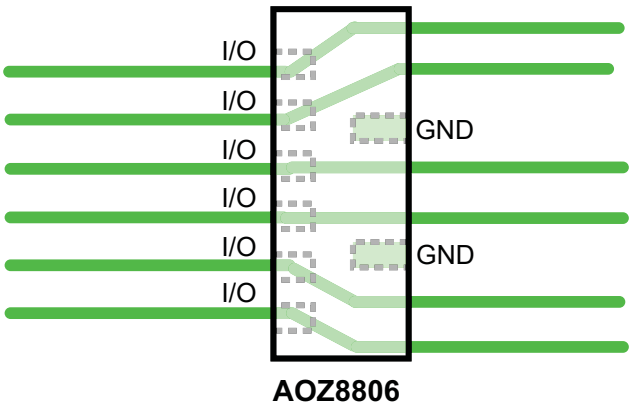


Figure 3. Layout Example

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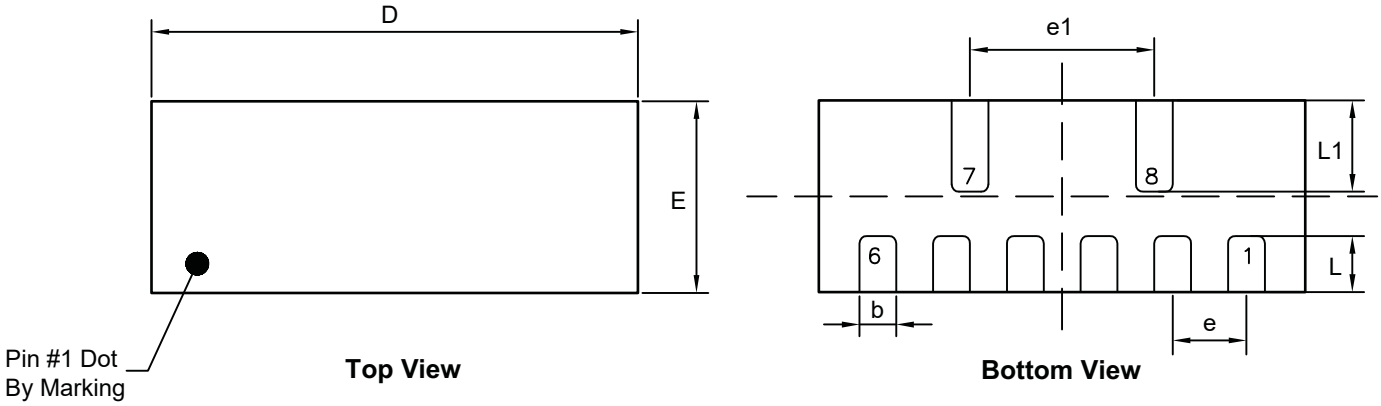
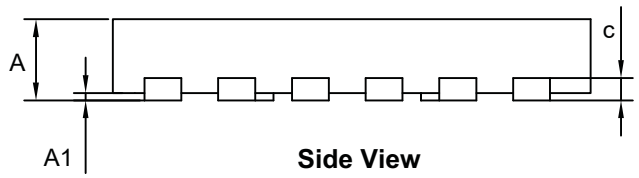
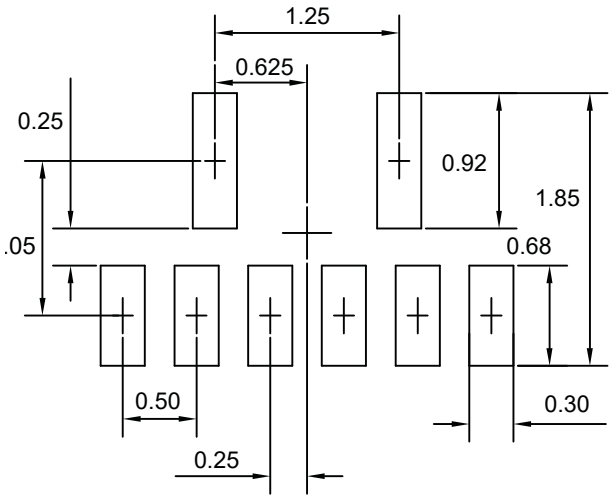
Package Dimensions, 3.3 mm x 1.3 mm x 0.55 mm, 8L





RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
C		0.152 REF	
D	3.25	3.30	3.38
E	1.25	1.30	1.38
e		0.50 BSC	
e1		1.25 BSC	
L	0.30	0.38	0.43
L1	0.54	0.62	0.67

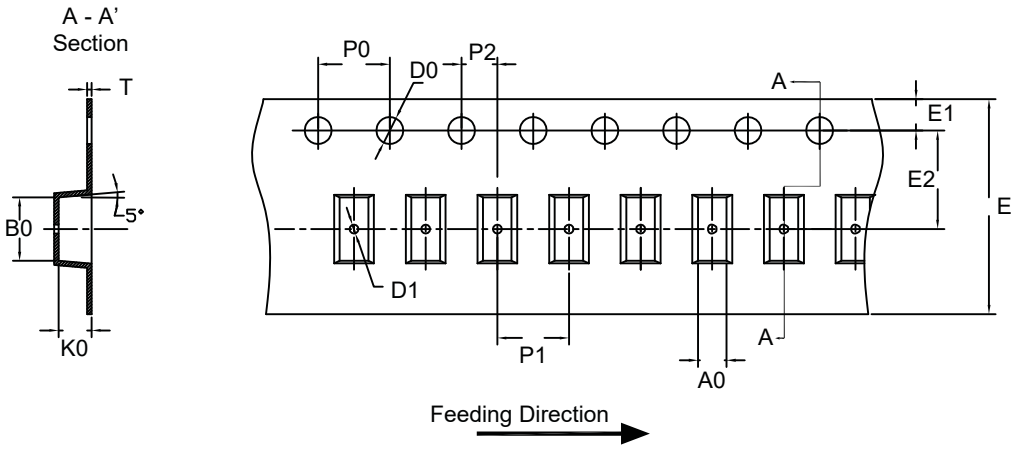
Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.025	0.022	0.024
A1	0.000	0.001	0.002
b	0.008	0.010	0.012
C		0.006 REF	
D	0.128	0.130	0.133
E	0.049	0.051	0.054
e		0.020 BSC	
e1		0.049 BSC	
L	0.012	0.015	0.017
L1	0.021	0.024	0.026

NOTE:
1. Controlling dimension is millimeters. Converted inches dimensions are not necessarily exact.

Tape and Reel Dimensions, 3.3 mm x 1.3 mm x 0.55 mm, 8L

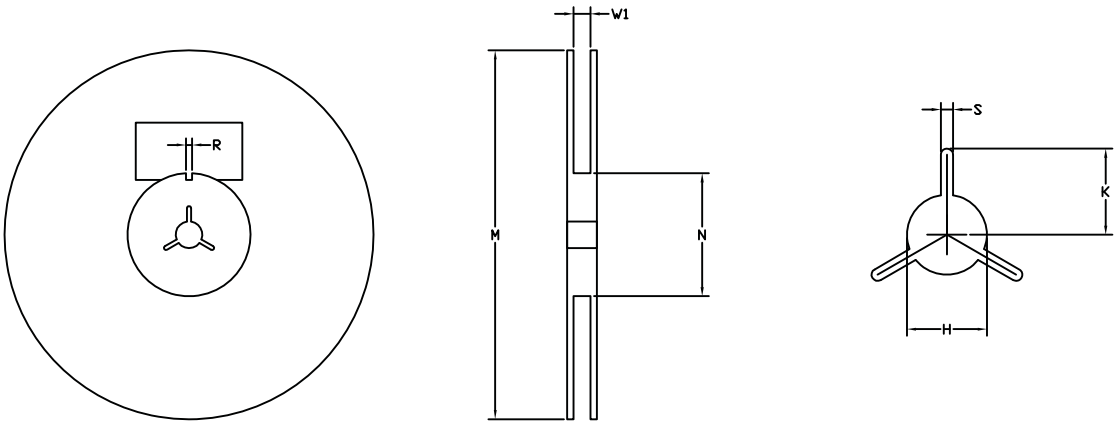
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
3.3x1.3x0.55	1.60 ±0.10	3.55 ±0.05	0.60 ±0.05	1.55 Max.	1.5 ±0.1/-0.0	12.0 ±0.30	1.75 ±0.10	5.50 ±0.10	4.0 ±0.10	4.0 ±0.10	2.0 ±0.10	0.25 ±0.05

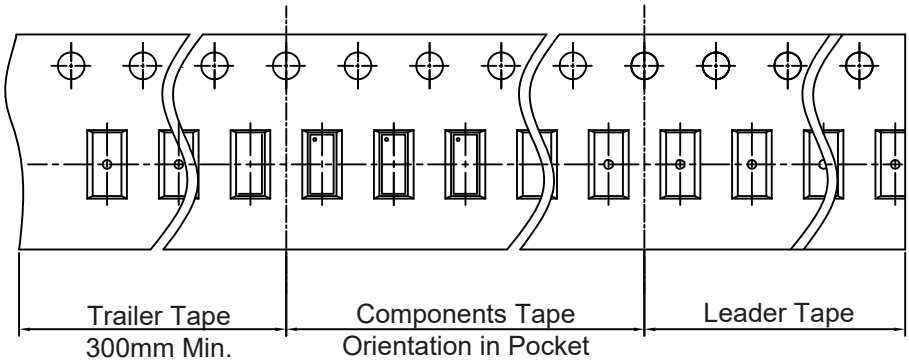
Reel



UNIT: mm

Tape Size	Reel Size	M	N	W1	H	S	K	R
12	Ø330	Ø330 ±0.3/-4.0	55.0 ±0.40	12.4 ±0.20	13.0 ±0.20	2.2 ±0.20	10.6 ±0.20	----

Leader/Trailer and Orientation



Part Marking

AOZ8806DI-03
AOZ8806DI-05
(3.3 x 1.3 x 0.55 DFN)