TABLE OF CONTENTS

REVISION HISTORY

10/09—Rev. SpA to Rev. B

Changes to Endnote 8, Table 3 7
Changes to Table 8 15
Changes to Ordering Guide 20

9/05—Rev. Sp 0 to Rev. SpA

Deleted EDTV ..... Universal
Added AVR Receiver to Applications Section 1
Changes to Table 3 7
Changes to Figure 2 10
Changes to Function Descriptions of Pin 37 and Pin 38 11
Change Pin 70 Type 11
Change to Crystal MHz Unit Value 13
Added Pixel Input Information to Table 9 and Table 10 17

4/05—Revision Sp0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

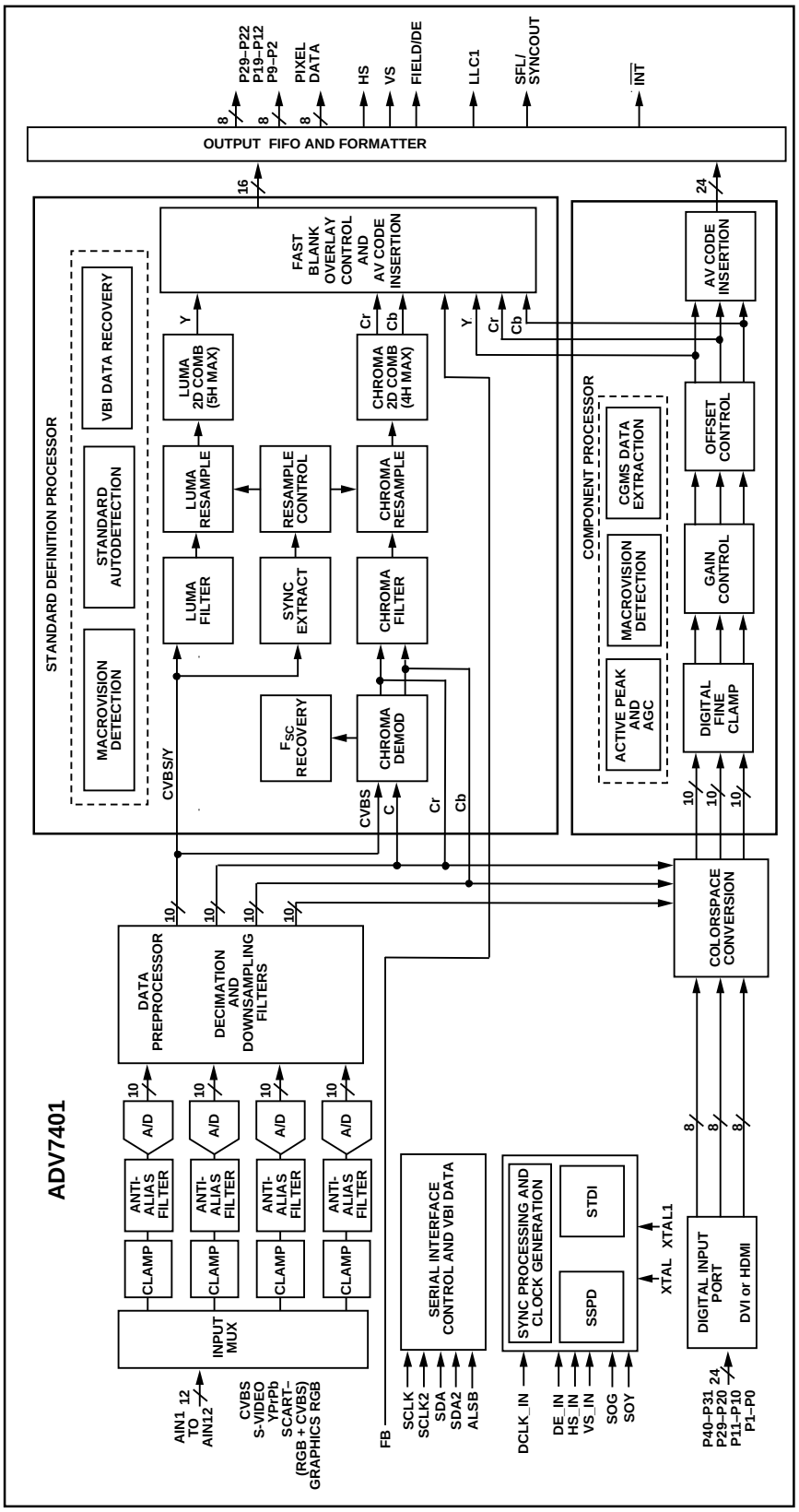


Figure. 1.

ELECTRICAL CHARACTERISTICS

@ AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V, nominal input range 1.6 V. Operating temperature range, unless otherwise noted.

Table 1.

Parameter[1, 2, 3]	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE[4, 5]						
Resolution (each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (at a 10-bit level)		±0.6	±2.5	LSB
Integral Nonlinearity	INL	BSL at 54 MHz (at a 10-bit level)		−0.6/+0.7		LSB
Integral Nonlinearity	INL	BSL at 74 MHz (at a 10-bit level)		±1.4		LSB
Integral Nonlinearity	INL	BSL at 110 MHz (at an 8-bit level)[6]		±0.9		LSB
Integral Nonlinearity	INL	BSL at 135 MHz (at an 8-bit level)[7]		±1.5		LSB
Differential Nonlinearity	DNL	At 27 MHz (at a 10-bit level)		−0.2/+0.25	−0.99/+2.5	LSB
Differential Nonlinearity	DNL	At 54 MHz (at a 10-bit level)		−0.2/+0.25		LSB
Differential Nonlinearity	DNL	At 74 MHz (at a 10-bit level)		±0.9		LSB
Differential Nonlinearity	DNL	At 110 MHz (at an 8-bit level)[6]		−0.2/+1.5		LSB
Differential Nonlinearity	DNL	At 135 MHz (at an 8-bit level)[7]		−0.9/+3.0		LSB
DIGITAL INPUTS[8]						
Input High Voltage[9]	V_{IH}		2			V
Input Low Voltage[10]	V_{IL}				0.8	V
Input High Voltage	V_{IH}	HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage	V_{IL}	HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I_{IN}	Pins listed in Note 11	−60		+60	µA
		All other input pins	−10		+10	µA
Input Capacitance[8]	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage[12]	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage[12]	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pins listed in Note 13			60	µA
		All other output pins			10	µA
Output Capacitance[8]	C_{OUT}				20	pF
POWER REQUIREMENTS[8]						
Digital Core Power Supply	DVDD		1.65	1.8	2	V
Digital I/O Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Digital Core Supply Current	IDVDD	CVBS input sampling at 54 MHz		105		mA
		Graphics RGB sampling at 135 MHz		137		mA
		SCART RGB FB sampling at 54 MHz		106		mA
Digital I/O Supply Current	IDVDDIO	CVBS input sampling at 54 MHz		4		mA
		Graphics RGB sampling at 135 MHz		19		mA
PLL Supply Current	IPVDD	CVBS input sampling at 54 MHz		11		mA
		Graphics RGB sampling at 135 MHz		12		mA
Analog Supply Current[14]	IAVDD	CVBS input sampling at 54 MHz		99		mA
		Graphics RGB sampling at 135 MHz		242		mA
		SCART RGB FB sampling at 54 MHz		269		mA
Power-Down Current	IPWRDN			2.25		mA
Green Mode Power-Down	IPWRDNG	Sync bypass function		16		mA
Power-Up Time	TPWRUP			20		ms

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C (0°C to 70°C temperature range for ADV7401KSTZ-140).

[3] All specifications obtained using programming scripts with the following sequence included: Addr 0x0E - data 0x80, Addr 0x54 - data 0x00, Addr 0x0E - data 0x00.
[4] All ADC linearity tests performed at input range of full scale – 12.5%, and at zero scale + 12.5%.
[5] Max INL and DNL specifications obtained with part configured for component video input.
[6] Specification for ADV7401BSTZ-110 and ADV7401KSTZ-140 only.
[7] Specification for ADV7401KSTZ-140 only.
[8] Guaranteed by characterization.
[9] To obtain specified V_{IH} level on Pin 38, Register 0x13 (wo) must be programmed with value 0x04. If Register 0x13 is programmed with value 0x00, then V_{IH} on Pin 38 = 1.2 V.
[10] To obtain specified V_{IL} level on Pin 38, Register 0x13 (wo) must be programmed with value 0x04. If Register 0x13 is programmed with value 0x00, then V_{IL} on Pin 38 = 0.4 V.
[11] Pins 1, 2, 13, 14, 16, 19, 24, 29, 30, 31, 32, 33, 34, 35, 45, 79, 83, 84, 87, 88, 95, 96, 97, 100.
[12] V_{OH} and V_{OL} levels obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[13] Pins 3, 13, 14, 19, 24, 29, 30, 31, 32, 33, 34, 45.
[14] Analog current measurements for CVBS made with ADC0 powered up only, For RGB, ADC0, ADC1 and ADC2 powered up only, for SCART FB, all ADCs powered up.

VIDEO SPECIFICATIONS

@ AVDD= 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted.

Table 2.

Parameter[1, 2, 3]	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulated 5 step		0.5		degree
Differential Gain	DG	CVBS input, modulated 5 step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5 step		0.5		%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
SNR Unweighted		Luma flat field	58	60		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
F_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock in Time				60		line
Sync Depth Range[4]			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		field
Horizontal Lock Time				100		line
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		degree
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		degree
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C (0°C to 70°C temperature range for ADV7401KSTZ-140).
[3] Guaranteed by characterization.
[4] Nominal sync depth is 300 mV at 100% sync depth range.

TIMING CHARACTERISTICS

@ AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC1 Frequency Range[4]			12.825		140	MHz
I²C PORT[5]						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA and CONTROL OUTPUTS						
Data Output Transition Time SDR (SDP)[6]	t_{11}	Negative clock edge to start of valid data			3.6	ns
Data Output Transition Time SDR (SDP)[6]	t_{12}	End of valid data to negative clock edge			2.4	ns
Data Output Transition Time SDR (CP)[7]	t_{13}	End of valid data to negative clock edge			2.8	ns
Data Output Transition Time SDR (CP)[7]	t_{14}	Negative clock edge to start of valid data			0.1	ns
Data Output Transition Time DDR (CP)[7, 8]	t_{15}	Positive clock edge to end of valid data	−4 + TLLC1/4			ns
Data Output Transition Time DDR (CP)[7, 8]	t_{16}	Positive clock edge to start of valid data	0.25 + TLLC1/4			ns
Data Output Transition Time DDR (CP)[7, 8]	t_{17}	Negative clock edge to end of valid data	−2.95 + TLLC1/4			ns
Data Output Transition Time DDR (CP)[7, 8]	t_{18}	Negative clock edge to start of valid data	−0.5 + TLLC1/4			ns
DATA and CONTROL INPUTS[5]						
Input Setup Time (Digital Input Port)	t_{19}	HS_IN, VS_IN	9			ns
		DE_IN, data inputs	2.2			ns
Input Hold Time (Digital Input Port)	t_{20}	HS_IN, VS_IN	7			ns
		DE_IN, data inputs	2			ns

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C (0°C to 70°C temperature range for ADV7401KSTZ-140).
[3] Guaranteed by characterization.
[4] Maximum LLC1 frequency is 80 MHz for ADV7401BSTZ-80 and is 110 MHz for ADV7401BSTZ-110.
[5] TTL input values are 0 V to 3 V, with rise/fall times ≤3 ns, measured between the 10% and 90% points.
[6] SDP timing figures obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[7] CP timing figures obtained using max drive strength value (0xFF) in register subaddress 0xF4.
[8] DDR timing specifications dependent on LLC1 output pixel clock; TLLC1/4 = 9.25 ns at LLC1 = 27 MHz.

ANALOG SPECIFICATIONS

@ AVDD = 3.1.5 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. Operating temperature range, unless otherwise noted. Recommended analog input video signal range: 0.5 V to 1.6 V, typically 1 V p-p.

Table 4.

Parameter[1, 2, 3]	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance[4]	Clamps switched off		10		MΩ
Input Impedance of Pin 51 (FB)			20		kΩ
CML			1.86		V
ADC Full-Scale Level			CML + 0.8 V		V
ADC Zero-Scale level			CML – 0.8 V		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML – 0.292 V		V
	SCART RGB input (R, G, B signals)		CML – 0.4 V		V
	S-Video input (Y signal)		CML – 0.292 V		V
	S-Video input (C signal)		CML – 0 V		V
	Component input (Y, Pr, Pb signals)		CML – 0.3 V		V
	PC RGB input (R, G, B signals)		CML – 0.3 V		V
Large Clamp Source Current	SDP only		0.75		mA
Large Clamp Sink Current	SDP only		0.9		mA
Fine Clamp Source Current	SDP only		17		µA
Fine Clamp Sink Current	SDP only		17		µA

[1] The min/max specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: –40°C to +85°C (0°C to 70°C temperature range for ADV7401KSTZ-140).
[3] Guaranteed by characterization.
[4] Except Pin 51 (FB).

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	4 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4 V
DVDDIO to AVDD	−0.3 V to +0.3 V
PVDD to DVDD	−0.3 V to +0.3 V
DVDDIO to PVDD	−0.3 V to +2 V
DVDDIO to DVDD	−0.3 V to +2 V
AVDD to PVDD	−0.3 V to +2 V
AVDD to DVDD	−0.3 V to +2 V
Digital Inputs Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage to DGND	DGND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs to AGND	AGND − 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

STRESS RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the part the user is advised to turn off any unused ADCs .

The junction temperature must always stay below the maximum junction temperature ($T_{J\ MAX}$) of 125°C. This equation shows how to calculate the junction temperature:

$$T_J = T_{A\ Max} + (\theta_{JA} \times W_{Max})$$

where:

$T_{A\ Max}$ = 85°C.

θ_{JA} = 30°C/W.

$W_{Max} = ((AVDD \times IAVDD) + (DVDD \times IDVDD) + (DVDDIO \times IDVDDIO) + (PVDD \times IPVDD))$.

THERMAL SPECIFICATIONS

Table 6.

Thermal Characteristics	Symbol	Test Conditions	Typ	Unit
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane	7	°C/W
Junction-to-Ambient Thermal Resistance	θ_{JA}	4-layer PCB with solid ground plane (still air)	30	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

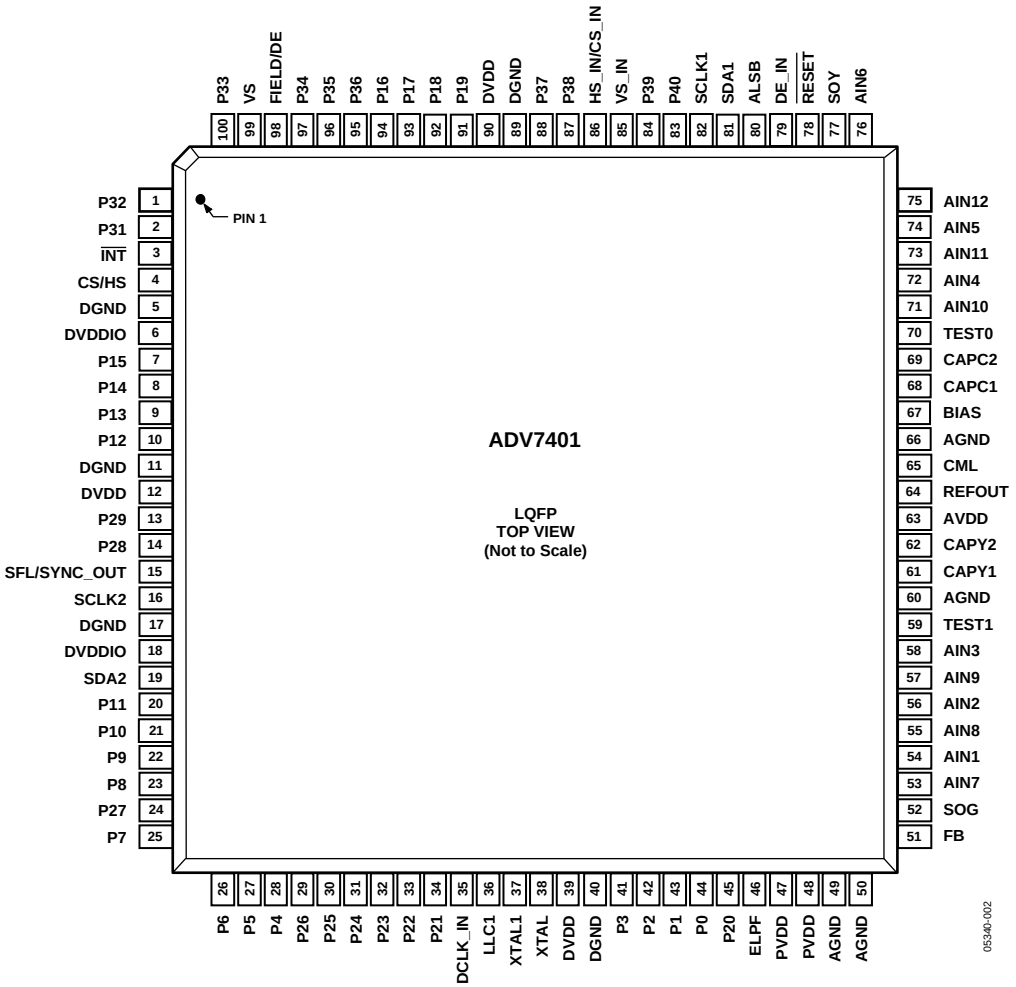


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
5, 11, 17, 40, 89	DGND	G	Digital Ground.
49, 50, 60, 66	AGND	G	Analog Ground.
6, 18	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
12, 39, 90	DVDD	P	Digital Core Supply Voltage (1.8 V).
63	AVDD	P	Analog Supply Voltage (3.3 V).
47, 48	PVDD	P	PLL Supply Voltage (1.8 V).
51	FB	I	Fast Switch Overlay Input. This pin switches between CVBS and RGB analog signals.
54, 56, 58, 72, 74, 76, 53, 55, 57, 71, 73, 75	AIN1 to AIN12	I	Analog Video Input Channels.
42, 41, 28, 27, 26, 25, 23, 22, 10, 9, 8, 7, 94, 93, 92, 91	P2 to P9, P12 to P19	O	Video Pixel Output Port.
33, 32, 31, 30, 29, 24, 14, 13	P22 to P29	I/O	Video Input/Output Port
44, 43, 21, 20, 45, 34, 2, 1, 100, 97, 96, 95, 88, 87, 84, 83	P0 to P1, P10 to P11, P20 to P21, P31 to P40	I	Video Pixel Input Port.
3	$\overline{\text{INT}}$	O	Interrupt. This pin can be active low or active high. When SDP/CP status bits change this pin triggers. The set of events that triggers an interrupt is under user control.

Pin No.	Mnemonic	Type	Function
4	HS/CS	O	HS is a Horizontal Synchronization Output Signal (SDP and CP modes). CS is a Digital Composite Synchronization Signal (and can be selected while in CP mode).
99	VS	O	Vertical Synchronization Output Signal (SDP and CP modes).
98	FIELD/DE	O	Field Synchronization Output Signal (all interlaced video modes). This pin also can be enabled as a Data Enable signal (DE) in CP mode to allow direct connection to a HDMI/DVI Tx IC.
81, 19	SDA1, SDA2	I/O	I^2C Port Serial Data Input/Output Pins. SDA1 is the data line for the control port and SDA2 is the data line for the VBI readback port.
82, 16	SCLK1, SCLK2	I	I^2C Port Serial Clock Input (max clock rate of 400 kHz). SCLK1 is the clock line for the control port and SCLK2 is the clock line for the VBI data readback port.
80	ALSB	I	This pin selects the I^2C address for the ADV7401 control and VBI readback ports. ALSB set to Logic 0 sets the address for a write to control port of 0x40 and the readback address for the VBI port of 0x21. ALSB set to a logic high sets the address for a write to control port of 0x42 and the readback address for the VBI port of 0x23.
78	$\overline{\text{RESET}}$	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7401 circuitry.
36	LLC1	O	LLC1 is a line-locked output clock for the pixel data (range is 12.825 MHz to 140 MHz for ADV7401KSTZ-140; 12.825 MHz to 110 MHz for ADV7401BSTZ-110; 12.825 MHz to 80 MHz for ADV7401BSTZ-80).
38	XTAL	I	Input pin for 28.63636 MHz crystal, or can be overdriven by an external 3.3 V 28.63636 MHz clock oscillator source to clock the ADV7401.
37	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V 28.63636 MHz clock oscillator source is used to clock the ADV7401. In crystal mode, the crystal must be a fundamental crystal.
46	ELPF	O	The recommend external loop filter must be connected to this ELPF pin.
70	TEST0	NC	This pin should be left unconnected or alternatively tied to AGND.
59	TEST1	O	This pin should be left unconnected.
15	SFL/SYNC_OUT	O	Subcarrier Frequency Lock (SFL). This pin contains a serial output stream which can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT is the sliced sync output signal available only in CP mode.
64	REFOUT	O	Internal Voltage Reference Output.
65	CML	O	Common-Mode Level Pin (CML) for the internal ADCs.
61, 62	CAPY1, CAPY2	I	ADC Capacitor Network.
68, 69	CAPC1, CAPC2	I	ADC Capacitor Network.
67	BIAS	O	External Bias Setting Pin. Connect the recommended resistor (1.35 kΩ) between pin and ground.
86	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
85	VS_IN	I	VS Input Signal. Used in CP mode for 5-wire timing mode.
79	DE_IN	I	Data Enable Input Signal. Used in 24-bit digital input port mode (for example, processing 24-bit RGB data from a DVI Rx IC).
35	DCLK_IN	I	Clock Input Signal. Used in 24-bit digital input mode (for example, processing 24-bit RGB data from a DVI Rx IC) and also in digital CVBS input mode.
52	SOG	I	Sync on Green Input. Used in embedded sync mode.
77	SOY	I	Sync on Luma Input. Used in embedded sync mode.

TIMING DIAGRAMS

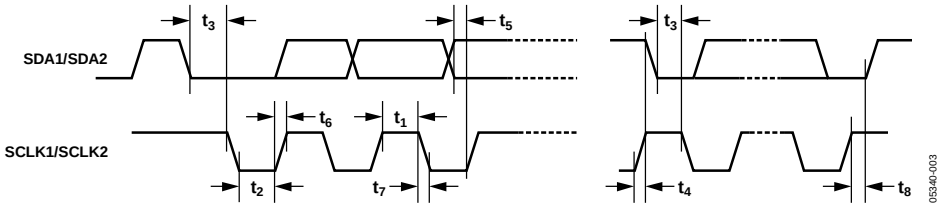


Figure 3. I²C Timing

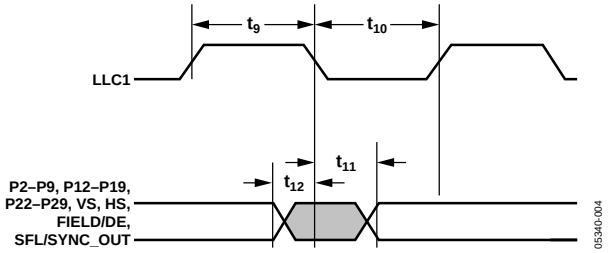


Figure 4. Pixel Port and Control SDR Output Timing (SD Core)

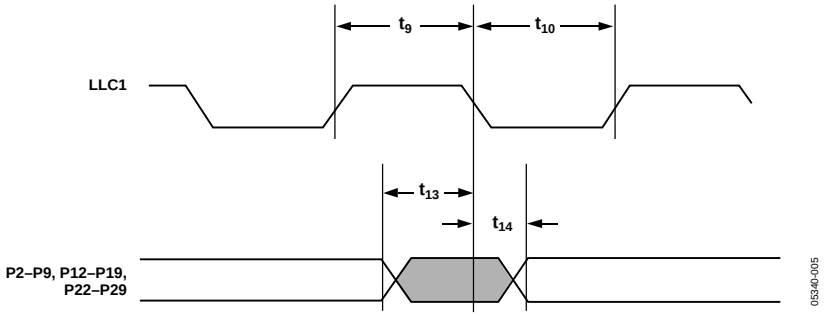


Figure 5. Pixel Port and Control SDR Output Timing (CP Core)

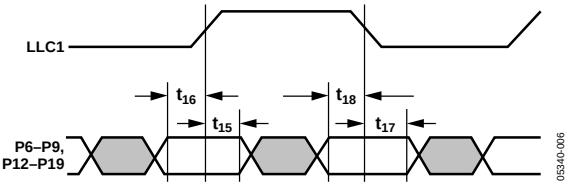


Figure 6. Pixel Port and Control DDR Output Timing (CP Core)

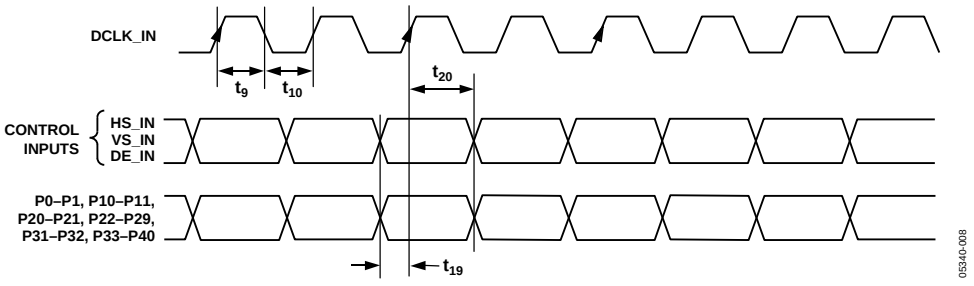


Figure 7. Digital Input Port and Control Input Timing

DETAILED FUNCTIONALITY

ANALOG FRONT END

- Four high quality 10-bit ADCs enable true 8-bit video decoder
- 12 analog input channel mux enables multisource connection without the requirement of an external mux
- Four current and voltage clamp control loops ensure any dc offsets are removed from the video signal
- SCART functionality and SD RGB overlay on CVBS controlled by fast blank input
- Four internal antialias filters to remove out-of-band noise on standard definition input video signals

SDP PIXEL DATA OUTPUT MODES

- 8-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD
- 16-bit YCrCb with embedded time codes and/or HS, VS, and FIELD
- 24-bit YCrCb with embedded time codes and/or HS, VS, and FIELD

CP PIXEL DATA OUTPUT MODES

- Single data rate (SDR) 8-bit 4:2:2 YCrCb for 525i, 625i
- Single data rate (SDR) 16-bit 4:2:2 YCrCb for all standards
- Single data rate (SDR) 24-bit 4:4:4 YCrCb/RGB for all standards
- Double data rate (DDR) 8-bit 4:2:2 YCrCb for all standards
- Double data rate (DDR) 12-bit 4:4:4 YCrCb/RGB for all standards

COMPOSITE AND S-VIDEO PROCESSING

- Support for NTSC (J, M, 4.43), PAL (B, D, I, G, H, M, N, 60) and SECAM B/D/G/K/L standards in the form of CVBS and S-video
- Superadaptive 2D 5-line comb filters for NTSC and PAL give superior chrominance and luminance separation for composite video
- Full automatic detection and autoswitching of all worldwide standards (PAL/NTSC/SECAM)
- Automatic gain control with white peak mode ensures the video is always processed without loss of the video processing range
- Adaptive digital line length tracking (ADLLT™)
- Proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block compensates for high frequency luma attenuation due to tuner SAW filter
- Chroma transient improvement (CTI)
- Luminance digital noise reduction (DNR)
- Color controls include hue, brightness, saturation, contrast, and Cr and Cb offset controls
- Certified Macrovision copy protection detection on composite and S-video for all worldwide formats (PAL/NTSC/SECAM)
- 4× oversampling (54 MHz) for CVBS, S-video, and YUV modes
- Line-locked clock output (LLC)
- Letterbox detection supported
- Free-run output mode provides stable timing when no video input is present
- Vertical blanking interval data processor

  TeleText
  Video Programming System (VPS)
  Vertical Interval Time Codes (VITC)
  Closed captioning (CC) and extended data service (EDS)
  Wide screen signaling (WSS)
  Copy generation management system (CGMS)
  Gemstar™ 1×/2× electronic program guide compatible
- Clocked from a single 28.63636 MHz crystal
- Subcarrier frequency lock (SFL) output for downstream video encoder
- Differential gain typically 0.5%
- Differential phase typically 0.5°

COMPONENT VIDEO PROCESSING

- Formats supported include 525i, 625i, 525p, 625p, 720p, 1080i, and many other HDTV formats
- Automatic adjustments include gain (contrast) and offset (brightness); manual adjustment controls are also supported
- Support for analog component YPrPb/RGB video formats with embedded sync or with separate HS, VS, or CS
- Any-to-any, 3 × 3 color space conversion matrix supports YCrCb-to-RGB and RGB-to-YCrCb
- Standard identification (STDI) enables system level component format detection
- Synchronization source polarity detector (SSPD) determines the source and polarity of the synchronization signals that accompany the input video
- Certified Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free-run output mode provides stable timing when no video input is present
- Arbitrary pixel sampling support for nonstandard video sources

RGB GRAPHICS PROCESSING

- 140 MSPS conversion rate supports RGB input resolutions up to 1280 × 1024 @ 75 Hz (SXGA)**;** (110 MSPS conversion rate for ADV7401BSTZ-110); (80 MSPS conversion rate for ADV7401BSTZ-80)
- Automatic or manual clamp and gain controls for graphics modes
- Contrast and brightness controls
- 32-phase DLL allows optimum pixel clock sampling
- Automatic detection of sync source and polarity by SSPD block
- Standard identification is enabled by STDI block
- RGB can be color space converted to YCrCb and decimated to a 4:2:2 format for video centric backend IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI/DVI Tx IC
- Arbitrary pixel sampling support for nonstandard video sources

DIGITAL VIDEO INPUT PORT

- Supports raw 8-bit CVBS data from digital tuner
- Support for 24-bit RGB input data from DVI Rx chip, output converted to YCrCb 4:2:2
- Support for 24-bit 4:4:4, 16-bit 4:2:2 525i, 625i, 525p, 625p, 1080i, 720p, VGA to SXGA @ 60 Hz input data from HDMI Rx chip, output converted to 16-bit 4:2:2 YCrCb

GENERAL FEATURES

- HS, VS, and FIELD output signals with programmable position, polarity, and width
- Programmable interrupt request output pin, $\overline{\text{INT}}$, signals SDP/CP status changes
- Supports two I^2C host port interfaces (control and VBI)
- Low power consumption: 1.8 V digital core, 3.3 V analog and digital I/O, low power power-down mode, and green PC mode
- Industrial temperature range (−40°C to +85°C) (except ADV7401KSTZ-140)
- 140 MHz speed grade (ADV7401KST-140)
- 100-lead, 14 mm × 14 mm, Pb-free LQFP

DETAILED DESCRIPTION

ANALOG FRONT END

The ADV7401 analog front end comprises four 10-bit ADCs that digitize the analog video signal before applying it to the SDP or CP (see Table 8 for sampling rates). The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7401. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in either the CP or SDP.

Optional antialiasing filters are positioned in front of each ADC. These filters can be used to band-limit standard definition video signals, removing spurious, out-of-band noise.

The ADCs are configured to run in 4× oversampling mode when decoding composite and S-video inputs; 2× oversampling is performed for component 525i, 625i, 525p, and 625p sources. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external anti-aliasing filters with the benefit of an increased signal-to-noise ratio (SNR).

The ADV7401 can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed and output under control of I^2C registers and the fast blank pin.

Table 8. Maximum ADC Sampling Rates

Model	Maximum ADC Sampling Rate
ADV7401BSTZ-80	80 MHz
ADV7401BSTZ-110	110 MHz
ADV7401WBSTZ-110	110 MHz
ADV7401KSTZ-140	140 MHz

STANDARD DEFINITION PROCESSOR (SDP)

The SDP section is capable of decoding a large selection of baseband video signals in composite S-video and YUV formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7401 can automatically detect the video standard and process it accordingly.

The SDP has a 5-line superadaptive 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required.

The SDP has an IF filter block that compensates for attenuation in the high frequency luma spectrum due to tuner SAW filter.

The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The ADV7401 implements a patented adaptive-digital-line-length-tracking (ADLLT) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7401 to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The SDP also contains a chroma transient improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP can process a variety of VBI data services, such as TeleText, closed captioning (CC), wide screen signaling (WSS), video programming system (VPS), vertical interval time codes (VITC), copy generation management system (CGMS), Gemstar 1×/2×, and extended data service (XDS). The ADV7401 SDP section has a Macrovision 7.1 detection circuit that allows it to detect Types I, II, and III protection levels. The decoder is also fully robust to all Macrovision signal inputs.

COMPONENT PROCESSOR

The CP section is capable of decoding/digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, 1250i, VGA up to SXGA @ 75 Hz (ADV7401KSTZ-140 only), and many other standards not listed here.

The CP section of the ADV7401 contains an AGC block. When no embedded sync is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit that ensures the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fully programmable, any-to-any, 3 × 3 color space conversion matrix is placed between the analog front end and the CP section. This enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The output section of the CP is highly flexible. It can be configured in single data rate mode (SDR) with one data packet per clock cycle or in a double data rate (DDR) mode where data is presented on the rising and falling edges of the clock. In SDR mode, a 16-bit 4:2:2 or 24-bit 4:4:4 output is possible. In these modes HS, VS, and FIELD/DE (where applicable) timing reference signals are provided. In DDR mode, the ADV7401 can be configured in an 8-bit 4:2:2 YCrCb or 12-bit 4:4:4 RGB/ YCrCb pixel output interface with corresponding timing signals.

The ADV7401 is capable of supporting an external DVI/ HDMI receiver. The digital interface expects 24-bit 4:4:4 or 16-bit 4:2:2 bit data (either graphics RGB or component video YCrCb), accompanied by HS, VS, DE, and a fully synchronous clock signal. The data is processed in the CP and output as 16-bit 4:2:2 YCrCb data.

The CP section contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of CGMS data is performed by the CP section of the ADV7401 for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface. For more detailed product information about the ADV7401, contact your local ADI sales office or email video.products@analog.com.

PIXEL INPUT/OUTPUT FORMATTING

Table 9. SDP, CP Pixel Input/Output Pin Map (P19 to P0)

Processor, Format, and Mode		Pixel Port Pins P[19:0]																			
		19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDP	Video out, 8-bit, 4:2:2	YCrCb[7:0]$_{OUT}$								-	-	-	-	-	-	-	-	-	-	-	-
SDP	Video out, 16-bit, 4:2:2	Y[7:0]$_{OUT}$								-	-	CrCb[7:0]$_{OUT}$								-	-
SDP	Video out, 24-bit, 4:4:4	Y[7:0]$_{OUT}$								-	-	Cb[7:0]$_{OUT}$								-	-
SM-SDP	Digital tuner input[1]	Output choices are the same as video out 16-bit or pseudo 8-bit DDR																			
CP	8-bit, 4:2:2, DDR	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	-	-	-	-	-	-	-	-
CP	12-bit, 4:4:4, RGB DDR	D7	D6	D5	D4	D3	D2	D1	D0	-	-	D11	D10	D9	D8	-	-	-	-	-	-
CP	Video out, 16-bit, 4:2:2	CHA[7:0]$_{OUT}$ (for example, Y[7:0])								-	-	CHB/C[7:0]$_{OUT}$ (for example, Cr/Cb[7:0])								-	-
CP	Video out, 24-bit, 4:4:4	CHA[7:0]$_{OUT}$ (for example, G[7:0])								-	-	CHB[7:0]$_{OUT}$ (for example, B[7:0])								-	-
SM-CP	HDMI receiver support, 24-bit, 4:4:4 input	CHA[7:0]$_{OUT}$ (for example, Y[7:0])								R[5:4]$_{IN}$		CHB/C[7:0]$_{OUT}$ (for example, Cr/Cb[7:0])								R[1:0]$_{IN}$	
SM-CP	HDMI receiver support, 16-bit, pass-through	CHA[7:0]$_{OUT}$ (for example, Y[7:0])								-	-	CHB/C[7:0]$_{OUT}$ (for example, Cr/Cb[7:0])								-	-

Table 10. SDP, CP Pixel Input/Output Pin Map (P40 to P20)

Processor, Format, and Mode		Pixel Port Pins P[40:31], P[29:20]																			
		40	39	38	37	36	35	34	33	32	31	29	28	27	26	25	24	23	22	21	20
SDP	Video out, 8-bit, 4:2:2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SDP	Video out, 16-bit, 4:2:2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SDP	Video out, 24-bit, 4:4:4	-	-	-	-	-	-	-	-	-	-	Cr[7:0]$_{OUT}$								-	-
SM-SDP	Digital tuner input[1]	DCVBS[7:0]$_{IN}$								-	-	-	-	-	-	-	-	-	-	-	-
CP	8-bit, 4:2:2, DDR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CP	12-bit, 4:4:4, RGB DDR	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CP	Video out, 16-bit, 4:2:2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CP	Video out, 24-bit, 4:4:4 input	-	-	-	-	-	-	-	-	-	-	CHC[7:0]$_{OUT}$ (for example, R[7:0])								-	-
SM-CP	HDMI receiver support, 24-bit, 4:4:4 input	G[7:0]$_{IN}$								R[7:6]$_{IN}$		B[7:0]$_{IN}$								R[3:2]$_{IN}$	
SM-CP	HDMI receiver support, 16-bit, pass-through	CHA[7:0]$_{IN}$								-	-	CHB/C[7:0]$_{IN}$								-	-

RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

The external loop filter components for the ELPF pin should be placed as close as possible to the respective pins. Figure 8 shows the recommended component values.

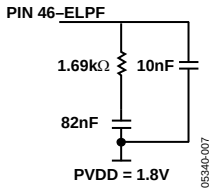


Figure 8. ELPF Components

TYPICAL CONNECTION DIAGRAM

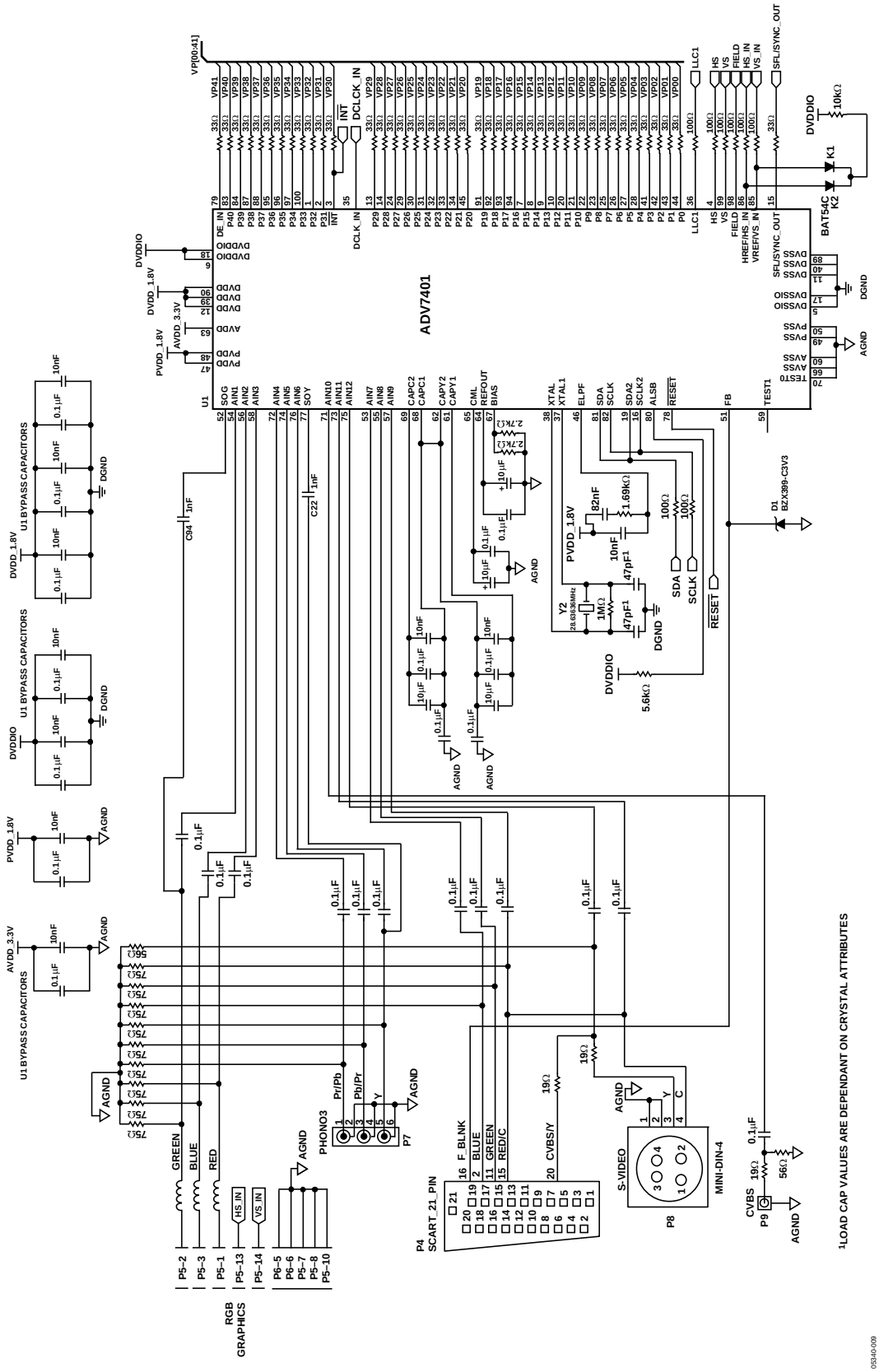
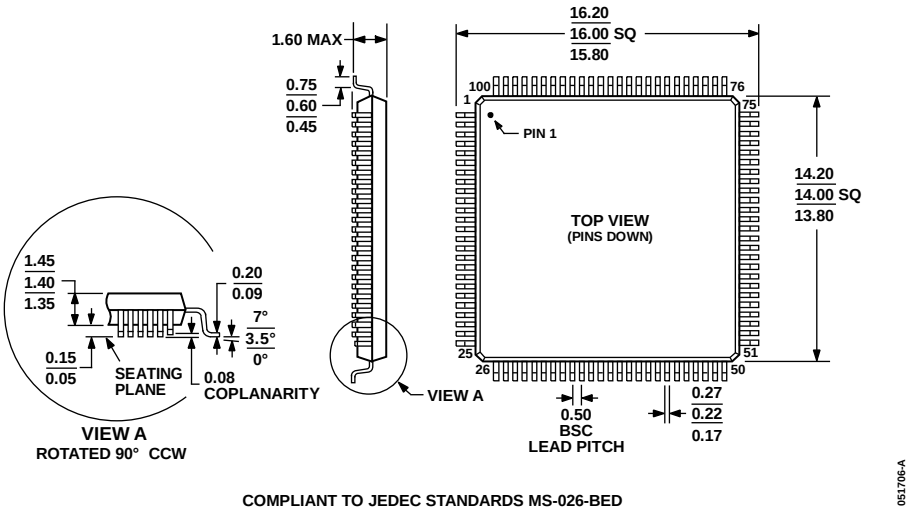


Figure 9. ADV7401

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 10. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV7401BSTZ-80[2]	−40°C to +85°C	100-Lead Low Profile Quad Flat Package (LQFP)	ST-100-1
ADV7401BSTZ-110[2]	−40°C to +85°C	100-Lead Low Profile Quad Flat Package (LQFP)	ST-100-1
ADV7401WBSTZ-110[2, 3]	−40°C to +85°C	100-Lead Low Profile Quad Flat Package (LQFP)	ST-100-1
ADV7401KSTZ-140[2]	0°C to 70°C	100-Lead Low Profile Quad Flat Package (LQFP)	ST-100-1
EVAL-ADV7401EBZ[2]		Evaluation Board	

[1] The ADV7401 is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and is able to withstand surface-mount soldering at up to 255°C (±5°C). In addition, it is backward compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with SnPb solder pastes at conventional reflow temperatures of 220°C to 235°C.
[2] Z = RoHS Compliant Part.
[3] Automotive Product.

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

D05340-0-10/09(B)