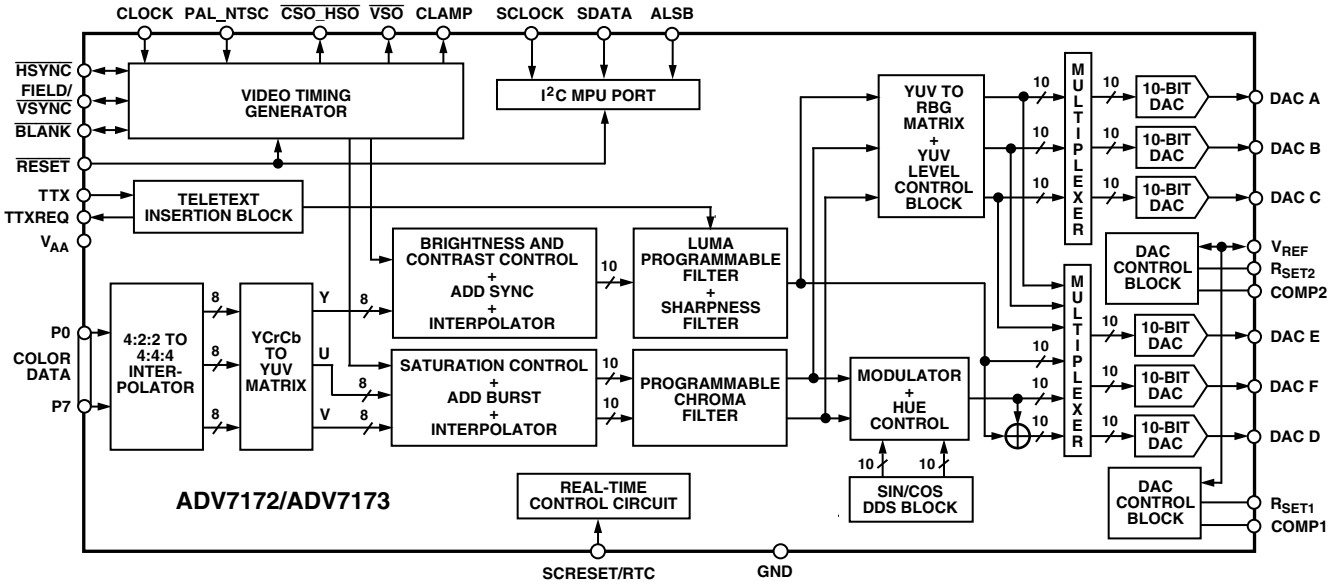
FUNCTIONAL BLOCK DIAGRAM



The ADV7172/ADV7173 is designed with four color controls (hue, contrast, brightness and saturation). All YUV formats (SMPTE/EBU N10, MII and Betacam) are supported in both PAL and NTSC.

The output video frames are synchronized with the incoming data Timing Reference Codes. Optionally the encoder accepts (and can generate) $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD timing signals. These timing signals can be adjusted to change pulsewidth and position while the part is in the master mode. The Encoder requires a single two times pixel rate (27 MHz) clock for standard operation. Alternatively the Encoder requires a 24.5454 MHz clock for NTSC or 29.5 MHz clock for PAL square pixel mode operation. All internal timing is generated on-chip.

HSO/CSO and VSO TTL outputs, synchronous to the analog output video, are also available. A programmable CLAMP output signal is also available to enable clamping in either the front or back porch of the video signal.

A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV7172/ADV7173 modes are set up over a 2-wire serial bidirectional port (I^2C-Compatible) with two slave addresses. Functionally the ADV7173 and ADV7172 are the same with the exception that the ADV7172 can output the Macrovision anti-copy algorithm.

The ADV7172/ADV7173 is packaged in a 48-lead LQFP package (1.4 mm thickness).

DATA PATH DESCRIPTION

For PAL B, D, G, H, I, M, N, and NTSC M, N modes, YCrCb 4:2:2 Data is input via the CCIR-656-Compatible Pixel Port at a 27 MHz Data Rate. The Pixel Data is demultiplexed to form three data paths. Y typically has a range of 16 to 235, Cr, and Cb typically have a range of 128 ± 112; however, it is possible to input data from 1 to 254 on both Y, Cb, and Cr. The ADV7172/ADV7173 supports PAL (B, D, G, H, I, N, M) and NTSC (with and without pedestal) standards. The Y data is then manipulated by being scaled for contrast control and a setup level is added for brightness control. The Cr, Cb data is also scaled and saturation control is added. The appropriate Sync, Blank and Burst levels are then added to the YCrCb data. Macrovision AntiTaping (ADV7172 only), Closed-Captioning and Teletext levels are also added to Y, and the resultant data is interpolated to a rate of 27 MHz. The interpolated data is filtered and scaled by three digital FIR Filters.

The U and V Signals are modulated by the appropriate subcarrier sine/cosine phases and a phase offset may be added onto the color subcarrier during active video to allow hue adjustment. The resulting U and V signals are then added together to make up the chrominance signal. The luma (Y) signal can be delayed 1–3 luma cycles (each cycle is 74 ns) with respect to the chroma signal. The luma and chroma signals are then added together to make up the composite video signal. All edges are slew rate limited.

The YCrCb data is also used to generate RGB data with appropriate Sync and Blank levels.

There are six DACs on the ADV7172/ADV7173. Three of these DACs are capable of providing 34.66 mA of current. The other three DACs provide 8.66 mA each.

The six l0-bit DACs can be used to output:

1. Composite Video + RGB Video + LUMA + CHROMA.
2. Composite Video + YUV Video + LUMA + CHROMA.

Alternatively, each DAC can be individually powered off if not required. A complete description of DAC output configurations is given in Appendix 8.

Video output levels are illustrated in Appendix 6.

SPECIFICATIONS

5 V SPECIFICATIONS (V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Test Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity[3]				±1.0	LSB
Differential Nonlinearity[3]	Guaranteed Monotonic			±1.0	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current (DACs A, B, C)[4]	R_{SET1} = 150 Ω, R_L = 37.5 Ω	33	34.7	37	mA
Output Current (DACs A, B, C)[5]	R_{SET1} = 1041 Ω, R_L = 262.5 Ω		5		mA
Output Current (DACs D, E, F)[6]	R_{SET2} = 600 Ω, R_L = 150 Ω	8.25	8.66	9.25	mA
Output Current (DACs D, E, F)[5]	R_{SET2} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching (DACs A, B, C)[7]			1	4.0	%
DAC-to-DAC Matching (DACs D, E, F)[7]			1	4.0	%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.112	1.235	1.359	V
POWER REQUIREMENTS					
V_{AA}		4.75	5.0	5.25	V
Normal Power Mode					
I_{DAC} (max)[8, 9]	$R_{SET1,2}$ = 600 Ω		59	65	mA
I_{DAC} (min)[8, 9]	$R_{SET1,2}$ = 1041 Ω		30		mA
I_{CCT}[10]			78	90	mA
Low Power Mode					
I_{DAC} (max)[11]	R_{SET1} = 150 Ω		64		mA
I_{DAC} (min)[11]			15		mA
I_{CCT}[10]			78	90	mA
Sleep Mode					
I_{DAC}[12]			0.1		μA
I_{CCT}[13]			0.1		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01	0.5	%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Characterized by design.

[4]Full drive into 75 Ω doubly terminated load.

[5]Minimum drive current (used with buffered/scaled output load).

[6]Full drive into 150 Ω load.

[7]Specification guaranteed by characterization.

[8]I_{DAC} is the total current (*"min" corresponds to 5 mA output per DAC, "max" corresponds to 8.66 mA output per DAC*) to drive DACs A, B, C, D, E, F. Turning off individual DACs reduces I_{DAC} correspondingly, also DACs A, B, C can be configured to output a max current of 37 mA but DAC D, E, F must be turned off.

[9]All six DACs on (DAC A, B, C, D, E, F).

[10]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[11]Only large DACs (DACs A, B, C) on per low power mode.

[12]Total DAC current in Sleep Mode.

[13]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

ADV7172/ADV7173–SPECIFICATIONS

3.3 V SPECIFICATIONS (V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Test Conditions[1]	Min	Typ	Max	Unit
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				1.0	LSB
Differential Nonlinearity	Guaranteed Monotonic			1.0	LSB
DIGITAL INPUTS[3]					
Input High Voltage, V_{INH}			2		V
Input Low Voltage, V_{INL}			0.8		V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[3]					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA		2.4		V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA		0.4		V
Three-State Leakage Current				10	μA
Three-State Output Capacitance			10		pF
ANALOG OUTPUTS[3]					
Output Current (DACs A, B, C)[4]	R_{SET1} = 150 Ω, R_L = 37.5 Ω		34.7		mA
Output Current (DACs A, B, C)[5]	R_{SET1} = 1041 Ω, R_L = 262.5 Ω		5		mA
Output Current (DACs D, E, F)[6]	R_{SET2} = 600 Ω, R_L = 150 Ω		8.66		mA
Output Current (DACs D, E, F)[5]	R_{SET2} = 1041 Ω, R_L = 262.5 Ω		5		mA
DAC-to-DAC Matching (DACs A, B, C)[3]			1	4.0	%
DAC-to-DAC Matching (DACs D, E, F)[3]			1	4.0	%
Output Compliance, V_{OC}				1.4	V
Output Impedance, R_{OUT}			30		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
POWER REQUIREMENTS[3, 7]					
V_{AA}		3.0	3.3	3.6	V
Normal Power Mode					
I_{DAC} (max)[8, 9]	$R_{SET1,2}$ = 600 Ω		58	65	mA
I_{DAC} (min)[8]	$R_{SET1,2}$ = 1041 Ω		30		mA
I_{CCT}[10]			40		mA
Sleep Mode					
I_{DAC}[11]			0.1		μA
I_{CCT}[12]			0.1		μA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.01		%/%

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]Guaranteed by characterization.

[4]Full drive into 75 Ω doubly terminated load.

[5]Minimum drive current (used with buffered/scaled output load).

[6]Full Drive into 150 Ω load.

[7]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 110°C.

[8]I_{DAC} is the total current (*"min" corresponds to 5 mA output per DAC, "max" corresponds to 8.66 mA output per DAC*) to drive DACs A, B, C, D, E, F. Turning off individual DACs reduces I_{DAC} correspondingly, also DACs A, B, C can be configured to output a max current of 37 mA.

[9]DACs A, B, C can output 35 mA typically at 3.3 V (R_{SET} = 150 Ω and R_L = 37.5 Ω), optimum performance obtained at 18 mA DAC Current (R_{SET} = 300 Ω and R_L = 75 Ω).

[10]I_{CCT} (Circuit Current) is the continuous current required to drive the device.

[11]Total DAC current in Sleep Mode.

[12]Total continuous current during Sleep Mode.

Specifications subject to change without notice.

5 V DYNAMIC SPECIFICATIONS

(V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3, 4]	Normal Power Mode		0.3	0.7	%
Differential Phase[3, 4]	Normal Power Mode		0.4	0.7	Degrees
Differential Gain[3, 4]	Lower Power Mode		0.5	1.0	%
Differential Phase[3, 4]	Lower Power Mode		2.0	3.0	Degrees
SNR[3, 4] (Pedestal)	RMS		75		dB rms
SNR[3, 4] (Pedestal)	Peak Periodic		66		dB p-p
SNR[3, 4] (Ramp)	RMS		60		dB rms
SNR[3, 4] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3, 4]			0.7		Degrees
Color Saturation Accuracy[3, 4]			0.9		%
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		1.2		±%
Chroma Nonlinear Phase[3, 4]			0.3	0.5	±Degrees
Chroma/Luma Intermod[3, 4]			0.2	0.4	±%
Chroma/Luma Gain Inequality[3, 4]			1.0		±%
Chroma/Luma Delay Inequality[3, 4]			0.5		ns
Luminance Nonlinearity[3, 4]			1.0	1.7	±%
Chroma AM Noise[3, 4]		79	82		dB
Chroma PM Noise[3, 4]		79	80		dB

NOTES
[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V range.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]These specifications are for the low-pass filter only and guaranteed by design.
[4]Guaranteed by characterization.

Specifications subject to change without notice.

3.3 V DYNAMIC SPECIFICATIONS

(V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions[1]	Min	Typ	Max	Unit
Differential Gain[3]	Normal Power Mode		0.6		%
Differential Phase[3]	Normal Power Mode		0.5		Degrees
Differential Gain[3]	Lower Power Mode		1.0		%
Differential Phase[3]	Lower Power Mode		0.5		Degrees
SNR[3] (Pedestal)	RMS		75		dB rms
SNR[3] (Pedestal)	Peak Periodic		70		dB p-p
SNR[3] (Ramp)	RMS		60		dB rms
SNR[3] (Ramp)	Peak Periodic		58		dB p-p
Hue Accuracy[3]			1.0		Degrees
Color Saturation Accuracy[3]			1.0		%
Luminance Nonlinearity[3]			1.1		±%
Chroma AM Noise[3]			83		dB
Chroma PM Noise[3]			79		dB
Chroma Nonlinear Gain[3, 4]	Referenced to 40 IRE		1.2		±%
Chroma Nonlinear Phase[3, 4]			0.3		±Degrees
Chroma/Luma Intermod[3, 4]			0.2		±%

NOTES
[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Guaranteed by characterization.
[4]These specifications are for the low-pass filter only and guaranteed by design.

Specifications subject to change without notice.

5 V TIMING SPECIFICATIONS (V_{AA} = 5 V ± 5%[1], V_{REF} = 1.235 V, R_{SET1} = 600 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			µs
SCLOCK Low Pulsewidth, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the 1st clock is generated	0.6			µs
Setup Time (Start Condition), t_4	relevant for repeated Start Condition.	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		4.0			ns
Data Hold Time, t_{12}		5.0			ns
Control Setup Time, t_{11}		4			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			15	24	ns
Digital Output Hold Time, t_{14}			10		ns
Pipeline Delay, t_{15}			37		Clock Cycles
TELETEXT PORT[3, 7]					
Digital Output Access Time, t_{16}			20		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3]					
$\overline{\text{RESET}}$ Low Time			3		ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 4.75 V to 5.25 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs:	P7–P0
Pixel Controls:	$\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSO}}$, $\overline{\text{CSO\_HSO}}$, CLAMP
Clock Input:	CLOCK

[7]Teletext Port consists of the following:

Teletext Output:	TTXREQ
Teletext Input:	TTX

Specifications subject to change without notice.

3.3 V TIMING SPECIFICATIONS (V_{AA} = 3.0 V–3.6 V[1], V_{REF} = 1.235 V, $R_{SET1,2}$ = 600 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
MPU PORT[3, 4]					
SCLOCK Frequency		0		400	kHz
SCLOCK High Pulsewidth, t_1		0.6			µs
SCLOCK Low Pulsewidth, t_2		1.3			µs
Hold Time (Start Condition), t_3	After this period the 1st clock is generated	0.6			µs
Setup Time (Start Condition), t_4	relevant for repeated Start Condition.	0.6			µs
Data Setup Time, t_5		100			ns
SDATA, SCLOCK Rise Time, t_6				300	ns
SDATA, SCLOCK Fall Time, t_7				300	ns
Setup Time (Stop Condition), t_8		0.6			µs
ANALOG OUTPUTS[3, 5]					
Analog Output Delay			7		ns
DAC Analog Output Skew			0		ns
CLOCK CONTROL AND PIXEL PORT[4, 5, 6]					
f_{CLOCK}			27		MHz
Clock High Time, t_9		8			ns
Clock Low Time, t_{10}		8			ns
Data Setup Time, t_{11}		4.0			ns
Data Hold Time, t_{12}		5			ns
Control Setup Time, t_{11}		5			ns
Control Hold Time, t_{12}		3			ns
Digital Output Access Time, t_{13}			20		ns
Digital Output Hold Time, t_{14}			12		ns
Pipeline Delay, t_{15}			37		Clock Cycles
TELETEXT PORT[3, 4, 7]					
Digital Output Access Time, t_{16}			23		ns
Data Setup Time, t_{17}			2		ns
Data Hold Time, t_{18}			6		ns
RESET CONTROL[3, 4]					
$\overline{\text{RESET}}$ Low Time			3		ns

NOTES

[1]The max/min specifications are guaranteed over this range. The max/min values are typical over 3.0 V to 3.6 V.

[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF.

[4]Guaranteed by characterization.

[5]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

[6]Pixel Port consists of the following:

Pixel Inputs: P7–P0

Pixel Controls: $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSO}}$, $\overline{\text{CSO\_HSO}}$, CLAMP

Clock Input: CLOCK

[7]Teletext Port consists of the following:

Teletext Output: TTXREQ

Teletext Input: TTX

Specifications subject to change without notice.

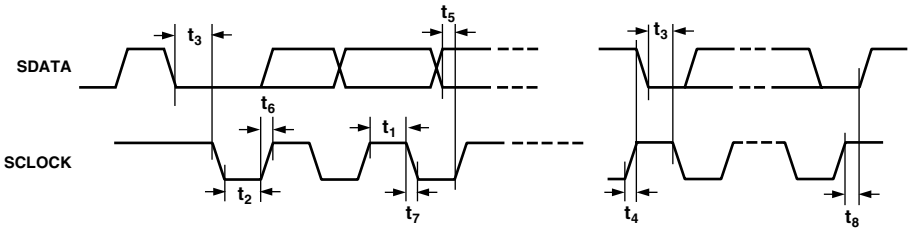


Figure 1. MPU Port Timing Diagram

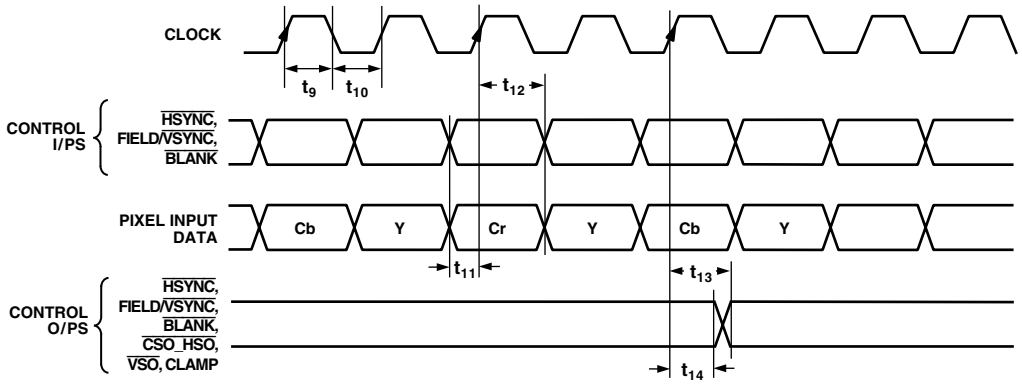


Figure 2. Pixel and Control Data Timing Diagram

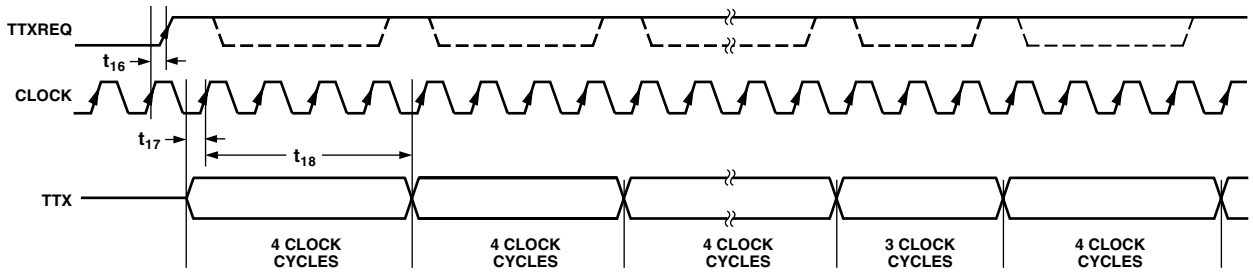


Figure 3. Teletext Timing Diagram

DAC Average Current Consumption

DAC D, E, F: The average current consumed by each DAC is the DAC output current as determined by R_{SET2}/V_{REF} (see Appendix 8).

DAC A, B, C: In *normal power mode* the average current consumed by each DAC is the DAC output current as determined by R_{SET1} (see Appendix 8).

In *Low Power Mode* the average current consumed by each DAC is approximately half the DAC output current as determined by R_{SET1}.

Consult AN-551 for detailed information on ADV7172/ADV7173 power management.

ABSOLUTE MAXIMUM RATINGS[1]

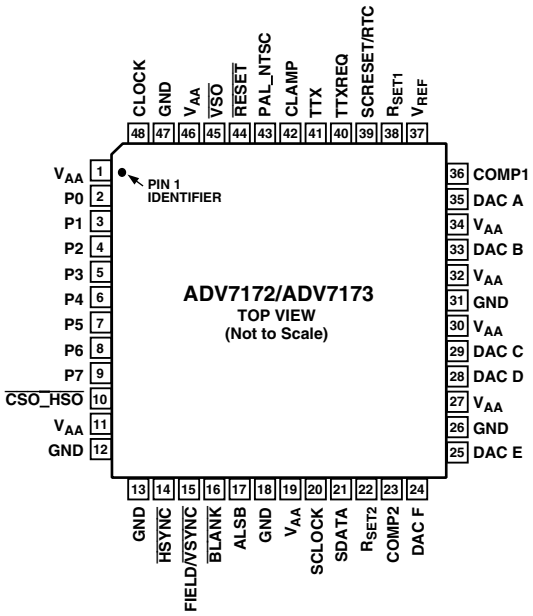
V_{AA} to GND . . . . . 7 V
Voltage on Any Digital Input Pin . GND – 0.5 V to V_{AA} + 0.5 V
Storage Temperature (T_S) . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . 150°C
Lead Temperature (Soldering, 10 sec) . . . . . 260°C
Analog Outputs to GND[2] . . . . . GND – 0.5 V to V_{AA}

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

PIN CONFIGURATION



PACKAGE THERMAL PERFORMANCE

The 48-lead LQFP package is used for this device. The junction-to-ambient (θ_{JA}) thermal resistance in still air on a four layer PCB is 54.6°C/W. The junction-to-case thermal resistance (θ_{JC}) is 16.7°C.

To reduce power consumption when using this part the user is advised to run the part on a 3.3 V supply, turn off any unused DACs. However, if 5 V operation is required the user can enable Low Power mode by setting MR16 to a Logic 1. Another alternative way to further reduce power is to use external buffers that dramatically reduce the DAC currents, the current can be lowered to as low as 5 mA (see AN-551 and Appendix 8 for more details) from a nominal value of 36 mA.

The user must at all times stay below the maximum junction temperature of 110°C. The following equation shows how to calculate this junction temperature:

$$Junction\ Temperature = [V_{AA}\ (I_{DAC} + I_{CCT}) \times \theta_{JA}\ ]\ 70°C$$

where

I_{DAC} = 10 mA + (sum of the average currents consumed by each powered-on DAC).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7172KST	0°C to 70°C	Plastic Thin Quad Flatpack	ST-48
ADV7173KST	0°C to 70°C	Plastic Thin Quad Flatpack	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7172/ADV7173 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Mnemonic	Input/Output	Function
P7–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or as an input and accept (Slave Mode) Sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or as an input (Slave Mode) and accept these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level "0." This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR42 and MR41 of Mode Register 4. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier phase to Field 0. Alternatively it may be configured as a Real-Time Control (RTC) Input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET1}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs A, B, and C (the "large" DACs).
R_{SET2}	I	A 600 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs D, E, and F (the "small" DACs).
COMP1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 µF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in Low Power Mode, the value of the COMP1 capacitor can be lowered to as low as 2.2 nF.
COMP2	O	Compensation Pin for DACs D, E, and F. Connect a 0.1 µF Capacitor from COMP to V_{AA}.
DAC A	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 34.66 mA output.
DAC B	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 34.66 mA output.
DAC C	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 34.66 mA output.
DAC D	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 8.66 mA output.
DAC E	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 8.66 mA output.
DAC F	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 8.66 mA output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
CLAMP	O	TTL Output Signal to external circuitry to enable clamping of all video signals.
PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic "1" selects PAL.
$\overline{\text{VSO}}$	O	$\overline{\text{VSO}}$ TTL Output Sync Signal.
$\overline{\text{CSO\_HSO}}$	O	Dual Function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ TTL Output Sync Signal.
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7172/ADV7173 into default mode. This is NTSC operation, Timing Slave Mode 0, DACs A, B, and C powered OFF, DACs D, E, and F powered ON, Composite and S-Video out.
TTX	I	Teletext Data Input Pin.
TTXREQ	O	Teletext Data Request output signal used to control teletext data transfer.
V_{AA}	P	Power Supply (3 V to 5 V).
GND	G	Ground Pin.

(*continued from page 2*)

INTERNAL FILTER RESPONSE

The Y Filter supports several different frequency responses, including two low-pass responses, two notch responses, an Extended (SSAF) response with or without gain boost/attenuation, a CIF response and a QCIF response. The UV Filter supports several different frequency responses, including four low-pass responses, a CIF response and a QCIF response. These can be seen in Figures 4 to 18.

In Extended Mode there is the option of twelve responses in the range from –4 dB to +4 dB. The desired response can be chosen by the user by programming the correct value via the I^2C. The variation of frequency responses can be seen in Figures 19 to 21.

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR04	MR03	MR02				
LOW-PASS (NTSC)	0	0	0	0.091	4.157	7.37	–56
LOW-PASS (PAL)	0	0	1	0.15	4.74	7.96	–64
NOTCH (NTSC)	0	1	0	0.015	6.54	8.3	–68
NOTCH (PAL)	0	1	1	0.095	6.24	8.0	–66
EXTENDED (SSAF)	1	0	0	0.051	6.217	8.0	–61
CIF	1	0	1	0.018	3.0	7.06	–61
QCIF	1	1	0	MONOTONIC	1.5	7.15	–50

Figure 4. Luminance Internal Filter Specifications

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE (dB)	3 dB BANDWIDTH (MHz)	STOPBAND CUTOFF (MHz)	STOPBAND ATTENUATION (dB)
	MR07	MR06	MR05				
1.3MHz LOW PASS	0	0	0	0.084	1.395	3.01	–45
0.65MHz LOW PASS	0	0	1	MONOTONIC	0.65	3.64	–58.5
1.0MHz LOW PASS	0	1	0	MONOTONIC	1.0	3.73	–49
2.0MHz LOW PASS	0	1	1	0.0645	2.2	5.0	–40
RESERVED	1	0	0				
CIF	1	0	1	0.084	0.7	3.01	–45
QCIF	1	1	0	MONOTONIC	0.5	4.08	–50

Figure 5. Chrominance Internal Filter Specifications

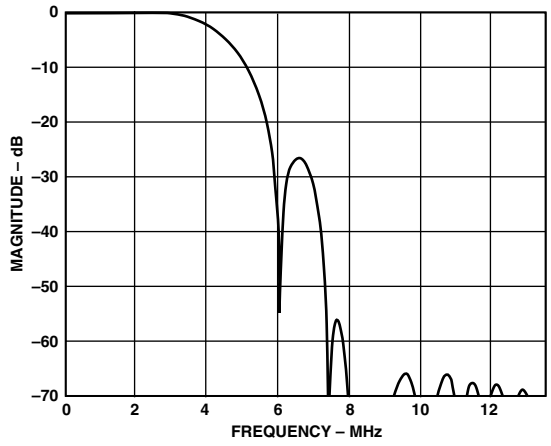


Figure 6. NTSC Low-Pass Luma Filter

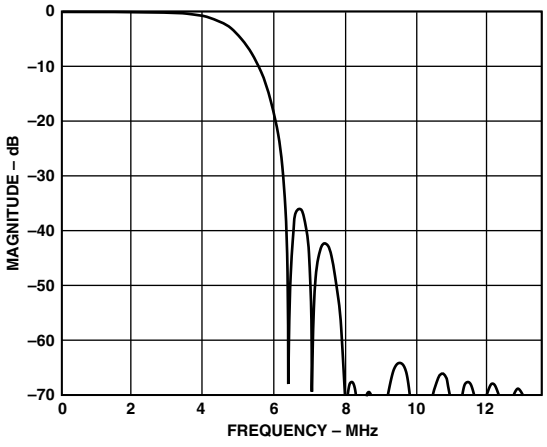


Figure 7. PAL Low-Pass Luma Filter

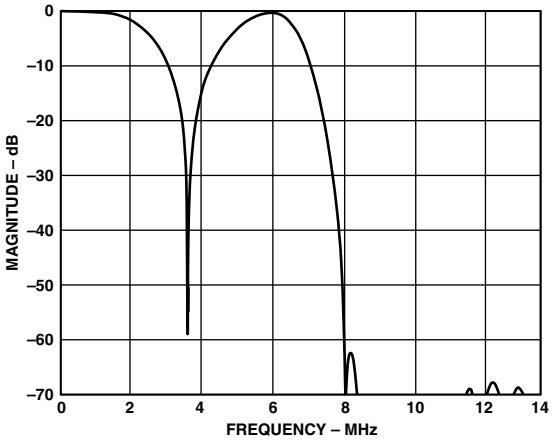


Figure 8. NTSC Notch Luma Filter

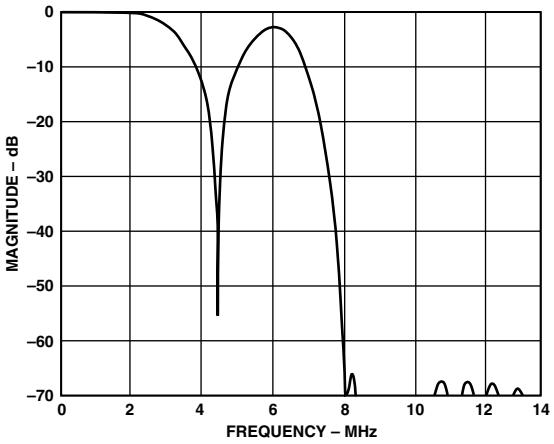


Figure 9. PAL Notch Luma Filter

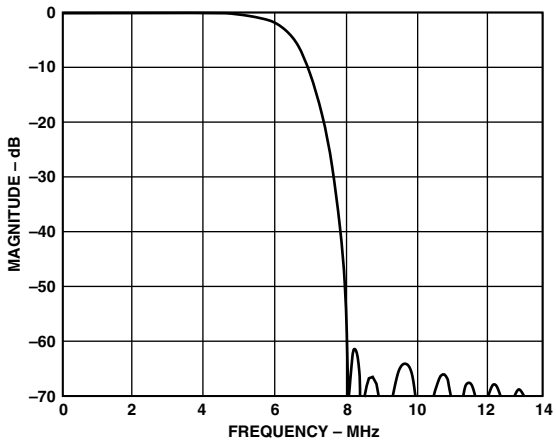


Figure 10. Extended Mode (SSAF) Luma Filter

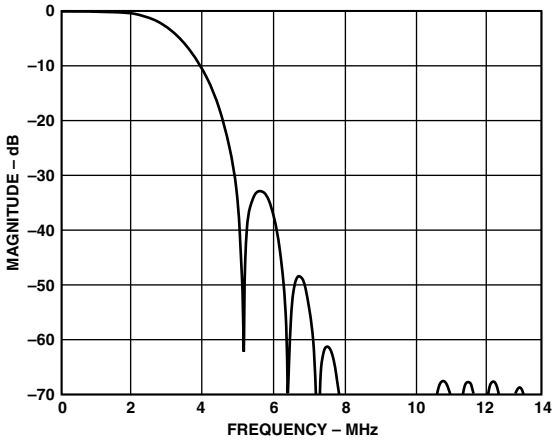


Figure 11. CIF Luma Filter

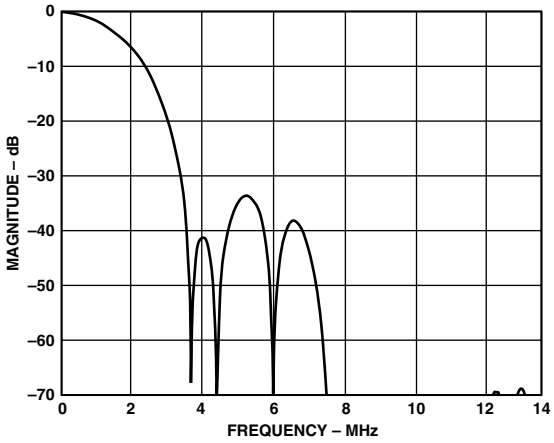


Figure 12. QCIF Luma Filter

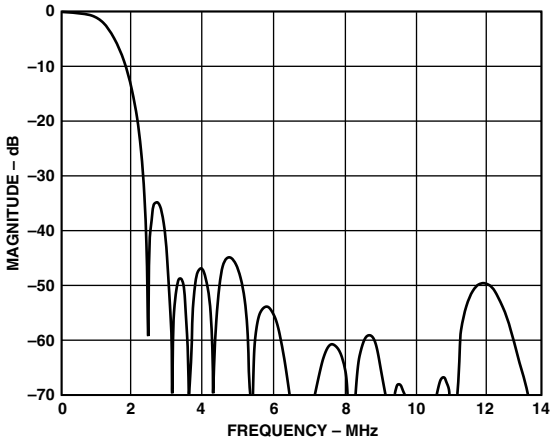


Figure 13. 1.3 MHz Low-Pass Chroma Filter

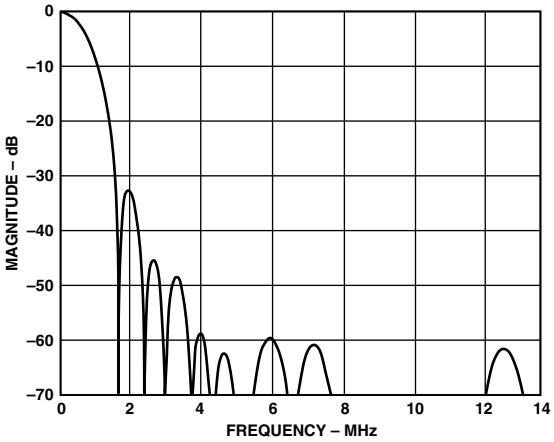


Figure 14. 0.65 MHz Low-Pass Chroma Filter

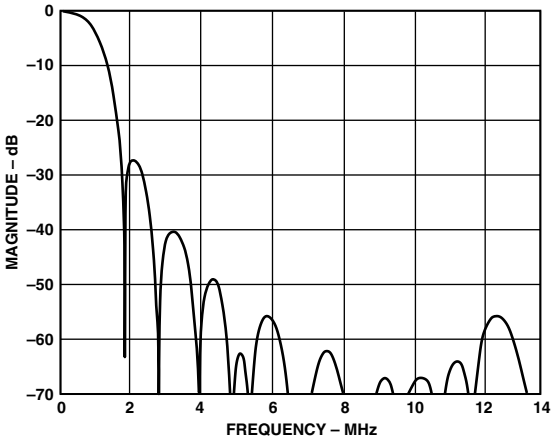


Figure 15. 1.0 MHz Low-Pass Chroma Filter

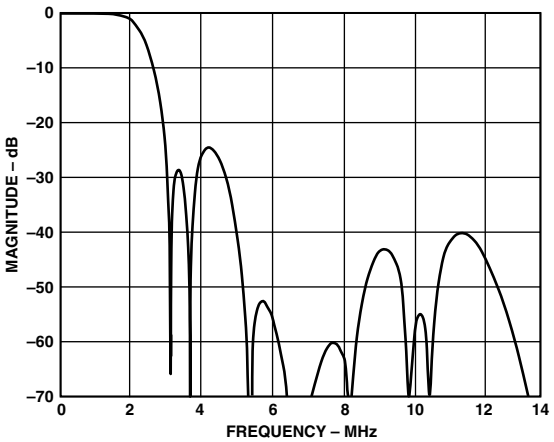


Figure 16. 2.0 MHz Low-Pass Chroma Filter

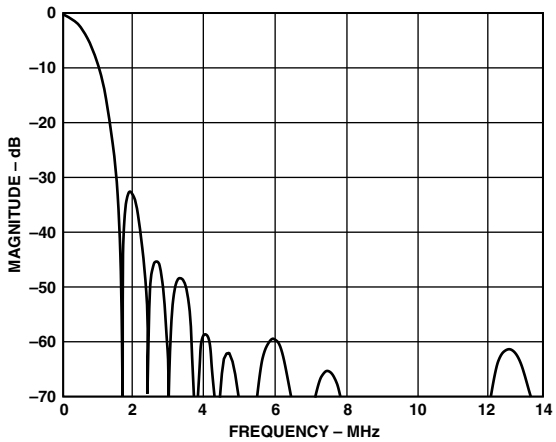


Figure 17. CIF Chroma Filter

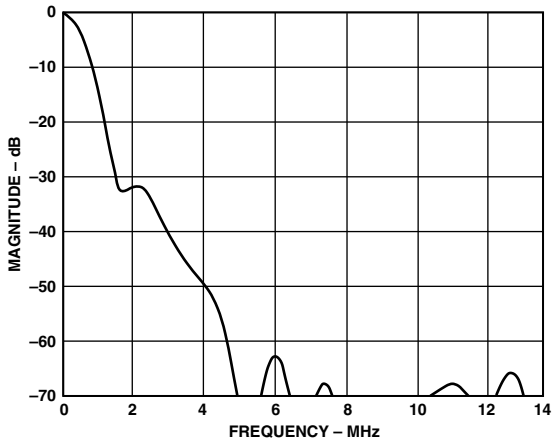


Figure 18. QCIF Chroma Filter

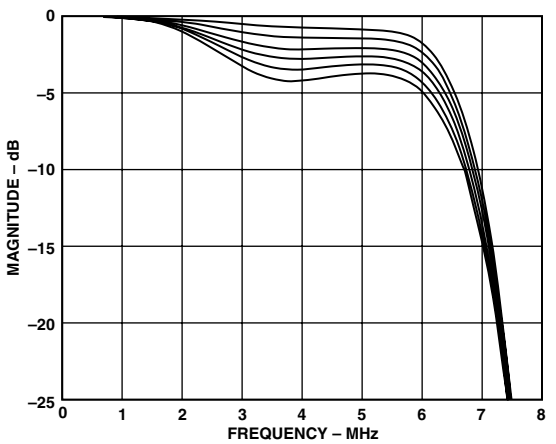


Figure 19. Extended Mode Luma Filter with Programmable Gain, Negative Response

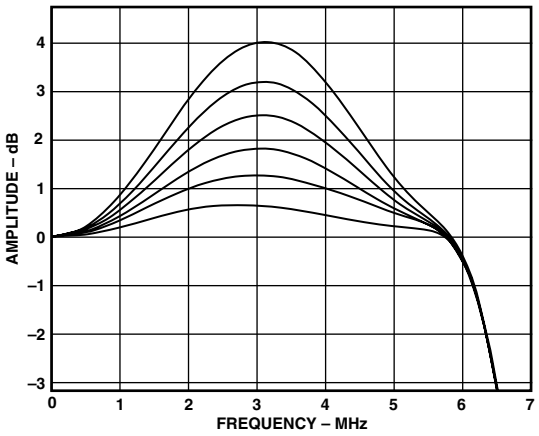


Figure 20. Extended Mode Luma Filter with Programmable Gain, Positive Response

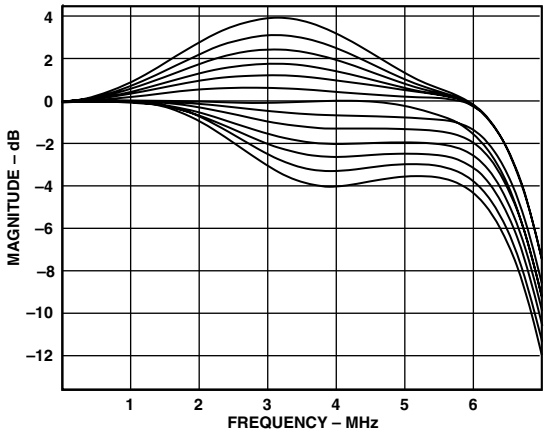


Figure 21. Extended Mode Luma Filter with Programmable Gain, Combined Response

COLOR BAR GENERATION

The ADV7172/ADV7173 can be configured to generate 100/7.5/75/7.5 color bars for NTSC or 100/0/75/0 color bars for PAL. These are enabled by setting MR46 of Mode Register 4 to Logic "1."

SQUARE PIXEL MODE

The ADV7172/ADV7173 can be used to operate in square pixel mode. For NTSC operation, an input clock of 24.5454 MHz is required. Alternatively, for PAL operation, an input clock of 29.5 MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation.

COLOR SIGNAL CONTROL

The color information can be switched on and off the video output using Bit MR44 of Mode Register 4.

BURST SIGNAL CONTROL

The burst information can be switched on and off the video output using Bit MR45 of Mode Register 4.

NTSC PEDESTAL CONTROL

The pedestal on both odd and even fields can be controlled on a line-by-line basis using the NTSC Pedestal Control Registers. This allows the pedestals to be controlled during the Vertical Blanking Interval.

COLOR CONTROLS

The ADV7172/ADV7173 allows the user the advantage of controlling the brightness, contrast, hue and saturation of the color.

Contrast Control

Contrast adjustment is achieved by scaling the Y input data by a factor programmed by the user into the Contrast Control Register Bits 5–0. This factor allows the data to be scaled between 75% and 125%.

Brightness Control

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the Y data in PAL mode, NTSC mode without pedestal or NTSC mode with pedestal, in which case it is added directly onto the 7.5 IRE pedestal already present.

The level added is programmed by the user into the Brightness Control Register (Bits 4–0) and the user is capable of adding from 0 IRE to a maximum of 14 IRE in 32 (2^5) steps. Because of different gains in the datapath for each mode, different values may need to be programmed to obtain the same IRE setup level in each mode. Maximum brightness is achieved when 31 is programmed into the Brightness Control Register. Table I illustrates the maximum setup/brightness amplitudes available in the various modes. Note that if a level of less than 7.5 IRE is required on the Y data in NTSC mode, then NTSC without pedestal must be the mode selected.

Table I. Maximum Brightness Levels Available

Mode	Brightness Control Register	Setup
NTSC No Pedestal	00011111	14 IRE
NTSC Pedestal	00011111	13 IRE
PAL	00011111	99 mV

Color Saturation Control

Color adjustment is achieved by scaling the Cr and Cb input data by a factor programmed by the user into the Color Control Registers 1 and 2, Bits 5–0. This factor allows the data to be scaled between 75% and 125%.

Hue Control

The hue adjustment is achieved on the composite and chroma outputs by adding a phase offset onto the color subcarrier in the active video but leaving the color burst unmodified, i.e., only the phase between the video and the color burst is modified and hence the hue is shifted. Hue adjustment is under the control of the Hue Control Register. The ADV7172/ADV7173 provides a range of ±22° change in increments of 0.17578125°.

YUV LEVELS

This functionality is under the control of Mode Register 5, Bits 2–0. Bit 0 (MR50) allows the ADV7172/ADV7173 to output SMPTE levels on the Y output when configured in NTSC mode, and Betacam levels on the Y output when configured in PAL mode and vice-versa.

	Video	Sync
Betacam	286 mV	714 mV
SMPTE	300 mV	700 mV
MII	300 mV	700 mV

As the datapath is branched at the output of the filters, the luma signal relating to the CVBS or S-Video Y/C output is unaltered. Only the Y output of the YUV outputs is scaled. Bits 2–1 (MR52–MR51) allow UV levels to have a peak-peak amplitude of 700 mV or 1000 mV, or the default values of 934 mV in NTSC and 700 mV in PAL.

AUTODETECT CONTROL

The ADV7172/ADV7173 provides the option of automatically powering down the DACs A, B and C if they are not correctly terminated (i.e., the 75 Ω cable is not connected to the DAC). The voltage at the output of DACs A and B are compared to a selected reference level. This reference voltage (MR64) will depend on whether the user terminates with 37.5 Ω (75 Ω connected on the DAC end and 75 Ω connected at TV end of cable, i.e., combined load of 37.5 Ω) or 75 Ω. It cannot operate in a DAC buffering configuration. There are two modes of autodetect operation provided by the ADV7172/ADV7173:

(1) Mode 0: The state of termination of the DAC may be read by reading the status bits in Mode Register 6. MR67 status bit indicates whether or not the composite DAC is terminated, MR66 status bit indicates whether or not the luma DAC is terminated. The user may then decide whether or not to power down the DACs using MR15–MR0.

(2) Mode 1: The state of the DACs may be read as in Mode 0. If either of the DACs is unterminated, they are automatically powered down. If the luma DAC, DAC B is powered down then DAC C, the chroma DAC, will also be powered down. The state of termination of the DAC is checked each frame to decide whether or not it is to be powered up or down.

Mode Register 6, Bits 3–2, indicates which mode of operation is used. Note that Mode Register 1, Bits 5-3, must be enabled ("1") for autodetect functionality to work. (DACs A, B, C are enabled.)

Vertical Blanking Data Insertion

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not have line sync or pre-/post-equalization pulses (see Figures 24 to 25). This mode of operation is called "Partial Blanking" and is selected by setting MR32 to "1." It allows the insertion of any VBI data (Opened VBI) into the encoded output waveform. This data is present in digitized incoming YCbCr data stream (e.g., WSS data, CGMS, VPS etc.). Alternatively the entire VBI may be blanked (no VBI data inserted) on these lines by setting MR32 to "0."

SUBCARRIER RESET

Together with the SCRESET/RTC PIN and Bits MR42 and MR41 of Mode Register 4, the ADV7172/ADV7173 can be used in subcarrier reset mode. The subcarrier phase will reset to Field 0 at the start of the following field when a low to high transition occurs on this input pin.

REAL-TIME CONTROL

Together with the SCRESET/RTC PIN and Bits MR42 and MR41 of Mode Register 4, the ADV7172/ADV7173 can be used to lock to an external video source. The real-time control mode allows the ADV7172/ADV7173 to automatically alter the subcarrier frequency to compensate for line length variation. When the part is connected to a device that outputs a digital data stream in the RTC format (such as a ADV7185 video decoder, see Figure 22), the part will automatically change to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00Hex should be written into all four subcarrier frequency registers when using this mode.

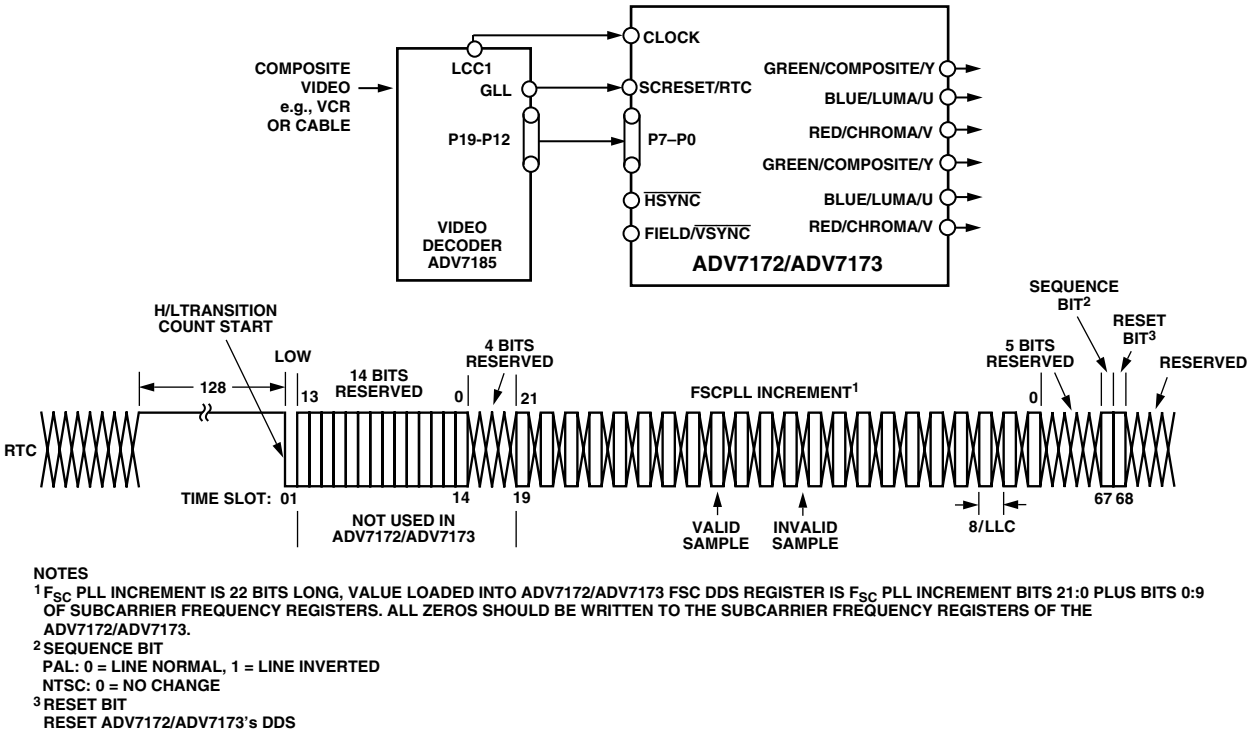
VIDEO TIMING DESCRIPTION

The ADV7172/ADV7173 is intended to interface to off-the-shelf MPEG1 and MPEG2 Decoders. As a consequence, the ADV7172/ADV7173 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 pixel port and has several video timing modes of operation that allow it to be configured as either system master video timing generator or a slave to the system video timing generator. The ADV7172/ADV7173 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7172/ADV7173 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalization pulses are inserted where required.

In addition, the ADV7172/ADV7173 supports a PAL or NTSC square pixel operation in slave mode. The part requires an input pixel clock of 24.5454 MHz for NTSC and an input pixel clock of 29.5 MHz for PAL. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7172/ADV7173 has four distinct master and four distinct slave timing configurations. Timing control is established with the bidirectional $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and FIELD/$\overline{\text{VSYNC}}$ pins. Timing Mode Register 1 can also be used to vary the timing pulsewidths and where they occur in relation to each other.



NOTES
[1] F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUE LOADED INTO ADV7172/ADV7173 FSC DDS REGISTER IS F_{SC} PLL INCREMENT BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7172/ADV7173.
[2] SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE
[3] RESET BIT
RESET ADV7172/ADV7173's DDS

Figure 22. RTC Timing and Connections

Mode 0 (CCIR–656): Slave Option
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7172/ADV7173 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data. All timing information is transmitted using a 4-byte Synchronization Pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 23. The $\overline{\text{HSYNC}}$, FIELD/$\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode.

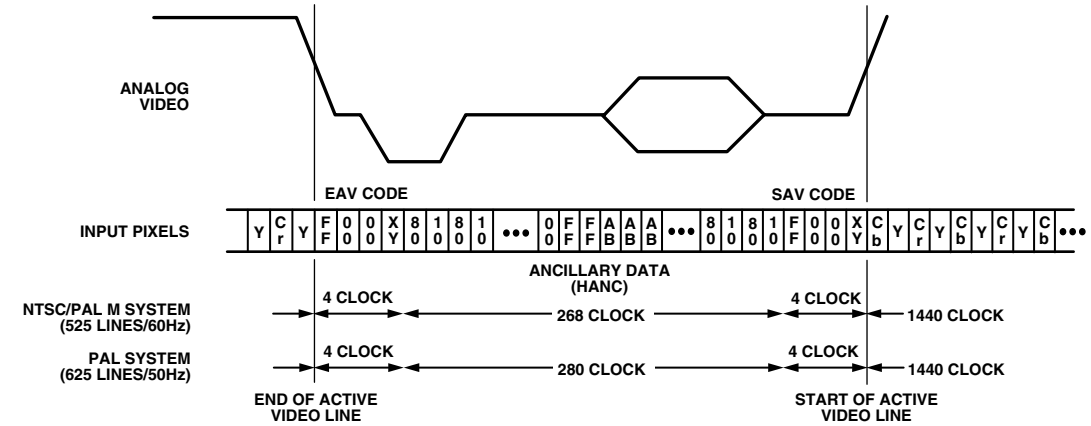


Figure 23. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR–656): Master Option
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7172/ADV7173 generates H, V, and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{\text{HSYNC}}$ pin, the V bit is output on the $\overline{\text{BLANK}}$ pin and the F bit is output on the FIELD/$\overline{\text{VSYNC}}$ pin. Mode 0 is illustrated in Figure 24 (NTSC) and Figure 25 (PAL). The H, V, and F transitions relative to the video waveform are illustrated in Figure 26.

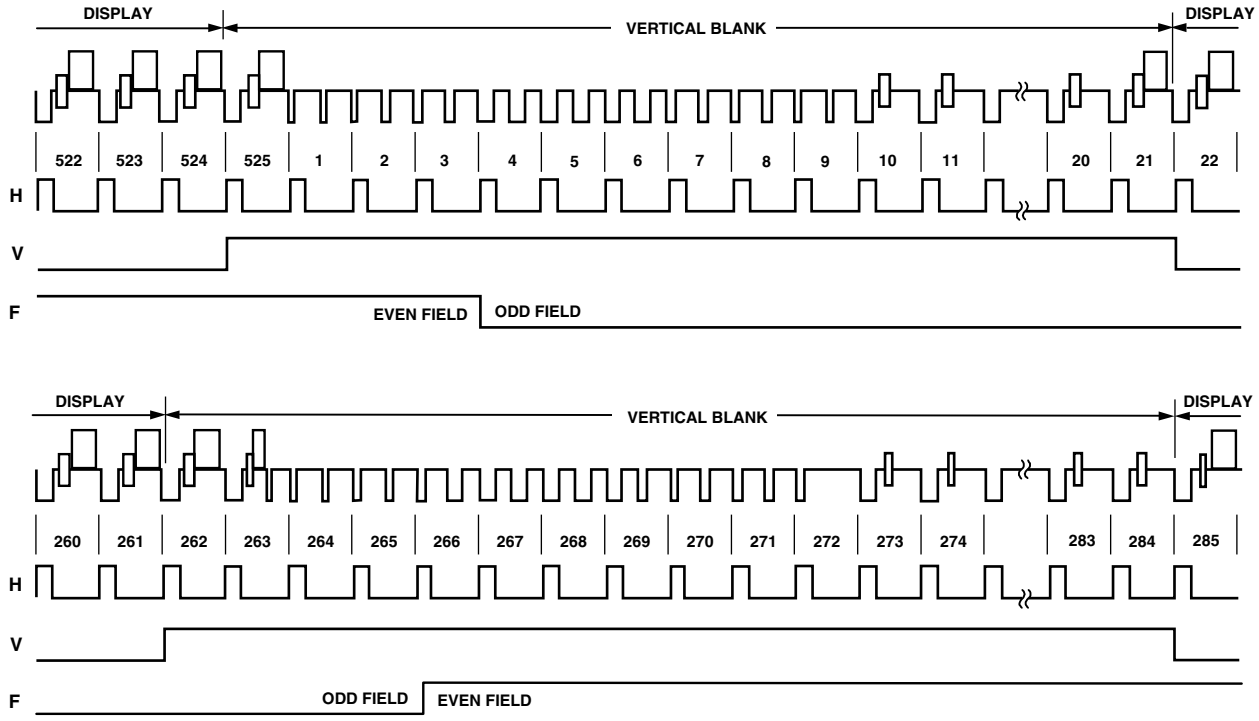


Figure 24. Timing Mode 0 (NTSC Master Mode)

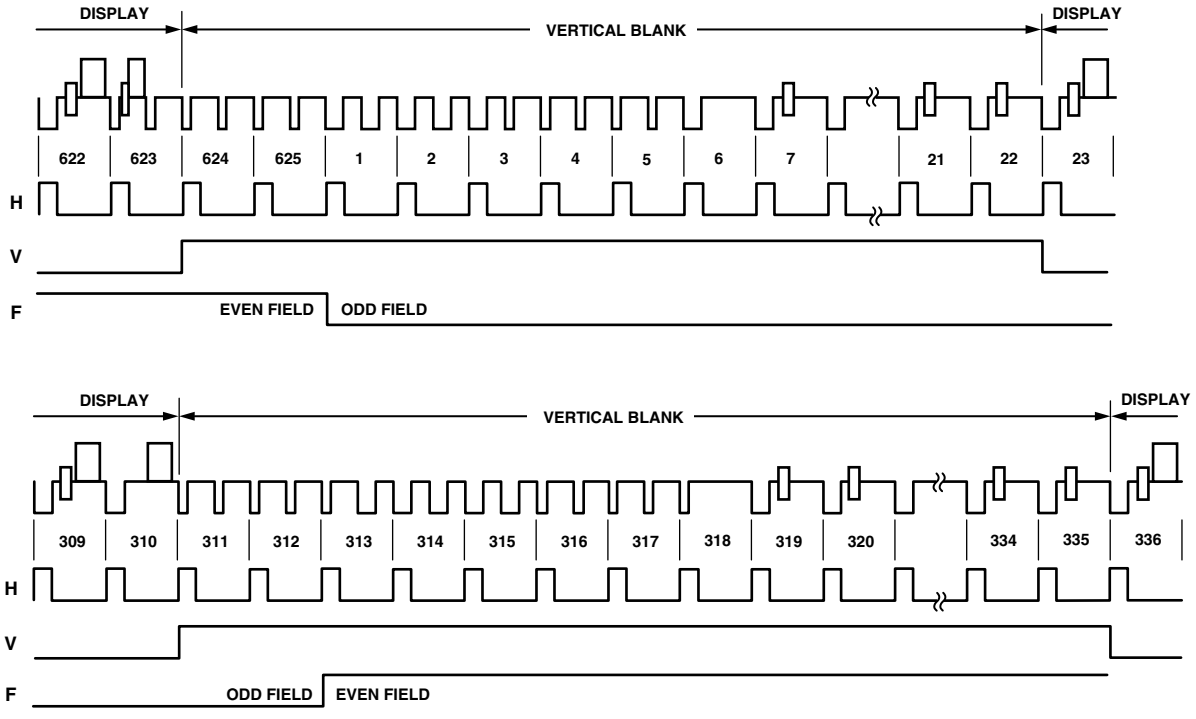


Figure 25. Timing Mode 0 (PAL Master Mode)

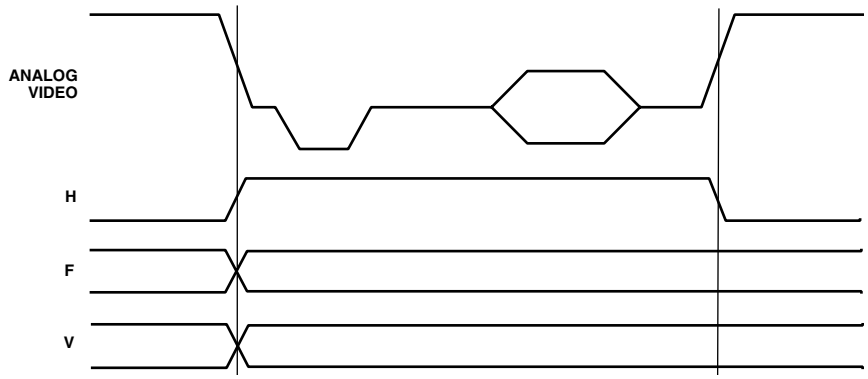


Figure 26. Timing Mode 0 Data Transitions (Master Mode)

Mode 1: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7172/ADV7173 accepts horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL).

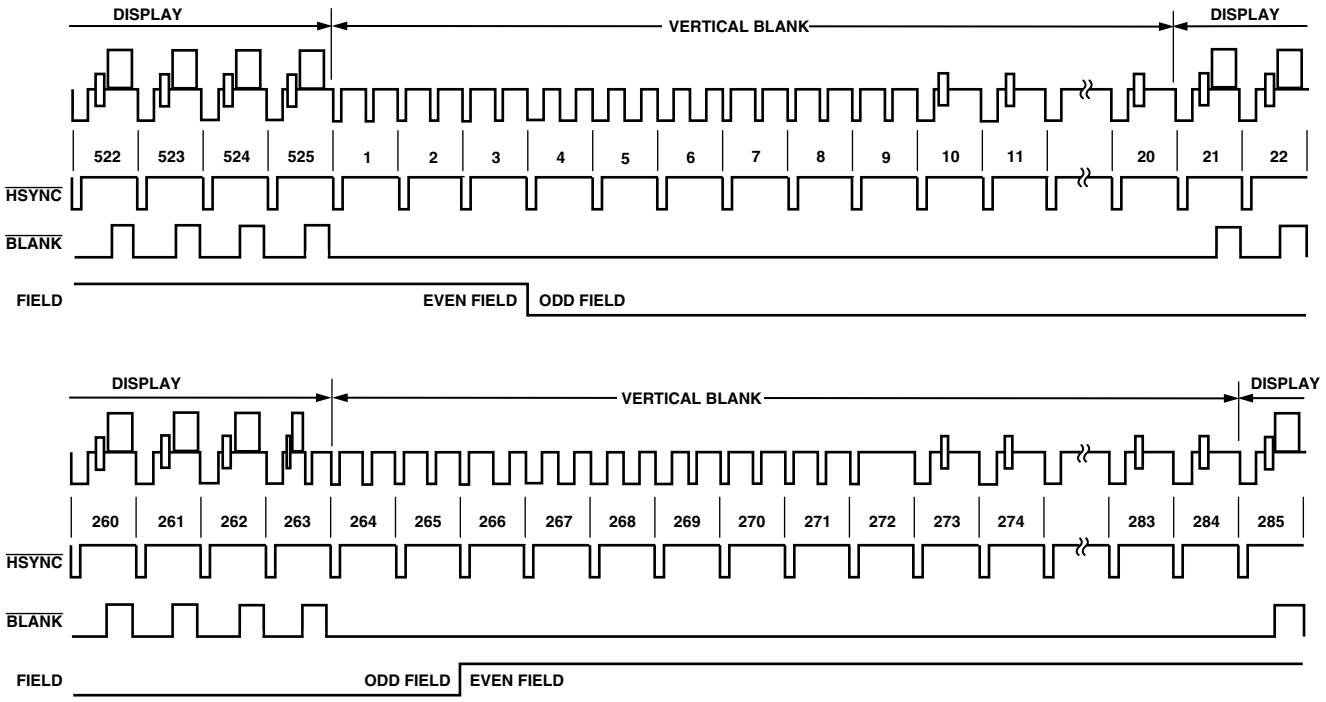


Figure 27. Timing Mode 1 (NTSC)

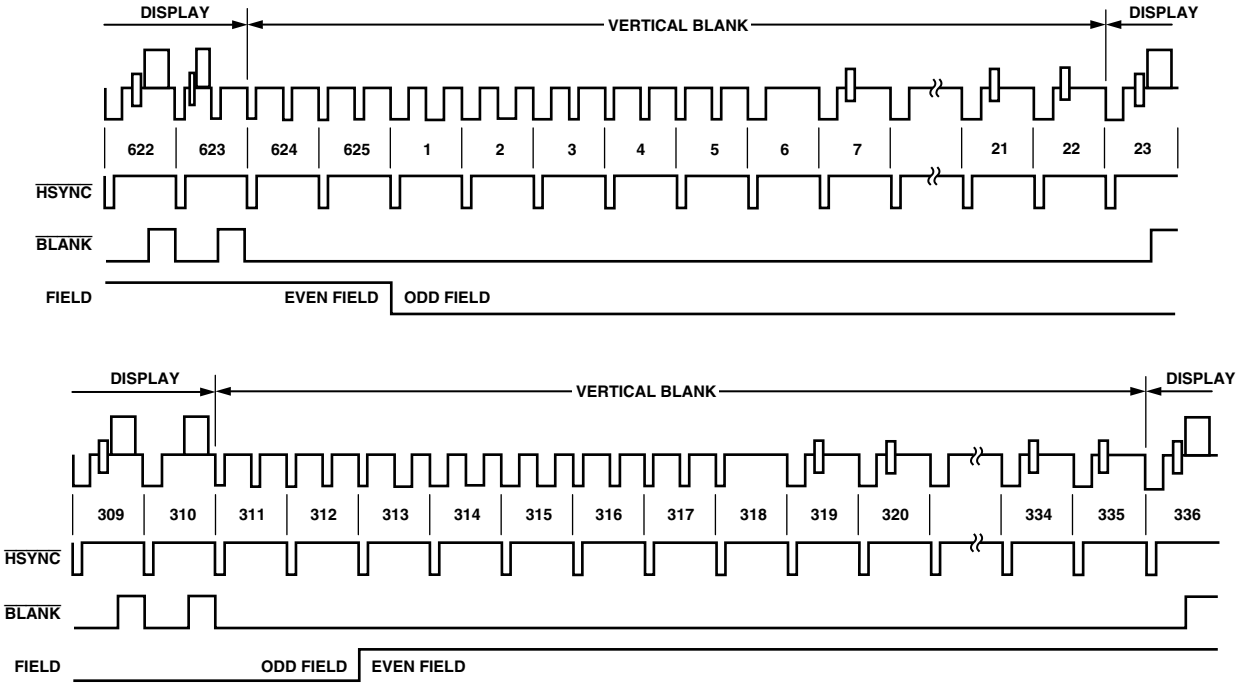


Figure 28. Timing Mode 1 (PAL)

Mode 1: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7172/ADV7173 can generate horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 27 (NTSC) and Figure 28 (PAL). Figure 29 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD for an odd-or-even field transition relative to the pixel data.

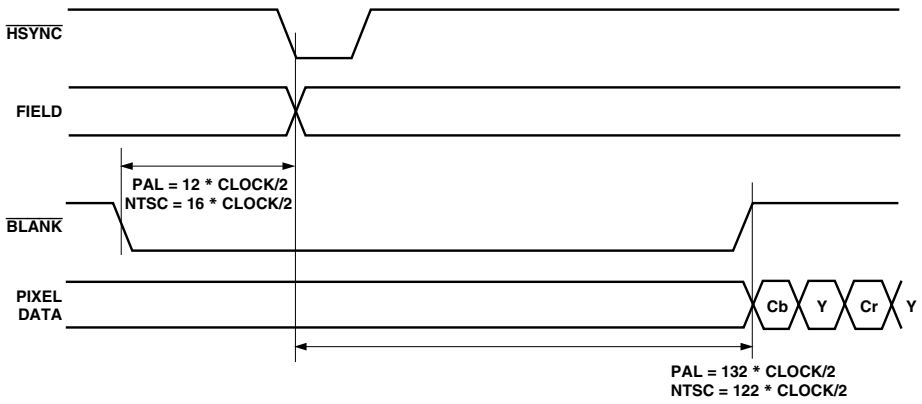


Figure 29. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2: Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7172/ADV7173 accepts horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an Even Field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 30 (NTSC) and Figure 31 (PAL).

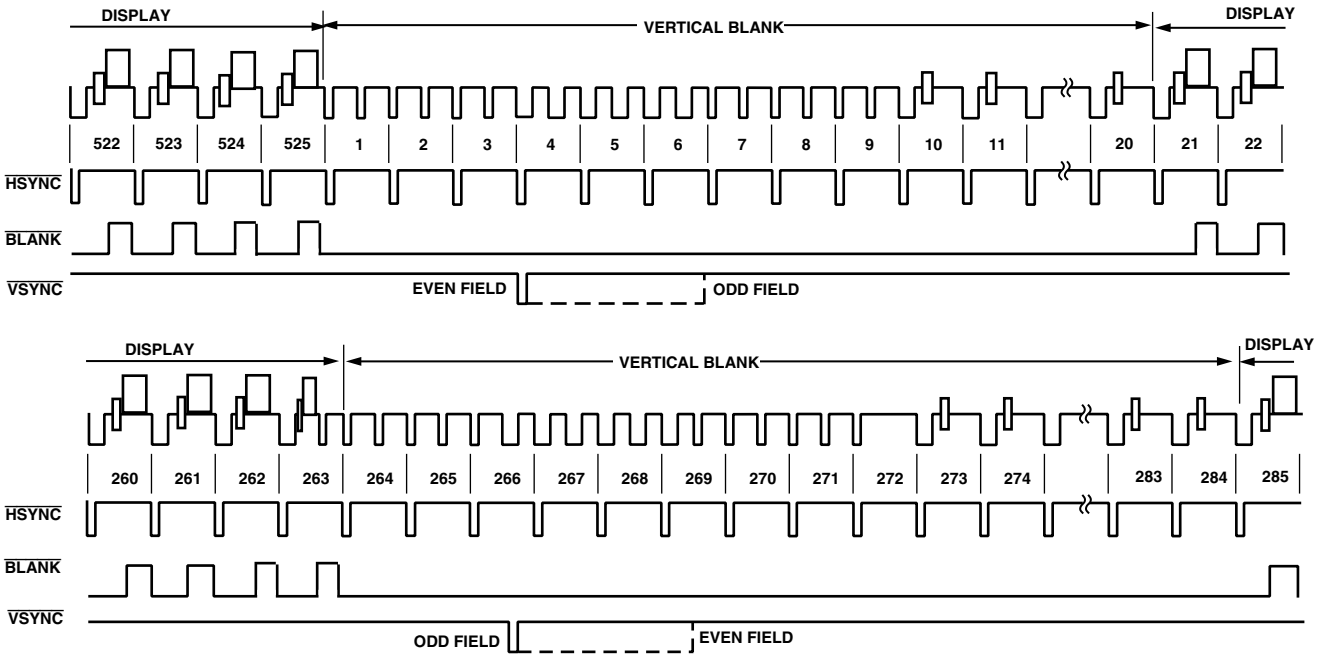


Figure 30. Timing Mode 2 (NTSC)

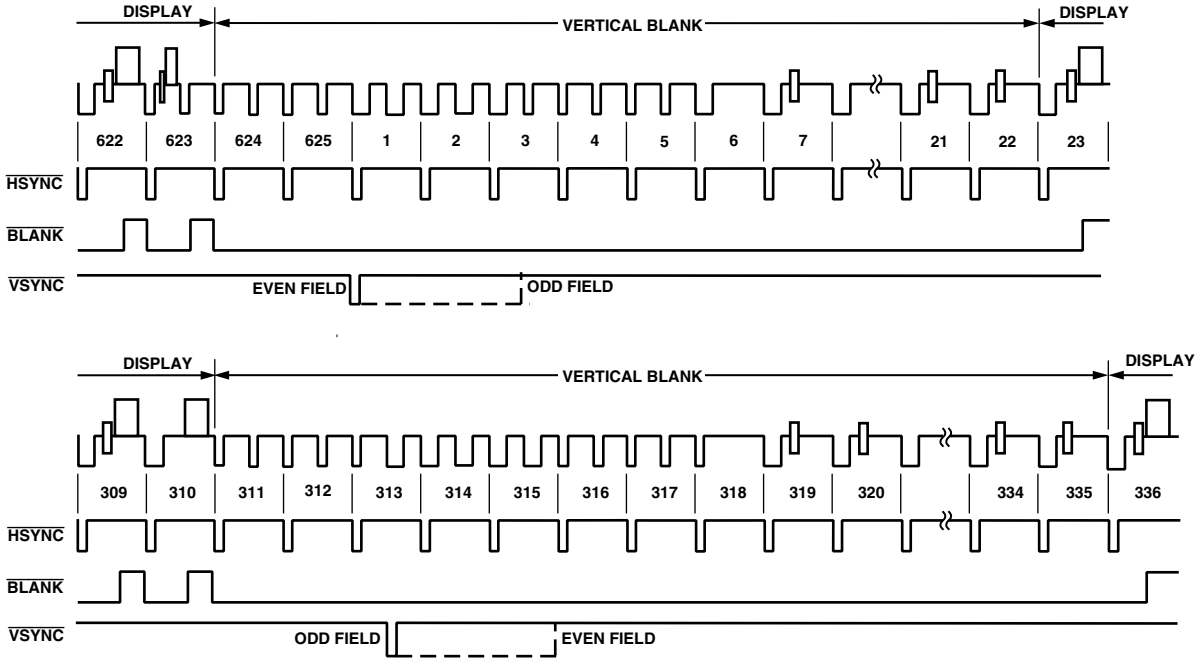


Figure 31. Timing Mode 2 (PAL)

Mode 2: Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7172/ADV7173 can generate horizontal and vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 30 (NTSC) and Figure 31 (PAL). Figure 32 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an even-to-odd field transition relative to the pixel data. Figure 33 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ for an odd-to-even field transition relative to the pixel data.

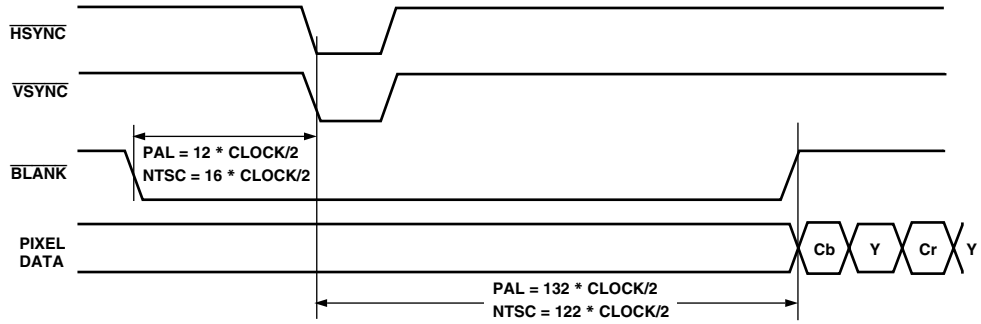


Figure 32. Timing Mode 2 Even-to-Odd Field Transition Master/Slave

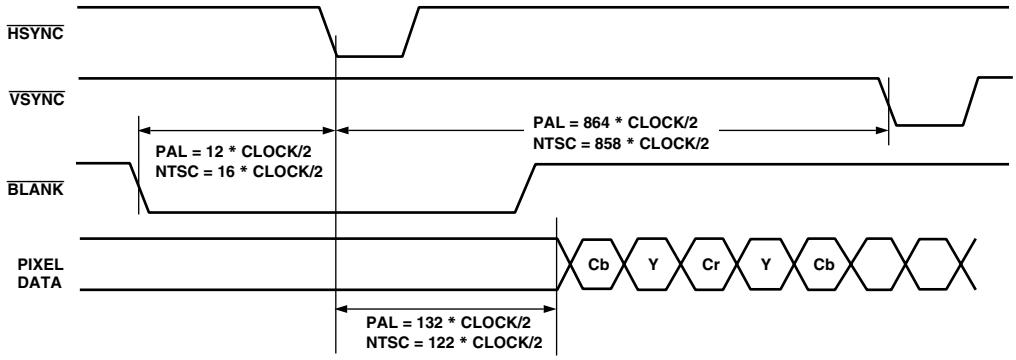


Figure 33. Timing Mode 2 Odd-to-Even Field Transition Master/Slave

Mode 3: Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7172/ADV7173 accepts or generates horizontal SYNC and Odd/Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7172/ADV7173 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 34 (NTSC) and Figure 35 (PAL).

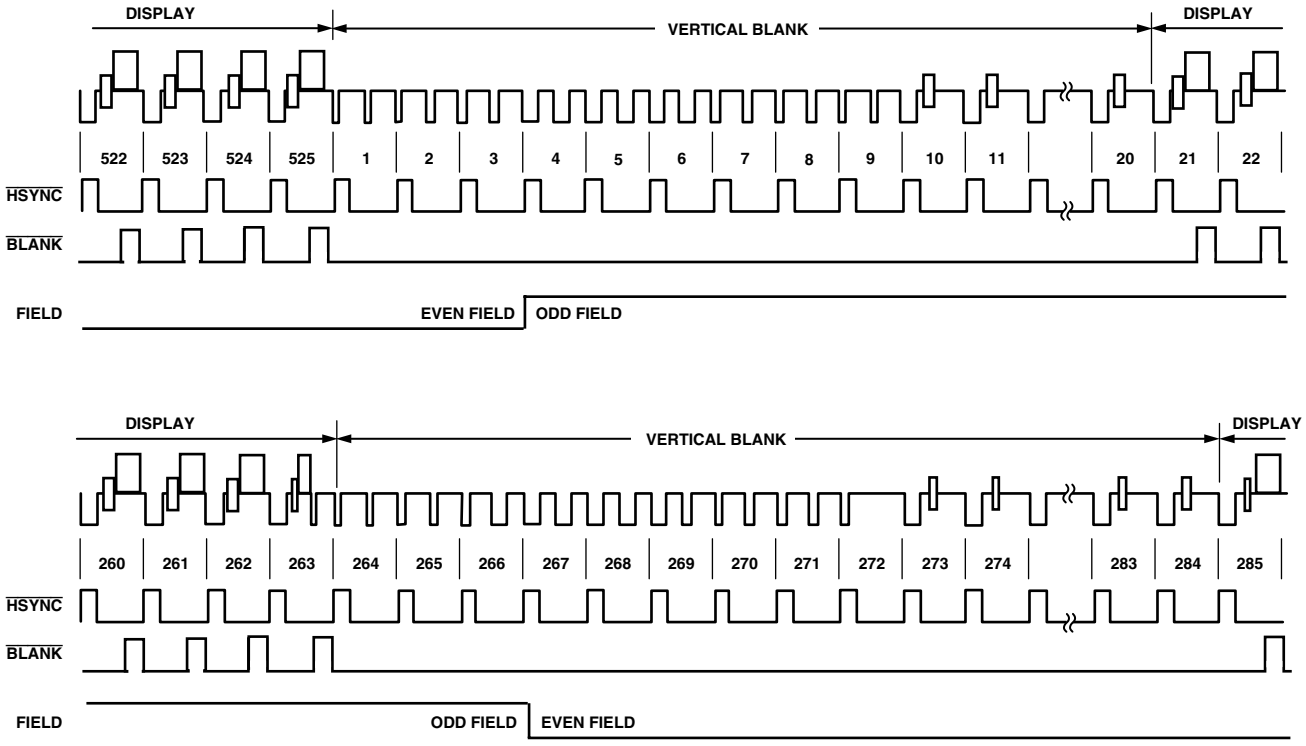


Figure 34. Timing Mode 3 (NTSC)

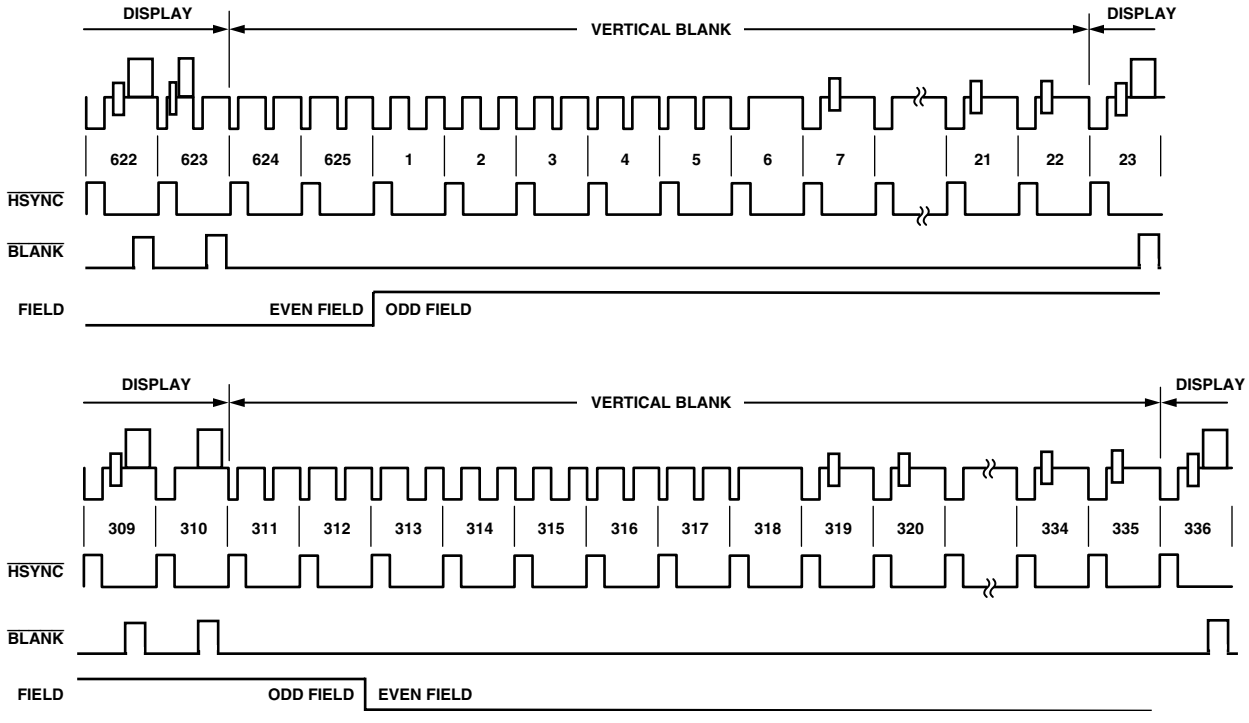


Figure 35. Timing Mode 3 (PAL)

POWER-ON RESET

After power-up, it is necessary to execute a reset operation. A reset occurs on the falling edge of a high-to-low transition on the $\overline{\text{RESET}}$ pin. This initializes the pixel port such that the pixel inputs P7–P0 are not selected. After reset, the ADV7172/ADV7173 is automatically set up to operate in NTSC/PAL mode, depending on the PAL_NTSC pin. The subcarrier frequency registers are automatically loaded with the correct values for PAL or NTSC. All other registers, with the exception of Mode Registers 1 and 2, are set to 00H. Mode Register 1 is set to 07H. This is to ensure DACs D, E, and F are ON after power-up. All bits of Mode Register 2 are set to "0," with the exception of Bit 3 (i.e., Mode Register 2 reads 08H). Bit MR23 of Mode Register 2 is set to Logic "1." This enables the 7.5 IRE pedestal.

RESET SEQUENCE

When $\overline{\text{RESET}}$ becomes active, the ADV7172/ADV7173 reverts to the default output configuration. DACs A, B, C are off and DACs D, E, F are powered on and output composite, luma and chroma signals respectively. Mode Register 2, Bit 6 (MR26), resets to "0." The ADV7172/ADV7173 internal timing is under the control of the logic level on the NTSC_PAL pin.

When $\overline{\text{RESET}}$ is released Y, Cr, Cb values corresponding to a black screen are input to the ADV7172/ADV7173. Output timing signals are still suppressed at this stage.

When the user requires valid data, MR26 is set to "1" to allow the valid pixel data to pass through the encoder. Digital output timing signals become active and the encoder timing is now under the control of the timing registers. If, at this stage, the user wishes to select a video standard different from that on the NTSC_PAL pin, Mode Register 2, Bit 5 (MR25) is set ("1") and the video standard required is selected by programming Mode Register 0. Figure 36 illustrates the reset sequence timing.

SLEEP MODE

If after reset the SCRESET/RTC and NTSC_PAL pins are both set to high, the part ADV7172/ADV7173 will power-up in sleep mode to facilitate low power consumption before all registers have been initialized. If Mode Register 6, Bit 0 (MR60) is then set to ("1") sleep mode control passes to Mode Register 2, Bit 7 (i.e., control via I^2C).

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four (NTSC) or eight (PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.

Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.

Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7172/ADV7173 is configured in RTC mode (MR41 = "1" and MR42 = "1"). Under these conditions (unstable video) the subcarrier phase reset should be enabled (MR42 = "0" and MR41 = "1") but no reset applied. In this configuration the SCH phase will never be reset, which that the output video will now track the unstable input video.

The subcarrier phase reset when applied will reset the SCH phase to Field 0 at the start of the next field (e.g., subcarrier phase reset applied in Field 5 (PAL) on the start of the next field SCH phase will be reset to Field 0).

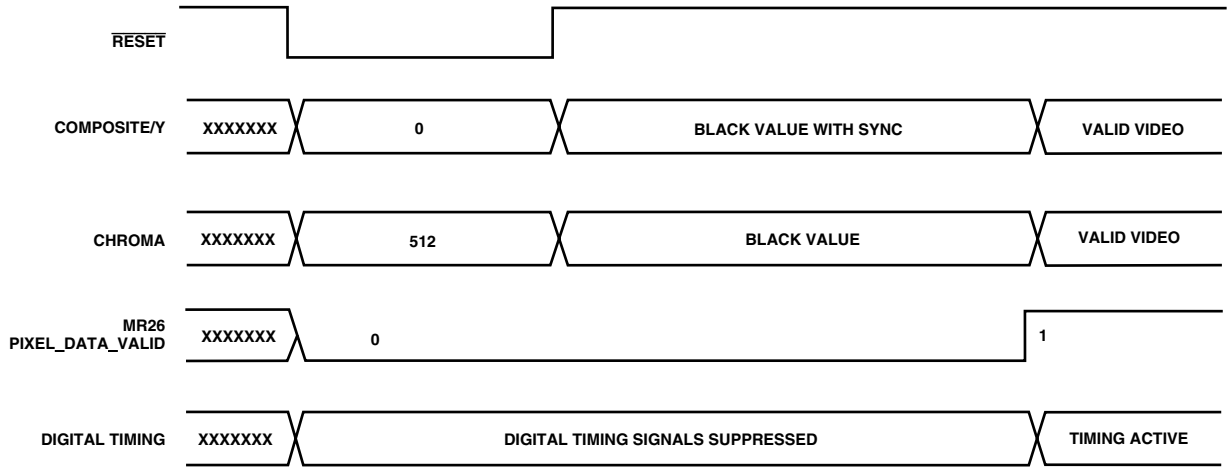


Figure 36. $\overline{\text{RESET}}$ Sequence Timing Diagram

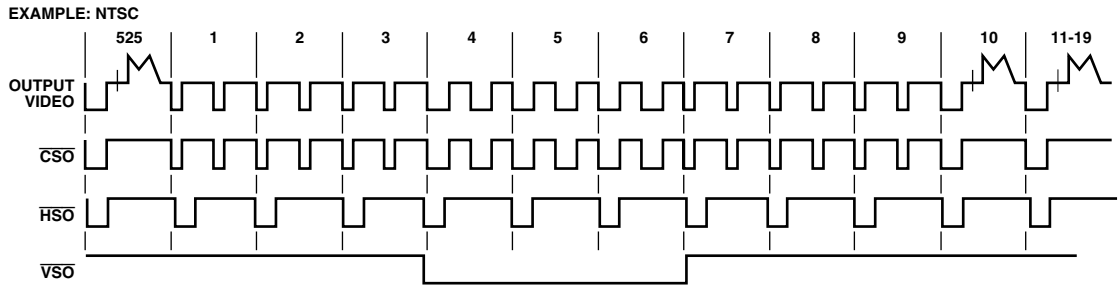


Figure 37. $\overline{CSO}$, $\overline{HSO}$, $\overline{VSO}$ Timing Diagram

$\overline{CSO}$, $\overline{HSO}$, AND $\overline{VSO}$ OUTPUTS

The ADV7172/ADV7173 supports three timing signals, $\overline{CSO}$ (composite sync signal), $\overline{HSO}$ (horizontal sync signal) and $\overline{VSO}$ (vertical sync signal). These output TTL signals are aligned with the analog video outputs. $\overline{HSO}$ and $\overline{CSO}$ are shared on Pin 10. Mode Register 7, Bit MR75 can be used to configure this output pin. See Figure 37 for an example of these waveforms.

CLAMP OUTPUT

The ADV7172/ADV7173 has a programmable clamp TTL output signal. The clamp signal is programmable to the front and back porch. Mode Register 5, Bit MR57 can be used to control the porch position. Also the position of the clamp signal can be varied by 1–3 clock cycles in a positive and negative direction from the default position. Mode Register 5, Bits MR56, MR55, and MR54 control this position.

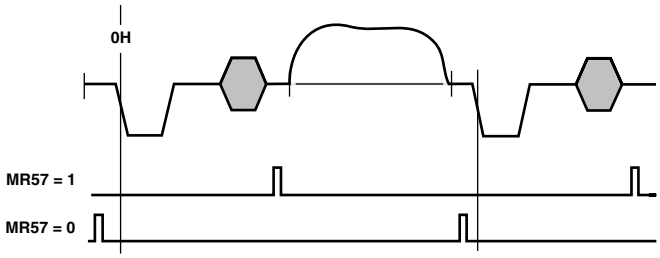


Figure 38. Clamp Output Timing

MPU PORT DESCRIPTION

The ADV7172 and ADV7173 support a 2-wire serial (I^2C-Compatible) microprocessor bus driving multiple peripherals. Two inputs serial data (SDATA) and serial clock (SCLOCK) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7172 and ADV7173 each have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 39 and Figure 40. The LSB sets either a read or write operation. Logic Level "1" corresponds to a read operation while Logic Level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7172/ADV7173 to Logic Level "0" or Logic Level "1." When ALSB is set to "0," there is greater bandwidth on the I^2C lines, which allows high-speed data transfers on this bus. When ALSB is set to "1," there is reduced input bandwidth on the I^2C lines, which means that impulses of less than 50 ns will not pass into the I^2C internal controller. This mode is recommended for noisy systems.

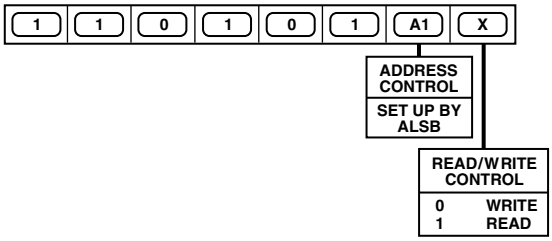


Figure 39. ADV7172 Slave Address

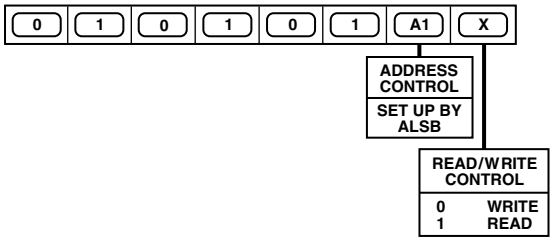


Figure 40. ADV7173 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDATA while SCLOCK remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLOCK lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data. A Logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A Logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7172/ADV7173 acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto increment allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers. There is one exception. The subcarrier frequency registers should be updated in sequence, starting with Subcarrier Frequency Register 0. The auto increment function should then be used to increment and access Subcarrier Frequency Registers 1, 2 and 3. The subcarrier frequency registers should not be accessed independently.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCLOCK high period, the user should issue only one start condition, one stop condition or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7172/ADV7173 will not issue an acknowledge and will return to the idle condition. If, in autoincrement mode, the user exceeds the highest subaddress, the following action will be taken:

1. In Read Mode the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDATA line is not pulled low on the ninth pulse.
2. In Write Mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7172/ADV7173 and the part will return to the idle condition.

Figure 41 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

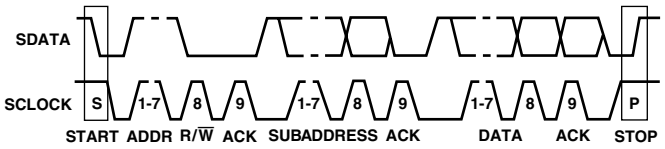


Figure 41. Bus Data Transfer

Figure 42 shows bus write and read sequences.

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7172/ADV7173 except the Subaddress Register, which is a write-only register. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. A read/write operation is then performed from/to the target address, which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register, including subaddress register, mode registers, subcarrier frequency registers, subcarrier phase register, timing registers, closed captioning extended data registers, closed captioning data registers, NTSC pedestal Control/PAL teletext control registers, CGMS/WSS registers, contrast register, U- or V-scale registers, hue adjust register, brightness control register and sharpness control register in terms of its configuration. All registers can be read from as well as written to.

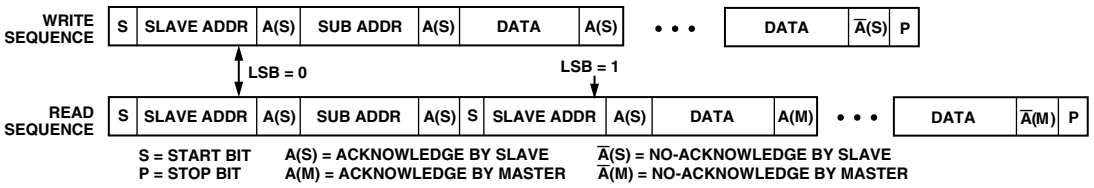
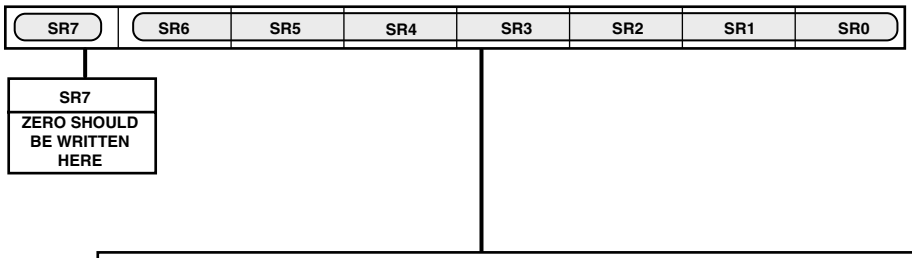


Figure 42. Write and Read Sequences

Subaddress Register (SR7–SR0)
The communications register is an 8-bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place.

Figure 43 shows the various operations under the control of the subaddress register. "0" should always be written to SR7.

Register Select (SR6–SR0)
These bits are set up to point to the required starting address.



ADV7172/73 SUBADDRESS REGISTER

Address	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	MODE REGISTER 6
07h	0	0	0	0	1	1	1	MODE REGISTER 7
08h	0	0	0	1	0	0	0	RESERVED
09h	0	0	0	1	0	0	1	RESERVED
0Ah	0	0	0	1	0	1	0	TIMING REGISTER 0
0Bh	0	0	0	1	0	1	1	TIMING REGISTER 1
0Ch	0	0	0	1	1	0	0	SUB CARRIER FREQUENCY REGISTER 0
0Dh	0	0	0	1	1	0	1	SUB CARRIER FREQUENCY REGISTER 1
0Eh	0	0	0	1	1	1	0	SUB CARRIER FREQUENCY REGISTER 2
0Fh	0	0	0	1	1	1	1	SUB CARRIER FREQUENCY REGISTER 3
10h	0	0	1	0	0	0	0	SUB CARRIER PHASE REGISTER
11h	0	0	1	0	0	0	1	CLOSED CAPTIONING EXTENDED DATA BYTE 0
12h	0	0	1	0	0	1	0	CLOSED CAPTIONING EXTENDED DATA BYTE 1
13h	0	0	1	0	0	1	1	CLOSED CAPTIONING DATA BYTE 0
14h	0	0	1	0	1	0	0	CLOSED CAPTIONING DATA BYTE 1
15h	0	0	1	0	1	0	1	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 0
16h	0	0	1	0	1	1	0	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 1
17h	0	0	1	0	1	1	1	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 2
18h	0	0	1	1	0	0	0	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 3
19h	0	0	1	1	0	0	1	CGMS/WSS 0
1Ah	0	0	1	1	0	1	0	CGMS/WSS 1
1Bh	0	0	1	1	0	1	1	CGMS/WSS 2
1Ch	0	0	1	1	1	0	0	TELETEXT REQUEST CONTROL REGISTER
1Dh	0	0	1	1	1	0	1	CONTRAST CONTROL REGISTER
1Eh	0	0	1	1	1	1	0	U SCALE REGISTER
1Fh	0	0	1	1	1	1	1	V SCALE REGISTER
20h	0	1	0	0	0	0	0	HUE ADJUST REGISTER
21h	0	1	0	0	0	0	1	BRIGHTNESS CONTROL REGISTER
22h	0	1	0	0	0	1	0	SHARPNESS CONTROL REGISTER
23h	0	1	0	0	0	1	1	RESERVED
24h	0	1	0	0	1	0	0	....
...	.	.	.	.	.	.	.	....
...	.	.	.	.	.	.	.	....
...	.	.	.	.	.	.	.	....
3Ah	0	1	1	1	0	1	0	MACROVISION REGISTER [ADV7172 ONLY]
3Bh	0	1	1	1	0	1	1	MACROVISION REGISTER [ADV7172 ONLY]
3Ch	0	1	1	1	1	0	0	MACROVISION REGISTER [ADV7172 ONLY]
3Dh	0	1	1	1	1	0	1	MACROVISION REGISTER [ADV7172 ONLY]
3Eh	0	1	1	1	1	1	0	MACROVISION REGISTER [ADV7172 ONLY]
3Fh	1	1	1	1	1	1	1	MACROVISION REGISTER [ADV7172 ONLY]
40h	1	0	0	0	0	0	0	MACROVISION REGISTER [ADV7172 ONLY]
41h	1	0	0	0	0	0	1	MACROVISION REGISTER [ADV7172 ONLY]
42h	1	0	0	0	0	1	0	MACROVISION REGISTER [ADV7172 ONLY]
43h	1	0	0	0	0	1	1	MACROVISION REGISTER [ADV7172 ONLY]
44h	1	0	0	0	1	0	0	MACROVISION REGISTER [ADV7172 ONLY]
45h	1	0	0	0	1	0	1	MACROVISION REGISTER [ADV7172 ONLY]
46h	1	0	0	0	1	1	0	MACROVISION REGISTER [ADV7172 ONLY]
47h	1	0	0	1	1	1	1	MACROVISION REGISTER [ADV7172 ONLY]
48h	1	0	0	1	0	0	0	MACROVISION REGISTER [ADV7172 ONLY]
49h	1	0	0	1	0	0	1	MACROVISION REGISTER [ADV7172 ONLY]
4Ah	1	0	0	1	0	1	0	MACROVISION REGISTER [ADV7172 ONLY]
4Bh	1	0	0	1	0	1	1	MACROVISION REGISTER [ADV7172 ONLY]

Figure 43. Subaddress Register

MODE REGISTER 0 MR0 (MR07–MR00)
(Address (SR4–SR0) = 00H)
Figure 44 shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION
Output Video Standard Selection (MR01–MR00)
These bits are used to set up the encoder mode. The ADV7172/ ADV7173 can be set up to output NTSC, PAL (B, D, G, H, I), PAL M or PAL N standard video.

Luma Filter Select (MR02–MR04)
These bits specify which luma filter is to be selected. The filter selection is made independent of whether PAL or NTSC is selected.

Chroma Filter Select (MR05–MR07)
These bits select the chroma filter. A low-pass filter can be selected with a choice of cutoff frequencies (0.65 MHz, 1.0 MHz, 1.3 MHz, or 2 MHz), along with a choice of CIF or QCIF filters.

MODE REGISTER 1 MR1 (MR17–MR10)
(Address (SR4–SR0) = 01H)
Figure 45 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION
DAC Control (MR15–MR10)
MR15–MR10 bits can be used to power down the DACs. This can be used to reduce the power consumption of the ADV7172/ ADV7173 if any of the DACs are not required in the application.

Low Power Mode Control (MR16)
This bit enables the lower power mode of the ADV7172/ ADV7173. This will reduce by approximately 50% the average supply current consumed by each large DAC which is powered on. For each DAC in low power mode, the relationship between R_{SET1}/V_{REF} and the output current is unchanged by this (see Appendix 8). This bit is only relevant to the larger DACs, DACs A, B, and C. DACs D, E, and F are not affected by this low power mode.

Reserved (MR17)
A Logic "0" must be written to this bit.

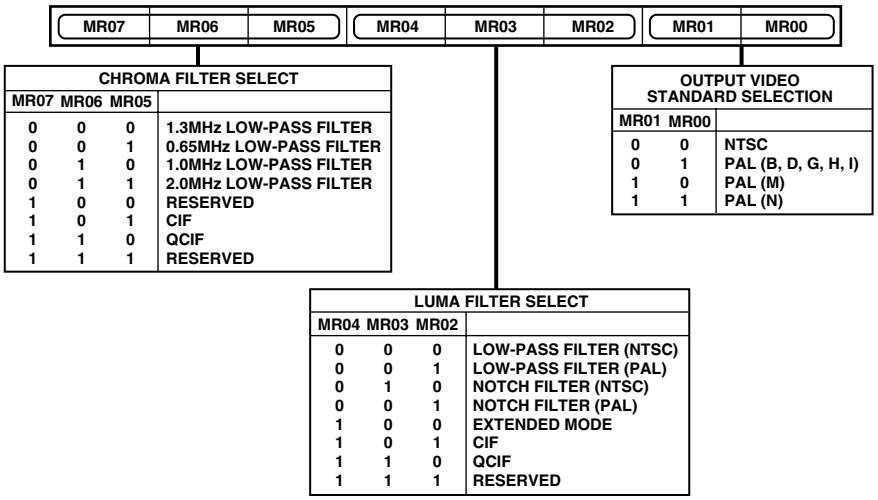


Figure 44. Mode Register 0 (MR0)

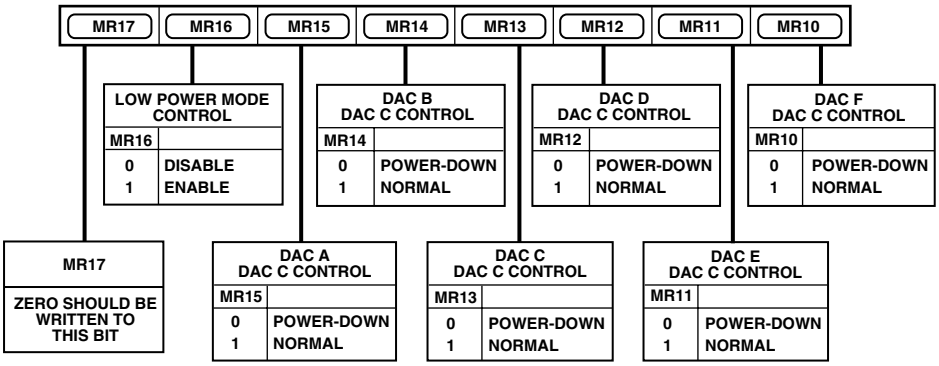


Figure 45. Mode Register 1 (MR1)

MODE REGISTER 2 MR2 (MR27–MR20)
(Address (SR4–SR0) = 02H)
Mode Register 2 is an 8-bit-wide register.

Figure 46 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION

RGB/YUV Control (MR20)
This bit enables the output from the DACs to be set to YUV or RGB output video standard.

Large DACs Control (MR21)
This bit controls the output from DACs A, B, and C. When this bit is set to "1," composite, luma, and chroma signals are output from DACs A, B, and C (respectively). When this bit is set to "0," RGB or YUV may be output from these DACs.

SCART Enable Control (MR22)
This bit is used to switch the DAC outputs from SCART to a EuroSCART configuration. A complete table of all DAC output configurations is shown in Table II.

Pedestal Control (MR23)
This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid in the PAL mode.

Square Pixel Control (MR24)
This bit is used to set up square pixel mode. This is available in slave mode only. For NTSC, a 24.54 MHz clock must be supplied. For PAL, a 29.5 MHz clock must be supplied.

Standard I²C Control (MR25)
This bit controls the video standard used by the ADV7172/ADV7173. When this bit is set to "1," the video standard bits programmed in Mode Register 0, Bits 0–1, indicate the video standard. When this bit is set to "0," the ADV7172/ADV7173 is forced into the standard selected by the NTSC_PAL pin.

Pixel Data Valid Control (MR26)
After reset, this bit has the value "0" and the pixel data input to the encoder is blanked such that a black screen is output from the DACs. The ADV7172/ADV7173 will be set to master mode timing. When this bit is set to "1" by the user (via the I²C), pixel data passes to the pins and the encoder reverts to the timing mode defined by Timing Mode Register 0.

Sleep Mode Control (MR27)
When this bit is set ("1"), sleep mode is enabled. With this mode enabled the ADV7172/ADV7173 power consumption is reduced to less than 20 μA. The I²C registers can be written to and read from when the ADV7172/ADV7173 is in sleep mode. If "0" is written to MR27 when the device is in sleep mode, the ADV7172/ADV7173 will come out of sleep mode and resume normal operation. Also, if the reset signal is applied during sleep mode, the ADV7172/ADV7173 will come out of sleep mode and resume normal operation. This mode will only operate when MR60 is set to a Logic "1"; otherwise sleep mode is controlled by the PAL_NTSC and SCRESET/RTC pin.

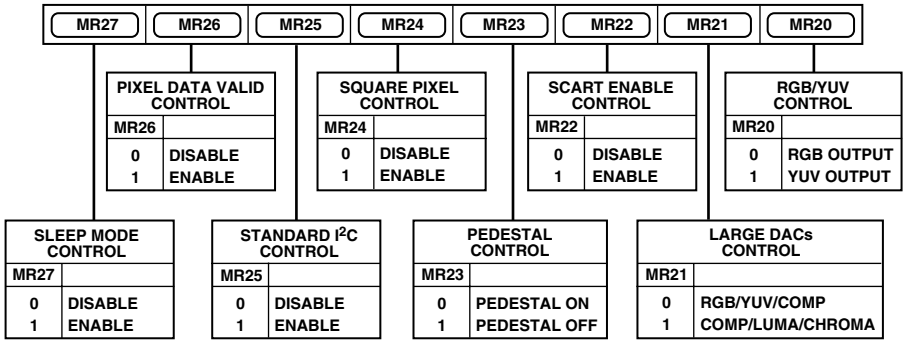


Figure 46. Mode Register 2 (MR2)

Table II. DAC Output Configuration Matrix

MR22	MR21	MR20	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
0	0	0	G	B	R	CVBS	LUMA	CHROMA
0	0	1	Y	U	V	CVBS	LUMA	CHROMA
0	1	0	CVBS	LUMA	CHROMA	G	B	R
0	1	1	CVBS	LUMA	CHROMA	Y	U	V
1	0	0	CVBS	B	R	G	LUMA	CHROMA
1	0	1	CVBS	U	V	Y	LUMA	CHROMA
1	1	0	CVBS	LUMA	CHROMA	G	B	R
1	1	1	CVBS	LUMA	CHROMA	Y	U	V

MODE REGISTER 3 MR3 (MR37–MR30)
(Address (SR4–SR0) = 03H)
Mode Register 3 is an 8-bit-wide register. Figure 47 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
Revision Code (MR31–MR30)
This bit is read-only and indicates the revision of the device.

VBI_Open (MR32)
This bit determines whether or not data in the vertical blanking interval (VBI) is output to the analog outputs or blanked. VBI_Open is available in all timing modes. Also, if both $\overline{\text{BLANK}}$ input (TR03) and VBI_Open are enabled, TR03 takes priority.

Teletext Enable (MR33)
This bit must be set to "1" to enable teletext data insertion on the TTX pin.

TTXRQ Bit Mode Control (MR34)
This bit enables switching of the teletext request signal from a continuous high signal (MR34 = "0") to a bit wise request signal (MR34 = "1").

Closed Captioning Field Selection (MR36–MR35)
These bits control the fields that closed captioning data is displayed on. Closed captioning information can be displayed on an odd field, even field, or both fields.

Active Video Filter (MR37)
This bit controls the filter mode applied outside the active video portion of the line. This filter ensures that the sync rise and fall times are always on spec regardless of which luma filter is selected.

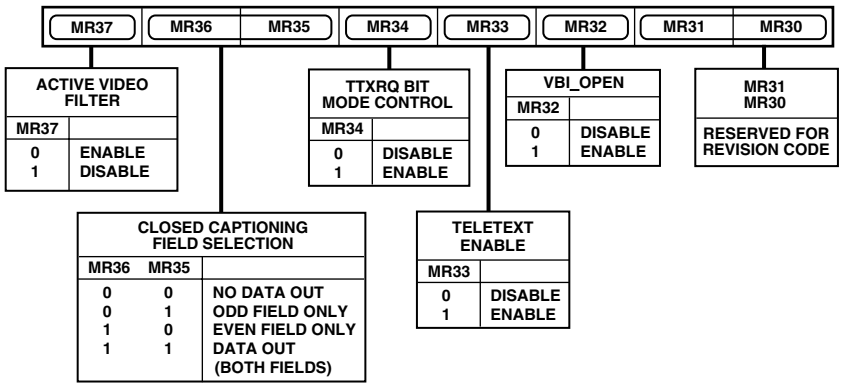


Figure 47. Mode Register 3 (MR3)

MODE REGISTER 4 MR4 (MR47–MR40)
(Address (SR4–SR0) = 04H)
Mode Register 4 is a 8-bit wide register. Figure 48 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
$\overline{\text{VSYNC}}$_3H (MR40)
When this bit is enabled ("1") in slave mode, it is possible to drive the $\overline{\text{VSYNC}}$ active low input for 2.5 lines in PAL mode and 3 lines in NTSC mode. When this bit is enabled in master mode, the ADV7172/ADV7173 outputs an active low $\overline{\text{VSYNC}}$ signal for 3 lines in NTSC mode and 2.5 lines in PAL mode.

Genlock Selection (MR42–MR41)
These bits control the genlock feature of the ADV7172/ADV7173. Setting MR41 to Logic "0" disables the SCRESET/RTC pin and allows the ADV7172/ADV7173 to operate in normal mode. By setting MR41 to "1," one of two operations may be enabled:

1. If MR42 is set to "0," the SCRESET/RTC pin is configured as a subcarrier reset input and the subcarrier phase will reset to Field 0 whenever a low-to-high field transition is detected on the SCRESET/RTC pin.
2. If MR42 is set to "1," the SCRESET/RTC pin is configured as a real-time control input and the ADV7172/ADV7173 can be used to lock to an external video source.

Active Video Line Duration (MR43)
This bit switches between two active video line durations. A "0" selects CCIR REC 601 (720 pixels PAL/NTSC) and a "1" selects ITU-R.BT 470 "analog" standard for active video duration (710 pixels NTSC, 702 pixels PAL).

Chrominance Control (MR44)
This bit enables the color information to be switched on and off the video output.

Burst Control (MR45)
This bit enables the color burst information to be switched on and off the video output.

Color Bar Control (MR46)
This bit can be used to generate and output an internal color bar test pattern. The color bar configuration is 100/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL. It is important to note that when color bars are enabled, the ADV7172/ADV7173 is configured in a master timing mode. The output pins $\overline{\text{VSYNC}}$/FIELD, $\overline{\text{HSYNC}}$ and $\overline{\text{BLANK}}$ are three-state during color bar mode.

Interlaced Mode Control (MR47)
This bit is used to set up the output to interlaced or noninterlaced mode.

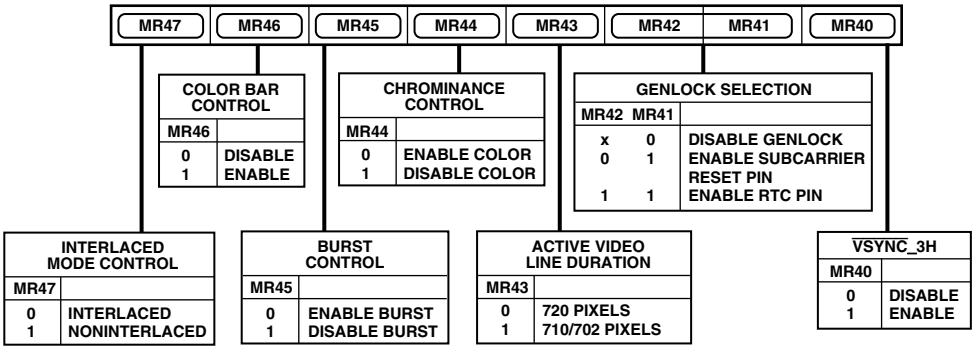


Figure 48. Mode Register 4 (MR4)

MODE REGISTER 5 MR5 (MR57–MR50)
(Address (SR4-SR0) = 05H)
Mode Register 5 is an 8-bit-wide register. Figure 49 shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION

Y-Level Control (MR50)
This bit controls the Y output level on the ADV7172/ADV7173. If this bit is set ("0"), the encoder outputs SMPTE levels when configured in PAL mode and Betacam levels when configured in NTSC mode. If this bit is set ("1"), the encoder outputs Betacam levels when configured in PAL mode and SMPTE levels when configured in NTSC mode.

UV-Levels Control (MR52–MR51)
These bits control the U and V output levels on the ADV7172/ADV7173. It is possible to have UV levels with a peak-peak amplitude of either 700 mV (MR52 + MR51 = "01") or 1000 mV (MR52 + MR51 = "10") in NTSC and PAL. It is also possible to have default values of 934 mV for NTSC and 700 mV for PAL (MR52 + MR51 = "00").

RGB Sync (MR53)
This bit is used to set up the RGB outputs with the sync information encoded on all RGB outputs.

Clamp Delay (MR55–MR54)
These bits control the delay or advance of the CLAMP signal in the front or back porch of the ADV7172/ADV7173. It is possible to delay or advance the pulse by 0, 1, 2 or 3 clock cycles.

Clamp Delay Direction (MR56)
This bit controls a positive or negative delay in the CLAMP signal. If this bit is set ("1"), the delay is negative. If it is not set ("0"), the delay is positive.

Clamp Position (MR57)
This bit controls the position of the CLAMP signal. If this bit is set ("1"), the CLAMP signal is located in the back porch position. If this bit is set to ("0"), the CLAMP signal is located in the front porch position.

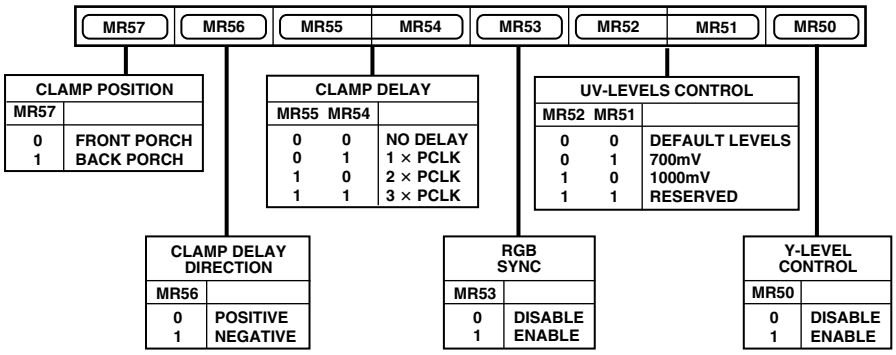


Figure 49. Mode Register 5 (MR5)

MODE REGISTER 6 MR6 (MR67–MR60)
(Address (SR4–SR0) = 06H)
Mode Register 6 is an 8-bit-wide register. Figure 50 shows the various operations under the control of Mode Register 6.

MR6 BIT DESCRIPTION

Power-Up Sleep Mode Control (MR60)
After reset this bit is set to "0," if both SCRESET/RTC and NTSC_PAL pins are tied high, the part will power-up in sleep mode (to facilitate low power consumption before the I^2C is initialized). When this bit is set to "1" (via the I^2C), sleep mode control passes to Mode Register 2, Bit 7.

Reserved (MR61)
A Logic "0" must be written to this bit.

Luma Autodetect Control (MR62)
This bit controls which mode of autodetect operation is being used on the luma DAC (DAC B) on the ADV7172/ADV7173. If this bit is set ("0"), Mode 0 is on; if this bit is set ("1"), then Mode 1 is being used.

Composite Autodetect Control (MR63)
This bit controls which mode of autodetect operation is being used on the composite DAC (DAC A) on the ADV7172/ ADV7173. If this bit is set ("0"), Mode 0 is on; if this bit is set ("1"), then Mode 1 is being used.

DAC Termination Control (MR64)
This bit controls the load termination resistance detected by the autodetect functionality. If this bit is set ("0"), the autodetect feature is used to determine if a 75 Ω termination is present. If this bit is set to ("1"), the autodetect feature is used to indicate if a 150 Ω termination is present.

Reserved (MR65)
A Logic "0" must be written to this bit.

Luma DAC Status Bit (MR66)
This bit is a read-only status bit for the autodetect feature of the ADV7172/ADV7173 and may be read to check whether or not the composite DAC is terminated. If this bit is set ("1"), there is no termination; if this bit is set ("0"), the composite DAC is terminated.

Composite DAC Status Bit (MR67)
This bit is a read only status bit for the autodetect feature of the ADV7172/ADV7173 and may be read to check whether or not the luma DAC is terminated. If this bit is set ("1"), there is no termination. If this bit is set ("0"), the luma DAC is terminated.

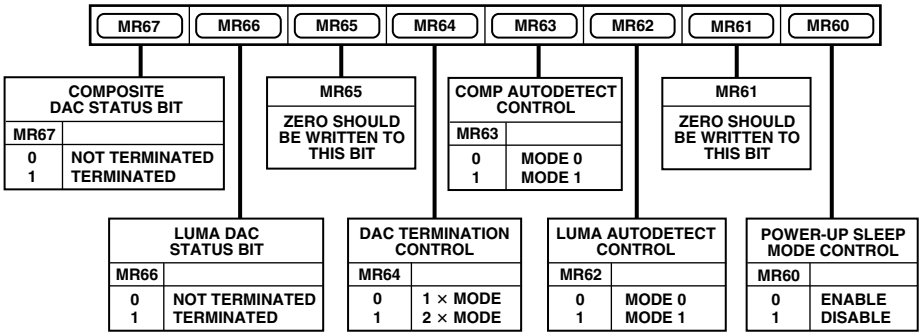


Figure 50. Mode Register 6 (MR6)

MODE REGISTER 7 MR7 (MR77–MR70)
(Address (SR4–SR0) = 07H)
Mode Register 7 is an 8-bit-wide register. Figure 51 shows the various operations under the control of Mode Register 7.

MR7 BIT DESCRIPTION

Color Control Enable (MR70)
This bit is used to enable control of contrast and saturation of color. If this bit is set ("1"), color controls are enabled; if this bit is set ("0"), the color control features are disabled.

Luma Saturation Control (MR71)
When this bit is set ("1"), the luma signal will be clipped if it reaches a limit that corresponds to an input luma value of 255 after scaling by the contrast control. This prevents the chrominance component of the composite video signal being clipped if the amplitude of the luma is too high. When this bit is set ("0"), this control is disabled.

Hue Adjust Enable (MR72)
This bit is used to enable hue adjustment on the composite and chroma output signals of the ADV7172/ADV7173. When this bit is set ("1"), the hue of the color is adjusted by the phase offset described in the Hue Control Register. When this bit is set ("0") hue adjustment is disabled.

Brightness Enable Control (MR73)
This bit is used to enable brightness control on the ADV7172/ADV7173 by enabling the programmable "setup level" or pedestal described in the Brightness Control Register to be added to the scaled Y data. When this bit is set ("1"), brightness control is enabled. When this bit is set ("0"), brightness control is disabled.

Sharpness Response Enable (MR74)
This bit is used to enable the sharpness of the luminance signal on the ADV7172/ADV7173 (MR04–MR02 = 100). The various responses of the filter are determined by the Sharpness Response Register. When this bit is set ("1") the luma response is altered by the amount described in the Sharpness Response Register. When this bit is set ("0"), the sharpness control is disabled (see Figures 19, 20, and 21 for luma signal responses).

$\overline{\text{CSO\_HSO}}$ Output Control (MR75)
This bit is used to determine whether $\overline{\text{HSO}}$ or $\overline{\text{CSO}}$ TTL output signal is output at the $\overline{\text{CSO\_HSO}}$ pin. If this bit is set ("1"), then the $\overline{\text{CSO}}$ TTL signal is output. If this bit is set ("0"), then the $\overline{\text{HSO}}$ TTL signal is output.

Reserved (MR77–MR76)
A Logic "0" must be written to these bits.

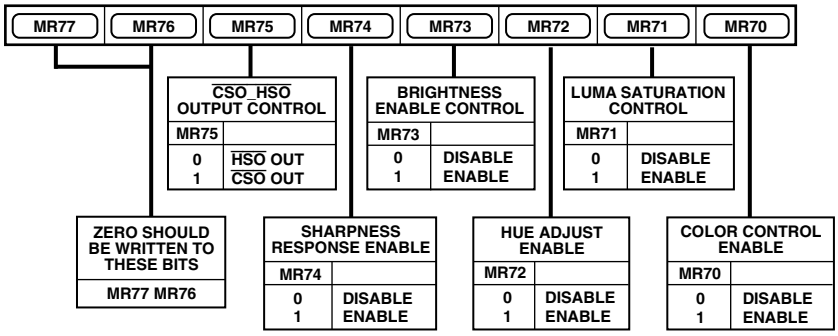


Figure 51. Mode Register 7 (MR7)

TIMING REGISTER 0 (TR07–TR00)
(Address (SR4–SR0) = 0AH)
Figure 52 shows the various operations under the control of Timing Register 0. This register can be read from as well as written to.

TR0 BIT DESCRIPTION
Master/Slave Control (TR00)
This bit controls whether the ADV7172/ADV7173 is in master or slave mode.

Timing Mode Selection (TR02–TR01)
These bits control the timing mode of the ADV7172/ADV7173. These modes are described in more detail in the Timing and Control section of the data sheet.

$\overline{\text{BLANK}}$ Input Control (TR03)
This bit controls whether the $\overline{\text{BLANK}}$ input is used when the part is in slave mode or whether $\overline{\text{BLANK}}$ is internally generated.

Luma Delay (TR05–TR04)
These bits control the addition of a delay to the luminance with respect to the chrominance. Each bit represents a delay of 74 ns.

Min Luma Value (TR06)
The bit is used to control the minimum luma value output by the ADV7172/ADV7173. When this bit is set to ("1"), the luma is limited to 7.5 IRE below the blank level. When this bit is set to ("0"), the luma value can be as low as the sync bottom level.

Timing Register Reset (TR07)
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after power-up, reset or changed to a new timing mode.

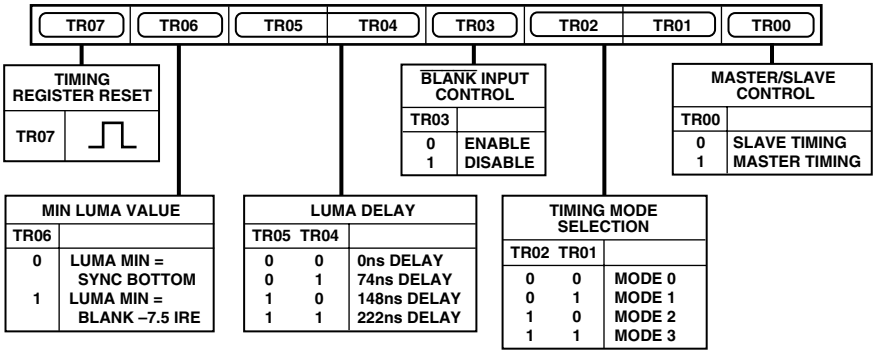


Figure 52. Timing Register 0

TIMING REGISTER 1 (TR17–TR10)
(Address (SR4–SR0) = 0BH)
Timing Register 1 is an 8-bit-wide register.

Figure 53 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

TR1 BIT DESCRIPTION
$\overline{\text{HSYNC}}$ Width (TR11–TR10)
These bits adjust the $\overline{\text{HSYNC}}$ pulsewidth.

$\overline{\text{HSYNC}}$ to FIELD/$\overline{\text{VSYNC}}$ Delay (TR13–TR12)
These bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD/$\overline{\text{VSYNC}}$ output.

$\overline{\text{HSYNC}}$ to FIELD Rising Edge Delay (TR15–TR14)
When the ADV7172/ADV7173 is in Timing Mode 1, these bits adjust the position of the $\overline{\text{HSYNC}}$ output relative to the FIELD output rising edge.

$\overline{\text{VSYNC}}$ Width (TR15–TR14)
When the ADV7172/ADV7173 is configured in Timing Mode 2, these bits adjust the $\overline{\text{VSYNC}}$ pulsewidth.

$\overline{\text{HSYNC}}$ to Pixel Data Adjust (TR17–TR16)
This enables the $\overline{\text{HSYNC}}$ to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.

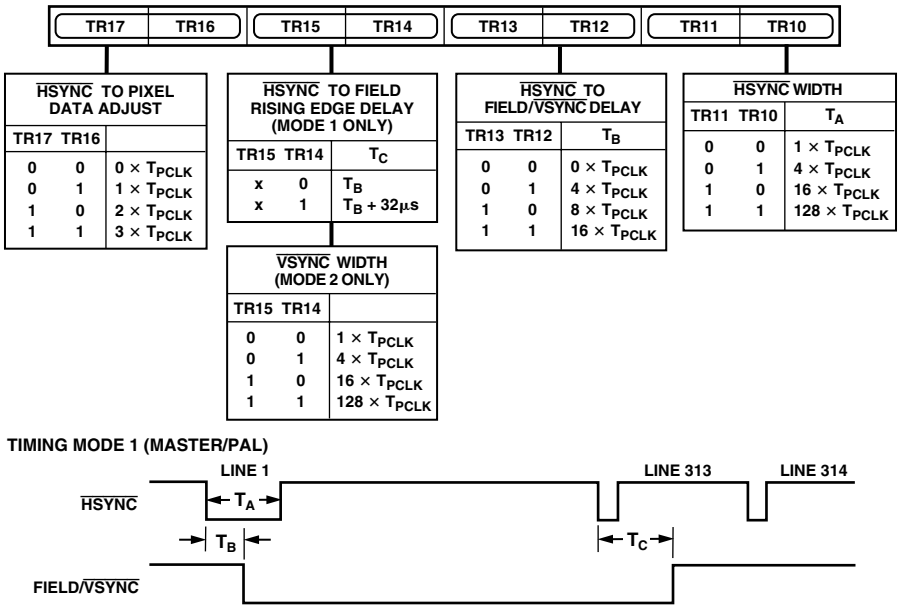


Figure 53. Timing Register 1

SUBCARRIER FREQUENCY REGISTERS 3–0 (FSC3–FSC0)
(Address (SR4–SR0) = 0CH–0FH)

These 8-bit-wide registers are used to set up the subcarrier frequency. The value of these registers is calculated by using the following equation:

$$Subcarrier\ Frequency\ Register = \frac{2^{32}-1}{f_{CLK}} \times f_{SCF}$$

Example: NTSC Mode,

f_{CLK} = 27 MHz,

f_{SCF} = 3.5795454 MHz

$$Subcarrier\ Frequency\ Value = \frac{2^{32}-1}{27\times10^{6}} \times 3.579454\times10^{6}$$

$$= 21F07C16\ HEX$$

Figure 54 shows how the frequency is set up by the four registers.

SUBCARRIER PHASE REGISTER (FP7–FP0)
(Address (SR4–SR0) = 10H)

This 8-bit-wide register is used to set up the subcarrier phase. Each bit represents 1.41°. For normal operation this register is set to 00Hex.

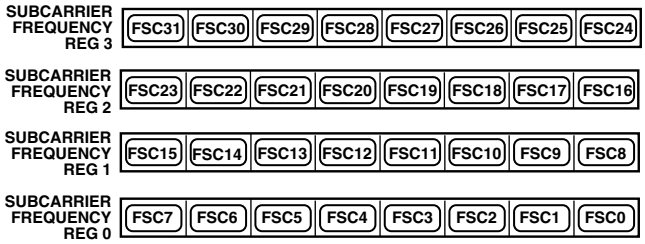


Figure 54. Subcarrier Frequency Registers

CLOSED CAPTIONING EVEN FIELD DATA REGISTER 1–0 (CED15–CED0)
(Address (SR4–SR0) = 11–12H)

These 8-bit wide registers are used to set up the closed captioning extended data bytes on even fields. Figure 55 shows how the high and low bytes are set up in the registers.

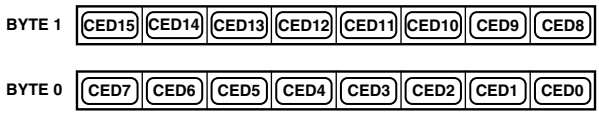


Figure 55. Closed Captioning Extended Data Register

CLOSED CAPTIONING ODD FIELD DATA REGISTER 1–0 (CCD15–CCD00)
(Subaddress (SR4–SR0) = 13–14H)

These 8-bit-wide registers are used to set up the closed captioning data bytes on odd fields. Figure 56 shows how the high and low bytes are set up in the registers.

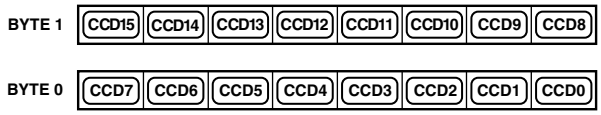


Figure 56. Closed Captioning Data Register

NTSC PEDESTAL/PAL TELETEXT CONTROL REGISTERS 3–0 (PCE15–0, PCO15–0)/(TXE15–0, TXO15–0)
(Subaddress (SR4–SR0) = 15–18H)

These 8-bit-wide registers are used to enable the NTSC pedestal/PAL Teletext on a line-by-line basis in the vertical blanking interval for both odd and even fields. Figures 57 and 58 show the four control registers. A Logic "1" in any of the bits of these registers has the effect of turning the Pedestal OFF on the equivalent line when used in NTSC. A Logic "1" in any of the bits of these registers has the effect of turning Teletext ON on the equivalent line when used in PAL.

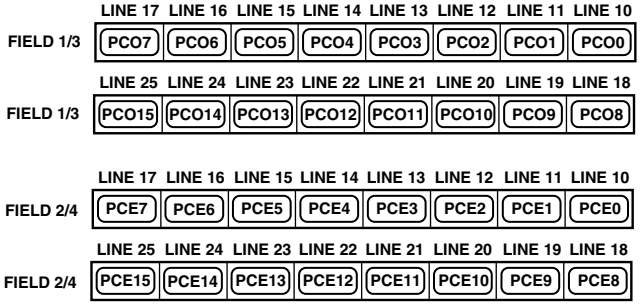


Figure 57. Pedestal Control Registers

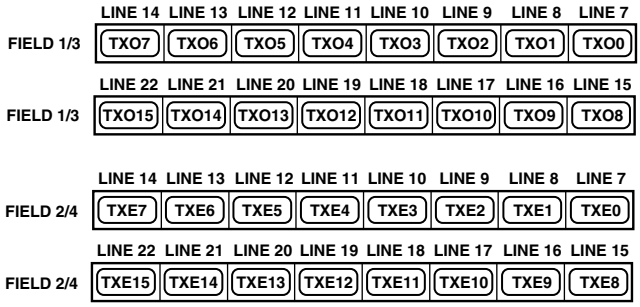


Figure 58. Teletext Control Registers

TELETEXT REQUEST CONTROL REGISTER TC07 (TC07–TC00)
(Address (SR4–SR0) = 1CH)
Teletext Control Register is an 8-bit-wide register. See Figure 59.

TTXREQ Rising Edge Control (TC07–TC04)
These bits control the position of the rising edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles.

TTXREQ Falling Edge Control (TC03–TC00)
These bits control the position of the falling edge of TTXREQ. It can be programmed from zero CLOCK cycles to a max of 15 CLOCK cycles. This controls the active window for Teletext data. Increasing this value reduces the amount of Teletext Bits below the default of 360. If Bits TC03–TC00 are 00Hex when Bits TC07–TC04 are changed, then the falling edge of TTXREQ will track that of the rising edge (i.e., the time between the falling and rising edge remains constant).

CGMS_WSS REGISTER 0 C/W0 (C/W07–C/W00)
(Address (SR4–SR0) = 19H)
CGMS_WSS Register 0 is an 8-bit-wide register. Figure 60 shows the operations under control of this register.

C/W BIT DESCRIPTION
CGMS Data (C/W03–C/W00)
These four data bits are the final four bits of CGMS data output stream. Note it is CGMS data ONLY in these bit positions i.e., WSS data does not share this location.

CGMS CRC Check Control (C/W04)
When this bit is enabled ("1"), the last six bits of the CGMS data, i.e., the CRC check sequence, are calculated internally by the ADV7172/ADV7173. If this bit is disabled ("0"), the CRC values in the register are output to the CGMS data stream.

CGMS Odd Field Control (C/W05)
When this bit is set ("1"), CGMS is enabled for odd fields. Note that this is only valid in NTSC mode.

CGMS Even Field Control (C/W06)
When this bit is set ("1"), CGMS is enabled for even fields. Note that this is only valid in NTSC mode.

Wide Screen Signal Control (C/W07)
When this bit is set ("1"), wide screen signalling is enabled. Note that this is only valid in PAL mode.

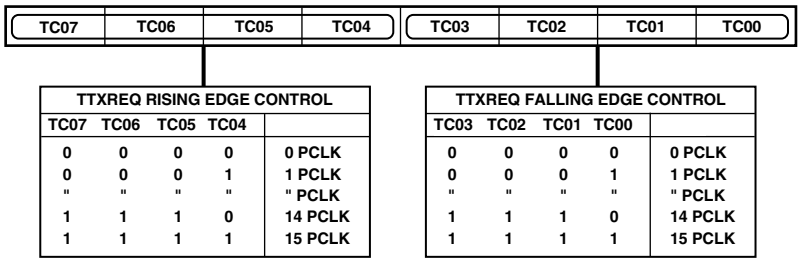


Figure 59. Teletext Request Control Register

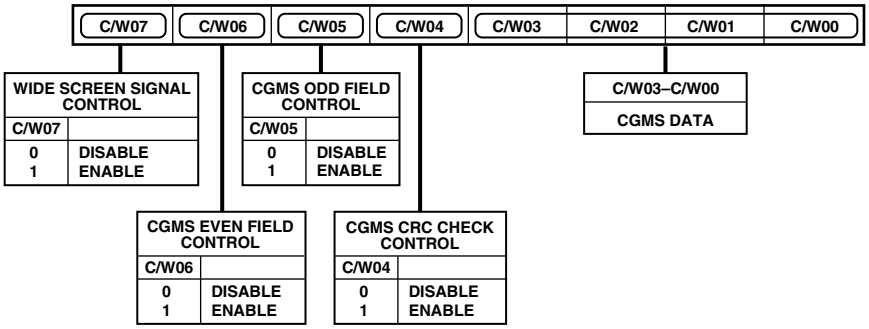


Figure 60. CGMS_WSS Register 0

CGMS_WSS REGISTER 1 C/W1 (C/W17–C/W10)
(Address (SR4–SR0) = 1AH)
CGMS_WSS Register 1 is an 8-bit-wide register. Figure 61 shows the operations under control of this register.

C/W1 BIT DESCRIPTION
CGMS/WSS Data (C/W15–C/W10)
These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

CGMS Data Only (C/W17–C/W16)
These bits are CGMS data bits only.

CGMS_WSS REGISTER 2 C/W1(C/W27–C/W20)
(Address (SR4-SR0) = 1BH)
CGMS_WSS Register 2 is an 8-bit-wide register. Figure 62 shows the operations under control of this register.

C/S BIT DESCRIPTION
CGMS/WSS Data (C/W27–C/W20)
These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

CONTRAST CONTROL REGISTER (CC07–CC00)
(Address (SR4–SR0) = 1DH)
The contrast control register is an 8-bit-wide register used to scale the Y output levels. Figure 63 shows the operations under control of this register.

CC0 BIT DESCRIPTION
Reserved (CC07–CC06)
A Logic "0" must be written to these bits.

Y Scalar Value (CC05–CC00)
These six bits represent the value required to scale the Y pixel data from 0.75 to 1.25 of its initial level. The value of these six bits is calculated using the following equation:

$$Contrast\ Control\ Register = (X - 0.785) \times 128$$

where X = Scaling factor for Y
e.g., Scale Y by 0.9

$$Contrast\ Control\ Register = (0.9 - 0.75) \times 128 = 19.2 = 010011$$

(rounded to the nearest integer)

Actual scaling factor = 0.898.

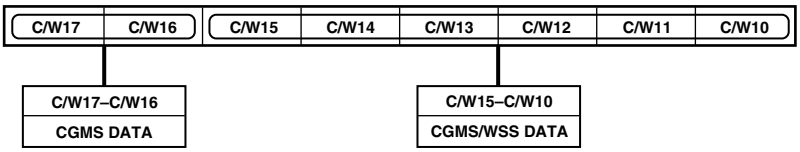


Figure 61. CGMS_WSS Register 1

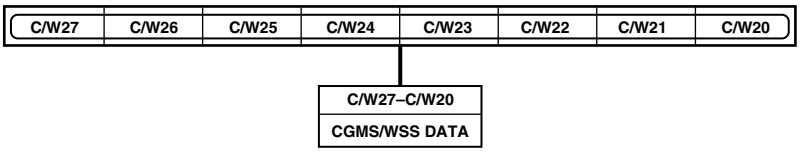


Figure 62. CGMS_WSS Register 2

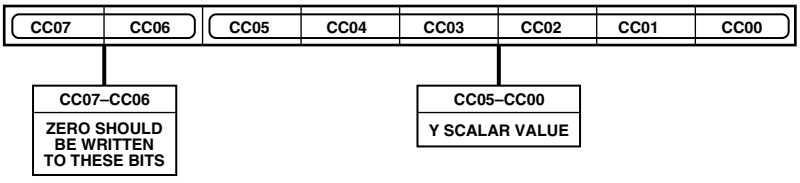


Figure 63. Contrast Control Register

COLOR CONTROL REGISTERS 2–1 (CC2–CC1)
(Address (SR4–SR0) = 1EH–1FH)
The color control registers are 8-bit-wide registers used to scale the U and V output levels. Figure 64 shows the operations under control of these registers.

CC1 BIT DESCRIPTION
Reserved (CC17–CC16)
A Logic "0" must be written to these bits.

U Scalar Value (CC15–CC10)
These six bits represent the value required to scale the U level from 0.75 to 1.25 of its initial level. The value of these six bits is calculated using the following equation:

$$Color\ Control\ Register\ 1 = (X - 0.75) \times 128$$

where X = Scaling factor for U
e.g., Scale U by 0.8

$$Color\ Control\ Register\ 1 = (0.8 - 0.75) \times 128 = 6.4 = 000110$$

(rounded to the nearest integer)

CC2 BIT DESCRIPTION
Reserved (CC27–CC26)
A Logic "0" must be written to these bits.

V Scalar Value (CC25–CC20)
These six bits represent the value required to scale the V pixel data from 0.75 to 1.25 of its initial level. The value of these six bits is calculated using the following equation:

$$Color\ Control\ Register\ 2 = (X - 0.75) \times 128$$

where X = Scaling factor for V
e.g., Scale V by 1.2

$$Color\ Control\ Register\ 2 = (1.2 - 0.75) \times 128 = 57.6 = 111001$$

(rounded to the nearest integer)

HUE CONTROL REGISTER (HCR)
(Address (SR5–SR0) = 20H)
The hue control register is an 8-bit-wide register used to adjust the hue on the composite and chroma outputs. Figure 65 shows the operation under control of this register.

HCR BIT DESCRIPTION
Hue Adjust Value (HCR7–HCR0)
These eight bits represent the value required to vary the hue of the video data, i.e., the variance in phase of the subcarrier with respect to the phase of the subcarrier during the color burst. The ADV7172/ADV7173 provides a range of ±22° in increments of 0.17578125°. For normal operation (zero adjustment) this register is set to 80 Hex. FFHex and 00Hex represent the upper and lower limit (respectively) of adjustment attainable.

$$Hue\ Adjust = (0.17568125 \times [HCR7 - HCR0 - 128]).$$

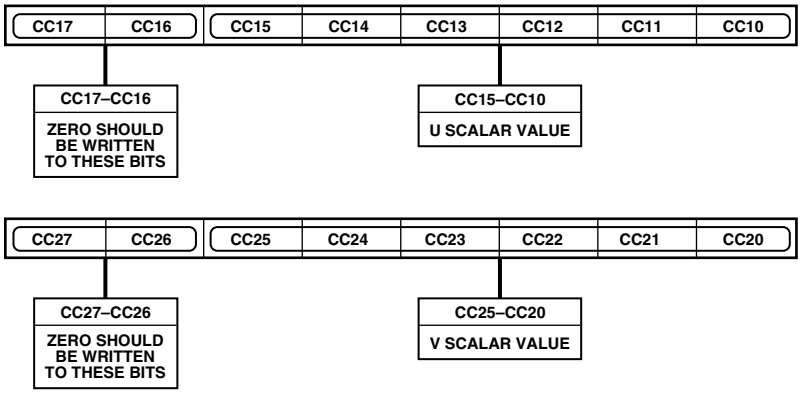


Figure 64. Color Control Registers

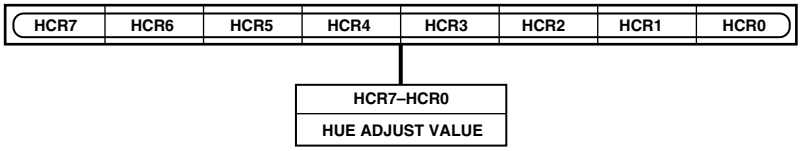


Figure 65. Hue Control Register

BRIGHTNESS CONTROL REGISTERS (BCR)
(Address (SR5–SR0) = 21H)
The brightness control register is an 8-bit-wide register which allows brightness control. Figure 66 shows the operation under control of this register.

BCR BIT DESCRIPTION
Reserved (BCR7–BCR5)
A Logic "0" must be written to these bits.

Brightness Value (BCR4–BCR0)
These five bits represent the value required to vary the "brightness level" or pedestal added to the luma data. The available range is from 0 IRE to 7.5 IRE in 18 steps. A value of 18 (10010) corresponds to 7.5 IRE setup level added onto the pixel data. This brightness control is possible in both PAL and NTSC.

SHARPNESS RESPONSE REGISTER (PR)
(Address (SR5-SR0) = 22H)
The sharpness response register is an 8-bit-wide register. The four MSBs are set to "0." The four LSBs are written to in order to select a desired filter response. Figure 67 shows the operation under control of this register.

PR BIT DESCRIPTION
Reserved (PR7–PR4)
A Logic "0" must be written to these bits.

Sharpness Response Value (PR3–PR0)
These four bits are used to select the desired luma filter response. The option of twelve responses is given supporting a gain boost/attenuation in the range –4 dB to +4 dB. The value 12 (1100) written to these four bits corresponds to a boost of +4 dB while the value 0 (0000) corresponds to –4 dB. For normal operation these four bits are set to 6 (0110). Refer to Figures 19–21 for filter plots.

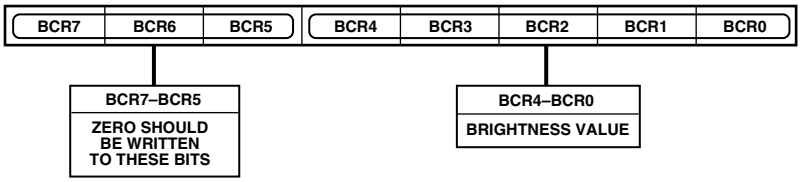


Figure 66. Brightness Control Register

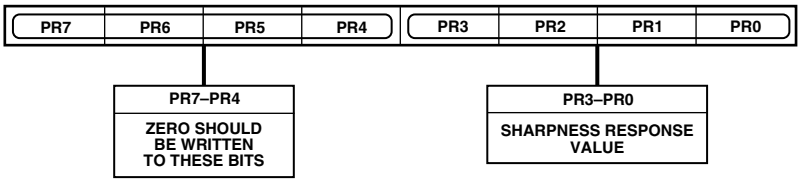


Figure 67. Sharpness Response Register

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7172/ADV7173 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design so that high speed, accurate performance is achieved. The Recommended Analog Circuit Layout shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7172/ADV7173 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized to minimize inductive ringing.

Ground Planes
The ground plane should encompass all ADV7172/ADV7173 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7172/ADV7173, the analog output traces, and all the digital signal traces leading up to the ADV7172/ADV7173. The ground plane is the board's common ground plane.

Power Planes
The ADV7172/ADV7173, and any associated analog circuitry, should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7172/ADV7173.

The metallization gap separating device power plane and board power plane should be as narrow as possible to minimize the obstruction to the flow of heat from the device into the general board.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7172/ADV7173 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane unless they can be arranged so that the plane-to-plane noise is common-mode.

Supply Decoupling
For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7172/ADV7173 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close to the device as possible.

It is important to note that while the ADV7172/ADV7173 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect
The digital inputs to the ADV7172/ADV7173 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7172/ADV7173 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}) and not the analog power plane.

Analog Signal Interconnect
The ADV7172/ADV7173 should be located as close to the output connectors as possible to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, not the analog power plane, to maximize the high frequency power supply rejection.

Digital inputs, especially pixel data inputs and clocking signals, should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7172/ADV7173 to minimize reflections.

The ADV7172/ADV7173 should have no inputs left floating. Any inputs that are not required should be tied to ground.

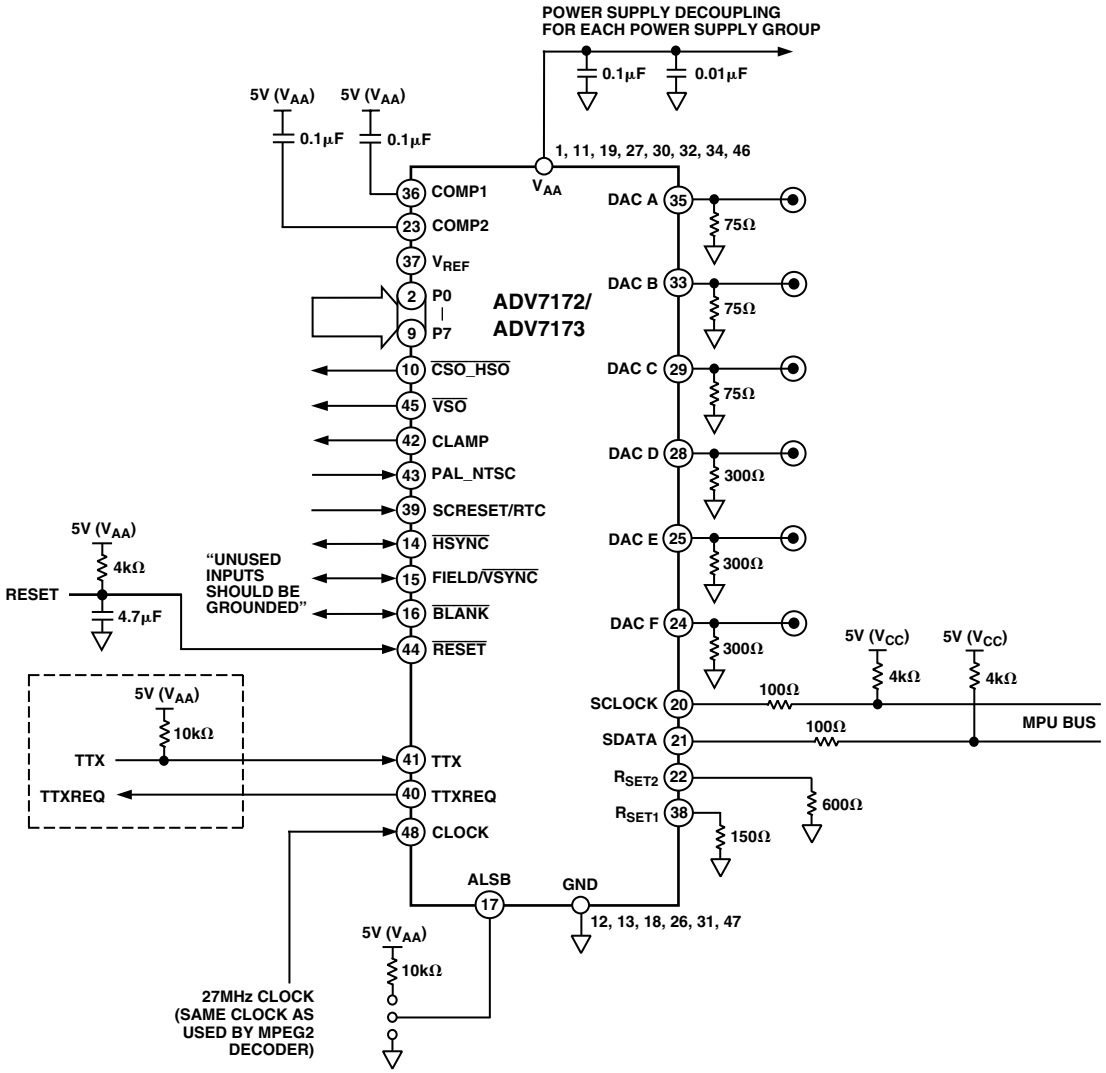


Figure 68. Recommended Analog Circuit Layout

APPENDIX 2

CLOSED CAPTIONING

The ADV7172/ADV7173 supports closed captioning, conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic Level "1" start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits and one odd parity bit. The data for these bytes is stored in closed captioning Data Registers 0 and 1.

The ADV7172/ADV7173 also supports the extended closed captioning operation, which is active during even fields, and is encoded on scan Line 284. The data for this operation is stored in closed captioning extended Data Registers 0 and 1.

All clock run-in signals, and timing to support closed captioning on Lines 21 and 284, are automatically generated by the ADV7172/ADV7173. All pixels inputs are ignored during Lines 21 and 284. Closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47 Section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7172/ADV7173 uses a single buffering method. This means that the closed captioning buffer is only one byte deep, therefore there will be no frame delay in outputting the closed captioning data, unlike other 2-byte deep buffering systems. The data must be loaded at least one line before (Line 20 or Line 283) it is outputted on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which will in turn load the new data (two bytes) every field. If no new data is required for transmission, zeros must be inserted in both data registers; this is called NULLING. It is also important to load "control codes," all of which are double bytes, on Line 21, or a TV will not recognize them. If there is a message like "Hello World," which has an odd number of characters, it is important to pad it out to an even number to get "end of caption" 2-byte control code to land in the same field.

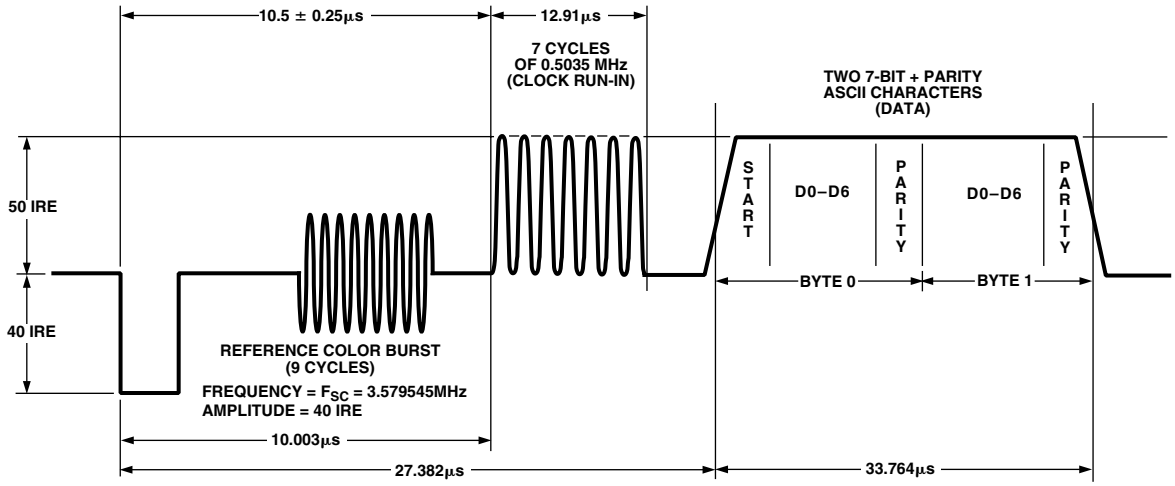


Figure 69. Closed Captioning Waveform (NTSC)

APPENDIX 3

COPY GENERATION MANAGEMENT SYSTEM (CGMS)

The ADV7172/ADV7173 supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of even fields. Bits C/W05 and C/W06 control whether or not CGMS data is output on ODD and EVEN fields. CGMS data can only be transmitted when the ADV7172/ADV7173 is configured in NTSC mode. The CGMS data is 20 bits long, the function of each of these bits is as shown below. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit (see Figure 70). These bits are output from the configuration registers in the following order: C/W00 = C16, C/W01 = C17, C/W02 = C18, C/W03 = C19, C/W10 = C8, C/W11 = C9, C/W12 = C10, C/W13 = C11, C/W14 = C12, C/W15 = C13, C/W16 = C14, C/W17 = C15, C/W20 = C0, C/W21 = C1, C/W22 = C2, C/W23 = C3, C/W24 = C4, C/W25 = C5, C/W26 = C6, C/W27 = C7. If the Bit C/W04 is set to a Logic "1," the last six bits, C19–C14, which comprise the 6-bit CRC check sequence, are calculated automatically on the ADV7172/ADV7173 based on the lower 14 bits (C0–C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $X^6 + X + 1$ with a preset value of 111111. If C/W04 is set to a Logic "0," all 20 bits (C0–C19) are directly output from the CGMS registers (no CRC calculated, must be calculated by the user).

Function of CGMS Bits

Word 0 – 6 Bits
Word 1 – 4 Bits
Word 2 – 6 Bits
CRC – 6 Bits CRC Polynomial = $X^6 + X + 1$ (Preset to 111111)

Word 0		1	0
B1	Aspect Ratio	16:9	4:3
B2	Display Format	Letterbox	Normal
B3	Undefined		

Word 0
B4, B5, B6 Identification information about video and other signals (e.g., audio)

Word 1
B7, B8, B9, B10 Identification signal incidental to Word 0

Word 2
B11, B12, B13, B14 Identification signal and information incidental to Word 0

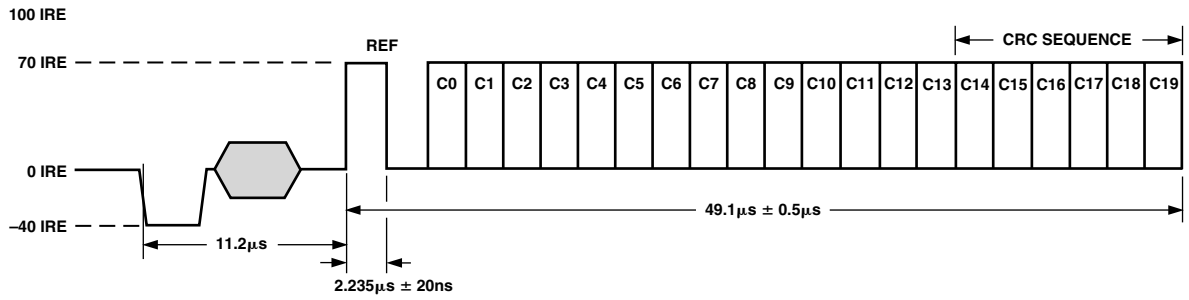


Figure 70. CGMS Waveform Diagram

APPENDIX 4

WIDE SCREEN SIGNALING

The ADV7172/ADV7173 supports Wide Screen Signaling (WSS) conforming to the standard. WSS data is transmitted on Line 23. WSS data can only be transmitted when the ADV7172/ADV7173 is configured in PAL mode. The WSS data is 14 bits long, the function of each of these bits is as shown below. The WSS data is preceded by a run-in sequence and a Start Code (see Figure 71). The bits are output from the configuration registers in the following order: C/W20 = W0, C/W21 = W1, C/W22 = W2, C/W23 = W3, C/W24 = W4, C/W25 = W5, C/W26 = W6, C/W27 = W7, C/W10 = W8, C/W11 = W9, C/W12 = W10, C/W13 = W11, C/W14 = W12, C/W15 = W13. If the Bit C/W07 is set to a Logic "1" it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5 µs from the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video.

Function of CGMS Bits

Bit 0–Bit 2 Aspect Ratio/Format/Position

Bit 3 is odd parity check of Bit 0–Bit 2

B0	B1	B2	B3	Aspect Ratio	Format	Position
0	0	0	1	4:3	Full Format	Nonapplicable
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	16:9	Letterbox	Top
1	0	1	1	>16:9	Letterbox	Center
0	1	1	1	14:9	Full Format	Center
1	1	1	0	16:9	Nonapplicable	Nonapplicable

B4	
0	Camera Mode
1	Film Mode
B5	
0	Standard Coding
1	Motion Adaptive Color Plus
B6	
0	No Helper
1	Modulated Helper
B7	RESERVED

B9 B10	
0 0	No Open Subtitles
1 0	Subtitles In Active Image Area
0 1	Subtitles Out of Active Image Area
1 1	Reserved
B11	
0	No Surround Sound Information
1	Surround Sound Mode
B12	RESERVED
B13	RESERVED

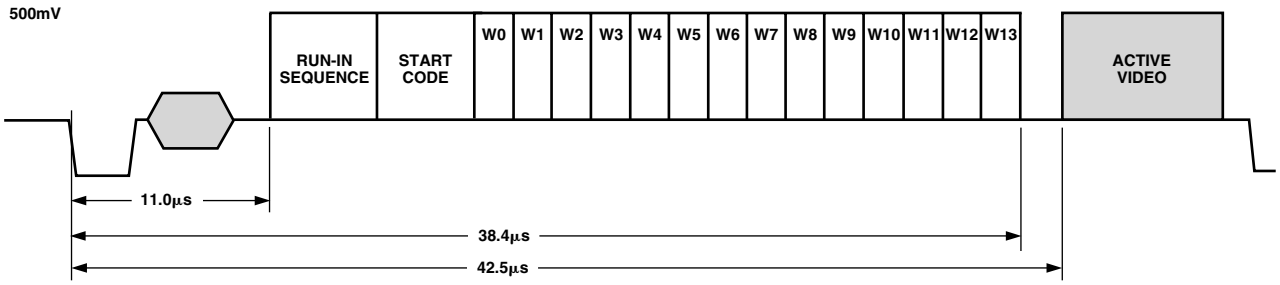


Figure 71. WSS Waveform Diagram

APPENDIX 5

TELETEXT INSERTION

Time, $t_{PD,}$ is the time needed by the ADV7172/ADV7173 to interpolate input data on TTX and insert it onto the CVBS or Y outputs, such that it appears $t_{SYNTTXOUT}$ = 10.2 µs after the leading edge of the horizontal signal. Time, TTX_{DEL}, is the pipeline delay time by the source that is gated by the TTXREQ signal in order to deliver TTX data.

With the programmability offered with TTXREQ signal on the Rising/Falling edges, the TTX data is always inserted at the correct position of 10.2 µs after the leading edge of horizontal sync pulse, thus enabling a source interface with variable pipeline delays.

The width of the TTXREQ signal must always be maintained such that it allows the insertion of 360 (in order to comply with the Teletext Standard "PAL-WST") teletext bits at a text data rate of 6.9375 Mbits/s. This is achieved by setting TC03–TC00 to "0." The insertion window is not open if the Teletext Enable (MR33) is set to "0."

Teletext Protocol

The relationship between the TTX bit clock (6.9375 MHz) and the system CLOCK (27 MHz) for 50 Hz is given as follows:

(27 MHz/4) = 6.75 MHz

$(6.9375 \times 10^6/6.75 \times 10^6) = 1.027777$

Thus 37 TTX bits correspond to 144 clocks (27 MHz) and each bit has a width of almost four clock cycles. The ADV7172/ADV7173 uses an internal sequencer and variable phase interpolation filter to minimize the phase jitter and thus generate a bandlimited signal that can be outputted on the CVBS and Y outputs.

At the TTX input the bit duration scheme repeats after every 37 TTX bits or 144 clock cycles. The protocol requires that TTX Bits 10, 19, 28, 37 are carried by three clock cycles, all other bits by four clock cycles. After 37 TTX bits, the next bits with three clock cycles are 47, 56, 65, and 74. This scheme holds for all following cycles of 37 TTX bits, until all 360 TTX bits are completed. All teletext lines are implemented in the same way. Individual control of teletext lines is controlled by Teletext Setup Registers.

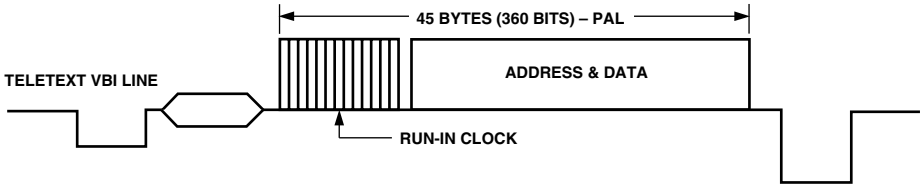


Figure 72. Teletext VBI Line

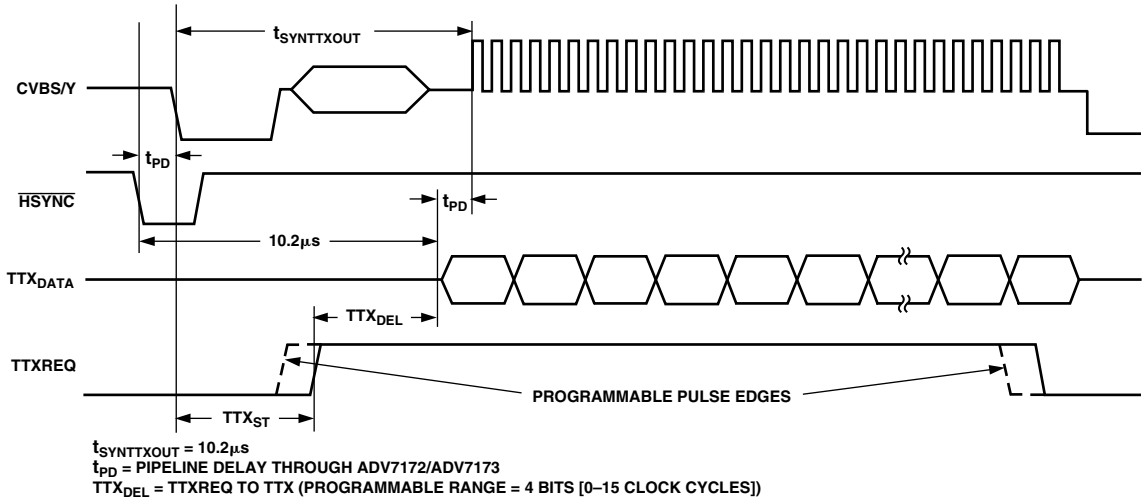


Figure 73. Teletext Functionality Diagram

APPENDIX 6

NTSC WAVEFORMS (WITH PEDESTAL)

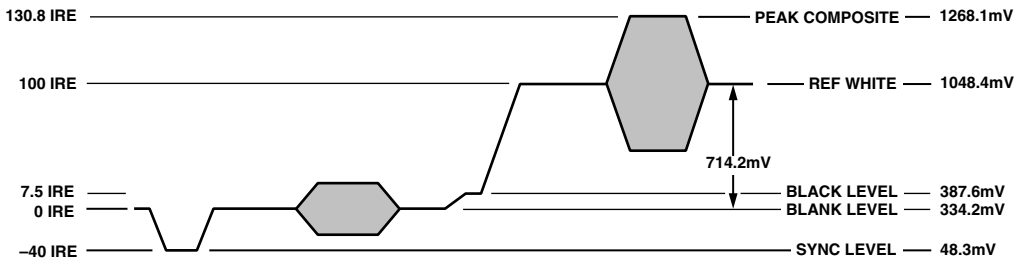


Figure 74. NTSC Composite Video Levels

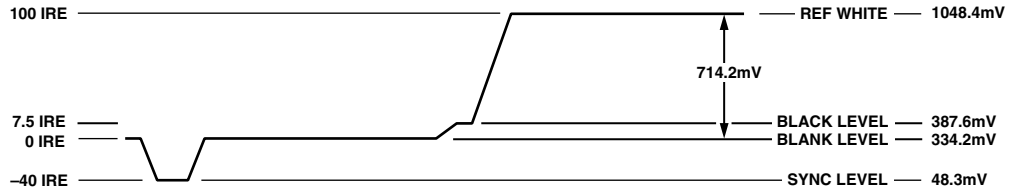


Figure 75. NTSC Luma Video Levels

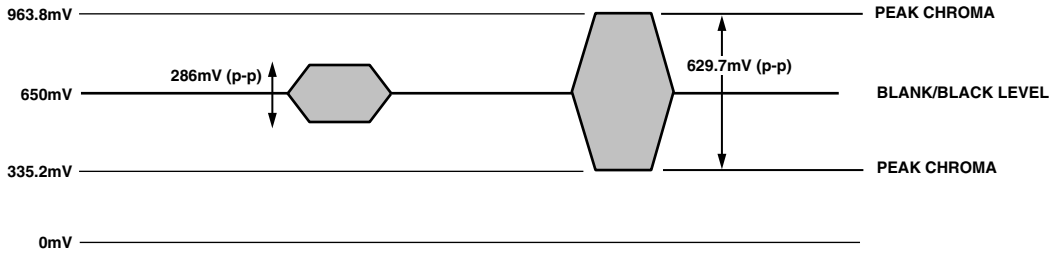


Figure 76. NTSC Chroma Video Levels

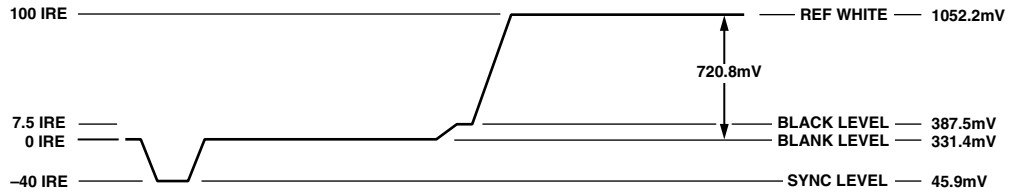


Figure 77. NTSC RGB Video Levels

NTSC WAVEFORMS (WITHOUT PEDESTAL)

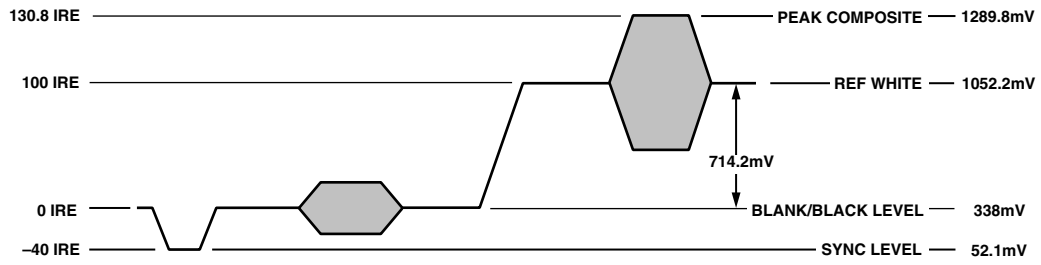


Figure 78. NTSC Composite Video Levels

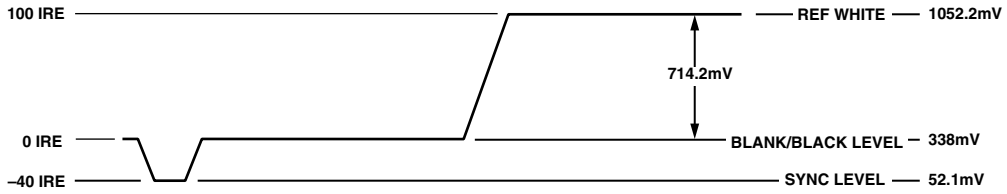


Figure 79. NTSC Luma Video Levels

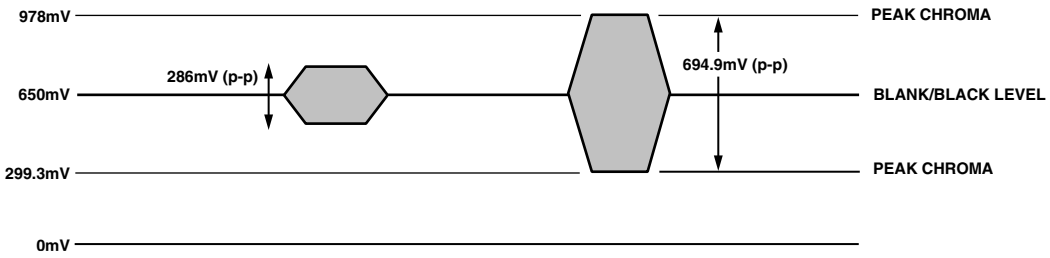


Figure 80. NTSC Chroma Video Levels

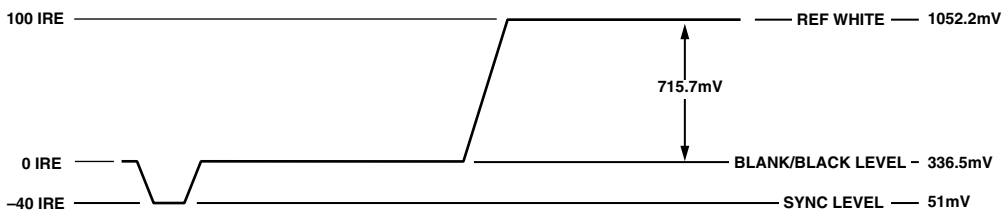


Figure 81. NTSC RGB Video Levels

PAL WAVEFORMS

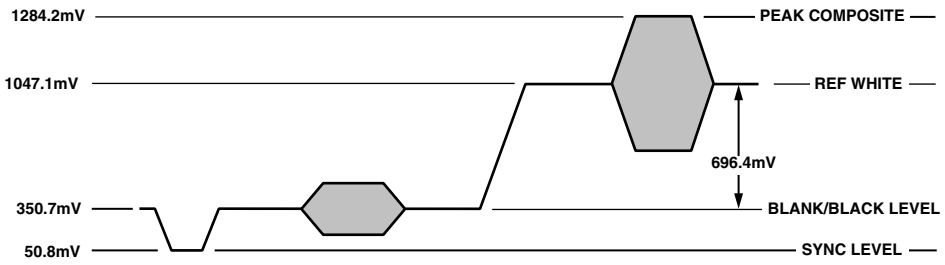


Figure 82. PAL Composite Video Levels

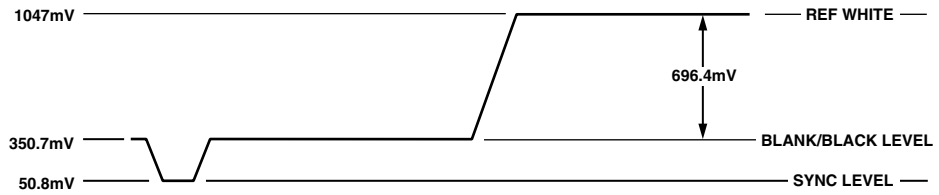


Figure 83. PAL Luma Video Levels

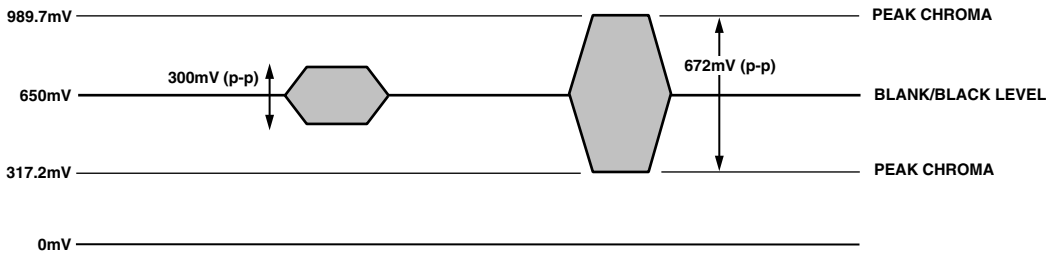


Figure 84. PAL Chroma Video Levels

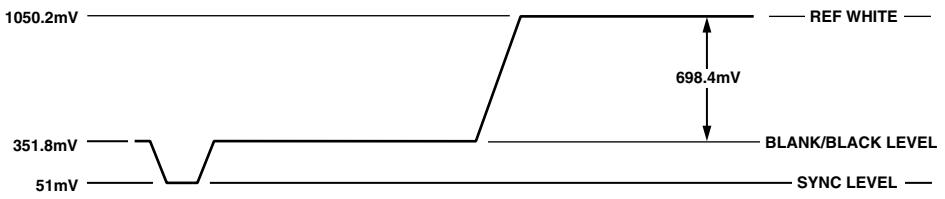


Figure 85. PAL RGB Video Levels

UV WAVEFORMS

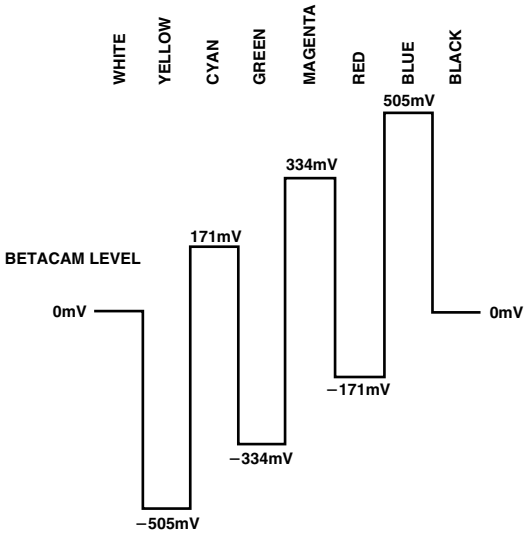


Figure 86. NTSC 100% Color Bars, No Pedestal U Levels

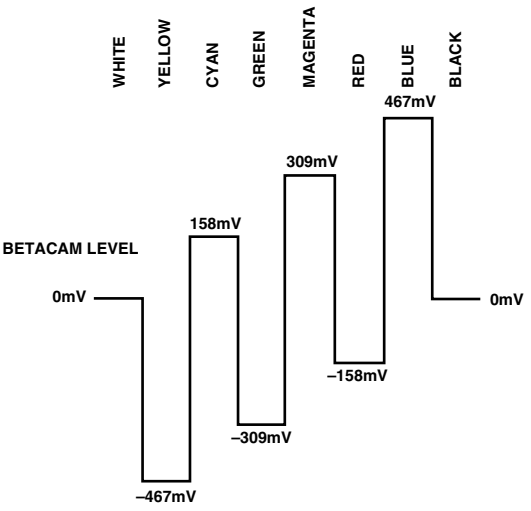


Figure 87. NTSC 100% Color Bars with Pedestal U Levels

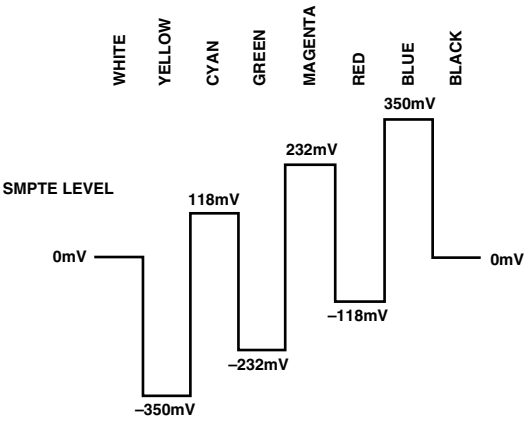


Figure 88. PAL 100% Color Bars, U Levels

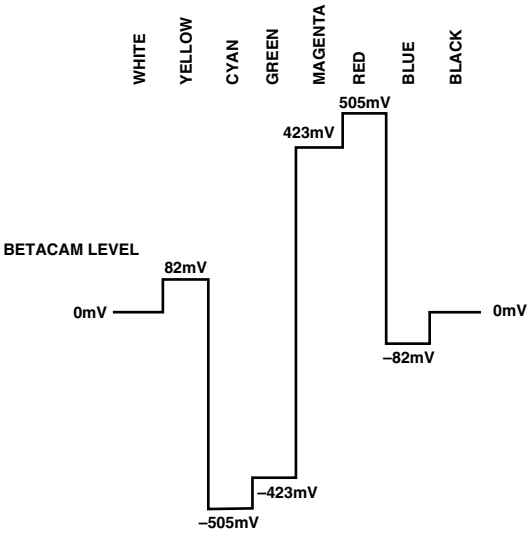


Figure 89. NTSC 100% Color Bars, No Pedestal V Levels

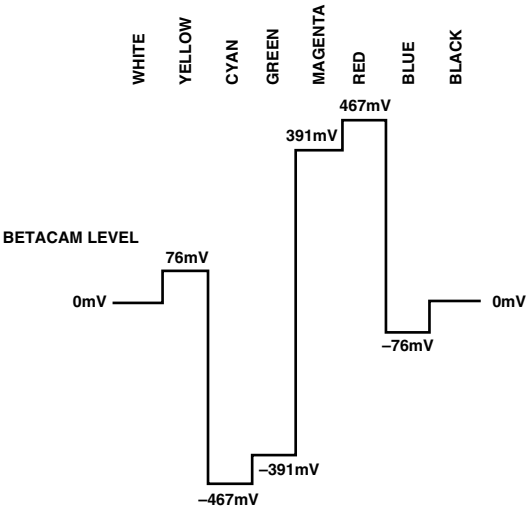


Figure 90. NTSC 100% Color Bars with Pedestal V Levels

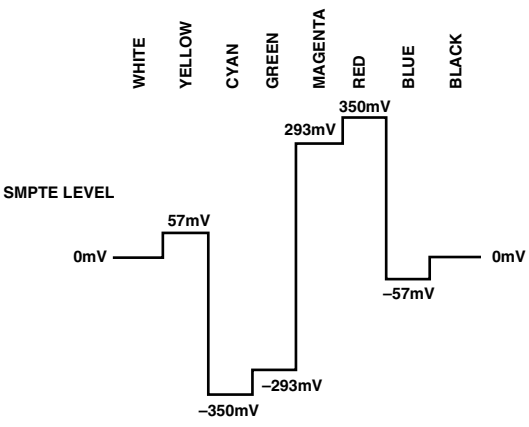


Figure 91. PAL 100% Color Bars, V Levels

APPENDIX 7

OPTIONAL OUTPUT FILTER

If an output filter is required for the CVBS, Y, UV, Chroma and RGB outputs of the ADV7172/ADV7173, the filter shown below can be used. The plot of the filter characteristics is shown in Figure 93. An Output Filter is not required if the outputs of the ADV7172/ADV7173 are connected to most analog monitors or analog TVs; however, if the output signals are applied to a system where sampling is used (e.g., Digital TVs), then a filter is required to prevent aliasing.

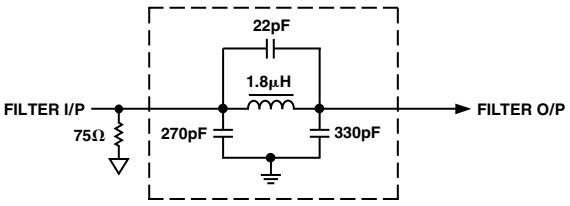


Figure 92. Output Filter Used with Output Buffer

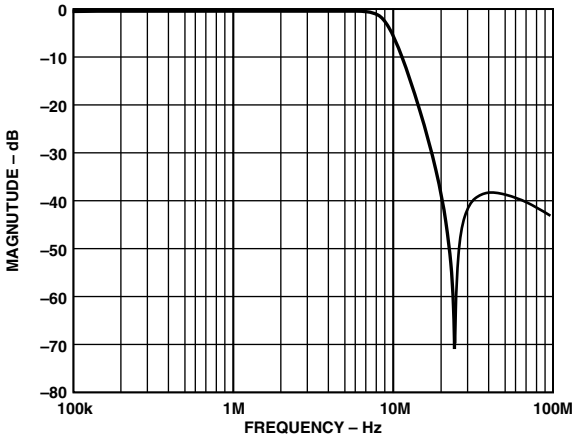


Figure 93. Output Filter Plot

APPENDIX 8

OPTIONAL DAC BUFFERING

When external buffering is needed of the ADV7172/ADV7173 DAC outputs, the configuration in Figure 94 is recommended. This configuration shows the DAC outputs, A, B, C, running at half (18 mA) their full current (36 mA) capability. This will allow the ADV7172/ADV7173 to dissipate less power; the analog current is reduced by 50% with a R_{SET1} = 300 Ω and R_{SET2} = 600 Ω and an R_{LOAD} of 75 Ω. This mode is recommended for 3.3 V operation as optimum performance is obtained from the DAC outputs at 18 mA with a V_{AA} of 3.3 V. This buffer also adds extra isolation on the video outputs (see buffer circuit in Figure 95). Note that DACs D, E, and F will always require buffering as the full-scale output current from these DACs is limited to 8.66 mA. With DACs A, B, and C, buffering is optional, based on the user requirements for performance and power consumption.

When calculating absolute output full-scale current and voltage, use the following equations:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

$$I_{OUT} = \frac{\left(V_{REF} \times K\right)}{R_{SET}}$$

$$K = 4.2146 \text{ constant}, V_{REF} = 1.235 \text{ V}$$

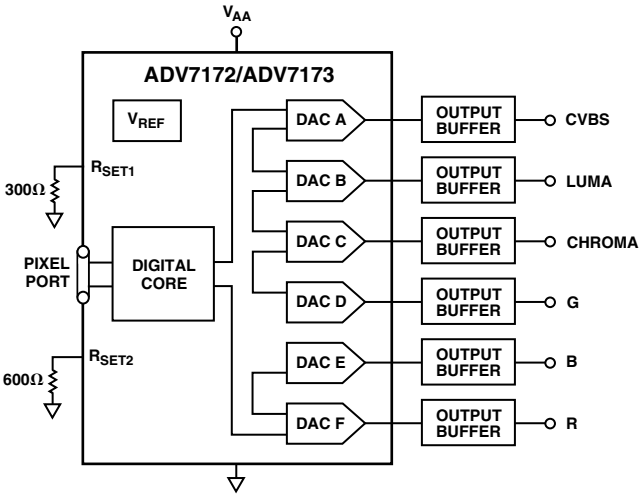


Figure 94. Output DAC Buffering Configuration

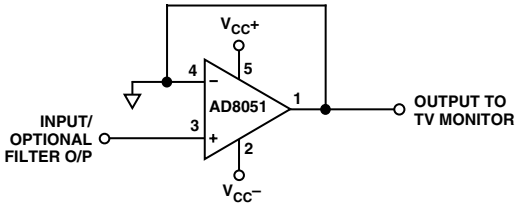


Figure 95. Recommended Output DAC Buffer

APPENDIX 9

RECOMMENDED REGISTER VALUES

The ADV7172/ADV7173 registers can be set depending on the user standard required.

The following examples give the various register formats for several video standards.

In each case the output is set to composite/luma/chroma outputs with DACs D, E and F powered up to provide 8.66 mA and with the $\overline{\text{BLANK}}$ input control disabled. Additionally, the burst and color information are enabled on the output and the internal color bar generator is switched off. In the examples shown, the timing mode is set to Mode 0 in slave format. TR02–TR00 of the Timing Register 0 control the timing modes. For a detailed explanation of each bit in the command registers, please turn to the Register Programming section of the data sheet. TR07 should be toggled after setting up a new timing mode. Timing Register 1 provides additional control over the position and duration of the timing signals. In the examples this register is programmed in default mode.

NTSC (F_{SC} = 3.5795454 MHz)

Address		Data
00Hex	Mode Register 0	10Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	68Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	16Hex
0DHex	Subcarrier Frequency Register 1	7CHex
0EHex	Subcarrier Frequency Register 2	F0Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

PAL B, D, G, H, I (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	11Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	68Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	01Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

PAL M (F_{SC} = 3.57561149 MHz)

Address		Data
00Hex	Mode Register 0	12Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	68Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	A3Hex
0DHex	Subcarrier Frequency Register 1	EFHex
0EHex	Subcarrier Frequency Register 2	E6Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex

PAL M (Continued) (F_{SC} = 3.57561149 MHz)

Address		Data
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

PAL N (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	13Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	68Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

PAL-60 (F_{SC} = 4.43361875 MHz)

Address		Data
00Hex	Mode Register 0	12Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	68Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

POWER ON RESET REG VALUES
(PAL_NTSC = 0, NTSC Selected)

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	00Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	16Hex
0DHex	Subcarrier Frequency Register 1	7CHex
0EHex	Subcarrier Frequency Register 2	F0Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

POWER ON RESET REG VALUES
(PAL_NTSC = 1, PAL Selected)

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
0AHex	Timing Register 0	00Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Request Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Control Register	00Hex

APPENDIX 10

OPTIONAL DAC BUFFERING

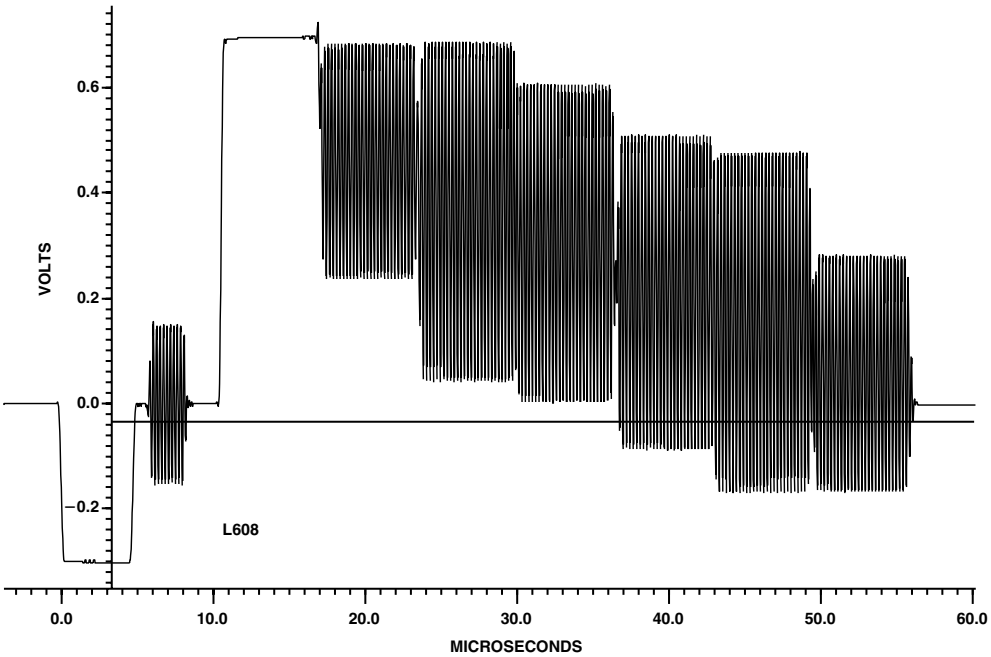


Figure 96. 100/0/75/0 PAL Color Bars

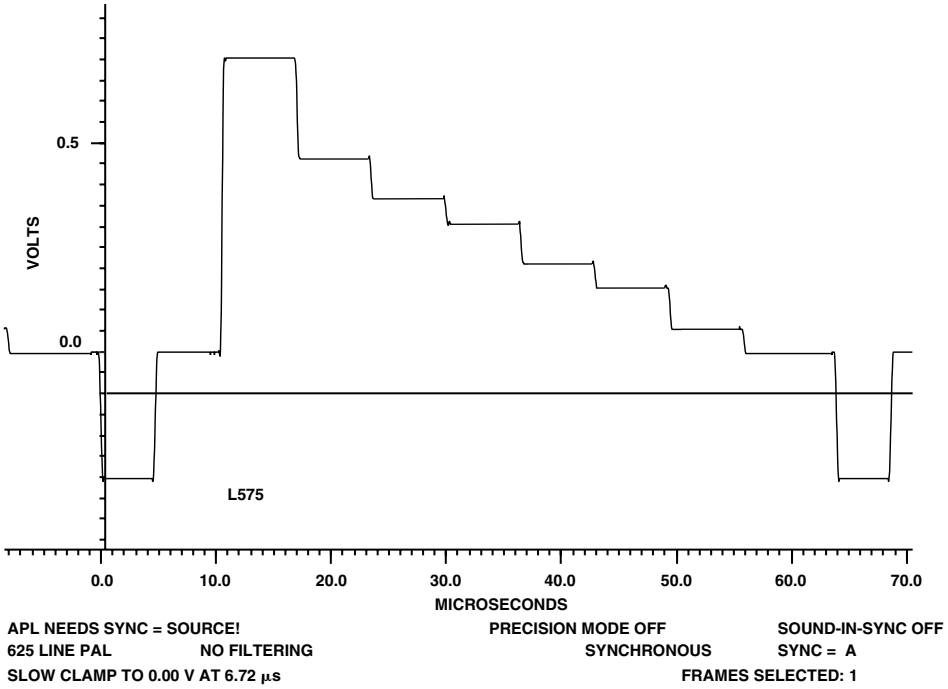


Figure 97. 100/0/75/0 PAL Color Bars Luminance

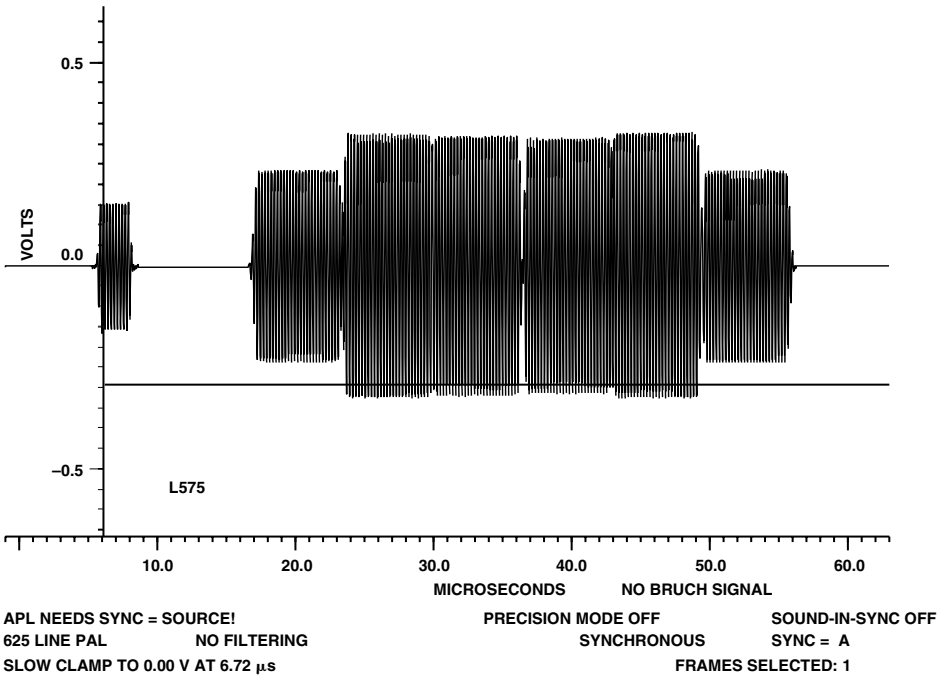


Figure 98. 100/0/75/0 PAL Color Bars Chrominance

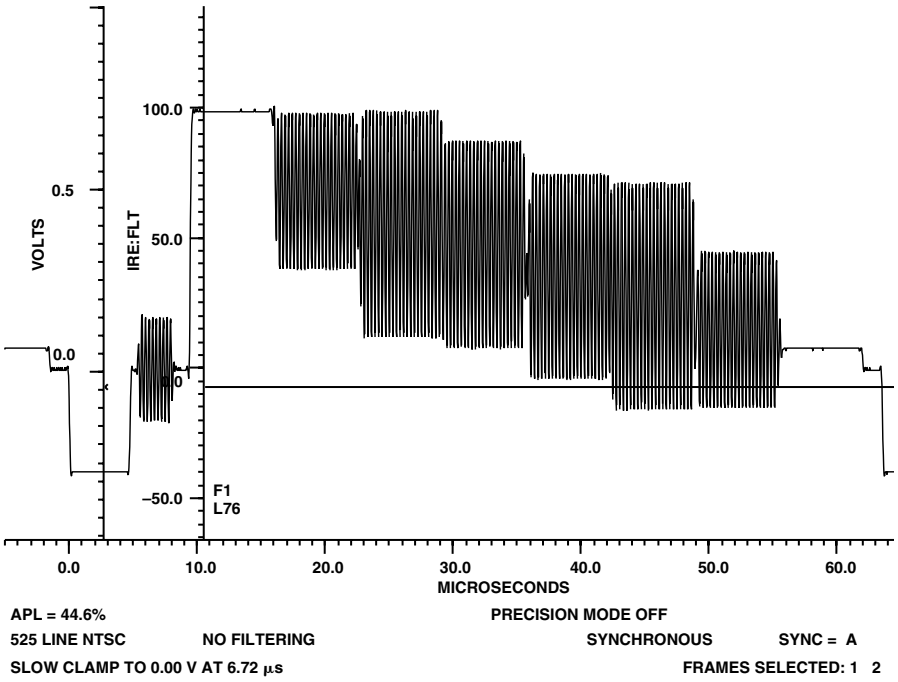


Figure 99. 100/7.5/75/7.5 NTSC Color Bars

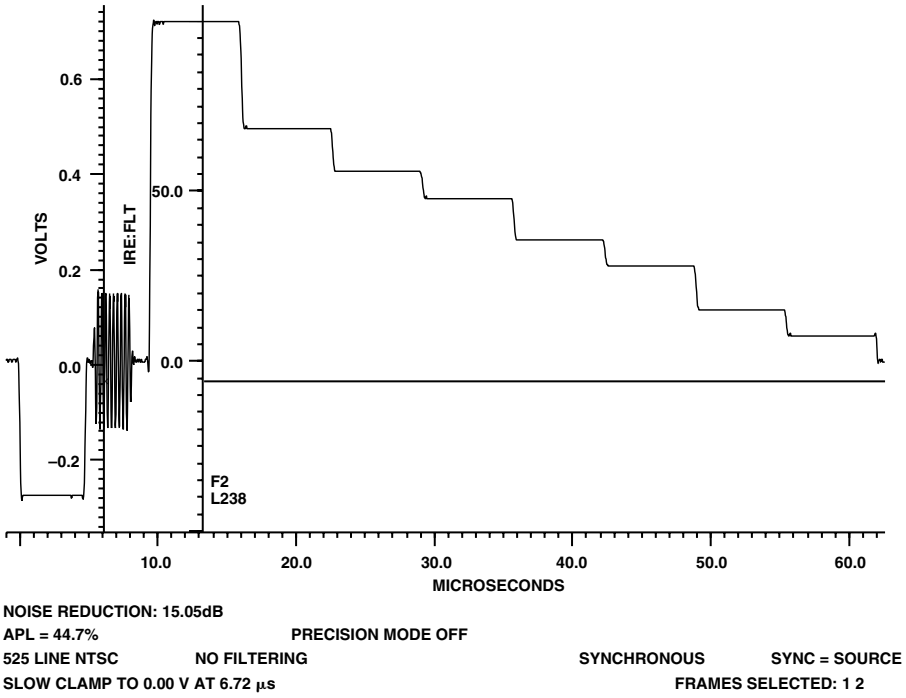


Figure 100. 100/7.5/75/7.5 NTSC Color Bars Luminance

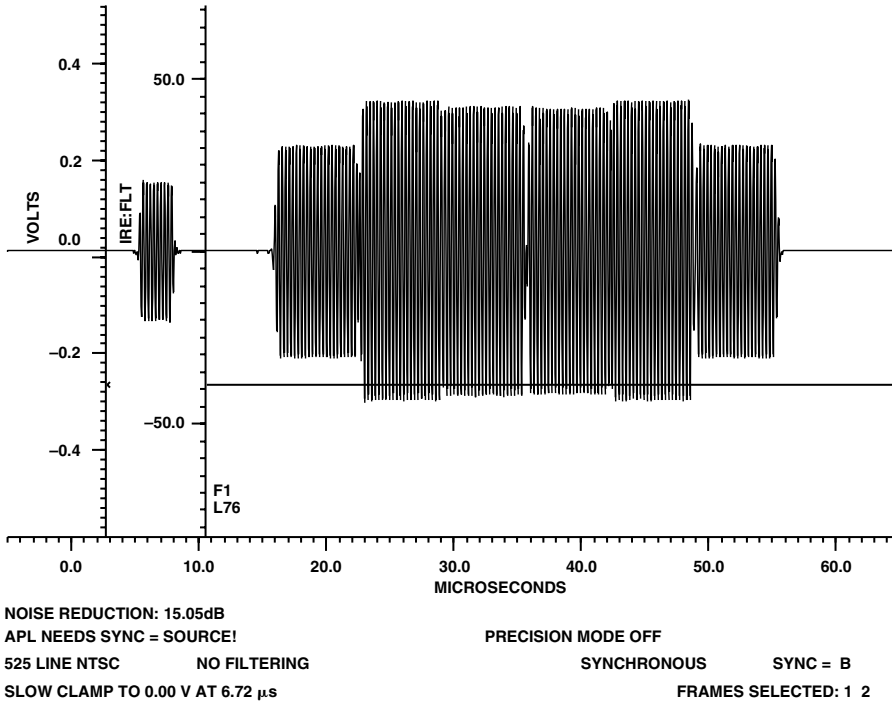


Figure 101. 100/7.5/75/7.5 NTSC Color Bars Chrominance

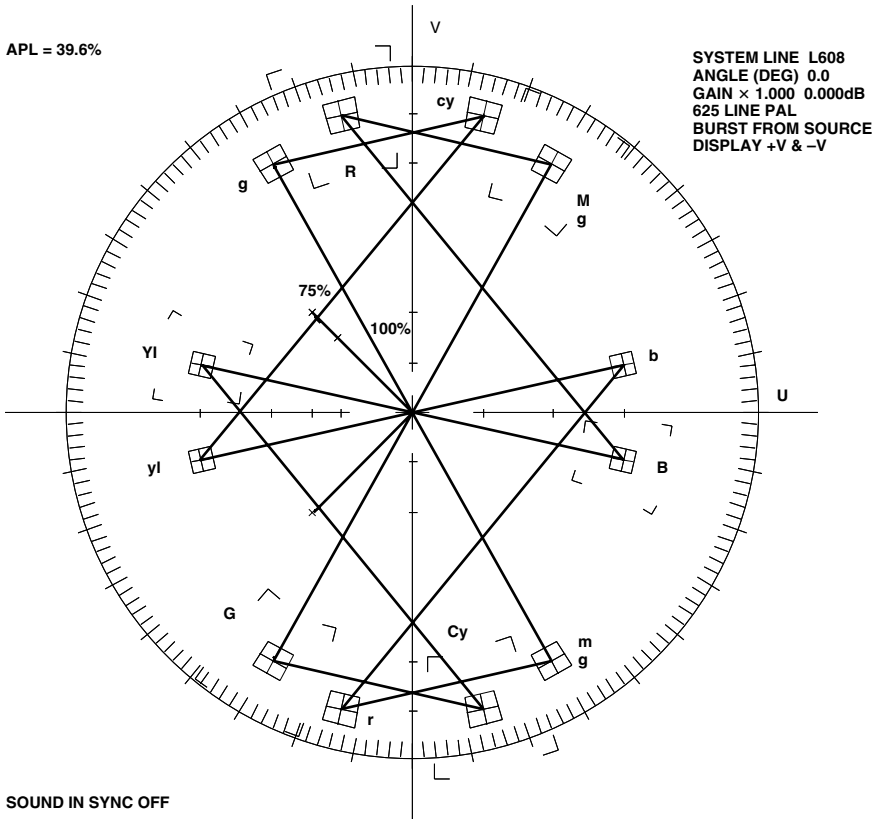


Figure 102. PAL Vector Plot

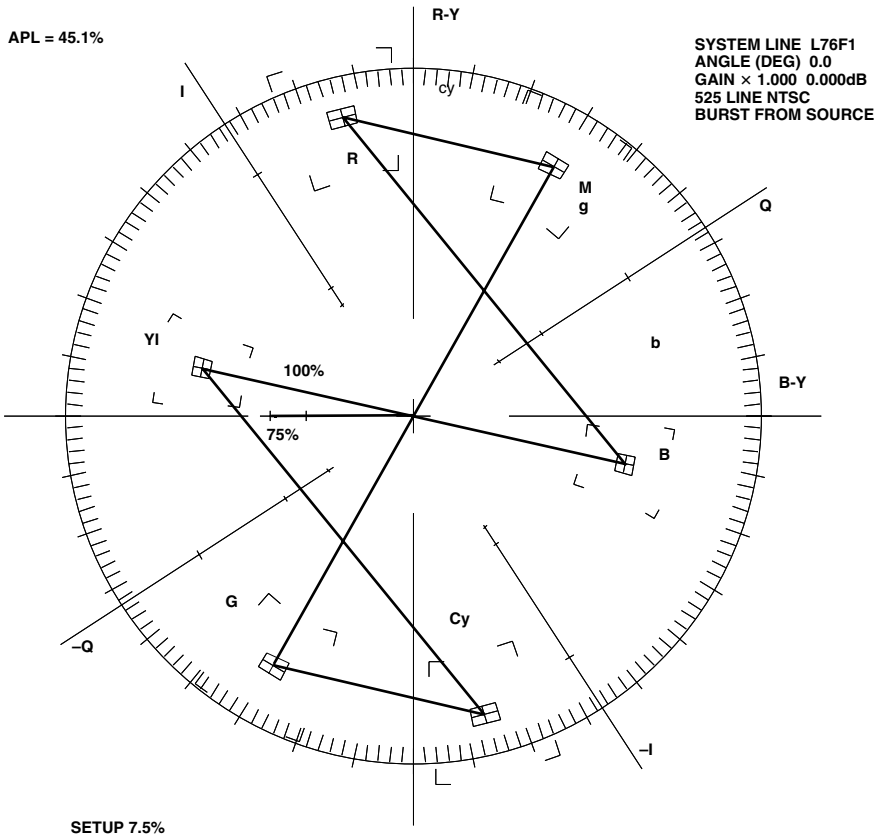
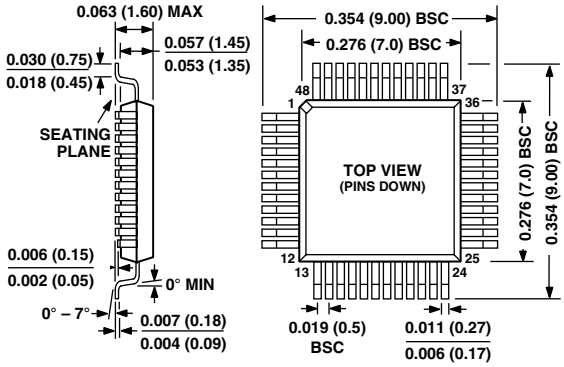


Figure 103. NTSC Vector Plot

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead LQFP
(ST-48)



C00222a–0–4/01(B)

PRINTED IN U.S.A.