TABLE OF CONTENTS

REVISION HISTORY

10/15—Rev. B to Rev. C

Changes to Table 2 ... 10

7/15—Revision B: Initial Version

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GENERAL DESCRIPTION

The ADuCM330/ADuCM331 are fully integrated, 8 kSPS, data acquisition systems that incorporate dual, high performance multichannel sigma-delta (Σ-Δ) ADCs, a 32-bit ARM® Cortex™-M3 processor, and flash. The ADuCM330 has 96 kB program flash and the ADuCM331 has 128 kB program flash. Both devices have 4 kB data flash.

The ADuCM330/ADuCM331 are complete system solutions for battery monitoring in 12 V automotive applications. The ADuCM330/ADuCM331 integrate all of the required features to precisely and intelligently monitor, process, and diagnose 12 V battery parameters including battery current, voltage, and temperature over a wide range of operating conditions.

Minimizing external system components, the devices are powered directly from a 12 V battery. On-chip, low dropout (LDO) regulators generate the supply voltage for two integrated Σ-Δ ADCs. The ADCs precisely measure battery current, voltage, and temperature to characterize the state of the health and the charge of the car battery.

The devices operate from an on-chip, 16.384 MHz high frequency oscillator that supplies the system clock. This clock is routed through a programmable clock divider from which the core clock operating frequency is generated. The devices also contain a 32 kHz oscillator for low power operation.

The analog subsystem consists of an ADC with a programmable gain amplifier (PGA) that allows the monitoring of various current and voltage ranges. It also includes a precision reference on chip.

The ADuCM330/ADuCM331 integrate a range of on-chip peripherals that can be configured under core software control as required in the application. These peripherals include a SPI serial input/output communication controller, six GPIO pins, one general-purpose timer, a wake-up timer, and a watchdog timer.

The ADuCM330/ADuCM331 are specifically designed to operate in battery-powered applications where low power operation is critical. The microcontroller core can be configured in normal operating mode, resulting in an overall system current consumption of <18.5 mA when all peripherals are active. The devices can also be configured in a number of low power operating modes under direct program control, consuming <100 µA. The ADuCM330/ADuCM331 also include a LIN physical interface for single wire, high voltage communications in automotive environments.

The devices operate from an external 3.6 V to 18 V (on VDD, Pin 26) voltage supply and is specified over the −40°C to +115°C temperature range, with additional typical specifications at +115°C to +125°C.

The information in this data sheet is relevant for silicon Revisions L6x, where x represents a number between 0 and 9.

For more information and register details for the ADuCM330/ADuCM331, see the user guide *ADuCM330/ADuCM331 Hardware Reference Manual*, UG-716.

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SPECIFICATIONS

VDD = 3.6 V to 18 V, f_{CORE} = 16.384 MHz, CD = 0, normal mode, VREF = 1.2 V (internal), unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise stated.

Parameters not specified in the 115°C to 125°C temperature range of operation are functional within this range but with degraded performance

Table 1.

		T_A = −40°C to +115°C			T_A = +115°C to +125°C[1]	
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Typ**	**Unit**
ADC SPECIFICATIONS						
Conversion Rate[1]	ADC normal operating mode	4		8000		Hz
	ADC low power mode, chop on	1		656		Hz
Current Channel (IIN+/IIN− Only)						
No Missing Codes[1]	Valid for all ADC update rates and ADC modes	20				Bits
Integral Nonlinearity[1,2]			±10	±200	±80	ppm of FSR
Positive Integral Nonlinearity (INL)[1,2,3]				±200	±80	ppm of FSR
Negative INL[1,2,3]				±200	±80	ppm of FSR
Offset Error[1,4,5]	Chop off, gain = 4, 8, or 16, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) µV	−100	±24	+100		LSBs
	Chop off, gain = 32 or 64, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) µV	−160	±48	+160		LSBs
	Chop off, gain = 512, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) µV	−1400	±60	+1400		LSBs
	Chop on, external short, low power mode, gain = 64 or 512, processor powered down	−300	±50	+250	±250	nV
	Chop on, external short, after user system calibration at 25°C, VDD = 18 V	−1.5		+1.5	±0.1	µV
Offset Error Drift[1,2,6]	Chop off, gains of 4 to 64, normal mode		±0.48			LSB/°C
	Chop on		±5		±5	nV/°C
Total Gain Error[1,4,5,7]	Factory calibrated at a gain of 8, normal mode	−0.5	±0.1	+0.5	±0.15	%
	Low power mode	−1	±0.2	+1	±0.2	%
Gain Drift[1,8]			±3		±3	ppm/°C
PGA Gain Mismatch Error			±0.1		±0.1	%
Output Noise[1]	ADC0CON[11:10], PGASCALE = 0x3					
	Gain = 64, ADCFLT = 0x08101		0.80	1.3	1.2	µV rms
	Gain = 64, ADCFLT = 0x00007		0.75	1.1		µV rms
	Gain = 32, ADCFLT = 0x08101		1.00	1.5	1.3	µV rms
	Gain = 32, ADCFLT = 0x00007		0.80	1.2		µV rms
	Gain = 16, ADCFLT = 0x08101		1.50	2.6	2.0	µV rms
	Gain = 16, ADCFLT = 0x00007		1.10	1.9		µV rms
	Gain = 8, ADCFLT = 0x08101		2.10	4.1	2.5	µV rms
	Gain = 8, ADCFLT = 0x00007		1.60	2.4		µV rms
	Gain = 4, ADCFLT = 0x08101		3.40	5.1	4.0	µV rms
	Gain = 4, ADCFLT = 0x00007		2.60	3.9		µV rms
	Gain = 64, ADCFLT = 0x10001		1.60	3	2.0	µV rms
	Gain = 32, ADCFLT = 0x10001		1.70	3.45	2.1	µV rms
	Gain = 16, ADCFLT = 0x10001		2.00	4.2	2.2	µV rms
	Gain = 8, ADCFLT = 0x10001		2.40	5.1	3.2	µV rms
	Gain = 4, ADCFLT = 0x10001		4.35	9.6	5.5	µV rms
	ADC low power mode, 221 Hz update rate, chop enabled, gain = 64		0.6	0.9	0.8	µV rms

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Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = +115°C to +125°C[1]	Unit
		Min	Typ	Max	Typ	
Voltage Channel[1,9]						
No Missing Codes	Valid at all ADC update rates	20				Bits
INL	From 6 V to 18 V		±10	±350	±150	ppm of FSR
Offset Error[4,5]	Chop off, 1 LSB = 27.4 µV, after two point calibration	−160	±16	+160		LSB
	Chop on, after two-point calibration, offset measured using 0 V differential into voltage ADC (VADC) auxiliary pins	−16	±4.8	+16	±4.8	LSB
Offset Error Drift[6]	Chop off		±0.48		±1	LSB/°C
Total Gain Error[4,5,7]	Includes resistor mismatch	−0.25	±0.06	+0.25	±0.1	%
	T_A = −25°C to +65°C	−0.15	±0.03	+0.15		%
Gain Drift[8]	Includes resistor mismatch drift		±3		±3	ppm/°C
Output Noise[10]	10 Hz update rate, chop on		50	80		µV rms
	ADCFLT = 0x00007		180	270		µV rms
	ADCFLT = 0x08101		280	350	300	µV rms
	ADCFLT = 0x10001		400	730	470	µV rms
Temperature Channel[1]						
No Missing Codes	Valid at all ADC update rates	20				Bits
INL			±10	±60	±15	ppm of FSR
Offset Error[4,11]	Chop off, 1 LSB = 1.14 µV (unipolar mode), after two point calibration	−160	±48	+160		LSB
Offset Error[4]	Chop on	−80	+16	+80	±16	LSB
Offset Error Drift	Chop off		±0.48		±0.48	LSB/°C
Total Gain Error[4,11]		−0.25	±0.06	+0.25	±0.10	%
Gain Drift[8]			3		3	ppm/°C
Output Noise	1 kHz update rate, ADCFLT = 0x00007		7.5	11.25	10	µV rms
ADC SPECIFICATIONS, ANALOG INPUT	PGASCALE[11:10] = 0x2					
Current Channel[1]						
Absolute Input Voltage Range	Applies to both IIN+ and IIN−	−200		+300		mV
Input Voltage Range[12]						
	Gain = 4, limited by absolute input voltage range		±300			mV
	Gain = 8		±150			mV
	Gain = 32		±37.5			mV
Input Leakage Current[13]		−3		+3	±0.2	nA
Input Offset Current[13]			0.2	0.6	0.4	nA
Voltage Channel						
Absolute Input Voltage Range[1]	Voltage ADC specifications are valid in this range	6		18		V
Input Voltage Range[1]			0 to 28.8			V
VBAT Input Current	VBAT = 18 V	5	9	13	11	µA
Temperature Channel	VREF = (AVDD18, GND_SW)					
Absolute Input Voltage Range[1,14]		100		1500		mV
Input Voltage Range[1]			0 to 1.4			V
VTEMP Input Current[1]			2.5	10		nA
VOLTAGE REFERENCE						
Internal Reference			1.2		1.2	V
Power-Up Time[1]			0.5		0.5	ms
Initial Accuracy[1]	Measured at T_A = 25°C	−0.15		+0.15		%
Temperature Coefficient[1,15]		−20	±5	+20	±8	ppm/°C
Long-Term Stability[16]			100			ppm/1000 hr

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Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = +115°C to +125°C[1]	Unit
		Min	Typ	Max	Typ	
ADC DIAGNOSTICS						
AVDD18/136 Accuracy[1, 2, 17]	At any gain setting	12		14	13	mV
Voltage Attenuator Current Source Accuracy	Differential voltage increase on the attenuator when current is on	2.4		3.2	2.8	V
RESISTIVE ATTENUATOR						
Divider Ratio			24			
Resistor Mismatch Drift	Implicit in the voltage channel gain error specification		±3			ppm/°C
ADC GROUND SWITCH						
Resistor to Ground		45	60	75		kΩ
TEMPERATURE SENSOR[1, 18]	Processor in hibernate mode					
Accuracy	T_A = 115°C to 125°C	−3.5	±1	+3.5	±1	°C
	T_A = −40°C to +115°C	−3	±1	+3		°C
	T_A = −25°C to +85°C	−2.5	±0.5	+2.5		°C
	T_A = −10°C to +55°C	−2	±0.5	+2		°C
POWER-ON RESET (POR)[1]	Refers to voltage at the VDD pin					
POR Trip Level		2.8	3.1	3.4	3.3	V
POR Hysteresis			0.1			V
LOW VOLTAGE FLAG (LVF)						
LVF Level	Refers to voltage at the VDD pin	2.6	2.75	3.00		V
WATCHDOG TIMER (WDT)						
Shortest Timeout Period	32,768 Hz clock with a prescaler of 1		30.5		30.5	µs
Longest Timeout Period	32,768 Hz clock with a prescaler of 4096		8192		8192	sec
FLASH/EE MEMORY						
Endurance[19]		10,000				Cycles
Data Retention[20]		20				Years
LOGIC INPUTS[1]						
Input Voltage						
Low, V_{INL}				0.4		V
High, V_{INH}		2.0				V
LOGIC OUTPUTS[1]	All logic outputs, measured with ±1 mA load					
Output Voltage						
High, V_{OH}		33VDD − 0.4				V
Low, V_{OL}				0.4		V
DIGITAL INPUTS[1]	All digital inputs except $\overline{\text{RESET}}$, SWDIO, and SWCLK					
Logic 1 Input Current (Leakage Current)	V_{INH} = 3.3 V		±1	±10		µA
Logic 0 Input Current (Leakage Current)	V_{INL} = 0 V		±1	±10		µA
Input Capacitance			10			pF
ON-CHIP OSCILLATORS						
Low Frequency Oscillator (LFOSC)			32,768			Hz
Accuracy			±5			%
	After a calibration from HFOSC	−6		+6		%
High Frequency Oscillator (HFOSC)			16.384			MHz
Accuracy (LINCAL)[1, 21]		−0.75	±0.5	+0.75		%
Accuracy (High Precision Mode)		−1		+1		%
Accuracy (Low Precision Mode)		−3		+3		%

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Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = +115°C to +125°C[1]	Unit
		Min	Typ	Max	Typ	
PROCESSOR START-UP TIME[1]						
At Power-On	Includes kernel power-on execution time, VDD drops to < 0.8 V		18			ms
Brownout	VDD drops below power on reset voltage but not below 0.8 V		1.15			ms
After Reset Event	Includes kernel power-on execution time		1.25			ms
Wake-Up from LIN			0.15			ms
LIN INPUT/OUTPUT GENERAL[1]						
Baud Rate		1000		20,000		Bits/sec
VDD	Supply voltage range for which the LIN interface is functional	7		18		V
LIN Comparator Response Time			38	90		µs
LIN DC PARAMETERS						
$I_{LIN\_DOM\_MAX}$	Current limit for driver when LIN bus is in dominant state, VBAT = VBAT (maximum)	40		200		mA
$I_{LIN\_PAS\_REC}$[1]	Driver off, 7.0 V < VBUS < 18 V, VDD = VLIN − 0.7 V			20		µA
$I_{LIN\_PAS\_DOM}$[1]	Input leakage, VLIN = 0 V, VBAT = 12 V, driver off	−1				mA
$I_{LIN\_NO\_GND}$[1, 22]	Control unit disconnected from ground, GND = VDD, 0 V < VLIN < 18 V, VBAT = 12 V	−1		+1		mA
$I_{BUS\_NO\_BAT}$[1]	VBAT disconnected, VDD = GND, 0 V < VBUS < 18 V			30		µA
V_{LIN_DOM}[1]	LIN receiver dominant state, VDD > 7.0 V			0.4 × VDD		V
V_{LIN_REC}[1]	LIN receiver recessive state, VDD > 7.0 V	0.6 VDD				V
V_{LIN_CNT}[1]	$V_{LIN\_CNT} = (V_{TH\_DOM} + V_{TH\_REC})/2$, VDD > 7.0 V	0.475 × VDD	0.5 × VDD	0.525 × VDD		V
V_{HYS}[1]	$V_{HYS} = V_{TH\_REC} - V_{TH\_DOM}$			0.175 × VDD		V
$V_{LIN\_DOM\_DRV\_LOSUP}$[1]	LIN dominant output voltage, VDD = 7.0 V					
R_L = 500 Ω				1.2		V
R_L = 1000 Ω		0.6				V
$V_{LIN\_DOM\_DRV\_HISUP}$[1]	LIN dominant output voltage, VDD = 18 V					
R_L = 500 Ω				2		V
R_L = 1000 Ω		0.8				V
$V_{LIN\_RECESSIVE}$[1]	LIN recessive output voltage	0.8 × VDD				V
VBAT Shift[1, 22]		0		0.115 × VDD		V
GND Shift[1, 22]		0		0.115 × VDD		V
R_{SLAVE}	Slave termination resistance	20	30	47	30	kΩ
V_{SERIAL_DIODE}[1]	Voltage drop at the serial diode, DSer_Int	0.4	0.7	1		V

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Parameter	Test Conditions/Comments	T_A = −40°C to +115°C Min	Typ	Max	T_A = +115°C to +125°C[1] Typ	Unit
LIN AC PARAMETERS[1]	Bus load conditions (CBUS||RBUS): 1 nF||1 kΩ, 6.8 nF||660 Ω, 10 nF||500 Ω					
D1	Duty Cycle 1 THREC(MAX) = 0.744 × VBAT THDOM(MAX) = 0.581 × VBAT VSUP = 7.0 V to 18 V, t_{BIT} = 50 µs D1 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$	0.396				
D2	Duty Cycle 2 THREC(MIN) = 0.284 × VBAT THDOM(MIN) = 0.422 × VBAT VSUP = 7.0 V to 18 V, t_{BIT} = 50 µs D2 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$			0.581		
D3[22]	THREC(MAX) = 0.778 × VBAT THDOM(MAX) = 0.616 × VBAT VDD = 7.0 V to 18 V t_{BIT} = 96 µs D3 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$	0.417				
D4[22]	THREC(MIN) = 0.389 × VBAT THDOM(MIN) = 0.251 × VBAT VDD = 7.0 V to 18 V t_{BIT} = 96 µs D4 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$			0.590		
t_{RX_PDR}[22]	Propagation delay of receiver			6		µs
t_{RX_SYM}[22]	Symmetry of receiver propagation delay rising edge, with respect to falling edge ($t_{RX\_SYM} = t_{RF\_PDR} - t_{RX\_PDF}$)	−2		+2		µs
PACKAGE THERMAL SPECIFICATIONS						
Thermal Impedance (θ_{JA})[23]	JEDEC 4-layer board		40			°C/W
POWER REQUIREMENTS						
Power Supply Voltages						
VDD (Pin 26)		3.6		18		V
DVDD33 (Pin 21)			3.3		3.3	V
AVDD18 (Pin 19)			1.88		1.88	V
DVDD18 (Pin 22)			1.88		1.88	V
POWER CONSUMPTION						
IDD (Processor Normal Mode)[24]	CD0 (PCLK = 16 MHz), 16 MHz 1% mode, ADCs off, reference buffer off, executing code from program flash		8	17	9	mA
	CD1 (PCLK = 8 MHz), 16 MHz 1% mode, ADCs off, reference buffer off, executing code from program flash		6		7	mA
	CD0 (PCLK = 16 MHz), 16 MHz 1% mode, ADCs on, reference buffer on, executing code from program flash		9.5	18.5	10	mA
IDD (Processor Powered Down)	Precision oscillator off, ADC off, external LIN master pull-up resistor present, measured with wake-up and watchdog timers clocked from low power oscillator, maximum value is at 105°C, and VDD = 18 V		60	100		µA
IDD LIN			500			µA
IDD IADC	Gain = 4, 8, or 16		700			µA
	Gain = 32 or 64		800			µA
	LPM, gain = 64		350			µA

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Parameter	Test Conditions/Comments	T_A = −40°C to +115°C			T_A = +115°C to +125°C[1]	Unit
		Min	Typ	Max	Typ	
IDD ADC1 VADC			550			µA
IDD Internal Reference (1.2 V)			150			µA
IDD HFOSC	Reduction from 1% to 3% mode		50			µA

[1] Not guaranteed by production test, but by design and/or characterization data at production release.
[2] Valid for PGA current ADC gain settings of 4, 8, 16, 32, and 64.
[3] System chopping enabled.
[4] These specifications include temperature drift.
[5] A user system calibration removes this error at a given temperature (and at a given gain for the current channel).
[6] The offset error drift is included in the offset error. This typical specification is an indicator of the offset error due to temperature drift. This typical value is the mean of the temperature drift characterization data distribution.
[7] Includes internal reference temperature drift.
[8] The gain drift is included in the total gain error. This typical specification is an indicator of the gain error due to the temperature drift in the ADC. This typical value is the mean of the temperature drift characterization data distribution.
[9] Voltage channel specifications include resistive attenuator input stage, unless otherwise stated.
[10] RMS noise is referred to voltage attenuator input; for example, at f_{ADC} = 1 kHz, the typical rms noise at the ADC input is 7.5 µV, scaling by the attenuator (24) yields these input referred noise figures.
[11] Valid after an initial self calibration.
[12] It is possible to extend the ADC input range by up to 10% by modifying the factory set value of the gain calibration register or using system calibration. This approach can also be used to reduce the ADC input range (LSB size).
[13] Valid for a differential input less than 10 mV.
[14] The absolute value of the voltage of VTEMP and GND_SW must be 100 mV (minimum) for accurate operation of the temperature analog-to-digital converter (T-ADC).
[15] Measured using box method.
[16] The long-term stability specification is accelerated and noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[17] Valid after an initial self gain calibration.
[18] Die temperature.
[19] Endurance is qualified to 10,000 cycles, as per JEDEC Standard 22 Method A117 and measured at −40°C, +25 °C, and +115°C. Typical endurance at +25°C is 100k cycles.
[20] Data retention lifetime equivalent at junction temperature (T_J) = 85°C, as per JEDEC Standard 22 Method A117. Data retention lifetime derates with junction temperature.
[21] Measured with LIN communication active.
[22] These specifications are not production tested but are supported by LIN compliance testing.
[23] Thermal impedance can be used to calculate the thermal gradient from ambient to die temperature.
[24] Typical additional supply current consumed during Flash/EE memory program and erase cycles is 3 mA and 1 mA, respectively.

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ABSOLUTE MAXIMUM RATINGS

The ADuCM330/ADuCM331 operate directly from the 12 V battery supply and is fully specified over the −40°C to +115°C temperature range, unless otherwise noted.

Table 2.

Parameter	Rating
AGND to DGND to VSS to IO_VSS	−0.3 V to +0.3 V
VBAT to AGND	−22 V to +40 V
VDD to VSS	−0.3 V to +40 V
LIN to IO_VSS	−18 V to +40 V
Digital Input/Output Voltage to DGND	−0.3 V to DVDD33 + 0.3 V
ADC Inputs to AGND	−0.3 V to AVDD18 + 0.3 V
ESD (Human Body Model) Rating HBM-ADI0082 (Based on ANSI/ ESD STM5.1-2007)	
All Pins Except LIN and VBAT	±2.0 kV
LIN	±6 kV
VBAT	±4 kV
IEC 61000-4-2	
LIN and VBAT	±8 kV
Storage Temperature Range	−55°C to +150°C
Junction Temperature	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow[1]	260°C
Lifetime[2]	
Normal Mode	480 hours at −40°C
	1600 hours at +23°C
	5200 hours at +60°C
	640 hours at +85°C
	80 hours at +105°C
Standby Mode	12,648 hours at −40°C
	60,000 hours at +25°C
	50,000 hours at +50°C

[1] JEDEC standard J-STD-020.
[2] Using an activation energy of 0.7 eV, verified using high temperature operating life (HTOL) at 125°C for 1000 hours.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

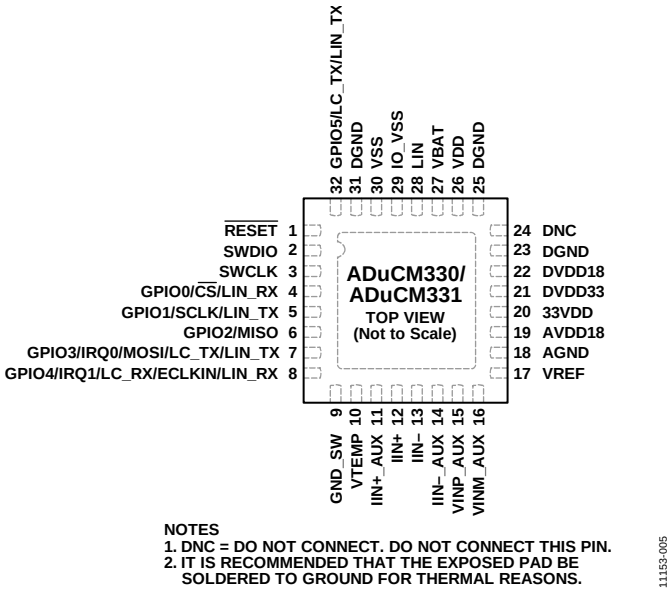

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	$\overline{\text{RESET}}$	I	Reset Input Pin. Active low. This pin has an internal pull-up resistor to 33VDD.
2	SWDIO	I/O	Cortex-M3 Debug Data Input and Output Channel. At power-on, this output is disabled and pulled high via an internal pull-up resistor. This pin can be left unconnected when not in use.
3	SWCLK	I	Cortex-M3 Debug Clock Input. This is an input pin only and has an internal pull-up resistor. This pin can be left unconnected when not in use.
4	GPIO0/$\overline{\text{CS}}$/LIN_RX	I/O	General-Purpose Input/Output 0 (P0.0) (GPIO0). By default, this pin is configured as an input. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. Chip Select ($\overline{\text{CS}}$). When configured, this pin also operates the SPI chip select input. Local Interconnect Network Receiver (Rx) (LIN_RX). This pin can be configured as the Rx pin for LIN frames in external transceiver mode.
5	GPIO1/SCLK/LIN_TX	I/O	General-Purpose Input/Output 1 (P0.1) (GPIO1). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330/ADuCM331 hardware reference manual for more information. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. Serial Clock Input (SCLK). When configured, this pin operates the SPI serial clock input. Local Interconnect Network Transmitter (Tx) (LIN_TX). This pin can be configured as the Tx pin for LIN frames in external transceiver mode.
6	GPIO2/MISO	I/O	General-Purpose Input/Output 2 (P0.2) (GPIO2). By default, this pin is configured as an input. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. Master Input/Slave Output (MISO). When configured, this pin also operates the SPI master input/slave output.
7	GPIO3/IRQ0/MOSI/ LC_TX/LIN_TX	I/O	General-Purpose Input/Output 3 (P0.3) (GPIO3). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330/ADuCM331 hardware reference manual for more information. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. Interrupt Request (IRQ0). This pin can also be configured as External Interrupt Request 0. Master Output/Slave Input (MOSI). This pin can be configured as an SPI master output/slave input pin. LIN Conformance Tx (LC_TX). This pin can be connected to the LIN physical Tx for LIN conformance testing. Local Interconnect Network Tx (LIN_TX). This pin can also be connected as the Tx pin for LIN frames in external transceiver mode.

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Pin No.	Mnemonic	Type[1]	Description
8	GPIO4/IRQ1/LC_RX/ ECLKIN/LIN_RX	I/O	General-Purpose Input/Output 4 (P0.4) (GPIO4). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330/ADuCM331 hardware reference manual for more information. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. Interrupt Request (IRQ1). This pin can be configured as External Interrupt Request 1. LIN Conformance Rx (LC_RX). This pin can be connected to LIN physical RX for LIN conformance testing. External Clock (ECLKIN). This pin can be configured as the external clock input. Local Interconnect Network Rx (LIN_RX). This pin can be configured as the receiving pin for LIN frames in external transceiver mode.
9	GND_SW	I	Switch to Internal Analog Ground Reference. This pin is the negative input for the external temperature channel.
10	VTEMP	I	External Pin for Negative Temperature Coefficient (NTC)/Positive Temperature Coefficient (PTC) Temperature Measurement.
11	IIN+_AUX	S	Auxiliary IIN+ Pin. Connect this pin to AGND.
12	IIN+	I	Positive Differential Input for Current Channel.
13	IIN–	I	Negative Differential Input for Current Channel.
14	IIN–_AUX	S	Auxiliary IIN– Pin. Connect this pin to AGND.
15	VINP_AUX	S	Auxiliary Input Voltage Positive Channel. Connect this pin to AGND.
16	VINM_AUX	S	Auxiliary Input Voltage Negative Channel. Connect this pin to AGND.
17	VREF	S	Voltage Reference Pin. Connect this pin via a 470 nF capacitor to ground. This pin can also be used to input an external voltage reference. This pin cannot be used to supply an external circuit.
18	AGND	S	Ground Reference for On-Chip Precision Analog Circuits.
19	AVDD18	S	Supply from Analog LDO. Do not connect this pin to an external circuit.[2]
20	33VDD	S	3.3 V Supply. Connect to Pin 21. Do not connect this pin to an external circuit.[2]
21	DVDD33	S	3.3 V Supply. Connect to Pin 20. Do not connect this pin to an external circuit.[2]
22	DVDD18	S	1.8 V Supply. Do not connect this pin to an external circuit.[2]
23	DGND	S	Ground Reference for On-Chip Digital Circuits.
24	DNC		Do Not Connect. This pin is internally connected; therefore, do not externally connect to this pin.
25	DGND	S	Ground Reference for On-Chip Digital Circuits.
26	VDD	S	Battery Power Supply for On-Chip Regulator.
27	VBAT	S	Battery Voltage Input fo Resistor Divider.
28	LIN	I/O	Local Interconnect Network (LIN) Physical Interface Input/Output.
29	IO_VSS	S	Ground Reference for the LIN Pin.
30	VSS	S	Ground Reference. This is the ground reference for the internal voltage regulators.
31	DGND	S	Ground Reference for On-Chip Digital Circuits.
32	GPIO5/LC_TX/LIN_TX	I/O	General-Purpose Input/Output 5 (P0.5) (GPIO5). By default, this pin is configured as an input. This pin is checked by the kernel on every reset. See the ADuCM330/ADuCM331 hardware reference manual for further information. The pin has an internal 25 kΩ pull-up resistor to 33VDD and, when not in use, can be left unconnected. LIN Conformance Tx (LC_TX). This pin can be connected to the LIN physical Tx for LIN conformance testing. Local Interconnect Network Tx (LIN_TX). This pin can be configured as the Tx pin for LIN frames in external transceiver mode.
33	EPAD		Exposed Pad. It is recommended that the exposed pad be soldered to ground for thermal reasons.

[1] I is input, O is output, and S is supply.
[2] Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, EMC, and self heating implications. Device evaluation and testing completed without an external load attached.

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TERMINOLOGY

Conversion Rate
The conversion rate specifies the rate at which an output result is available from the ADC, after the ADC has settled.

The Σ-Δ conversion techniques used on this device means that although the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output, giving a valid 20-bit data conversion result at output rates from 1 Hz to 8 kHz.

Note that, when software switches from one input to another (on the same ADC), the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this averaging can require multiple conversion cycles.

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition (111…110 to 111…111). The error is expressed as a percentage of full scale.

Positive INL is defined as the deviation from a straight line through ½ LSB above midscale code transition to ½ LSB above the last code transition.

Negative INL is defined as the deviation from a straight line from a point ½ LSB below the first code transition to a point ½ LSB above the midscale code transition.

No Missing Codes
No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2^N bits, where N = no missing codes, guaranteed to occur through the full ADC input range.

Offset Error
Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift
Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as LSB/°C or nV/°C.

Gain Error
Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise
The output noise is specified as the standard deviation (or 1 × Σ) of ADC output codes distribution collected when the ADC input voltage is at a dc voltage. It is expressed as μV rms or nV rms. The output, or rms noise, is used to calculate the effective resolution of the ADC as defined by the following equation:

$$\textit{Effective Resolution} = \log_2(\textit{Full-Scale Range/rms Noise}) \text{ bits}$$

The peak-to-peak noise is defined as the deviation of codes that fall within 6.6 × Σ of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is therefore calculated as 6.6 × the rms noise.

The peak-to-peak noise can be used to calculate the ADC (noise free, code) resolution for which there is no code flicker within a 6.6 × Σ limit as defined by the following equation:

$$\textit{Noise Free Code Resolution} = \log_2(\textit{Full-Scale Range/Peak-to-Peak Noise}) \text{ bits}$$

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APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the ADuCM330/ADuCM331 on a printed circuit board (PCB), it is recommended that the designer become familiar with the following guidelines that describe any special circuit considerations and layout requirements needed.

POWER AND GROUND RECOMMENDATIONS

Place capacitors that are connecting to the ADuCM330/ADuCM331 as close to the pins of the device as possible, with minimal trace length.

Capacitors connected to the 33VDD, AVDD18, and DVDD18 pins must have a low equivalent series resistance (ESR) rating.

All components must be rated accordingly to the temperature range expected by the application.

EXPOSED PAD THERMAL RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADuCM330/ADuCM331 be connected to ground to achieve the best electrical and thermal performance. It is recommended that the user connect an exposed continuous copper plane on the PCB to the ADuCM330/ADuCM331 exposed pad, and that the copper plane has several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. It is recommended that these vias be solder filled or plugged.

GENERAL RECOMMENDATIONS

It is highly recommended to use the schematic given with component values specified (see Figure 3). The component values shown in Figure 3 are chosen from the characterization tests and evaluated for optimum performance of the ADuCM330/ADuCM331.

Configure the GPIOs as inputs with pull-up resistors enabled to obtain the lowest possible current consumption in hibernate mode.

Set the Cortex-M3 core clock speed to the minimum required to meet the application requirements.

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RECOMMENDED SCHEMATIC

Figure 3 shows external components recommended for proper operation of the ADuCM330/ADuCM331.

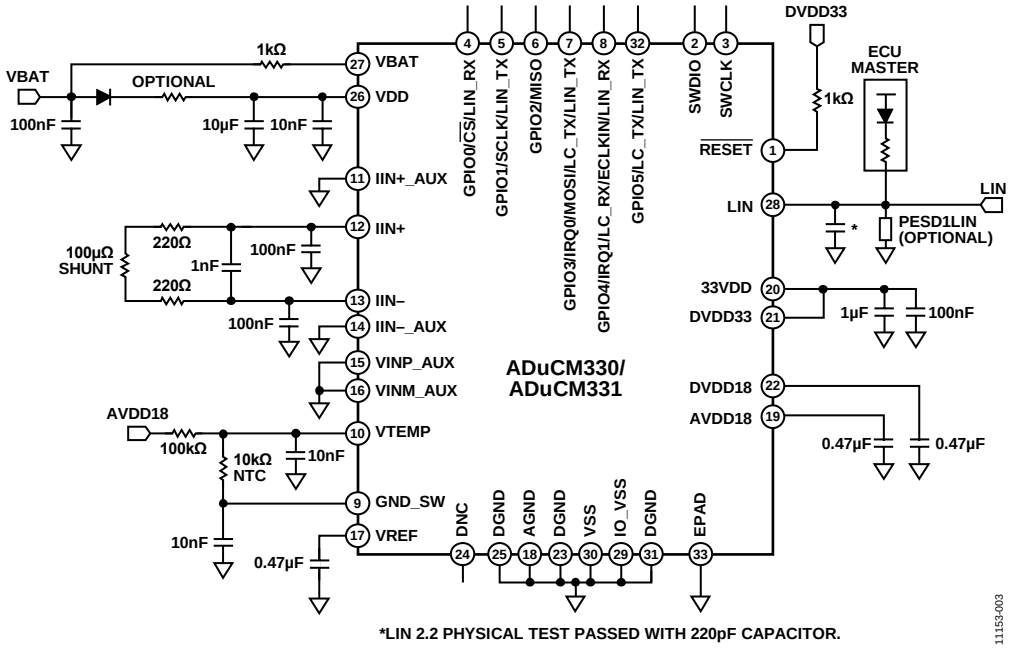

Figure 3. Recommended Schematic

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OUTLINE DIMENSIONS

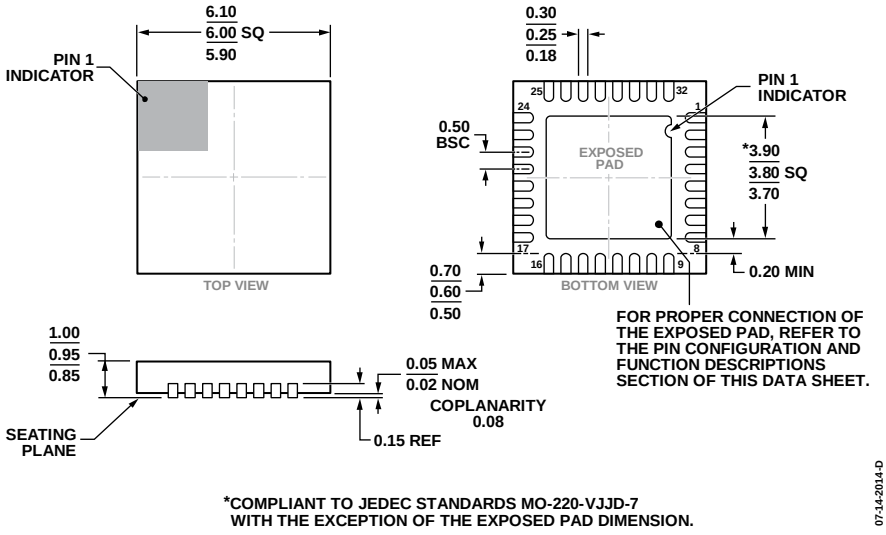

Figure 4. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-32-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range[3]	Program Flash/ Data Flash/SRAM	Package Description	Package Option
ADuCM330WDCPZ	−40°C to +115°C	96 kB/4 kB/6 kB	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-15
ADuCM330WDCPZ-RL	−40°C to +115°C	96 kB/4 kB/6 kB	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-15
ADuCM331WDCPZ	−40°C to +115°C	128 kB/4 kB/6 kB	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-15
ADuCM331WDCPZ-RL	−40°C to +115°C	128 kB/4 kB/6 kB	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-15
EVAL-ADUCM331QSPZ			Socketed Evaluation Board with Switches and LEDs	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] The ADuCM330/ADuCM331 are functional but have degraded performance at temperatures from 115°C to 125°C.

AUTOMOTIVE PRODUCTS

The ADuCM330W/ADuCM331W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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