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REVISION HISTORY

2/2017—Rev. A to Rev. B

Deleted B Version	Throughout
Changes to Features Section, Applications Section, and Product Highlights Section	1
Added Note 2 to Table 1; Renumbered Sequentially	3
Added Note 2 to Table 2; Renumbered Sequentially	4
Added Note 2 to Table 3; Renumbered Sequentially	5
Added Note 1 to Table 4; Renumbered Sequentially	6
Changes to Figure 3 and Table 6.....	7
Updated Outline Dimensions	14
Changes to Ordering Guide	14

11/2009—Rev. 0 to Rev. A

Changes to Table 4.....	6
Added Table 5; Renumbered Sequentially	7
Changes to Table 6.....	7
Update Outline Dimensions	14
Changes to Ordering Guide	14

2/2003—Revision 0: Initial Version

SPECIFICATIONS

DUAL-SUPPLY OPERATION

$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On Resistance, R_{ON}	52	90	100	Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = 1\text{ mA}$; see Figure 20
	75			Ω max	$V_S = \pm 4.5\text{ V}$, $I_S = 1\text{ mA}$; see Figure 20
On-Resistance Match Between Channels, ΔR_{ON}	0.8			Ω typ	$V_S = \pm 3.5\text{ V}$, $I_S = 1\text{ mA}$
	1.3	1.8	2	Ω max	$V_S = \pm 3.5\text{ V}$, $I_S = 1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	9			Ω typ	$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$, $V_S = \pm 3\text{ V}$, $I_S = 1\text{ mA}$
	12	13	14	Ω max	$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$, $V_S = \pm 3\text{ V}$, $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, $I_{S(OFF)}$	± 0.005			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.2		± 5	nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 21
Drain Off Leakage, $I_{D(OFF)}$	± 0.005			nA typ	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 21
	± 0.2		± 5	nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 22
Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$	± 0.005			nA typ	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 22
	± 0.2		± 5	nA max	$V_D = V_S = \pm 4.5\text{ V}$; see Figure 23
					$V_D = V_S = \pm 4.5\text{ V}$; see Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	$V_{IN} = V_{INL}$ or V_{INH} $V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	
			± 1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS¹					
$t_{TRANSITION}$	60	110	130	ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 24
	90			ns max	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 24
$t_{ON}(\overline{EN})$	70	120	135	ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
	95			ns max	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
$t_{OFF}(\overline{EN})$	25	45	50	ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
	40			ns max	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
Break-Before-Make Time Delay, t_{BBM}	40		10	ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 25
				ns min	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 25
Charge Injection	2			pC typ	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$; see Figure 27
	4			pC max	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$; see Figure 27
Off Isolation	−90			dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Total Harmonic Distortion, THD + N	0.025			% typ	$R_L = 600\text{ }\Omega$, 2 V p-p , $f = 20\text{ Hz}$ to 20 kHz
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30
−3 dB Bandwidth	580			MHz typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$; see Figure 29
$C_{S(OFF)}$	4			pF typ	$f = 1\text{ MHz}$
$C_{D(OFF)}$	7			pF typ	$f = 1\text{ MHz}$
$C_{D(ON)}$, $C_{S(ON)}$	12			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS²					
I_{DD}	0.01		1	μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
				μA max	Digital inputs = 0 V or 5.5 V
I_{SS}	0.01		1	μA typ	Digital inputs = 0 V or 5.5 V
				μA max	Digital inputs = 0 V or 5.5 V

¹ Guaranteed by design; not subject to production test.

² The device is fully specified at a $\pm 5\text{ V}$ dual supply and at 5 V and 3.3 V single supplies. It is possible to operate the ADG633 with unbalanced supplies or at other voltage supplies ($\pm 2\text{ V}$ to $\pm 6\text{ V}$, and 2 V to 12 V); however, the switch characteristics change. These changes include, but are not limited to: analog signal range, on resistance, leakage, V_{INL} , V_{INH} , and switching times. The optimal power-up sequence for the device is: ground, V_{DD} , V_{SS} , and then the digital inputs, before applying the analog input signal.

SINGLE-SUPPLY OPERATION

$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance, R_{ON}	85	160	200	Ω typ	$V_S = 0\text{ V}$ to 4.5 V , $I_S = 1\text{ mA}$; see Figure 20
	150			Ω max	$V_S = 0\text{ V}$ to 4.5 V , $I_S = 1\text{ mA}$; see Figure 20
On-Resistance Match Between Channels, ΔR_{ON}	4.5			Ω typ	$V_S = +3.5\text{ V}$, $I_S = 1\text{ mA}$
	8	9	10	Ω max	$V_S = +3.5\text{ V}$, $I_S = 1\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	13	14	16	Ω typ	$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_S = 1.5\text{ V}$ to 4 V , $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, $I_{S(OFF)}$	± 0.005			nA typ	$V_{DD} = 5.5\text{ V}$
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 21
Drain Off Leakage, $I_{D(OFF)}$	± 0.005			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 21
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 22
Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$	± 0.005			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 22
	± 0.2		± 5	nA max	$V_S = V_D = 1\text{ V}$ or 4.5 V ; see Figure 23
				nA max	$V_S = V_D = 1\text{ V}$ or 4.5 V ; see Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 1	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
				μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS ¹					
$t_{TRANSITION}$	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 24
	150	190	220	ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 24
$t_{ON}(\overline{EN})$	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
	150	190	220	ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
$t_{OFF}(\overline{EN})$	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
	35	45	50	ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 26
Break-Before-Make Time Delay, t_{BBM}	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 25
			10	ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 25
Charge Injection	0.5			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 27
	1			pC max	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 27
Off Isolation	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30
−3 dB Bandwidth	520			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29
$C_{S(OFF)}$	5			pF typ	$f = 1\text{ MHz}$
$C_{D(OFF)}$	8			pF typ	$f = 1\text{ MHz}$
$C_{D(ON)}$, $C_{S(ON)}$	12			pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS ²					
I_{DD}	0.01			μA typ	$V_{DD} = 5.5\text{ V}$
			1	μA max	Digital inputs = 0 V or 5.5 V
					Digital inputs = 0 V or 5.5 V

¹ Guaranteed by design; not subject to production test.

² The device is fully specified at a $\pm 5\text{ V}$ dual supply and at 5 V and 3.3 V single supplies. It is possible to operate the ADG633 with unbalanced supplies or at other voltage supplies ($\pm 2\text{ V}$ to $\pm 6\text{ V}$, and 2 V to 12 V); however, the switch characteristics change. These changes include, but are not limited to: analog signal range, on resistance, leakage, V_{INL} , V_{INH} , and switching times. The optimal power-up sequence for the device is: ground, V_{DD} , V_{SS} , and then the digital inputs, before applying the analog input signal.

$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 2.7 \text{ V}$, $V_{SS} = 0 \text{ V}$
On Resistance, R_{ON}	185			Ω typ	$V_S = 0 \text{ V to } 2.7 \text{ V}$, $I_S = 0.1 \text{ mA}$; see Figure 20
	300	350	400	Ω max	$V_S = 0 \text{ V to } 2.7 \text{ V}$, $I_S = 0.1 \text{ mA}$; see Figure 20
On-Resistance Match Between Channels, ΔR_{ON}	2			Ω typ	$V_S = +1.5 \text{ V}$, $I_S = 0.1 \text{ mA}$
	4.5	6	7	Ω max	$V_S = +1.5 \text{ V}$, $I_S = 0.1 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, $I_{S(OFF)}$	± 0.005			nA typ	$V_{DD} = 3.3 \text{ V}$
	± 0.2		± 5	nA max	$V_S = 1 \text{ V/3 V}$, $V_D = 3 \text{ V/1 V}$; see Figure 21
Drain Off Leakage, $I_{D(OFF)}$	± 0.005			nA typ	$V_S = 1 \text{ V/3 V}$, $V_D = 3 \text{ V/1 V}$; see Figure 21
	± 0.2		± 5	nA max	$V_S = 1 \text{ V/3 V}$, $V_D = 3 \text{ V/1 V}$; see Figure 22
Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$	± 0.005			nA typ	$V_S = V_D = 1 \text{ V or } 3 \text{ V}$; see Figure 23
	± 0.2		± 5	nA max	$V_S = V_D = 1 \text{ V or } 3 \text{ V}$; see Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{INL}$ or V_{INH} $V_{IN} = V_{INL}$ or V_{INH}
Input Low Voltage, V_{INL}			0.5	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	
			± 1	μA max	
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS¹					
$t_{TRANSITION}$	170			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 24
	300	370	400	ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 24
$t_{ON}(\overline{EN})$	200			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 26
	310	380	420	ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 26
$t_{OFF}(\overline{EN})$	30			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 26
	40	55	75	ns max	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_S = 1.5 \text{ V}$; see Figure 26
Break-Before-Make Time Delay, t_{BBM}	180			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 25
			10	ns min	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$, $V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 25
Charge Injection	1			pC typ	$V_S = 1.5 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 27
	2			pC max	$V_S = 1.5 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 27
Off Isolation	−90			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 30
−3 dB Bandwidth	500			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 29
$C_{S(OFF)}$	5			pF typ	$f = 1 \text{ MHz}$
$C_{D(OFF)}$	8			pF typ	$f = 1 \text{ MHz}$
$C_{D(ON)}$, $C_{S(ON)}$	12			pF typ	$f = 1 \text{ MHz}$
POWER REQUIREMENTS²					
I_{DD}	0.01			μA typ	$V_{DD} = 3.3 \text{ V}$
			1	μA max	Digital inputs = 0 V or 3.3 V
					Digital inputs = 0 V or 3.3 V

¹ Guaranteed by design; not subject to production test.

² The device is fully specified at a $\pm 5 \text{ V}$ dual supply and at 5 V and 3.3 V single supplies. It is possible to operate the ADG633 with unbalanced supplies or at other voltage supplies ($\pm 2 \text{ V to } \pm 6 \text{ V}$, and 2 V to 12 V); however, the switch characteristics change. These changes include, but are not limited to: analog signal range, on resistance, leakage, V_{INL} , V_{INH} , and switching times. The optimal power-up sequence for the device is: ground, V_{DD} , V_{SS} , and then the digital inputs, before applying the analog input signal.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS} ¹	13 V
V_{DD} to GND	−0.3 V to +13 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs ²	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Digital Inputs ²	GND − 0.3 V to $V_{DD} + 0.3\text{ V}$ or 10 mA, whichever occurs first
Peak Current, S or D	40 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	20 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead TSSOP	150.4°C/W
16-Lead LFCSP, 4-Layer Board	70°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	220°C
(Pb-Free) Soldering	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec
ESD	4 kV

¹ The device is fully specified at a $\pm 5\text{ V}$ dual supply and at 5 V and 3.3 V single supplies. It is possible to operate the ADG633 with unbalanced supplies or at other voltage supplies ($\pm 2\text{ V}$ to $\pm 6\text{ V}$, and 2 V to 12 V); however, the switch characteristics change. These changes include, but are not limited to: analog signal range, on resistance, leakage, V_{INL} , V_{INH} , and switching times. The optimal power-up sequence for the device is: ground, V_{DD} , V_{SS} , and then the digital inputs, before applying the analog input signal.

² Overvoltages at Ax, EN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

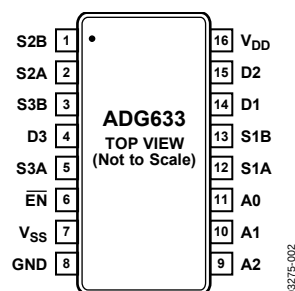
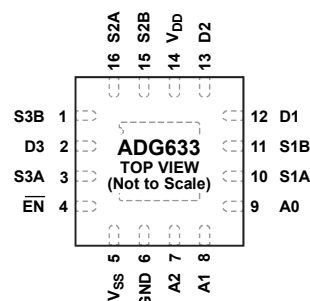


Figure 2. 16-Lead TSSOP Pin Configuration



NOTES
1. THE EXPOSED PADDLE CAN BE LEFT FLOATING OR BE TIED TO V_{DD} , V_{SS} , OR GND.

Figure 3. 16-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	S2B	Source Terminal of Multiplexer 2. Can be an input or output.
2	16	S2A	Source Terminal of Multiplexer 2. Can be an input or output.
3	1	S3B	Source Terminal of Multiplexer 3. Can be an input or output.
4	2	D3	Drain Terminal of Multiplexer 3. Can be an input or output.
5	3	S3A	Source Terminal of Multiplexer 3. Can be an input or output.
6	4	EN	Digital Control Input. Disables all multiplexers when set high.
7	5	V_{SS}	Most Negative Power Supply Terminal. Tie this pin to GND when using the device with single-supply voltages.
8	6	GND	Ground (0 V) Reference.
9	7	A2	Digital Control Input.
10	8	A1	Digital Control Input.
11	9	A0	Digital Control Input.
12	10	S1A	Source Terminal of Multiplexer 1. Can be an input or output.
13	11	S1B	Source Terminal of Multiplexer 1. Can be an input or output.
14	12	D1	Drain Terminal of Multiplexer 1. Can be an input or output.
15	13	D2	Drain Terminal of Multiplexer 2. Can be an input or output.
16	14	V_{DD}	Most Positive Power Supply Terminal.
Not applicable	EP	EP	Exposed Paddle. The exposed paddle can be left floating or be tied to V_{DD} , V_{SS} , or GND.

Table 6. ADG633 Truth Table

A2	A1	A0	EN	Switch Condition					
				Switch S1A/D1	Switch S1B/D1	Switch S2A/D2	Switch S2B/D2	Switch S3A/D3	Switch S3B/D3
X ¹	X ¹	X ¹	1	Off	Off	Off	Off	Off	Off
0	0	0	0	On	Off	On	Off	On	Off
0	0	1	0	Off	On	On	Off	On	Off
0	1	0	0	On	Off	Off	On	On	Off
0	1	1	0	Off	On	Off	On	On	Off
1	0	0	0	On	Off	On	Off	Off	On
1	0	1	0	Off	On	On	Off	Off	On
1	1	0	0	On	Off	Off	On	Off	On
1	1	1	0	Off	On	Off	On	Off	On

¹ X means the logic state does not matter; it can be either 0 or 1.

TYPICAL PERFORMANCE CHARACTERISTICS

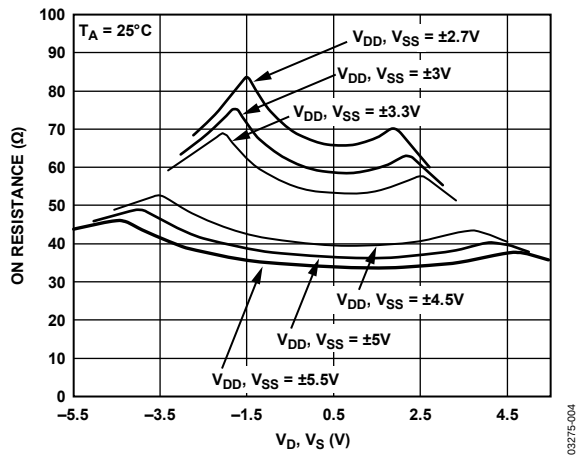
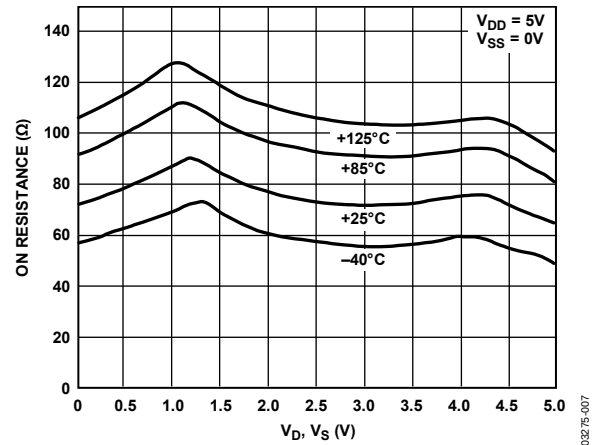
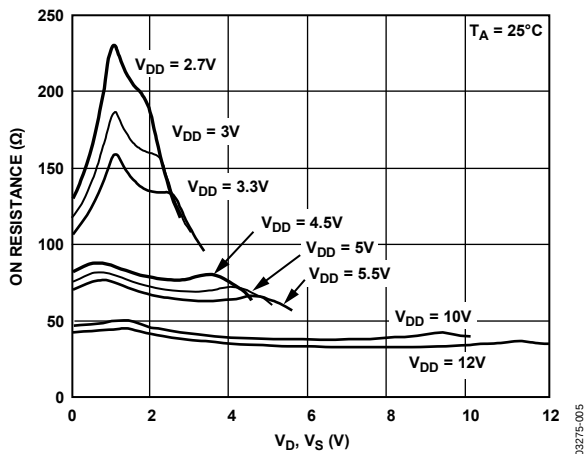
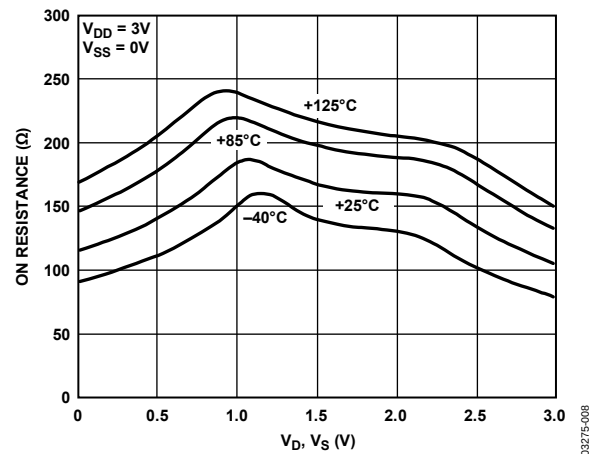
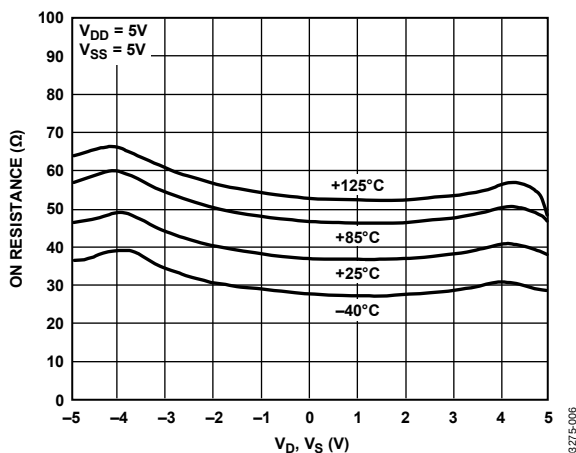
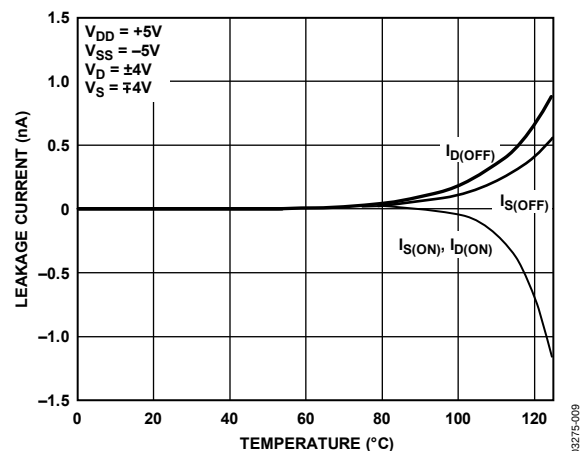
Figure 4. On Resistance vs. V_D (V_S), Dual SuppliesFigure 7. On Resistance vs. V_D (V_S) for Various Temperatures, Single SupplyFigure 5. On Resistance vs. V_D (V_S), Single SupplyFigure 8. On Resistance vs. V_D (V_S) for Various Temperatures, Single SupplyFigure 6. On Resistance vs. V_D (V_S) for Various Temperatures, Dual Supplies

Figure 9. Leakage Current vs. Temperature, Dual Supplies

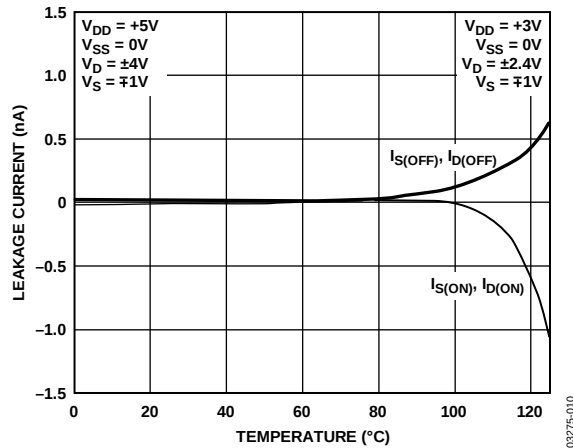


Figure 10. Leakage Current vs. Temperature, Single Supply

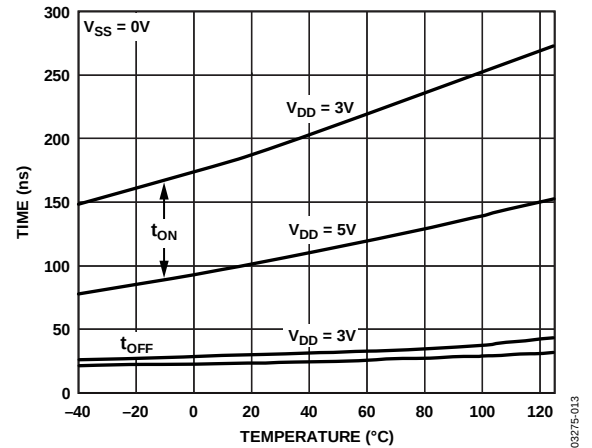
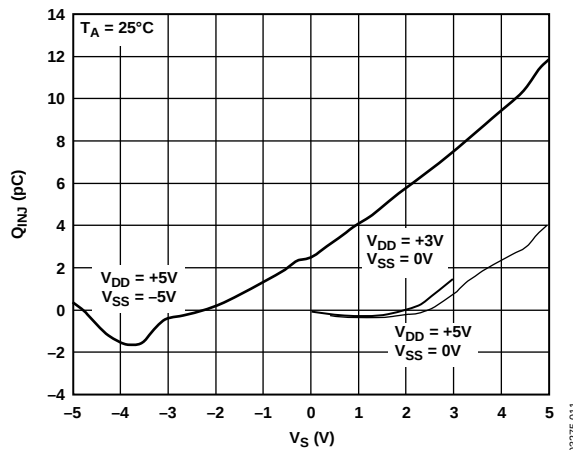
Figure 13. t_{ON}/t_{OFF} Times vs. Temperature, Single Supply

Figure 11. Charge Injection vs. Source Voltage

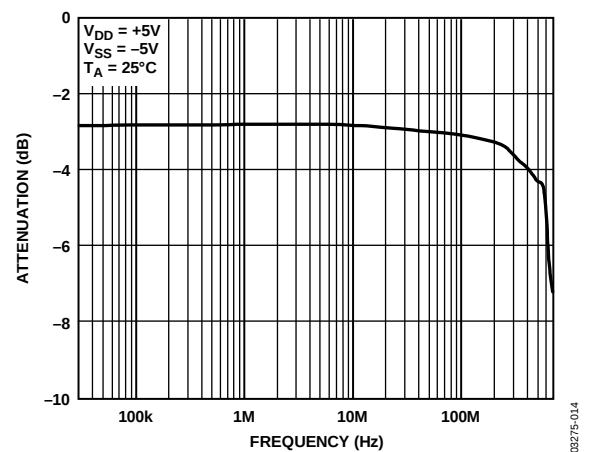


Figure 14. On Response vs. Frequency

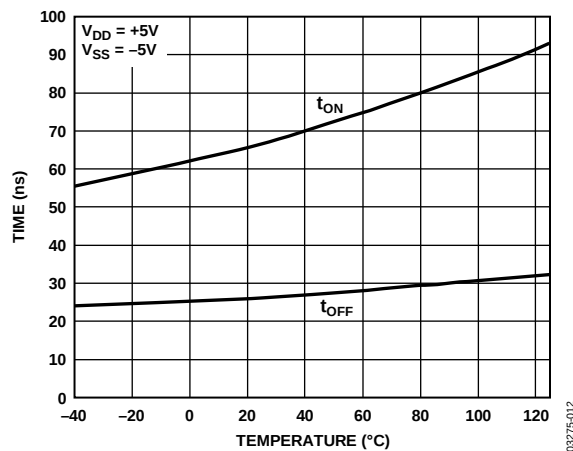
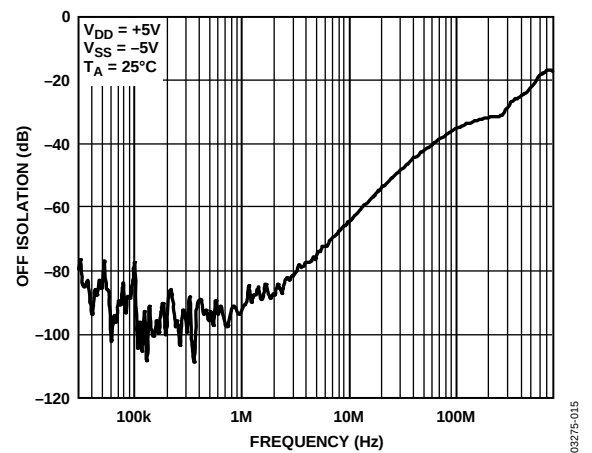
Figure 12. t_{ON}/t_{OFF} Times vs. Temperature, Dual Supplies

Figure 15. Off Isolation vs. Frequency

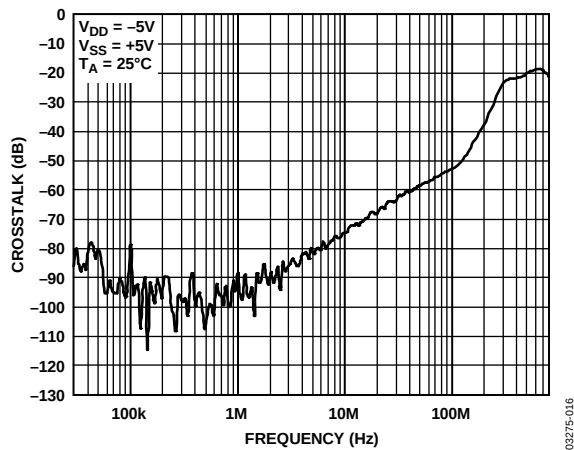


Figure 16. Crosstalk vs. Frequency

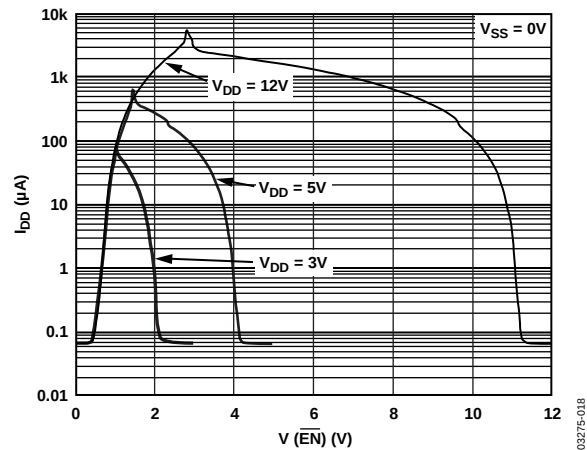


Figure 18. V_{DD} Current vs. Logic Level

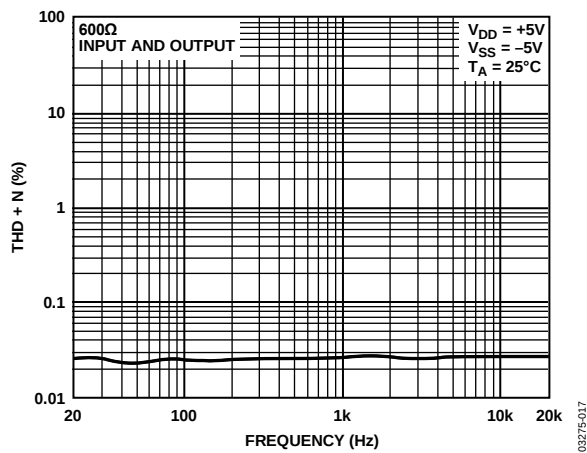


Figure 17. THD + Noise vs. Frequency

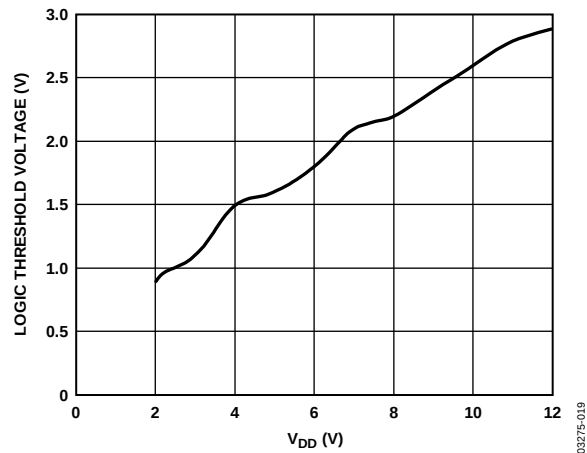


Figure 19. Logic Threshold Voltage vs. V_{DD}

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}

Most negative power supply potential.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

GND

Ground (0 V) reference.

S

Source terminal. Can be an input or output.

D

Drain terminal. Can be an input or output.

A_x

Logic control input.

$\overline{EN}$

Active low digital input. When $\overline{EN}$ is high, the device is disabled and all switches are off. When $\overline{EN}$ is low, the A_x logic inputs determine the on switches.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

On-resistance match between any two channels, that is, $R_{ONMAX} - R_{ONMIN}$.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

$I_{S(OFF)}$

Source leakage current with the switch off.

$I_{D(OFF)}$

Drain leakage current with the switch off.

$I_{D(ON)}, I_{S(ON)}$

Channel leakage current with the switch on.

V_{INH}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

$C_{S(OFF)}$

Off switch source capacitance. Measured with reference to ground.

$C_{D(OFF)}$

Off switch drain capacitance. Measured with reference to ground.

$C_{D(ON)}, C_{S(ON)}$

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

$t_{ON}(\overline{EN})$

Delay between applying the digital control input and the output switching on (see Figure 26).

$t_{OFF}(\overline{EN})$

Delay between applying the digital control input and the output switching off (see Figure 26).

t_{BBM}

On time, measured between 80% points of both switches when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

TEST CIRCUITS

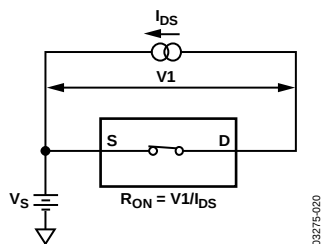


Figure 20. On Resistance

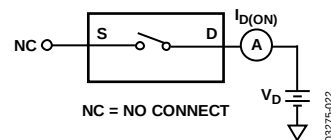


Figure 22. Drain Off Leakage

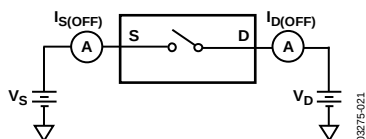


Figure 21. Source Off Leakage

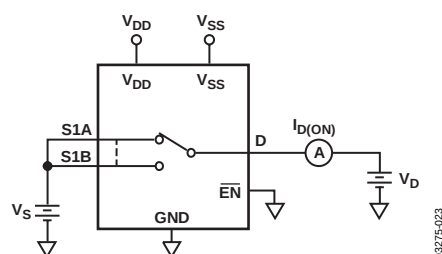
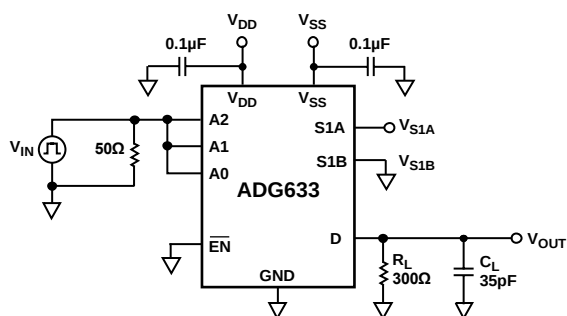
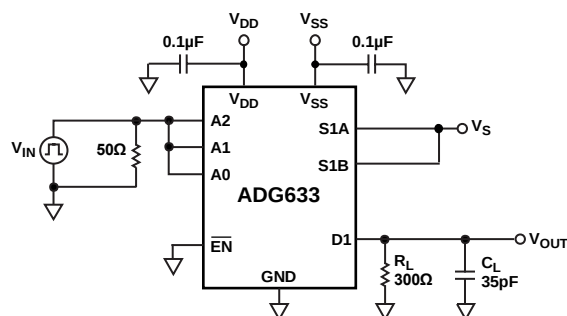
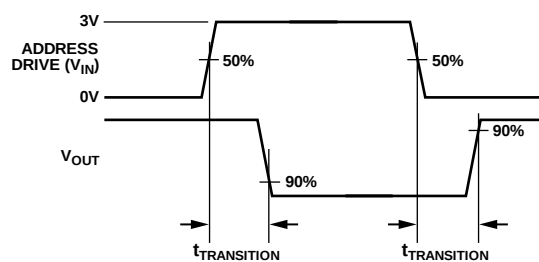
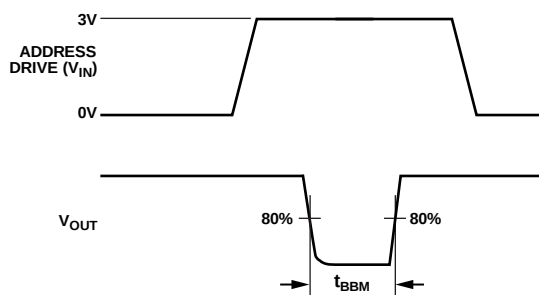


Figure 23. Channel On Leakage

Figure 24. Transition Time, $t_{TRANSITION}$ Figure 25. Break-Before-Make Delay, t_{BBM} 

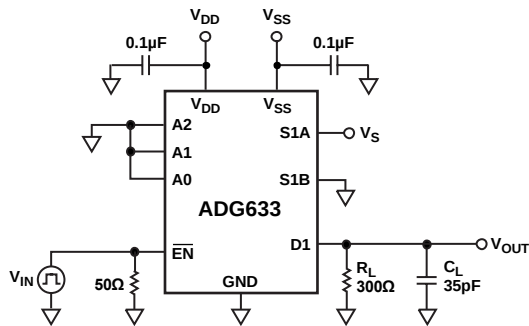
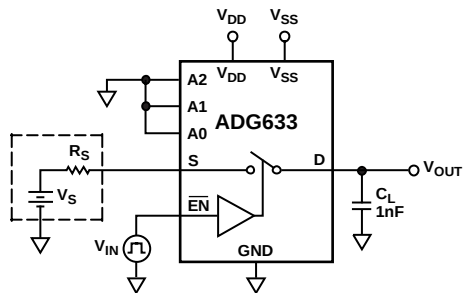
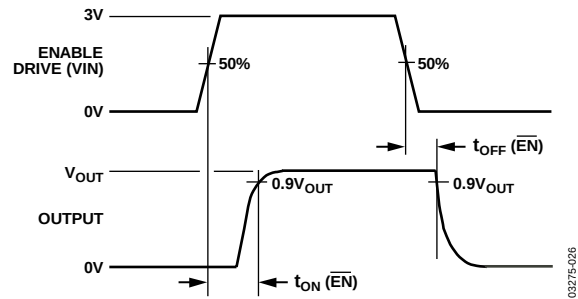
Figure 26. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$ 

Figure 27. Charge Injection

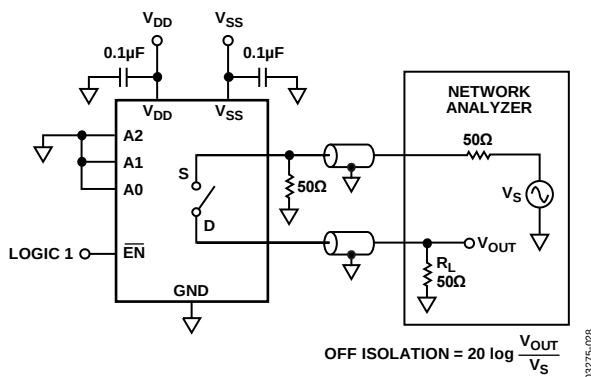
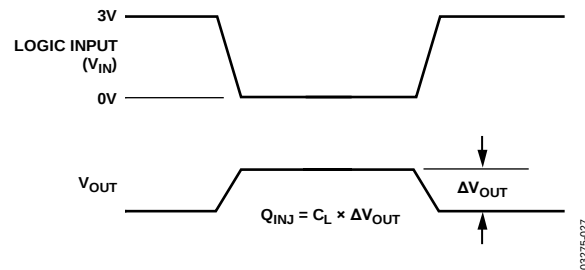


Figure 28. Off Isolation

$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

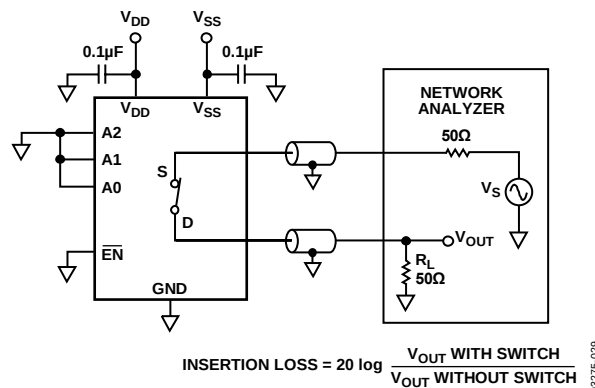


Figure 29. Bandwidth

$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

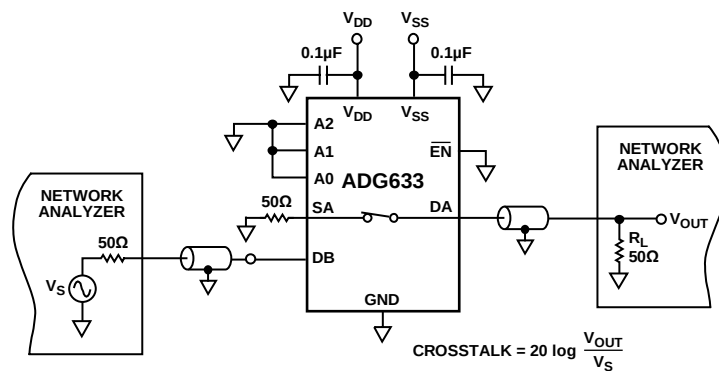
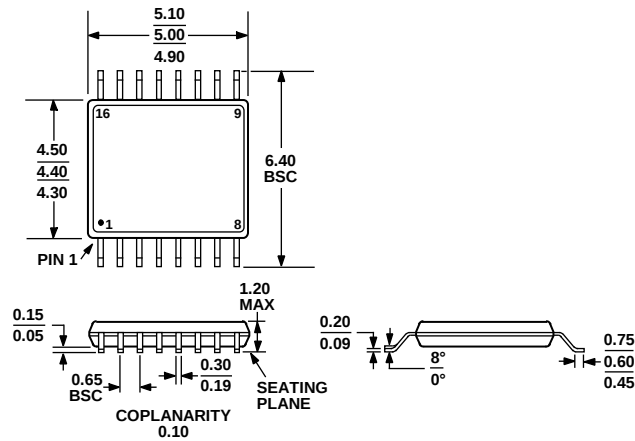


Figure 30. Channel-to-Channel Crosstalk

$$\text{CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

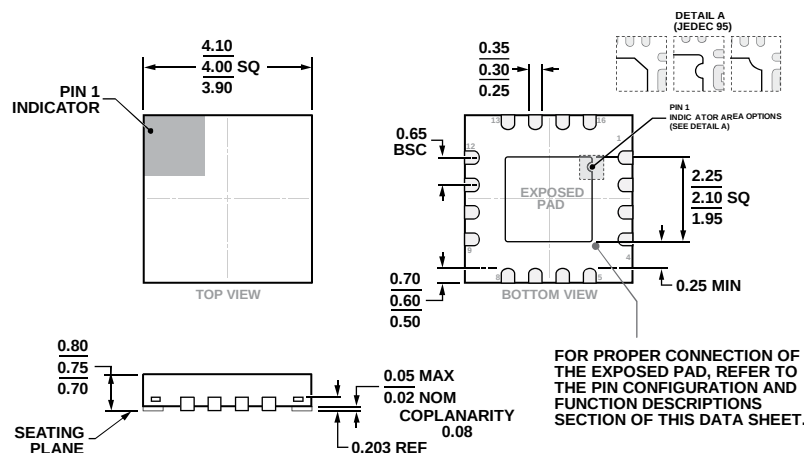
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 31. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 32. 16-Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG633YRU	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG633YRU-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG633YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG633YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG633YCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG633YCPZ-REEL7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23

¹ Z = RoHS Compliant Part.

NOTES

NOTES