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REVISION HISTORY

8/09—Rev. B to Rev. C

Updated Format ..... Universal
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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = 5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

	B Version			T Version			
Parameter[1]	**+25°C**	**−40°C to +85°C**	**−40°C to +125°C**	**+25°C**	**−55°C to +125°C**	**Unit**	**Test Conditions/Comments**
ANALOG SWITCH							
Analog Signal Range			V_{SS} to V_{DD}		V_{SS} to V_{DD}		
R_{ON}	25			25		Ω typ	V_D = ±12.5 V, I_S = −10 mA
	35	45	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
LEAKAGE CURRENTS							V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V; see Figure 12
	±0.25	±5	±15	±0.25	±15	nA max	
Drain Off Leakage, I_D (Off)	±0.1			±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V; see Figure 12
	±0.75	±5	±30	±0.75	±30	nA max	
Channel On Leakage, I_D, I_S (On)	±0.4			±0.4		nA typ	V_S = V_D = ±15.5 V; see Figure 13
	±0.75	±5	±30	±0.75	±30	nA max	
DIGITAL INPUTS							
Input High Voltage, V_{INH}		2.4	2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8		0.8	V max	
Input Current							
I_{INL} or I_{INH}		±0.005	±0.005		±0.005	μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]							
$t_{TRANSITION}$	160	200	200	145	200	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = ±10 V, V_{S2} = ∓10 V; see Figure 14
Break-Before-Make Time Delay, t_D	30			30		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = ±10 V; see Figure 15
	5			5		ns min	
Off Isolation	80			80		dB typ	R_L = 50 Ω, f = 1 MHz; see Figure 16
Channel-to-Channel Crosstalk	90			70		dB typ	R_L = 50 Ω, f = 1 MHz; see Figure 17
C_S (Off)	6			6		pF typ	f = 1 MHz
C_D, C_S (On)	55			55		pF typ	f = 1 MHz
POWER REQUIREMENTS							V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.0001			0.0001		μA typ	V_{IN} = 0 V or 5 V
	1	2.5	2.5	1	2.5	μA max	
I_{SS}	0.0001			0.0001		μA typ	
	1	2.5	2.5	1	2.5	μA max	
I_L	0.0001			0.0001		μA typ	V_L = 5.5 V
	1	2.5	2.5	1	2.5	μA max	

[1] Temperature ranges are as follows: B Version: −40°C to +125°C; T Version: −55°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter[1]	B Version +25°C	B Version −40°C to +85°C	B Version −40°C to +125°C	T Version +25°C	T Version −55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH							
Analog Signal Range			0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	40			40		Ω typ	V_D = 3 V, 8.5 V, I_S = −10 mA
		60	70		70	Ω max	V_{DD} = 10.8 V
LEAKAGE CURRENT							V_{DD} = 13.2 V
Source OFF Leakage, I_S (Off)	±0.1			±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V; see Figure 12
	±0.25	±5	±15	±0.25	±15	nA max	
Drain OFF Leakage, I_D (Off)	±0.1			±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V; see Figure 12
	±0.75	±5	±30	±0.75	±30	nA max	
Channel ON Leakage, I_D, I_S (On)	±0.4			±0.4		nA typ	V_S = V_D = 12.2 V/1 V; see Figure 13
	±0.75	±5	±30	±0.75	±30	nA max	
DIGITAL INPUTS							
Input High Voltage, V_{INH}		2.4	2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8		0.8	V max	
Input Current							
I_{INL} or I_{INH}		±0.005	±0.005		±0.005	μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	±0.5		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]							
$t_{TRANSITION}$	180	250	250	170	250	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = 0 V/8 V, V_{S2} = 8 V/0 V; see Figure 14
Break-Before-Make Time Delay, t_D	60			60		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = 8 V; see Figure 15
Off Isolation	80			80		dB typ	R_L = 50 Ω, f = 1 MHz; see Figure 16
Channel-to-Channel Crosstalk	90			70		dB typ	R_L = 50 Ω, f = 1 MHz; see Figure 17
C_S (Off)	13			13		pF typ	f = 1 MHz
C_D, C_S (On)	65			65		pF typ	f = 1 MHz
POWER REQUIREMENTS							V_{DD} = 13.2 V
I_{DD}	0.0001			0.0001		μA typ	V_{IN} = 0 V or 5 V
	1	2.5	2.5	1	2.5	μA max	
I_L	0.0001			0.0001		μA typ	V_L = 5.5 V
	1	2.5	2.5	1	2.5	μA max	

[1] Temperature ranges are as follows: B Version: −40°C to +125°C; T Version: −55°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A= 25°C unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[1]	V_{SS} − 2 V to V_{DD} + 2 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
CERDIP Package, Power Dissipation	600 mW
θ_{JA}, Thermal Impedance	110°C/W
Lead Temperature, Soldering (10 sec)	300°C
PDIP Package, Power Dissipation	400 mW
θ_{JA}, Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	400 mW
θ_{JA}, Thermal Impedance	155°C/W
MSOP Package, Power Dissipation	315 mW
θ_{JA}, Thermal Impedance	205°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1]Overvoltages at IN, S or D is clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

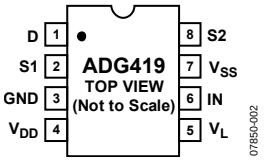


Figure 2. Pin Configuration

Table 4. Pin Function Description

Pin No.	Mnemonic	Description
1	D	Drain terminal. May be an input or an output.
2	S1	Source terminal. May be an input or an output.
3	GND	Ground (0 V) reference.
4	V_{DD}	Most positive power supply potential.
5	V_L	Logic power supply (5 V).
6	IN	Logic control input.
7	V_{SS}	Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND.
8	S2	Source terminal. May be an input or an output.

Table 5. Truth Table

Logic	Switch 1	Switch 2
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

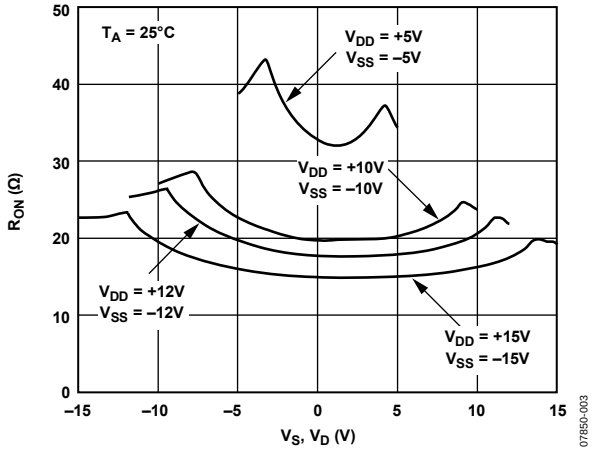


Figure 3. R_{ON} as a Function of V_D (V_S), Dual-Supply Voltage

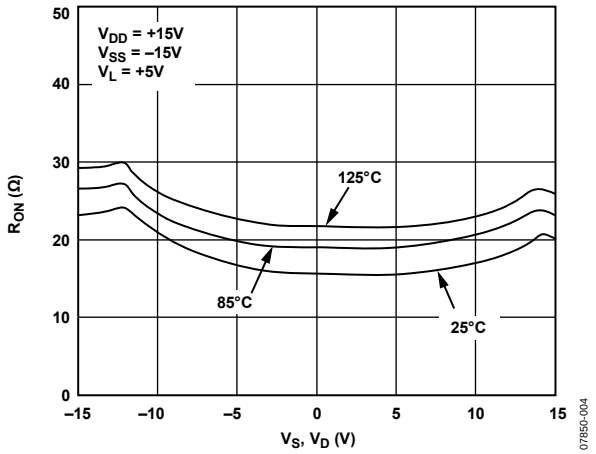


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

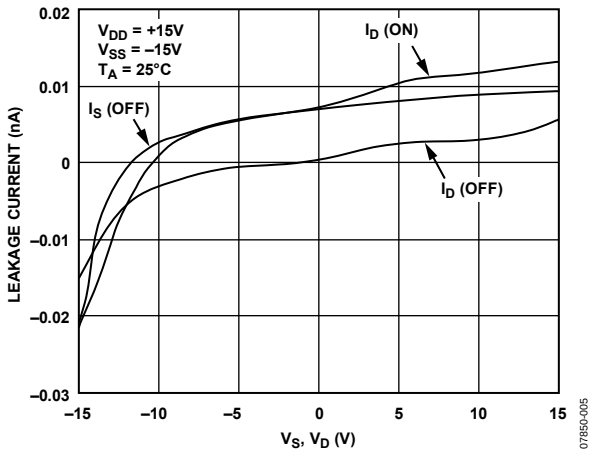


Figure 5. Leakage Currents as a Function of V_S (V_D)

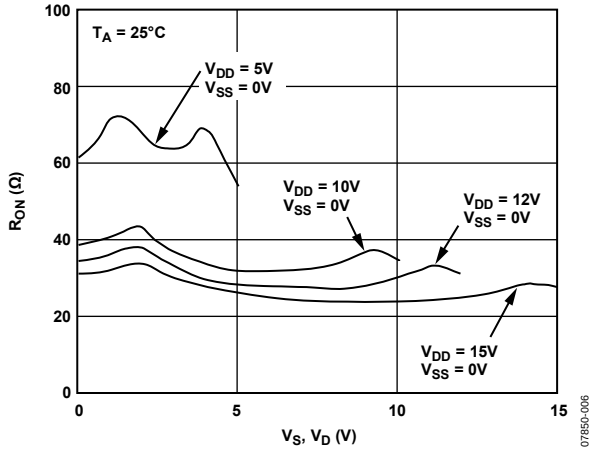


Figure 6. R_{ON} as a Function of V_D (V_S), Single-Supply Voltage

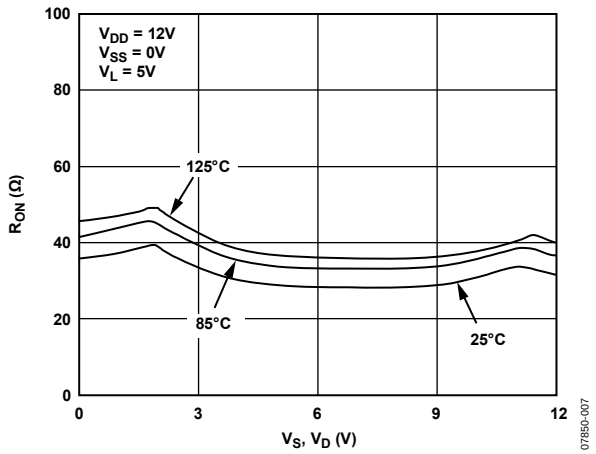


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

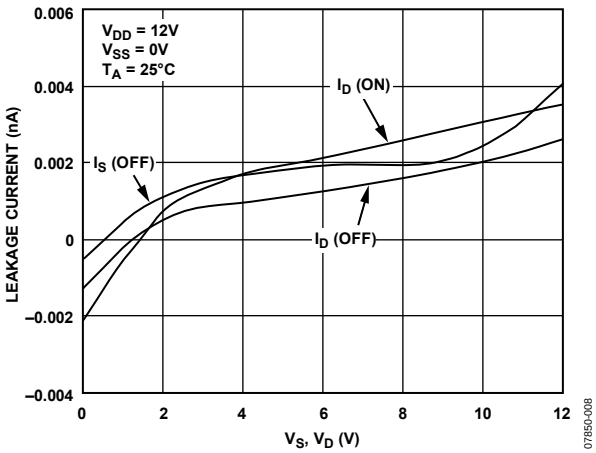


Figure 8. Leakage Currents as a Function of V_S (V_D)

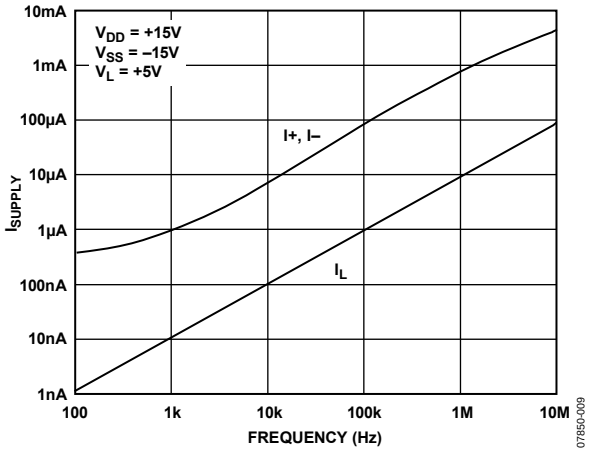


Figure 9. Supply Current (I_{SUPPLY}) vs. Input Switching Frequency

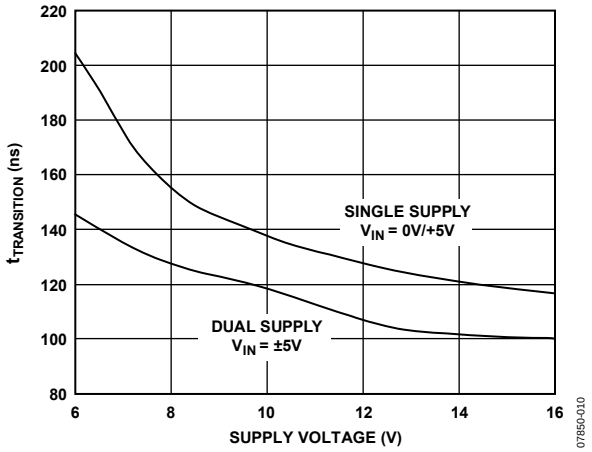


Figure 10. Transition Time ($t_{TRANSITION}$) vs. Power Supply Voltage

TEST CIRCUITS

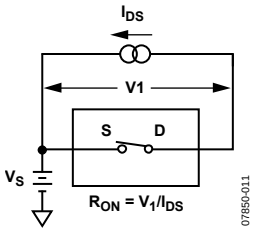


Figure 11. On Resistance

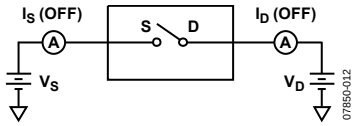


Figure 12. Off Leakage

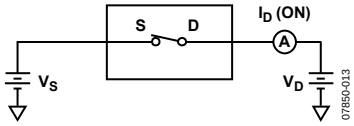


Figure 13. On Leakage

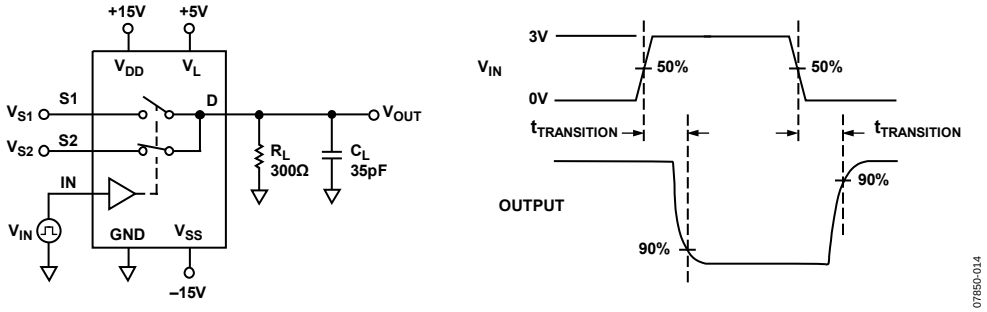


Figure 14. Transition Time, $t_{TRANSITION}$

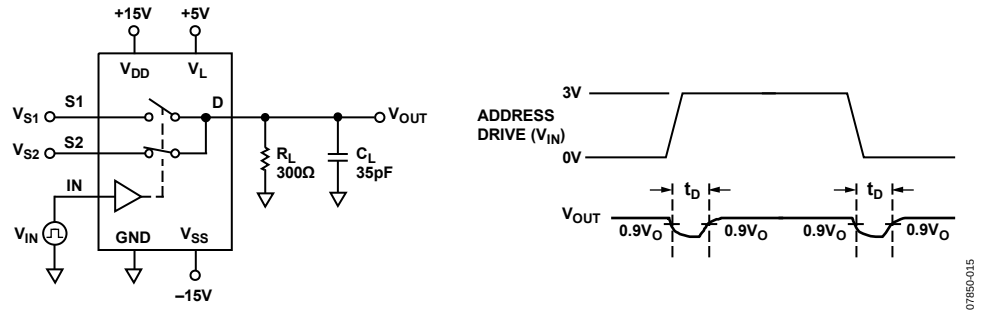


Figure 15. Break-Before-Make Time Delay, t_D

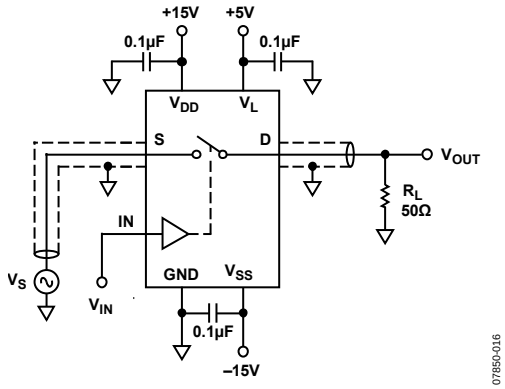


Figure 16. Off Isolation

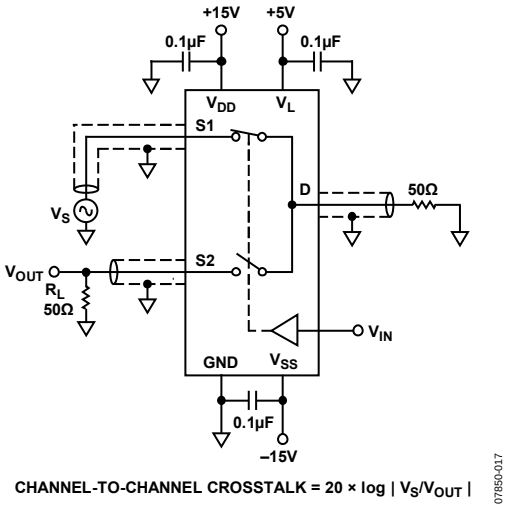


Figure 17. Crosstalk

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential in dual-supply applications. In single-supply applications, it may be connected to GND.

V_L
Logic power supply (5 V).

GND
Ground (0 V) reference.

S
Source terminal. May be an input or an output.

D
Drain terminal. May be an input or an output.

IN
Logic control input.

R_{ON}
Ohmic resistance between D and S.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on terminals D, S.

C_S (Off)
Off switch source capacitance.

C_D, C_S (On)
On switch capacitance.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D
Off time or on time measured between the 90% points of both switches when switching from one address state to the other.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

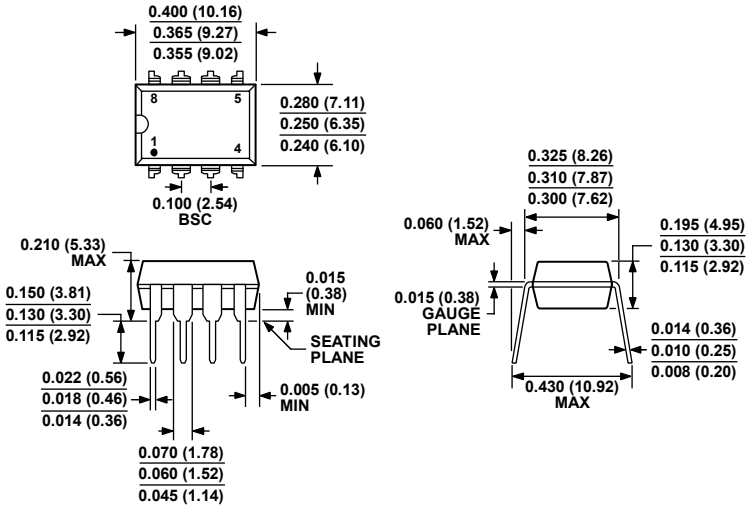
Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off channel.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

OUTLINE DIMENSIONS

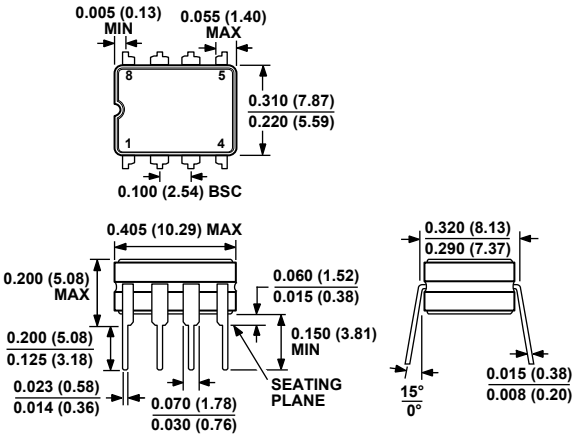


COMPLIANT TO JEDEC STANDARDS MS-001

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

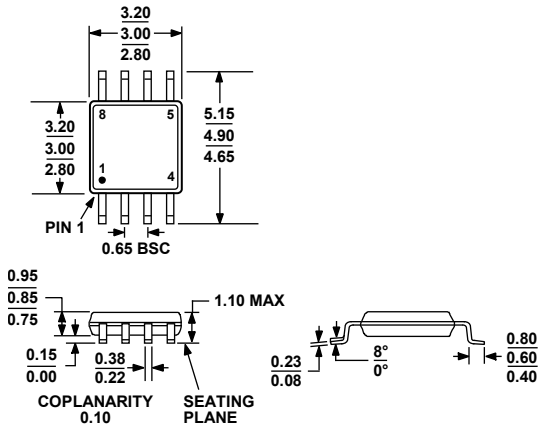
070606-A

Figure 18. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



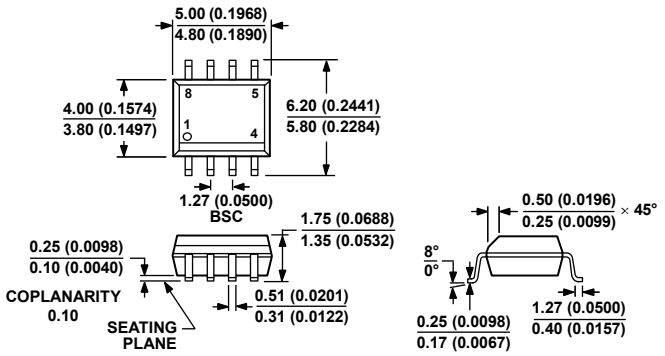
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 20. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG419BN	−40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BNZ[1]	−40°C to +125°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8	
ADG419BR	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BR-REEL7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRZ-REEL7[1]	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADG419BRM	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRM-REEL7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB
ADG419BRMZ[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419BRMZ-REEL7[1]	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBB#
ADG419TQ	−55°C to +125°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8	

[1] Z = RoHS Compliant Part, # denotes that RoHS compliant part is top or bottom marked.

NOTES

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NOTES

D07850-0-8/09(B)