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REVISION HISTORY

3/15—Rev. C to Rev. D

Changes to Figure 12 and Figure 15	9
Updated Outline Dimensions	16
Changes to Ordering Guide	16

10/06—Rev. B to Rev. C

Updated Format	Universal
Changes to Table 3	6
Inserted Table 4 and Table 5	7
Updated Outline Dimensions	14
Changes to Ordering Guide	15

3/03—Rev. A to Rev. B

Changes to Ordering Guide	4
Updated Outline Dimensions	11

2/01—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range		V _{SS} to V _{DD}		V _{SS} to V _{DD}	V	
R _{ON}	40		40		Ω typ	V _D = ±10 V, I _S = −10 mA
	100	125	100	125	Ω max	
ΔR _{ON}	15		15		Ω max	V _D = +10 V, −10 V
LEAKAGE CURRENTS						
Source Off Leakage I _S (Off)	±0.5	±50	±0.5	±50	nA max	V _D = ±10 V, V _S = ∓ 10 V; see Figure 19
Drain Off Leakage I _D (Off)						V _D = ±10 V, V _S = ∓ 10 V; see Figure 20
ADG408	±1	±100	±1	±100	nA max	
ADG409	±1	±50	±1	±50	nA max	
Channel On Leakage I _D , I _S (On)						V _S = V _D = ±10 V; see Figure 21
ADG408	±1	±100	±1	±100	nA max	
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V _{INH}		2.4		2.4	V min	
Input Low Voltage, V _{INL}		0.8		0.8	V max	
Input Current						
I _{INL} or I _{INH}		±10		±10	μA max	V _{IN} = 0 or V _{DD}
C _{IN} , Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS ¹						
t _{TRANSITION}		120		120	ns typ	R _L = 300 Ω, C _L = 35 pF;
		250		250	ns max	V _{S1} = ±10 V, V _{S8} = ∓ 10 V; see Figure 22
t _{OPEN}	10	10	10	10	ns min	R _L = 300 Ω, C _L = 35 pF;
						V _S = 5 V; see Figure 23
t _{ON} (EN)	85	125	85	125	ns typ	R _L = 300 Ω C _L = 35 pF;
	150	225	150	225	ns max	V _S = 5 V; see Figure 24
t _{OFF} (EN)		65		65	ns typ	R _L = 300 Ω, C _L = 35 pF;
		150		150	ns max	V _S = 5 V; see Figure 24
Charge Injection	20		20		pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 10 nF; see Figure 25
OFF Isolation	−75		−75		dB typ	R _L = 1 kΩ, f = 100 kHz;
						V _{EN} = 0 V; see Figure 26
Channel-to-Channel Crosstalk	85		85		dB typ	R _L = 1 kΩ, f = 100 kHz; see Figure 27
C _S (OFF)	11		11		pF typ	f = 1 MHz
C _D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C _D , C _S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	+25°C	–55°C to +125°C		
POWER REQUIREMENTS						
I_{DD}		1		1	$\mu\text{A typ}$	$V_{IN} = 0\text{ V}, V_{EN} = 0\text{ V}$
		5		5	$\mu\text{A max}$	
I_{SS}		1		1	$\mu\text{A typ}$	
		5		5	$\mu\text{A max}$	
I_{DD}	100		100		$\mu\text{A typ}$	$V_{IN} = 0\text{ V}, V_{EN} = 2.4\text{ V}$
	200	500	200	500	$\mu\text{A max}$	

¹ Guaranteed by design, not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $\text{GND} = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	+25°C	–55°C to +125°C		
ANALOG SWITCH						
Analogue Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		$\Omega\text{ typ}$	$V_D = 3\text{ V}, 10\text{ V}, I_S = -1\text{ mA}$
LEAKAGE CURRENTS						
Source Off Leakage I_S (Off)	± 0.5	± 50	± 0.5	± 50	nA max	$V_D = 8\text{ V}/0\text{ V}, V_S = 0\text{ V}/8\text{ V}$; see Figure 19
Drain Off Leakage I_D (Off)						$V_D = 8\text{ V}/0\text{ V}, V_S = 0\text{ V}/8\text{ V}$; see Figure 20
ADG408	± 1	± 100	± 1	± 100	nA max	
ADG409	± 1	± 50	± 1	± 50	nA max	
Channel On Leakage I_D, I_S (On)						$V_S = V_D = 8\text{ V}/0\text{ V}$; see Figure 21
ADG408	± 1	± 100	± 1	± 100	nA max	
ADG409	± 1	± 50	± 1	± 50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		± 10		± 10	$\mu\text{A max}$	$V_{IN} = 0\text{ or }V_{DD}$
C_{IN} , Digital Input Capacitance	8		8		pF typ	$f = 1\text{ MHz}$
DYNAMIC CHARACTERISTICS ¹						
$t_{TRANSITION}$	130		130		ns typ	$R_L = 300\ \Omega, C_L = 35\text{ pF}$; $V_{S1} = 8\text{ V}/0\text{ V}, V_{S8} = 0\text{ V}/8\text{ V}$; see Figure 22
t_{OPEN}	10		10		ns typ	$R_L = 300\ \Omega, C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 23
t_{ON} (EN)	140		140		ns typ	$R_L = 300\ \Omega, C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 24
t_{OFF} (EN)	60		60		ns typ	$R_L = 300\ \Omega, C_L = 35\text{ pF}$; $V_S = 5\text{ V}$; see Figure 24
Charge Injection	5		5		pC typ	$V_S = 0\text{ V}, R_S = 0\ \Omega, C_L = 10\text{ nF}$; see Figure 25
Off Isolation	–75		–75		dB typ	$R_L = 1\text{ k}\Omega, f = 100\text{ kHz}$; $V_{EN} = 0\text{ V}$; see Figure 26

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	+25°C	–55°C to +125°C		
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 1\text{ k}\Omega$, $f = 100\text{ kHz}$; see Figure 27
C_S (Off)	11		11		pF typ	$f = 1\text{ MHz}$
C_D (Off)						$f = 1\text{ MHz}$
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C_D , C_S (On)						$f = 1\text{ MHz}$
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I_{DD}		1		1	$\mu\text{A typ}$	$V_{IN} = 0\text{ V}$, $V_{EN} = 0\text{ V}$
		5		5	$\mu\text{A max}$	
I_{DD}	100		100		$\mu\text{A typ}$	$V_{IN} = 0\text{ V}$, $V_{EN} = 2.4\text{ V}$
	200	500	200	500	$\mu\text{A max}$	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +32 V
V_{SS} to GND	+0.3 V to −32 V
Analog, Digital Inputs	$V_{SS} - 2\text{ V}$ to $V_{DD} + 2\text{ V}$ or 20 mA, whichever occurs first
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
CERDIP Package, Power Dissipation	900 mW
θ_{JA} , Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	300°C
PDIP Package, Power Dissipation	470 mW
θ_{JA} , Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	260°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} , Thermal Impedance	155°C/W
θ_{JC} , Thermal Impedance	50°C/W
SOIC Package, Power Dissipation	600 mW
θ_{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

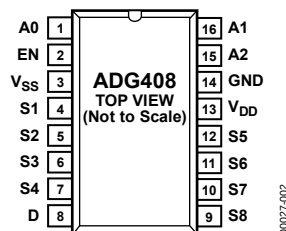


Figure 2. ADG408 Pin Configuration

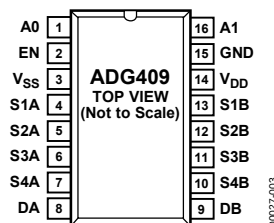


Figure 3. ADG409 Pin Configuration

Table 4. ADG408 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
4	S1	Source Terminal 1. Can be an input or an output.
5	S2	Source Terminal 2. Can be an input or an output.
6	S3	Source Terminal 3. Can be an input or an output.
7	S4	Source Terminal 4. Can be an input or an output.
8	D	Drain Terminal. Can be an input or an output.
9	S8	Source Terminal 8. Can be an input or an output.
10	S7	Source Terminal 7. Can be an input or an output.
11	S6	Source Terminal 6. Can be an input or an output.
12	S5	Source Terminal 5. Can be an input or an output.
13	V _{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

Table 6. ADG408 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

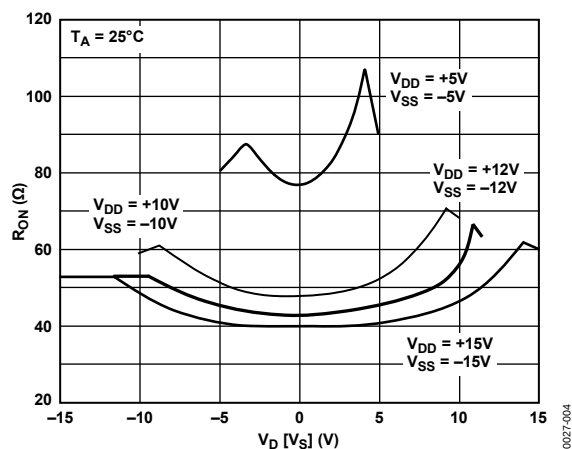
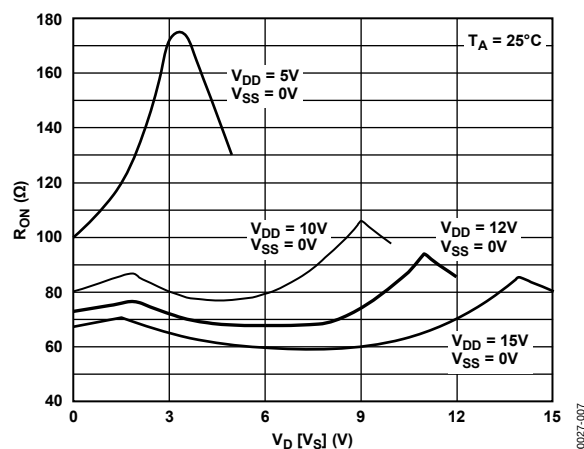
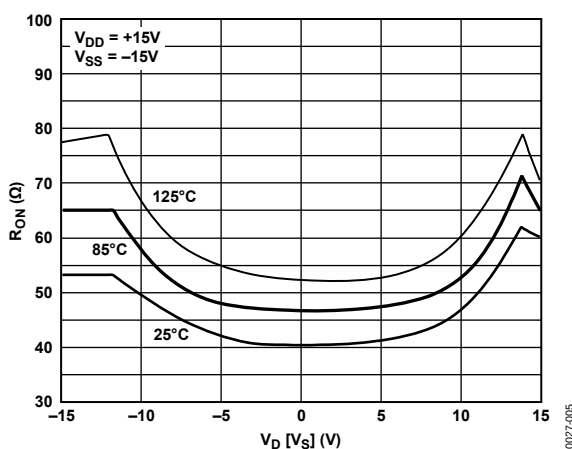
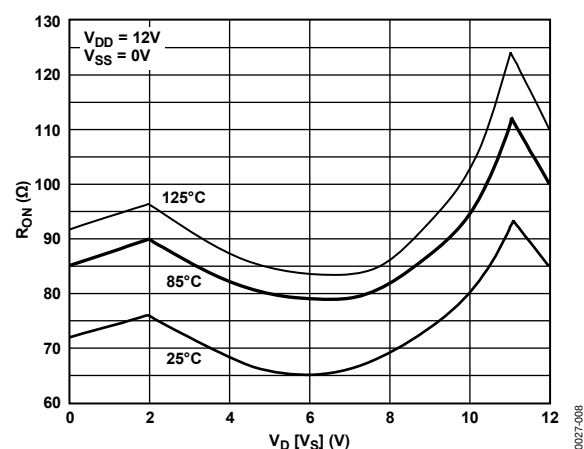
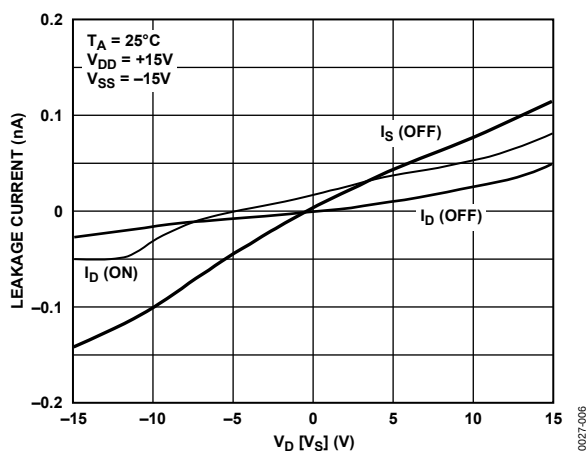
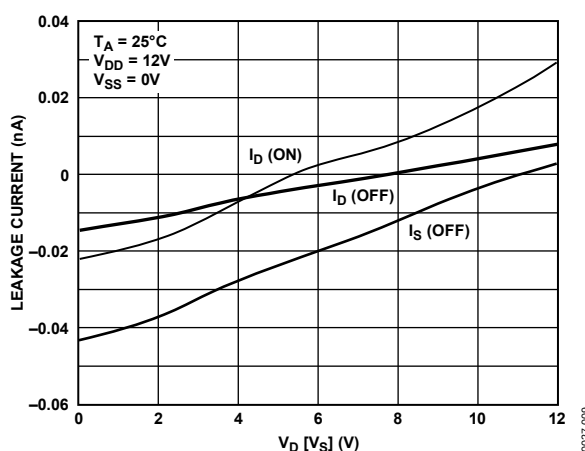
Table 5. ADG409 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V _{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
4	S1A	Source Terminal 1A. Can be an input or an output.
5	S2A	Source Terminal 2A. Can be an input or an output.
6	S3A	Source Terminal 3A. Can be an input or an output.
7	S4A	Source Terminal 4A. Can be an input or an output.
8	DA	Drain Terminal A. Can be an input or an output.
9	DB	Drain Terminal B. Can be an input or an output.
10	S4B	Source Terminal 4B. Can be an input or an output.
11	S3B	Source Terminal 3B. Can be an input or an output.
12	S2B	Source Terminal 2B. Can be an input or an output.
13	S1B	Source Terminal 1B. Can be an input or an output.
14	V _{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

Table 7. ADG409 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. R_{ON} as a Function of V_D (V_S): Dual-Supply VoltageFigure 7. R_{ON} as a Function of V_D (V_S): Single-Supply VoltageFigure 5. R_{ON} as a Function of V_D (V_S) for Different TemperaturesFigure 8. R_{ON} as a Function of V_D (V_S) for Different TemperatureFigure 6. Leakage Currents as a Function of V_D (V_S)Figure 9. Leakage Currents as a Function of V_D (V_S)

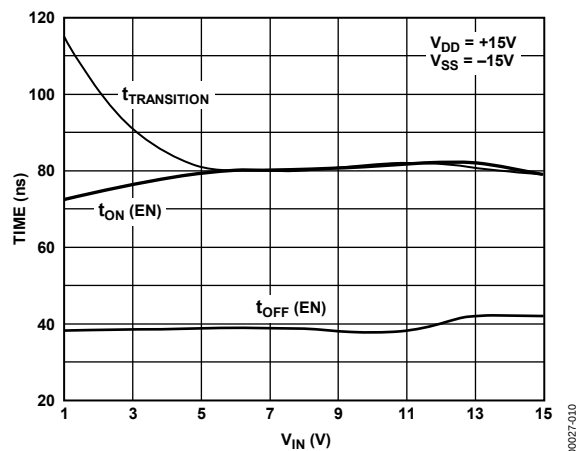
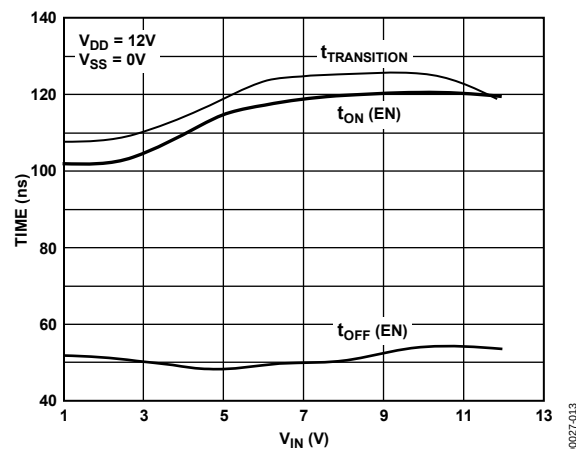
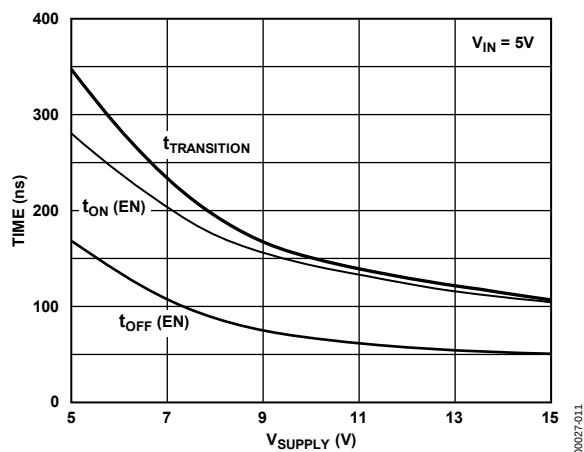
Figure 10. Switching Time vs. V_{IN} (Bipolar Supply)Figure 13. Switching Time vs. V_{IN} (Single Supply)

Figure 11. Switching Time vs. Single Supply

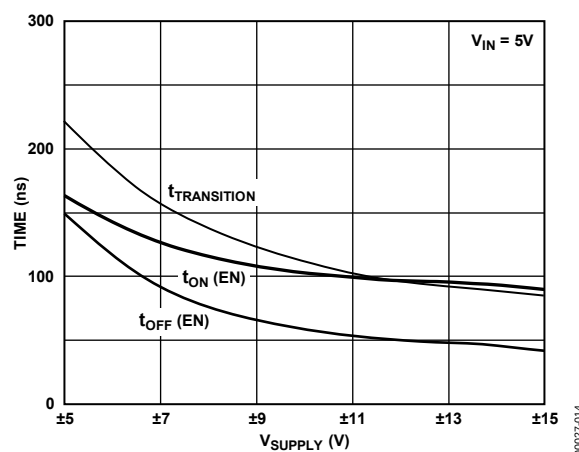


Figure 14. Switching Time vs. Bipolar Supply

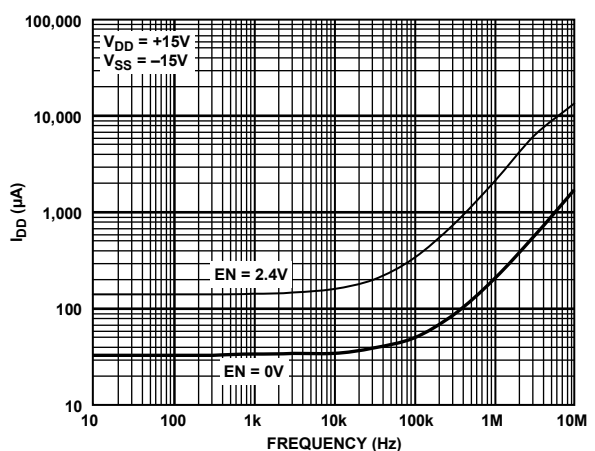


Figure 12. Positive Supply Current vs. Switching Frequency

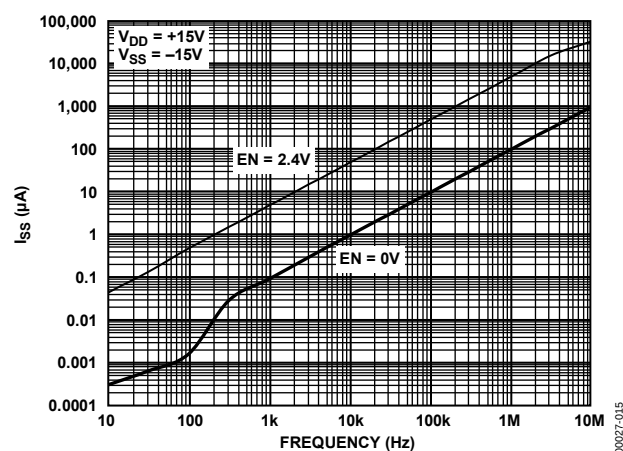


Figure 15. Negative Supply Current vs. Switching Frequency

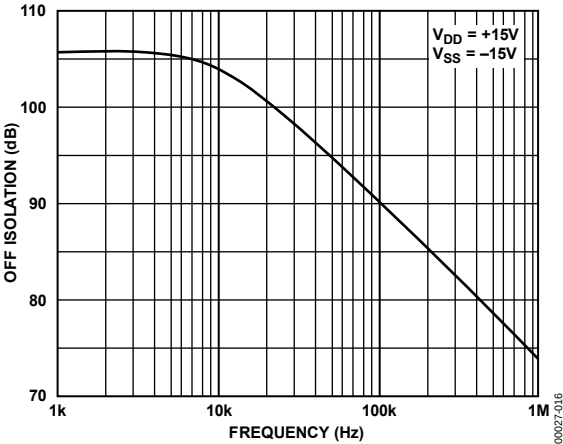


Figure 16. Off Isolation vs. Frequency

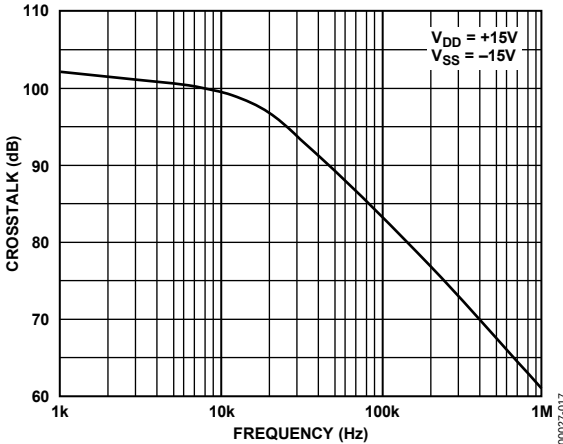


Figure 17. Crosstalk vs. Frequency

TEST CIRCUITS

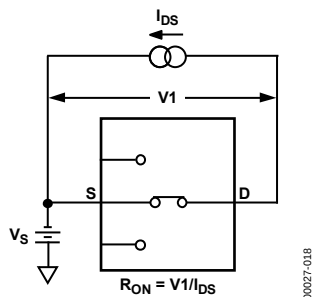
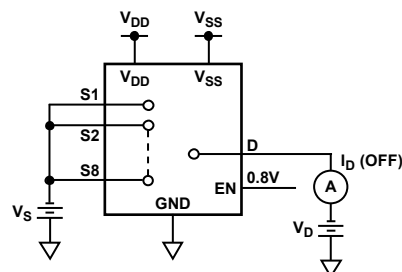
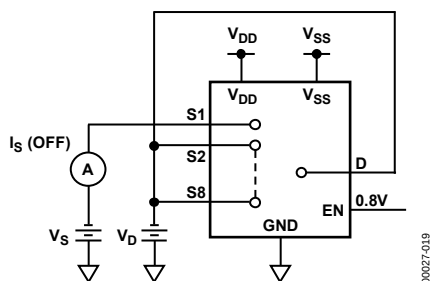
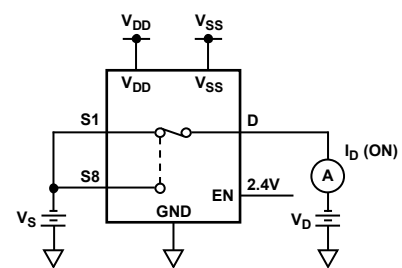
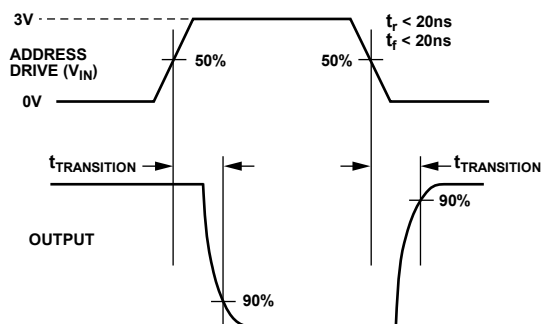
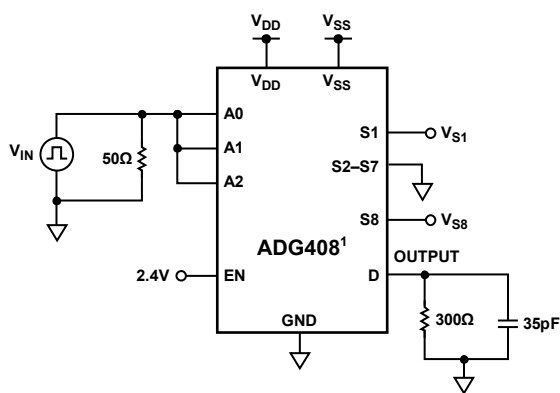
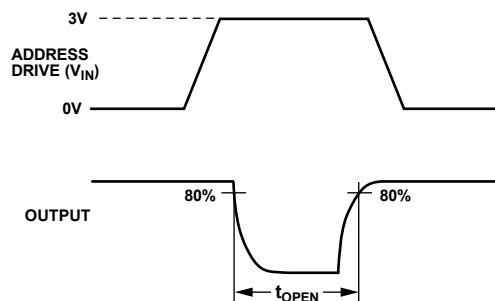
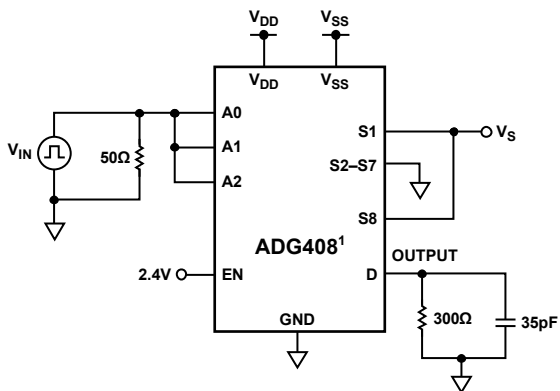
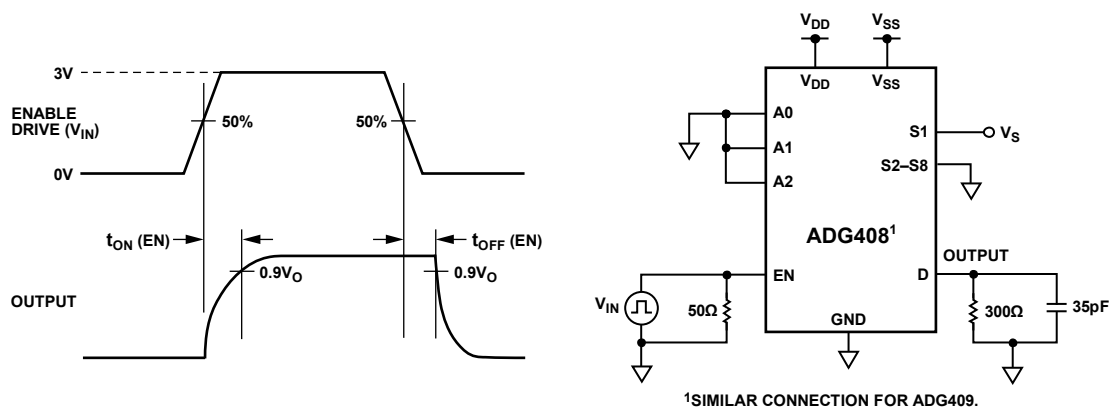
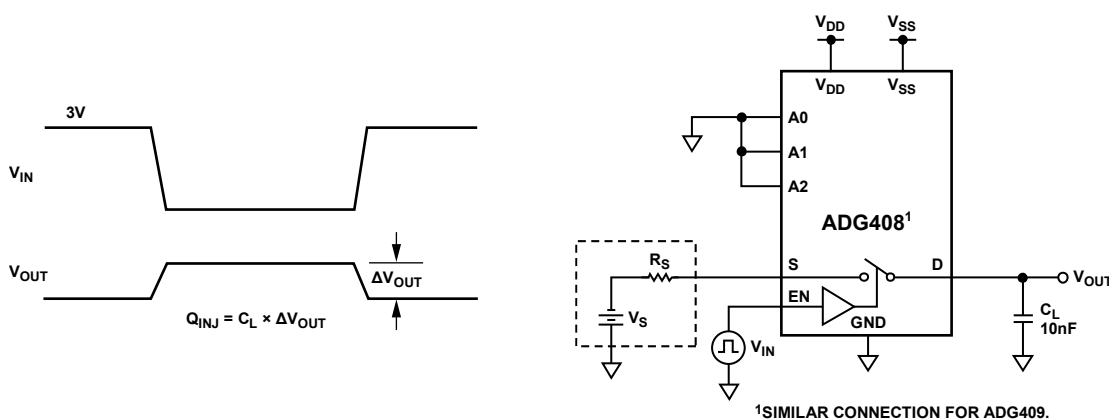


Figure 18. On Resistance

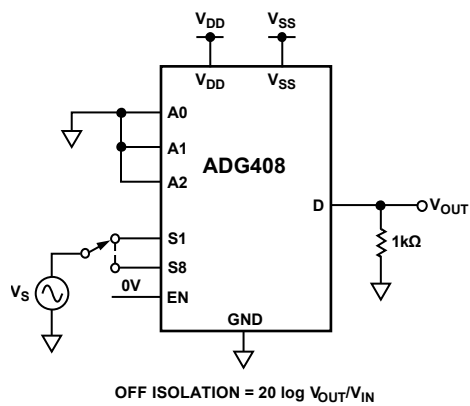
Figure 20. I_D (Off)Figure 19. I_S (Off)Figure 21. I_D (On)Figure 22. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$ ¹SIMILAR CONNECTION FOR ADG409.Figure 23. Break-Before-Make Delay, t_{OPEN} ¹SIMILAR CONNECTION FOR ADG409.



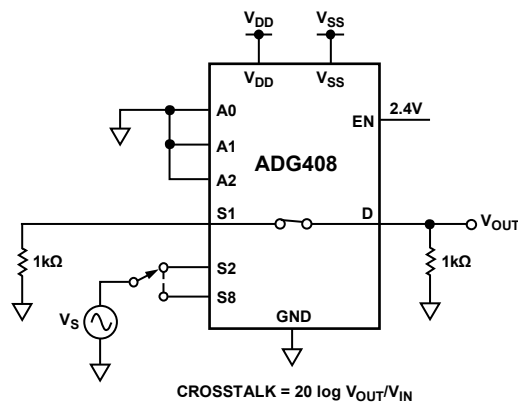
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TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

Difference between the R_{ON} of any two channels.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

C_S (Off)

Channel input capacitance for off condition.

C_D (Off)

Channel output capacitance for off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Technical drawing of a 16-pin connector showing three views: TOP VIEW, SIDE VIEW, and END VIEW. Dimensions are in inches.

TOP VIEW:

- Overall width: 0.775
- Width of pin area: 0.755
- Width of body: 0.735
- Pin pitch (center-to-center): 0.100
- Pin diameter: 0.010
- Pin length (BSC): 0.100
- Body height: 0.280, 0.250, 0.240
- Pin 1 Indicator: Located at the bottom left corner.

SIDE VIEW:

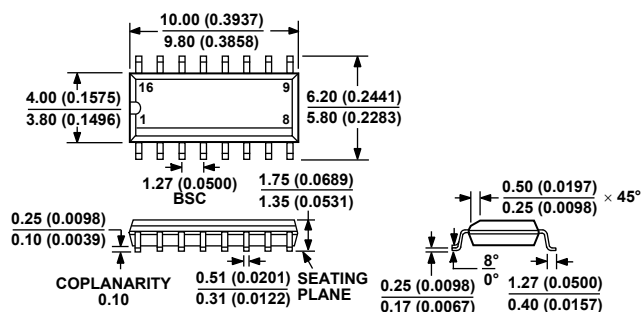
- Overall height: 0.210 MAX
- Height of pin area: 0.150
- Height of body: 0.130
- Height of base: 0.115
- Pin length (MIN): 0.015
- Seating Plane: Indicated by a horizontal line across the pins.
- Pin diameter: 0.022
- Pin pitch (center-to-center): 0.070
- Pin length (BSC): 0.021
- Pin length (MIN): 0.016
- Pin length (MAX): 0.011
- Pin length (MIN): 0.045
- Pin length (MIN): 0.039
- Pin length (MIN): 0.055
- Pin length (MIN): 0.030

END VIEW:

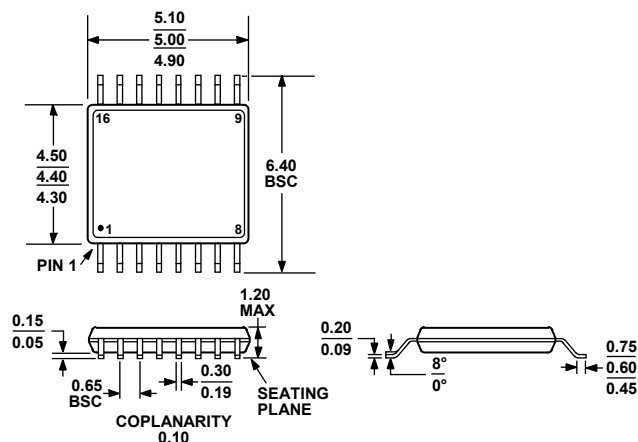
- Overall width: 0.325
- Width of pin area: 0.310
- Width of body: 0.300
- Pin diameter: 0.012
- Pin length (MIN): 0.010
- Pin length (MAX): 0.008
- Gauge Plane: Indicated by a horizontal line across the pins.
- Seating Plane: Indicated by a horizontal line across the pins.
- Pin length (MAX): 0.430

Dimensions shown in inches and (millimeters)

03-07-2014-D



Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG408BN	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG408BNZ	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG408BR	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BR-REEL	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BR-REEL7	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRUZ-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG408BRZ	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BRZ-REEL	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BRZ-REEL7	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG408BCHIPS		DIE	
ADG409BNZ	−40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG409BR	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG409BR-REEL7	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG409BRUZ	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG409BRUZ-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG409BRZ	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG409BRZ-REEL	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16
ADG409BRZ-REEL7	−40°C to +85°C	16-Lead Narrow Body Small Outline Package [SOIC_N]	R-16

¹ Z = RoHS Compliant Part