TABLE OF CONTENTS

REVISION HISTORY

6/2016—Rev. 0 to Rev. A

Changes to Table 7 ... 8
Deleted Table 9; Renumbered Sequentially ... 8
Change to Figure 6 ... 9

10/2009—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	2.1			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 22
	2.4	2.8	3.2	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.2	0.25	0.3	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.4			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.5	0.6	0.65	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 23
	±0.5	±2	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.2			nA typ	V_S = ±10 V, V_S = ±10 V; see Figure 23
	±0.6	±3	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.2			nA typ	V_S = V_D = ±10 V; see Figure 24
	±1	±3	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	155	190	220	ns max	V_S = +10 V; see Figure 25
t_{ON} (EN)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	110	125	140	ns max	V_S = 10 V; see Figure 27
t_{OFF} (EN)	115			ns typ	R_L = 300 Ω, C_L = 35 pF
	140	160	180	ns max	V_S = 10 V; see Figure 27
Break-Before-Make Time Delay, t_D	15			ns typ	R_L = 300 Ω, C_L = 35 pF
			8	ns min	V_{S1} = V_{S2} = 10 V; see Figure 26
Charge Injection	−16			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
Total Harmonic Distortion Plus Noise (THD + N)	0.016			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz; see Figure 32
−3 dB Bandwidth	135			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.16			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	19			pF typ	f = 1 MHz; V_S = 0 V
C_D (Off)	44			pF typ	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	114			pF typ	f = 1 MHz; V_S = 0 V

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}, 8-Lead MSOP	58			μA typ	Digital inputs = 5 V
			95	μA max	
I_{DD}, 8-Lead LFCSP	120			μA typ	Digital inputs = 5 V
			190	μA max	
I_{SS}	0.002			μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	Ground = 0 V

[1] Guaranteed by design, not subject to production test.

+12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 22
	4.6	5.5	6.2	Ω max	V_{DD} = +10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.08			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.25	0.3	0.35	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.5	1.75	1.9	Ω max	
LEAKAGE CURRENTS					V_{DD} = +13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 23
	±0.5	±2	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.2			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 23
	±0.6	±3	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.2			nA typ	V_S = V_D = 1 V or 10 V; see Figure 24
	±1	±3	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	200			ns typ	R_L = 300 Ω, C_L = 35 pF
	255	265	370	ns max	V_S = 8 V; see Figure 25
t_{ON} (EN)	145			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	220	245	ns max	V_S = 8 V; see Figure 27
t_{OFF} (EN)	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	205	220	ns max	V_S = 8 V; see Figure 27
Break-Before-Make Time Delay, t_D	55			ns typ	R_L = 300 Ω, C_L = 35 pF
			33	ns min	V_{S1} = V_{S2} = 8 V; see Figure 26
Charge Injection	13			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
−3 dB Bandwidth	95			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	32			pF typ	f = 1 MHz; V_S = 6 V
C_D (Off)	72			pF typ	f = 1 MHz; V_S = 6 V
C_D, C_S (On)	123			pF typ	f = 1 MHz; V_S = 6 V
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}, 8-Lead MSOP	58			μA typ	Digital inputs = 5 V
			95	μA max	
I_{DD}, 8-Lead LFCSP	120			μA typ	Digital inputs = 5 V
			190	μA max	
V_{DD}			5/16.5	V min/max	Ground = 0 V, V_{SS} = 0 V

[1] Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.5			Ω typ	V_S = ±4.5V, I_S = −10 mA; see Figure 22
	5.2	6.2	7	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±4.5V, I_S = −10 mA
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.3			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.6	1.85	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 23
	±0.5	±2	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 23
	±0.6	±3	±100	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = ±4.5 V; see Figure 24
	±1	±3	±100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	310			ns typ	R_L = 300 Ω, C_L = 35 pF
	410	495	560	ns max	V_S = 3 V; see Figure 25
t_{ON} (EN)	230			ns typ	R_L = 300 Ω, C_L = 35 pF
	305	355	390	ns max	V_S = 3 V; see Figure 27
t_{OFF} (EN)	220			ns typ	R_L = 300 Ω, C_L = 35 pF
	290	335	365	ns max	V_S = 3 V; see Figure 27
Break-Before-Make Time Delay, t_D	65			ns typ	R_L = 300 Ω, C_L = 35 pF
			31	ns min	V_{S1} = V_{S2} = 3 V; see Figure 26
Charge Injection	59			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
Total Harmonic Distortion Plus Noise	0.04			% typ	R_L = 10 kΩ, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 32
−3 dB Bandwidth	105			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.28			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	26			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	62			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	128			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	Ground = 0 V

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL[1]					
±15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
8-Lead MSOP (θ_{JA} = 206°C/W)	215	135	80	mA maximum	
8-Lead LFCSP (θ_{JA} = 50.8°C/W)	390	215	100	mA maximum	
+12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
8-Lead MSOP (θ_{JA} = 206°C/W)	175	115	70	mA maximum	
8-Lead LFCSP (θ_{JA} = 50.8°C/W)	320	185	95	mA maximum	
±5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
8-Lead MSOP (θ_{JA} = 206°C/W)	165	110	70	mA maximum	
8-Lead LFCSP (θ_{JA} = 50.8°C/W)	310	180	95	mA maximum	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	
8-Lead MSOP (4-Layer Board)	400 mA
8-Lead LFCSP	600 mA
Continuous Current per Channel, S or D	Data in Table 4 + 15% mA
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

[1] Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

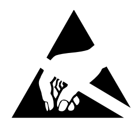
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (4-Layer Board)	206	44	°C/W
8-Lead LFCSP	50.8		°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

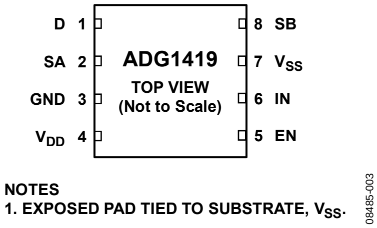


Figure 3. 8-Lead LFCSP Pin Configuration

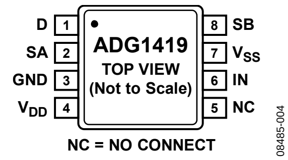


Figure 4. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
LFCSP	**MSOP**	**Mnemonic**	**Description**
1	1	D	Drain Terminal. This pin can be an input or output.
2	2	SA	Source Terminal. This pin can be an input or output.
3	3	GND	Ground (0 V) Reference.
4	4	V_{DD}	Most Positive Power Supply Potential.
5	Not applicable	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the IN logic input determines which switch is turned on.
Not applicable	5	NC	No Connect.
6	6	IN	Logic Control Input.
7	7	V_{SS}	Most Negative Power Supply Potential.
8	8	SB	Source Terminal. This pin can be an input or output.
0	Not applicable	EPAD	Exposed Pad. Exposed pad tied to substrate, V_{SS}.

Table 8. 8-Lead LFCSP Truth Table

EN	IN	Switch A	Switch B
0	X	Off	Off
1	0	On	Off
1	1	Off	On

Table 9. 8-Lead MSOP Truth Table

IN	Switch A	Switch B
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

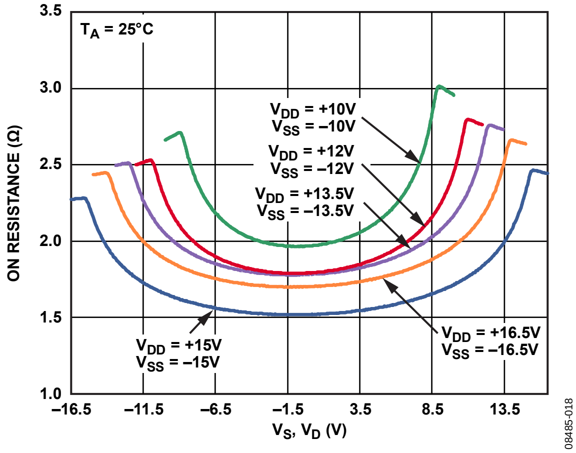


Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

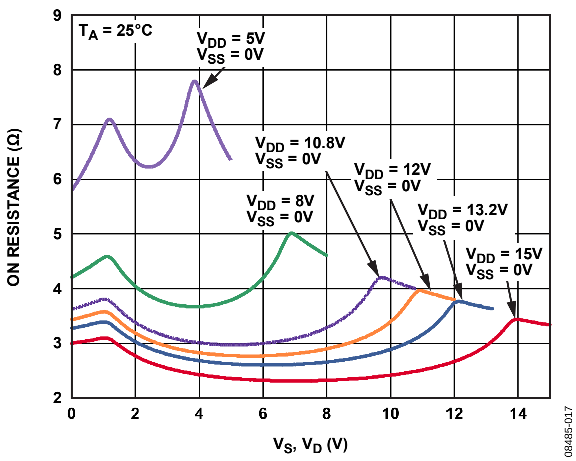


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

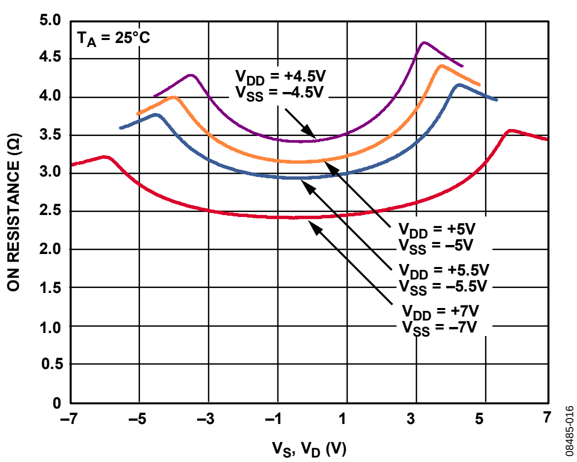


Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

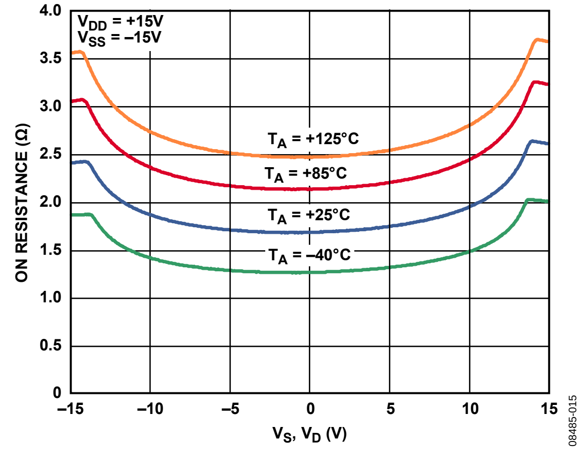


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, ±15 V Dual Supply

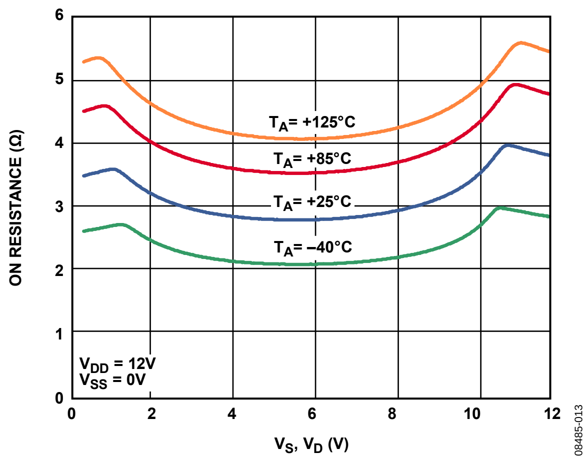


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, +12 V Single Supply

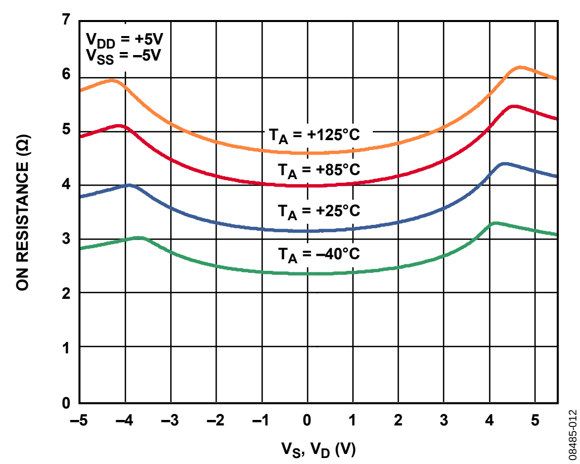


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, ±5 V Dual Supply

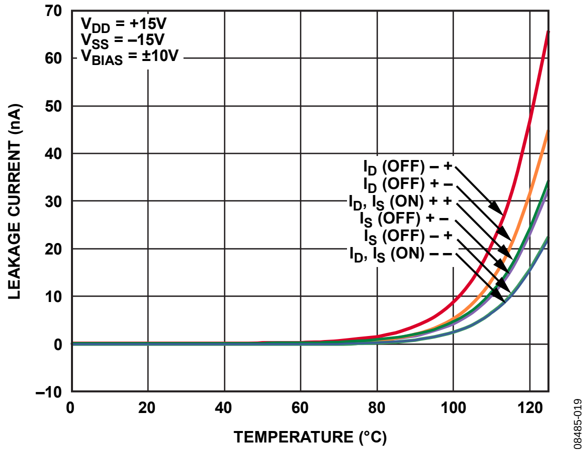


Figure 11. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

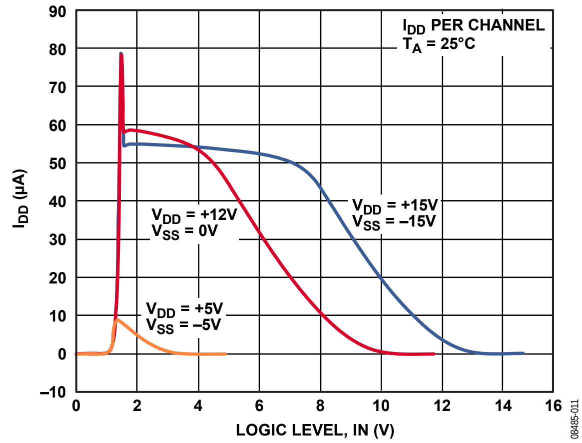


Figure 14. I_{DD} vs. Logic Level

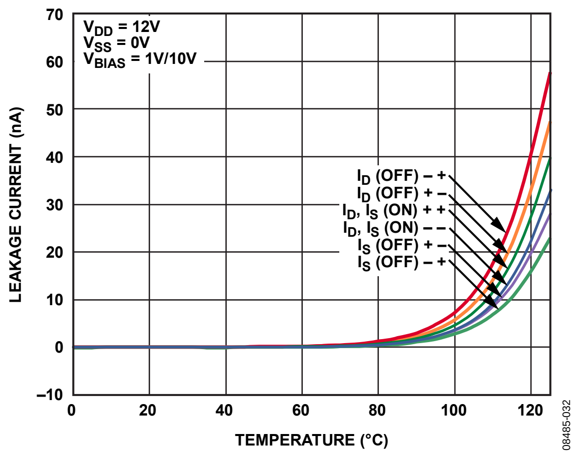


Figure 12. Leakage Currents as a Function of Temperature, +12 V Single Supply

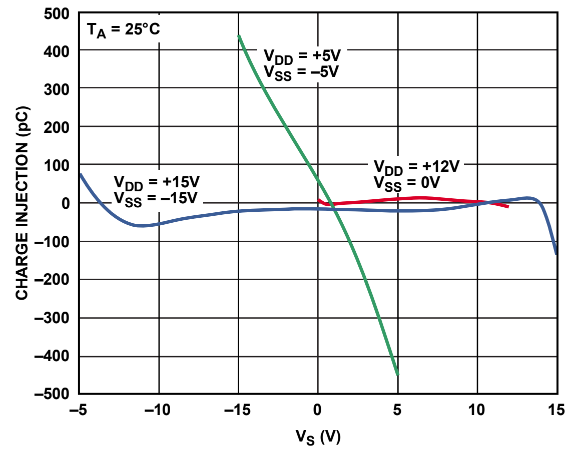


Figure 15. Charge Injection vs. Source Voltage

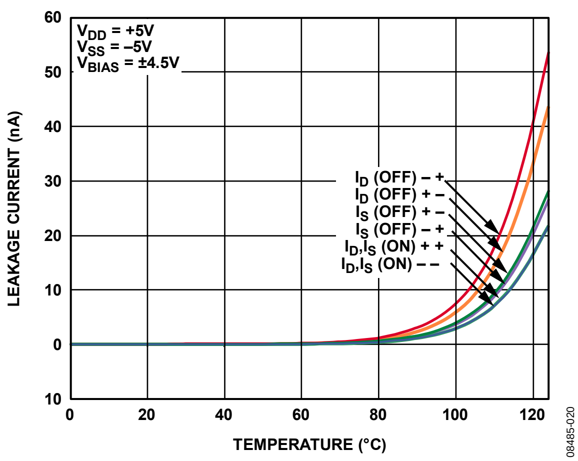


Figure 13. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

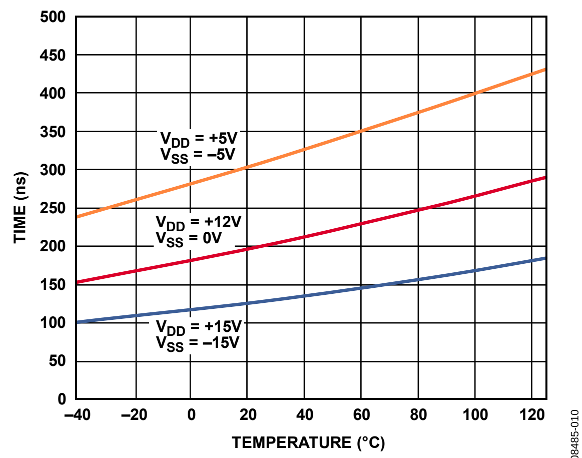


Figure 16. $t_{TRANSITION}$ Times vs. Temperature

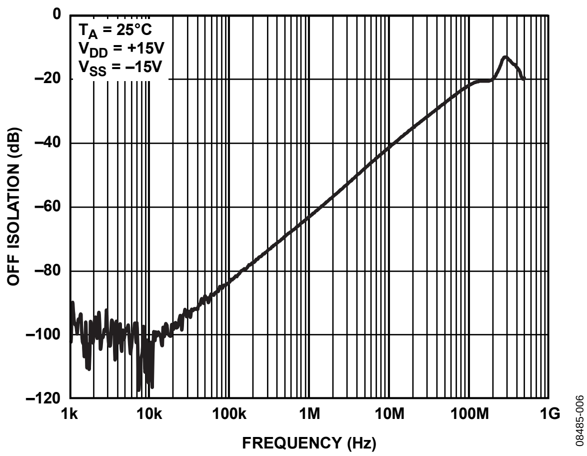


Figure 17. Off Isolation vs. Frequency

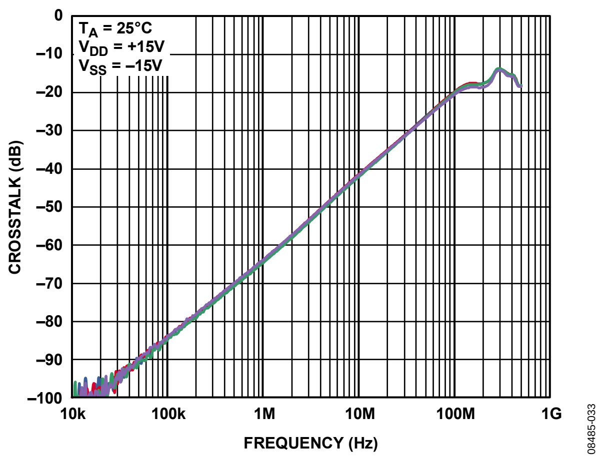


Figure 18. Crosstalk vs. Frequency

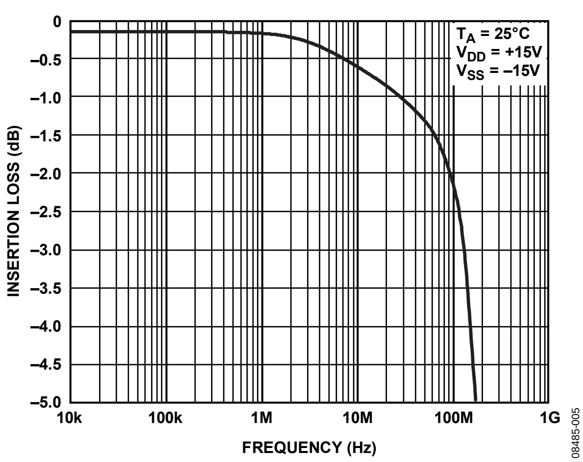


Figure 19. On Response vs. Frequency

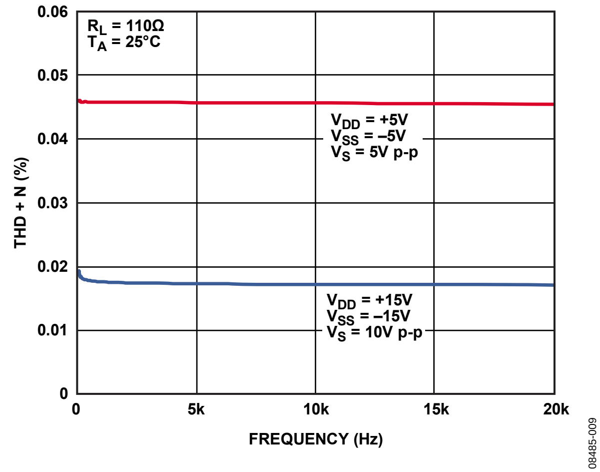


Figure 20. THD + N vs. Frequency

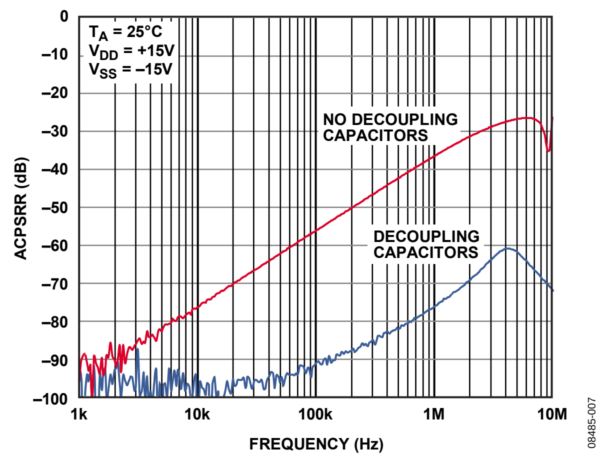


Figure 21. ACPSRR vs. Frequency

TEST CIRCUITS

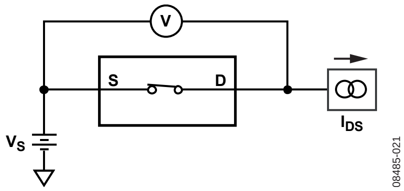


Figure 22. On Resistance

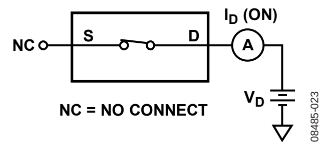


Figure 24. On Leakage

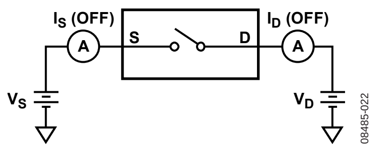


Figure 23. Off Leakage

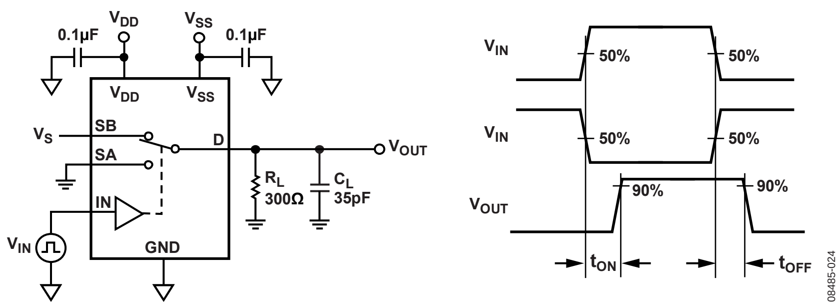


Figure 25. Switching Times, t_{ON} and t_{OFF}

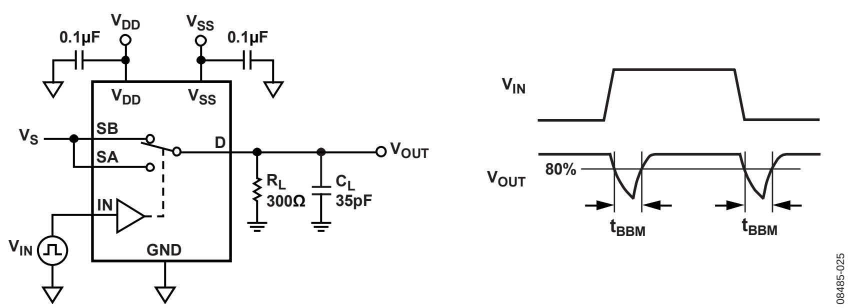


Figure 26. Break-Before-Make Time Delay

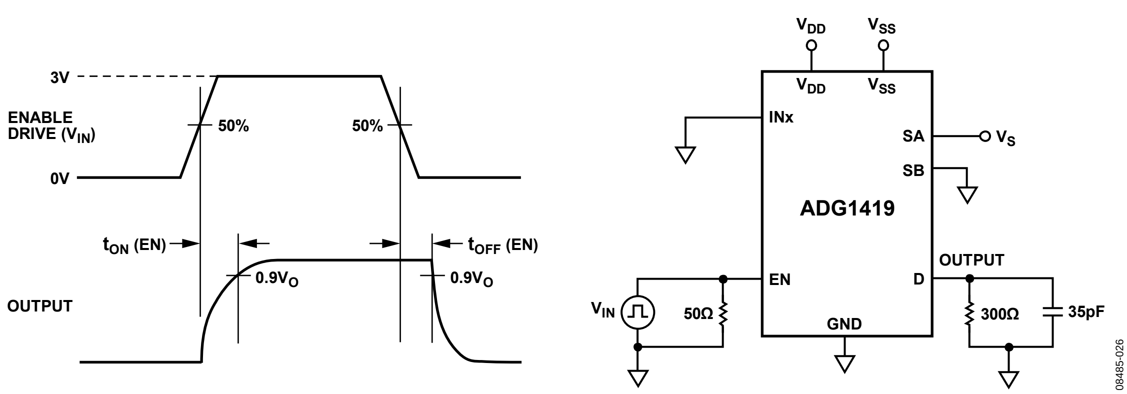


Figure 27. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

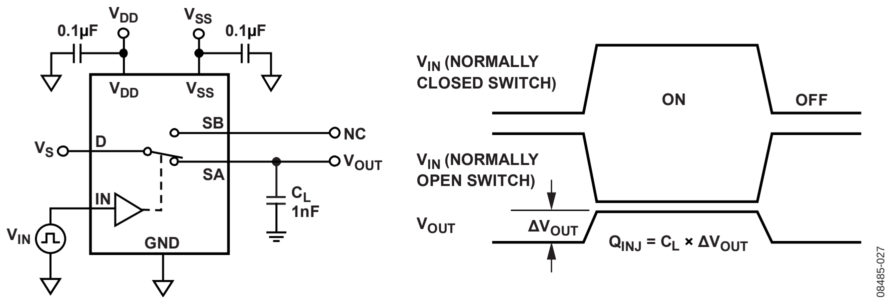


Figure 28. Charge Injection

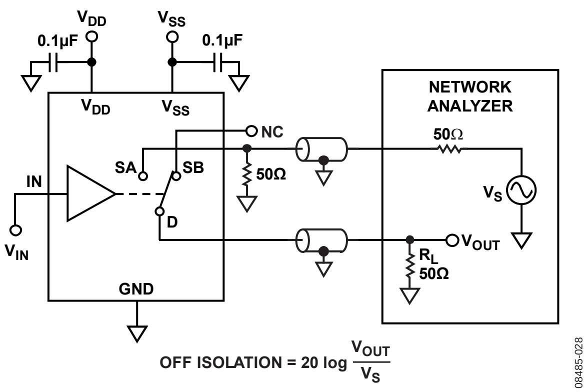


Figure 29. Off Isolation

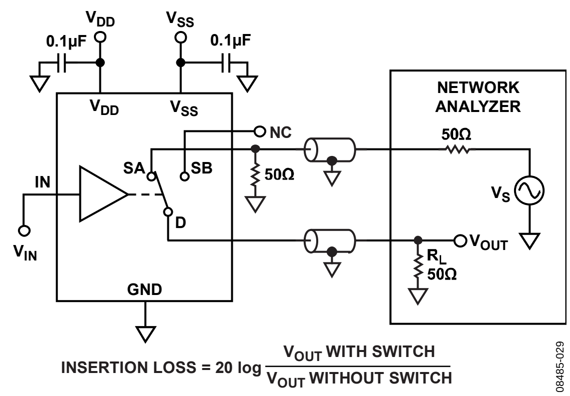


Figure 31. Bandwidth

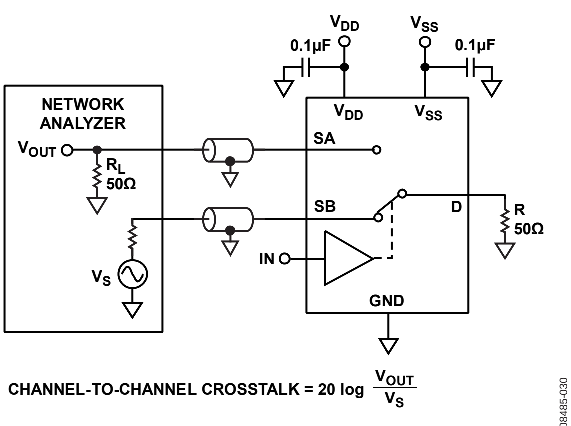


Figure 30. Channel-to-Channel Crosstalk

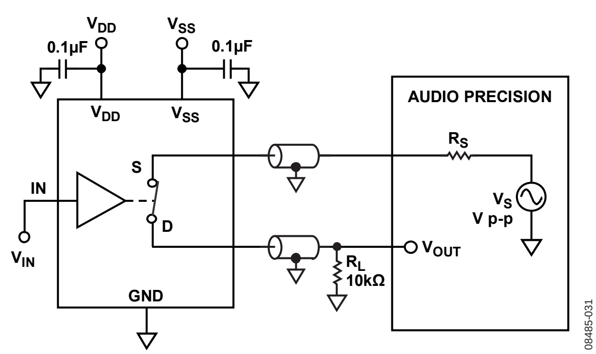


Figure 32. THD + N

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 27.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 27.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another. See Figure 26.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 28.

Off Isolation
A measure of unwanted signal coupling through an off switch. See Figure 29.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 30.

Bandwidth
The frequency at which the output is attenuated by 3 dB. See Figure 31.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch. See Figure 31.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 32.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 21.

OUTLINE DIMENSIONS

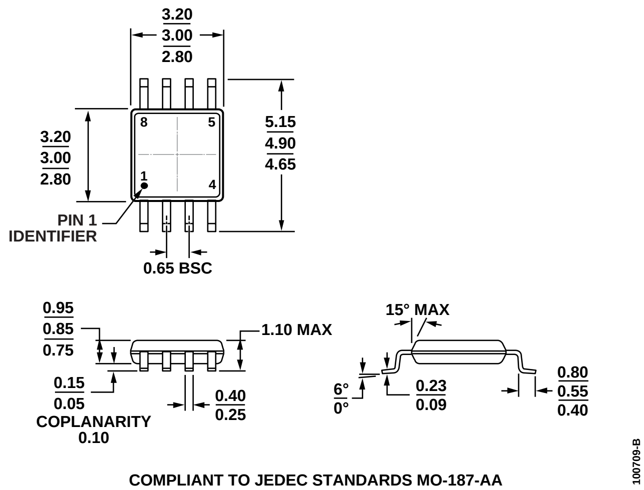


Figure 33. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

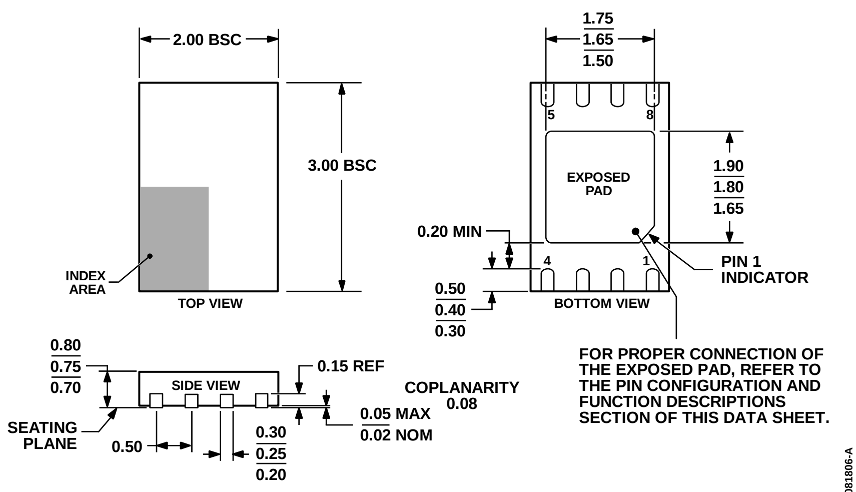


Figure 34. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 2 mm Body, Very Very Thin, Dual Lead
(CP-8-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG1419BRMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1L
ADG1419BRMZ-REEL7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1L
ADG1419BCPZ-REEL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-4	1C

[1] Z = RoHS Compliant Part.

NOTES