TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Revision History ... 3
Functional Block Diagrams ... 5
Specifications ... 9
  Timing Characteristics ... 12
Absolute Maximum Ratings ... 15
  Thermal Resistance ... 15
  ESD Caution ... 15
Pin Configuration and Function Descriptions ... 16
Typical Performance Characteristics ... 18
Test Circuit ... 21
Terminology ... 22
Power Management ... 23
  PSM0—Normal Power Mode (All Parts) ... 23
  PSM1—Reduced Power Mode (ADE7868, ADE7878 Only) 23
  PSM2—Low Power Mode (ADE7868, ADE7878 Only) ... 23
  PSM3—Sleep Mode (All Parts) ... 24
  Power-Up Procedure ... 26
  Hardware Reset ... 27
  Software Reset Functionality ... 27
Theory of Operation ... 28
  Analog Inputs ... 28
  Analog-to-Digital Conversion ... 28
  Current Channel ADC ... 29
  di/dt Current Sensor and Digital Integrator ... 31
  Voltage Channel ADC ... 32
  Changing Phase Voltage Datapath ... 33
  Power Quality Measurements ... 34
  Phase Compensation ... 39
  Reference Circuit ... 41
  Digital Signal Processor ... 42
  Root Mean Square Measurement ... 43
  Active Power Calculation ... 47
  Reactive Power Calculation—ADE7858, ADE7868, ADE7878 Only ... 52
  Apparent Power Calculation ... 57
  Waveform Sampling Mode ... 60
  Energy-to-Frequency Conversion ... 60
  No Load Condition ... 64
  Checksum Register ... 65
  Interrupts ... 66
  Serial Interfaces ... 68
  Quick Setup as Energy Meter ... 75
  Layout Guidelines ... 75
  Crystal Circuit ... 76
  ADE7878 Evaluation Board ... 76
  Die Version ... 76
Silicon Anomaly ... 77
  ADE7854/ADE7858/ADE7868/ADE7878 Functionality Issues ... 77
  Functionality Issues ... 77
  Section 1. ADE7854/ADE7858/ADE7868/ADE7878 Functionality Issues ... 79
Registers List ... 80
Outline Dimensions ... 98
  Ordering Guide ... 98

Downloaded from Arrow.com.

REVISION HISTORY

4/14—Rev. G to Rev. H

Changes to Power-Up Procedure Section 26
Changes to Crystal Circuit Section 76

10/13—Rev. F to Rev. G

Changes to Product Title and Features Section 1
Changes to Table 2 9
Deleted Junction Temperature; Table 6 15
Changes to NC and CLKIN Pin Descriptions 16
Replaced Typical Performance Characteristics Section 18
Added Text to Test Circuit Section 21
Changes to Terminology Section 22
Changes to PSM2—Low Power Mode (ADE7868, ADE7878 Only) Section and Added Figure 25 24
Changes to Changing Phase Voltage Datapath Section and Figure 42 33
Changes to Reference Circuit Section; Added Figure 56, Figure 57, and Figure 58; Renumbered Sequentially 41
Changes to Current RMS Compensation Section 44
Changes to Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only and Figure 60 45
Changes to Voltage RMS Offset Compensation Section 47
Changes to Line Cycle Active Energy Accumulation Mode Section 51
Changes to Quick Setup as Energy Meter Section and Figure 95 75
Changes to Figure 96 and Figure 97; Added Crystal Circuit Section 76
Changes to Address 0xE520 Description; Table 33 84
Changes to Bit 11, Bit 12, Bit 13 Descriptions; Table 43 91
Updated Outline Dimensions 99

10/12—Rev. E to Rev. F

Changes to Figure 1 4
Changes to Figure 2 5
Changes to Figure 3 6
Changes to Figure 4 7
Changes to Table 2 8
Changes to Figure 5 11
Added Text under Table 6 14
Changes to Figure 9 and to Table 8 15
Changes to Power-Up Procedure Section 24
Changes to Figure 31 and Figure 32 28
Changes to Figure 39 30
Changes to Voltage Waveform Gain Register Section 31
Changes to Figure 41 32
Changes to Phase Compensation Section 37
Changes to Digital Signal Processor Section 39
Changes to Equation 12 40
Changes to Current RMS Offset Compensation Section 42
Changes to Voltage Channel RMS Calculation Section 43
Changes to Voltage RMS Offset Compensation Section and to Figure 59 44
Changes to Equation 20 and to Equation 21 45
Changes to Active Energy Calculation Section 46
Changes to Figure 62 and to following text and to Equation 25 47
Changes to Equation 32, Equation 34, and to Reactive Power Gain Calibration Section 50
Changes to Reactive Energy Calculation Section 51
Changes to Figure 66 52
Changes to Energy Accumulation Modes Sections and to Caption for Figure 67 53
Changes to Equation 40 54
Changes to Apparent Power Calculation Using VNOM Section 55
Changes to CF Outputs for Various Accumultation Modes Section 60
Changes to Sign of Sum-of-Phase Powers in the CFx Datapath Section and to Equation 47 61
Changes to Equation 48 62
Changes to Checksum Register Section and to Table 23 63
Changes to Figure 81 66
Changes to Figure 82 67
Changes to SPI-Compatible Interface Section 68
Changes to HSDC Interface Section 70
Changes to Figure 88 71
Changes to Figure 89, added Quick Setup as Energy Meter Section, added Layout Guidelines, and added Figure 90; Renumbered Sequentially 72
Added Figure 91 and Figure 92 73
Changes to Table 30 78
Changes to Table 33 79
Changes to Table 46 90

4/11—Rev. D to Rev. E

Changes to Input Clock FrequencyParameter, Table 2 10
Changes to Current RMS Offset Compensation Section 42
Changes to Voltage RMS Offset Compensation Section 44
Changes to Note 2, Table 30 77
Changes to Address 0xE707, Table 33 80
Changes to Table 45 87
Changes to Table 46 88
Changes to Bit Location 7:3, Default Value, Table 54 92

2/11—Rev. C to Rev. D

Changes to Figure 1 4
Changes to Figure 2 5
Changes to Figure 3 6
Changes to Figure 4 7
Changes to Table 2 8
Changed SCLK Edge to HSCLK Edge, Table 5 13
Change to Current Channel HPF Section 28
Change to di/dt Current Sensor and Digital Integrator Section 30
Changes to Digital Signal Processor Section 39
Changes to Figure 59 44
Changes to Figure 62 47
Changes to Figure 65 49
Changes to Figure 66 52

Downloaded from Arrow.com.

Changes to Line Cycle Reactive Energy Accumulation Mode Section and to Figure 67 53
No Load Detection Based On Total Active, Reactive Powers Section 61
Change to Equation 50 63
Changes to the HSDC Interface Section 70
Changes to Figure 87 and Figure 88 71
Changes to Figure 89 72
Changes to Table 30 77
Changes to Table 46 88

11/10—Rev. B to Rev. C

Change to Signal-to-Noise-and-Distortion Ratio, SINAD Parameter, Table 1 9
Changes to Figure 18 18
Changes to Figure 22 19
Changes to Silicon Anomaly Section 72
Added Table 28 to Silicon Anomaly Section 73

8/10—Rev. A to Rev. B

Changes to Figure 1 4
Changes to Figure 2 5
Changes to Figure 3 6
Changes to Figure 4 7
Change to Table 8 16
Changes to Power-Up Procedure Section 23
Changes to Equation 6 and Equation 7 33
Changes to Equation 17 43
Changes to Active Power Offset Calibration Section 45
Changes to Figure 63 46
Changes to Reactive Power Offset Calibration Section 49
Changes to Figure 82 65
Added Silicon Anomaly Section, Renumbered Tables Sequentially 71

3/10—Rev. 0 to Rev. A

Added ADE7854, ADE7858, and ADE7878 ..... Universal
Reorganized Layout ..... Universal
Added Table 1, Renumbered Sequentially 1
Added Figure 1, Renumbered Sequentially 3
Added Figure 2 4
Added Figure 3 5
Changes to Specifications Section 7
Changes to Figure 9 and changes to Table 8 14
Changes to Typical Performance Characteristics Section 16
Changes to Figure 22 18
Changes to the Power Management Section 20
Changes to the Theory of Operation Section 25
Changes to Figure 31 and Figure 32 27
Change to Equation 28 47
Changes to Figure 83 66
Changes to Figure 86 68
Changes to the Registers List Section 72
Changes to Ordering Guide 91

2/10—Revision 0: Initial Version

Downloaded from Arrow.com.

FUNCTIONAL BLOCK DIAGRAMS

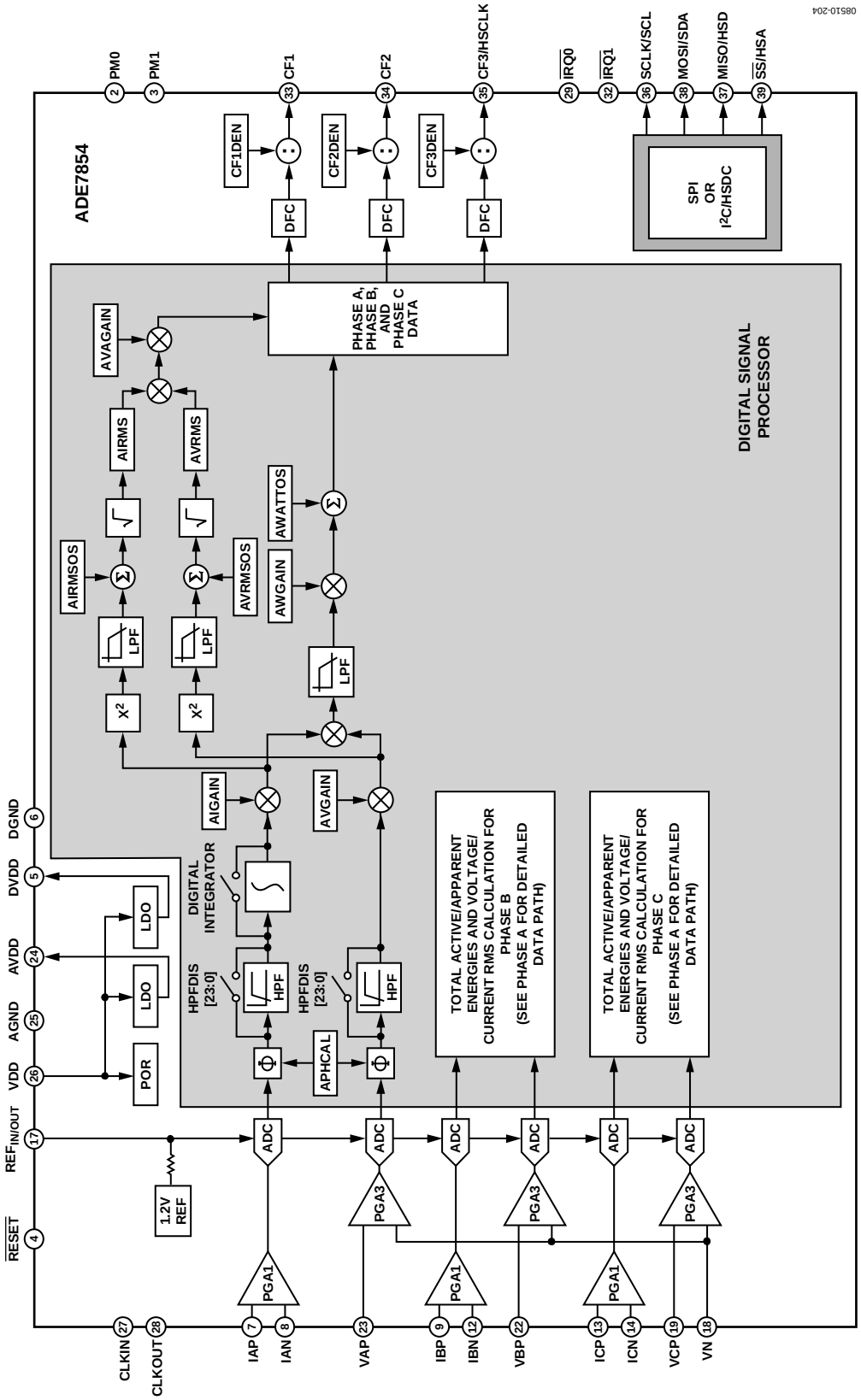

Figure 1. ADE7854 Functional Block Diagram

Downloaded from Arrow.com.

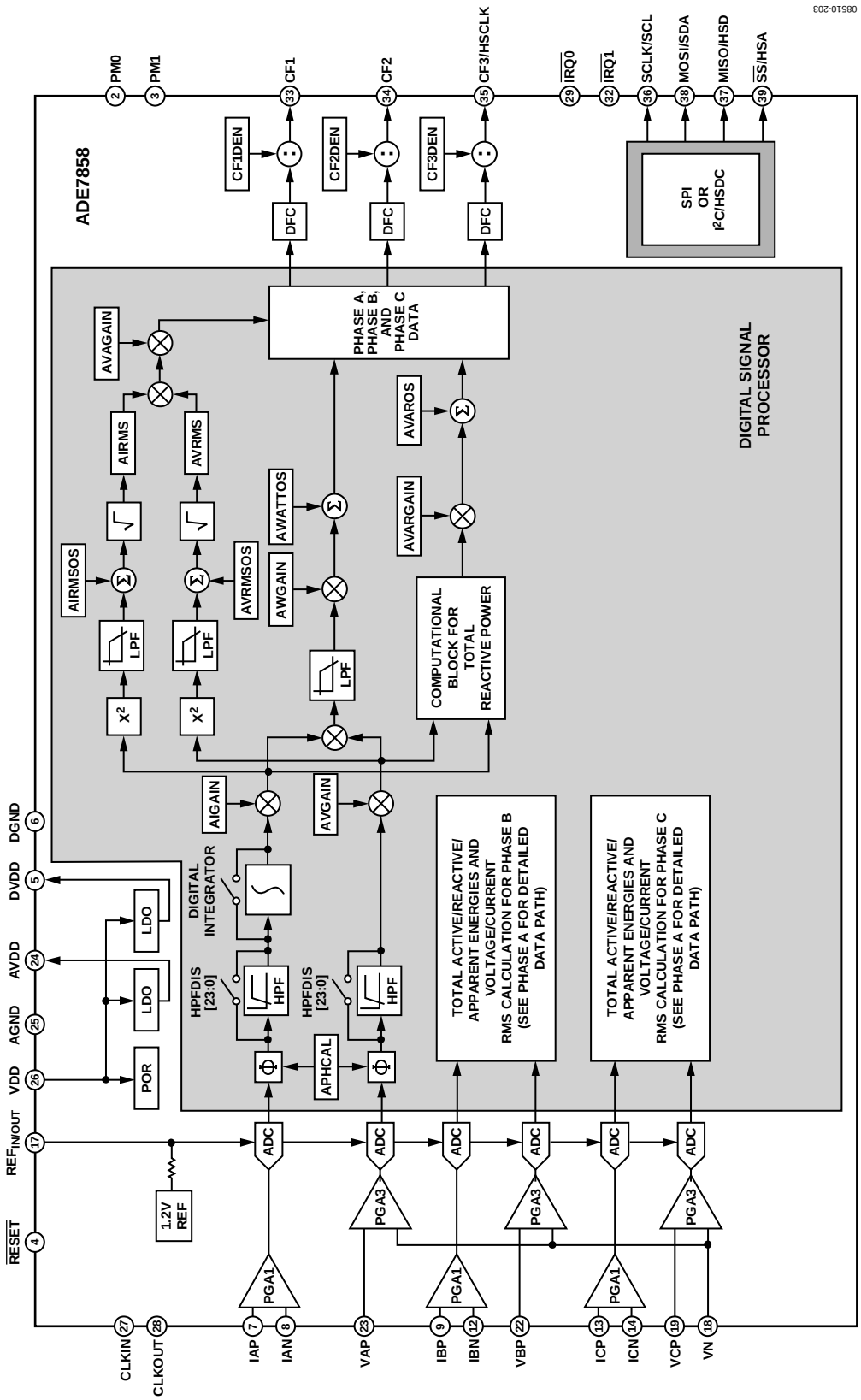

Figure 2. ADE7858 Functional Block Diagram

Downloaded from Arrow.com.

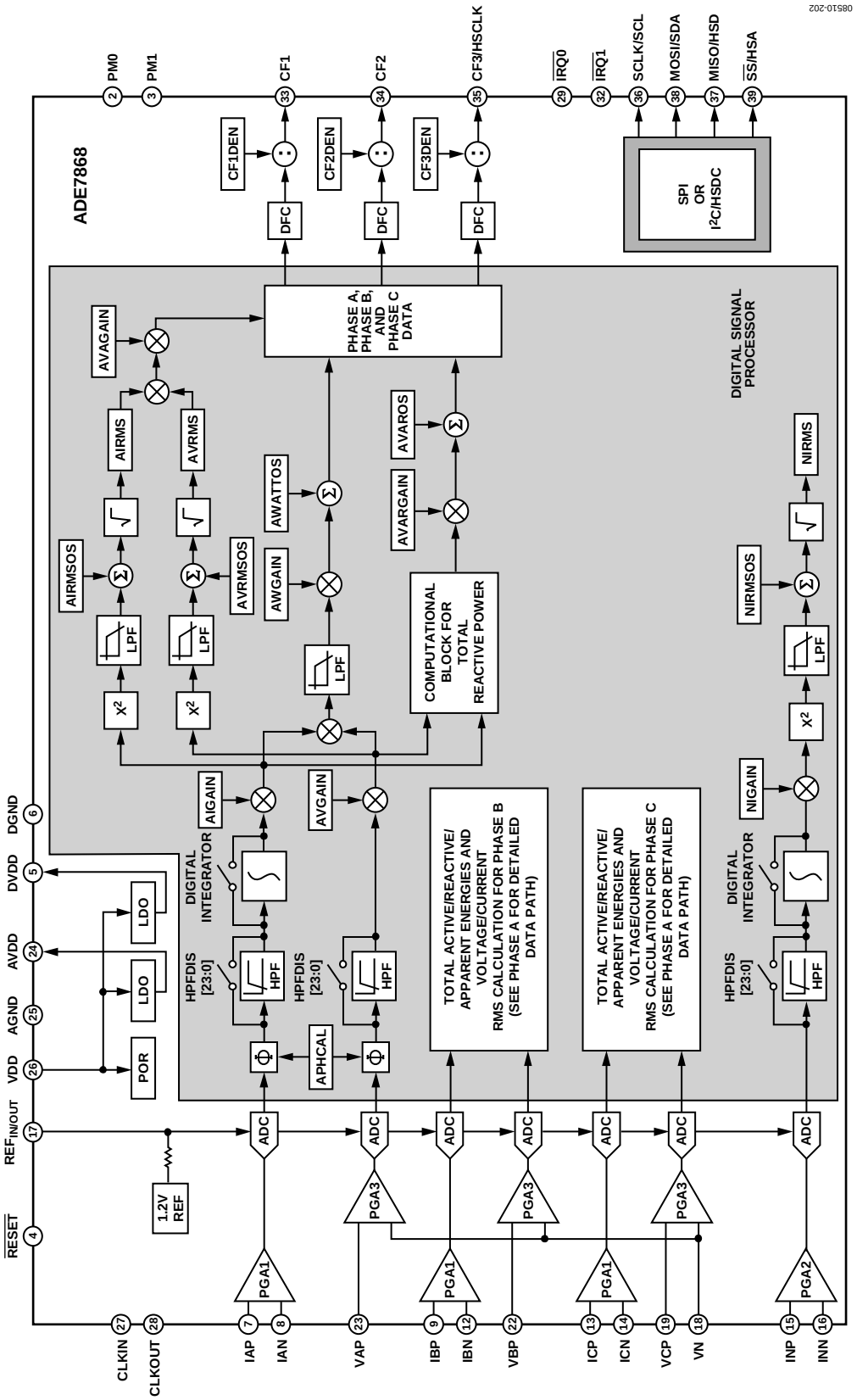

Figure 3. ADE7868 Functional Block Diagram

Downloaded from Arrow.com.

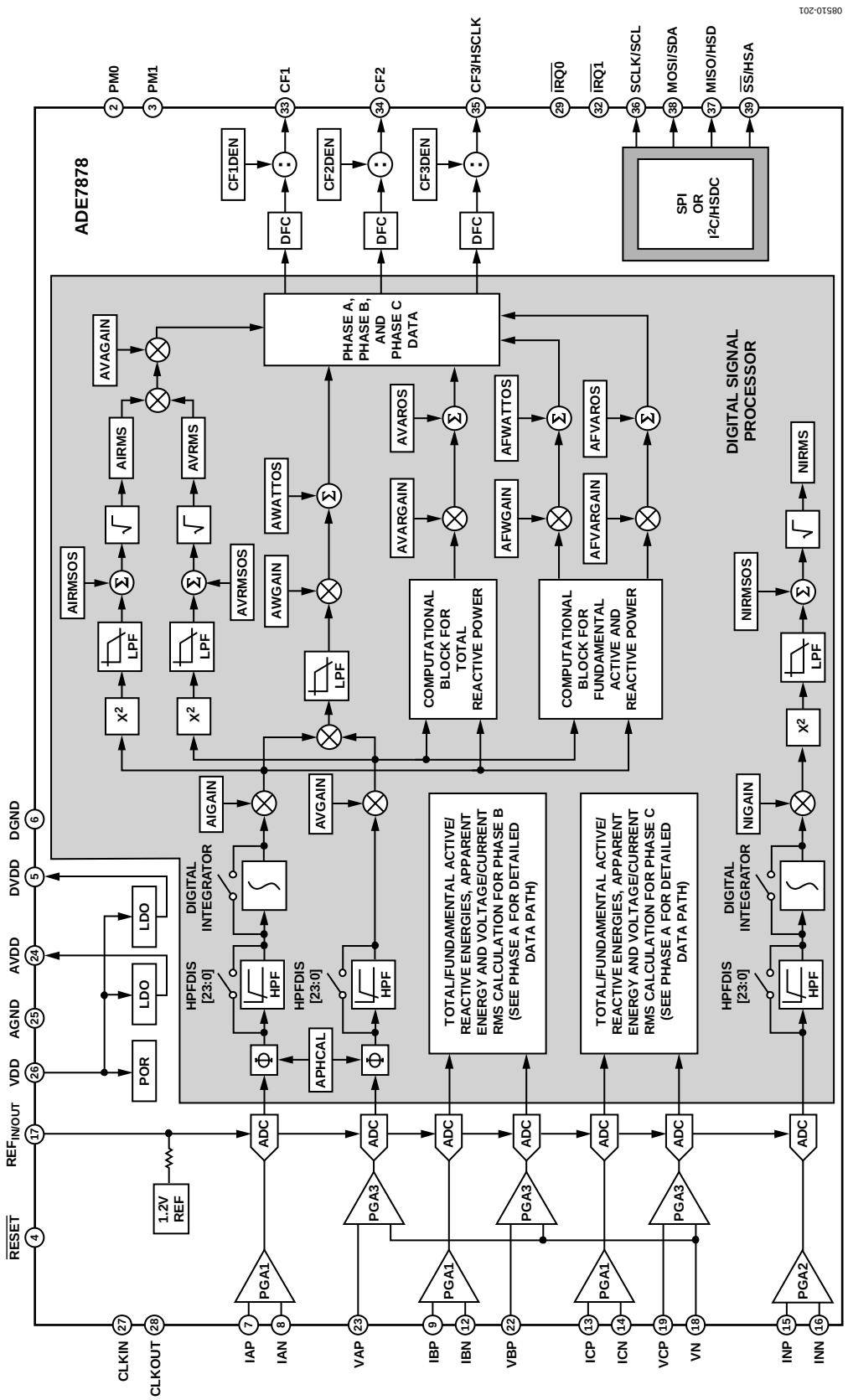

Figure 4. ADE7878 Functional Block Diagram

Downloaded from Arrow.com.

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP}= 25°C.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Active Energy Measurement					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Active Energy (ADE7878 Only)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		2		kHz	
REACTIVE ENERGY MEASUREMENT (ADE7858, ADE7868, AND ADE7878)					
Reactive Energy Measurement Error (per Phase)					
Total Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Reactive Energy (ADE7878 Only)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS					
I rms and V rms Measurement Bandwidth		2		kHz	
I rms and V rms Measurement Error (PSM0 Mode)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1

Downloaded from Arrow.com.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (ADE7868 AND ADE7878)					
I mav Measurement Bandwidth (PSM1 Mode)		260		Hz	
I mav Measurement Error (PSM1 Mode)		0.5		%	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	PGA = 1, differential inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP, and VN
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins	400			kΩ	
VN Pin	130			kΩ	
ADC Offset		−24		mV	PGA = 1, uncalibrated error, see the Terminology section
Gain Error		±4		%	External 1.2 V reference
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		74		dB	PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section
Signal-to-Noise-and-Distortion Ratio, SINAD		74		dB	PGA = 1; fundamental frequency: 45 Hz to 65 Hz, see the Terminology section
Bandwidth (−3 dB)		2		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		8		kHz	WTHR = VARTHR = VATHR = PMAX = 33,516,139
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1
		(1 + 1/CFDEN) × 50%			If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.2 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
PSM0 and PSM1 Modes					
Temperature Coefficient	−50	±5	+50	ppm/°C	Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details
CLKIN					All specifications CLKIN of 16.384 MHz. See the Crystal Circuit section for more details.
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, $\overline{RESET}$, PM0, AND PM1					
Input High Voltage, V_{INH}	2.0			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			−8.7	µA	Input = 0 V, VDD = 3.3 V
			3	µA	Input = VDD = 3.3 V
Input Capacitance, C_{IN}		10		pF	

Downloaded from Arrow.com.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			800	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			2	mA	
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			2	mA	
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		24.4	27.2	mA	
PSM1 and PSM2 Modes (ADE7868 and ADE7878)					
VDD Pin	2.4		3.7	V	
I_{DD}					
PSM1 Mode		6.0		mA	
PSM2 Mode		0.2		mA	
PSM3 Mode					
VDD Pin	2.4		3.7	V	
I_{DD} in PSM3 Mode		1.7		µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.

Downloaded from Arrow.com.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams; see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions.

Table 3. I²C-Compatible Interface Timing Parameter

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

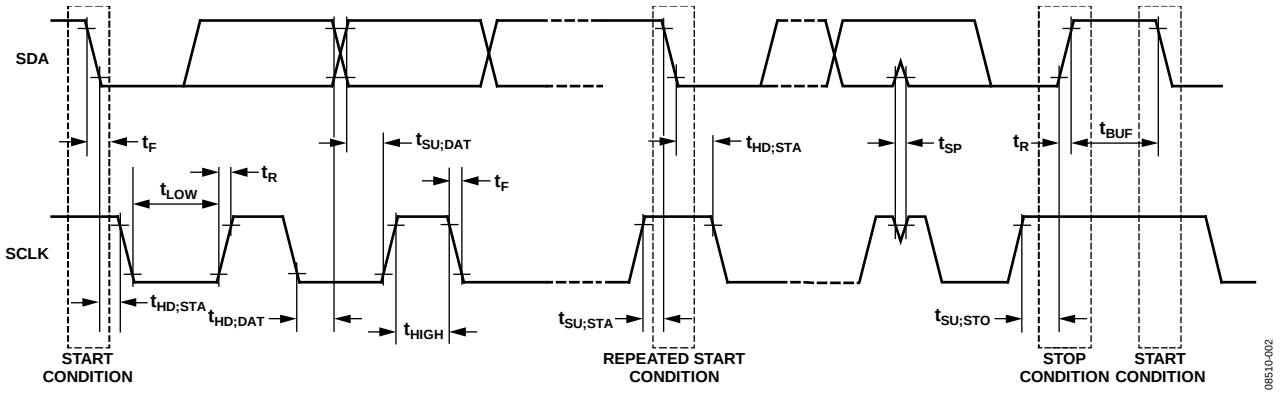

Figure 5. I²C-Compatible Interface Timing

Downloaded from Arrow.com.

Table 4. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

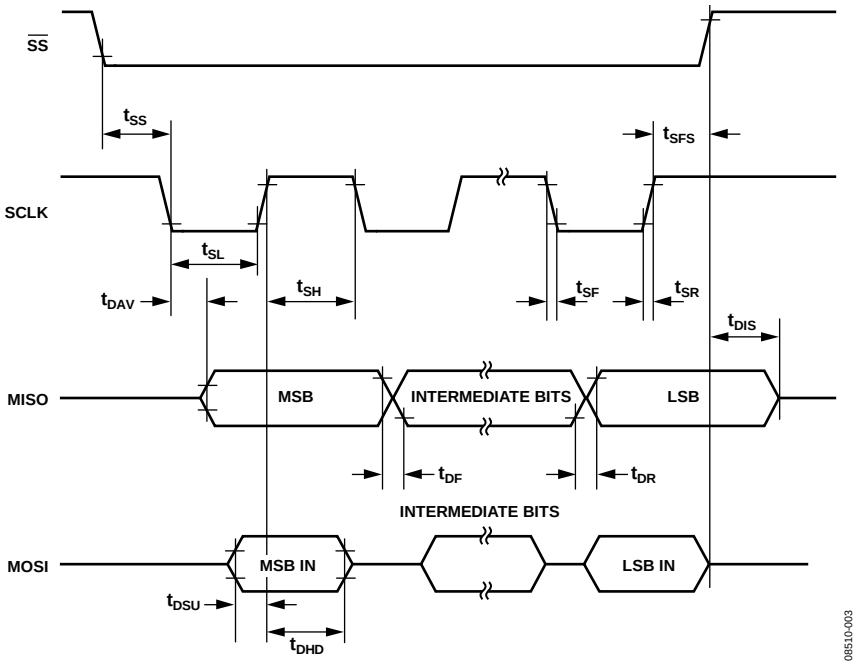

Figure 6. SPI Interface Timing

Downloaded from Arrow.com.

Table 5. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

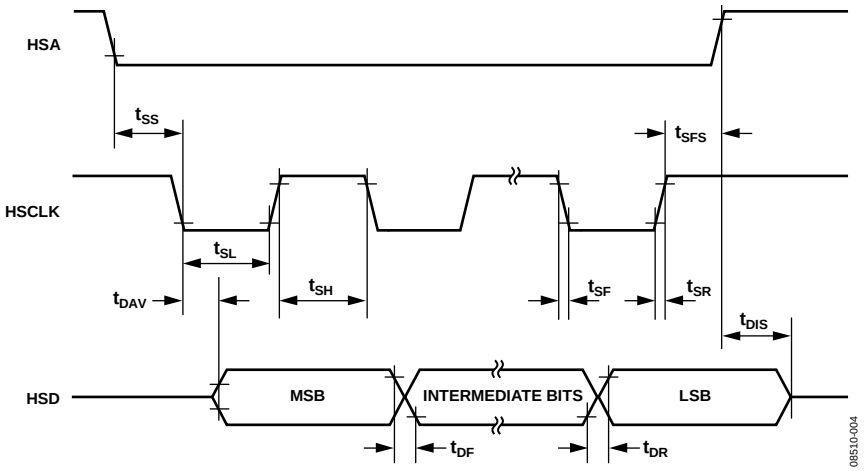

Figure 7. HSDC Interface Timing

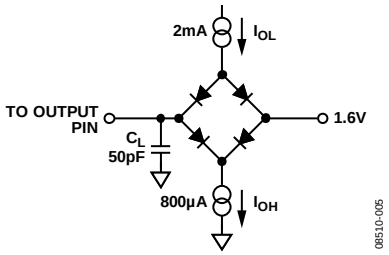

Figure 8. Load Circuit for Timing Specifications

Downloaded from Arrow.com.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	−2 V to +2 V
Analog Input Voltage to INP and INN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note that, regarding the temperature profile used in soldering RoHS compliant parts, Analog Devices advises that reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for the latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 29.3°C/W; θ_{JC} is specified equal to 1.8°C/W.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Downloaded from Arrow.com.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

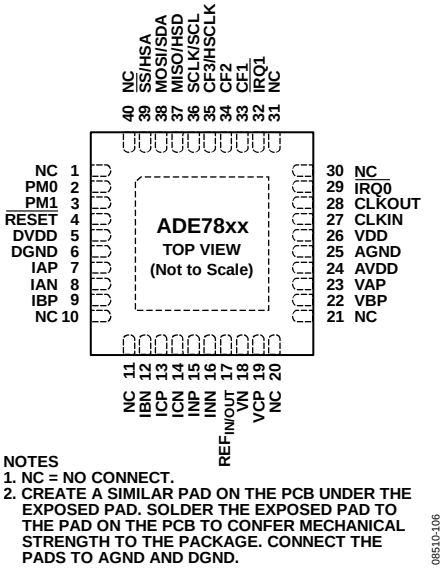

Figure 9. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. These pins are not connected internally. It is recommended to ground these pins.
2	PM0	Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878, as described in Table 9.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878 when combined with PM0, as described in Table 9.
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin should stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	2.5 V output of the digital low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this document as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this document as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this document as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B.
15, 16	INP, INN	Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this document as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels. The neutral current channel is available in the ADE7878 and ADE7868. In the ADE7858 and ADE7854, connect these pins to AGND.
17	$\text{REF}_{\text{IN/OUT}}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.

Downloaded from Arrow.com.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. This channel also has an internal PGA.
24	AVDD	2.5 V output of the analog low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7868/ADE7878 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. The only modes available on the ADE7858 and ADE7854 are the PSM0 and PSM3 power modes.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7854/ADE7858/ADE7868/ADE7878. The clock frequency for specified operation is 16.384 MHz. See the Crystal Circuit section for details on choosing a suitable crystal.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7854/ADE7858/ADE7868/ADE7878.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF3 is multiplexed with the serial clock output of the HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I^2C Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
37	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
38	MOSI/SDA	Data In for SPI Port/Data Out for I^2C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

Downloaded from Arrow.com.

TYPICAL PERFORMANCE CHARACTERISTICS

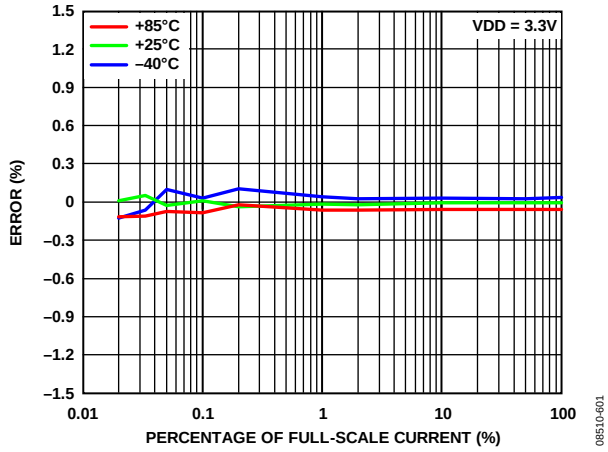

Figure 10. Total Active Energy Error As Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

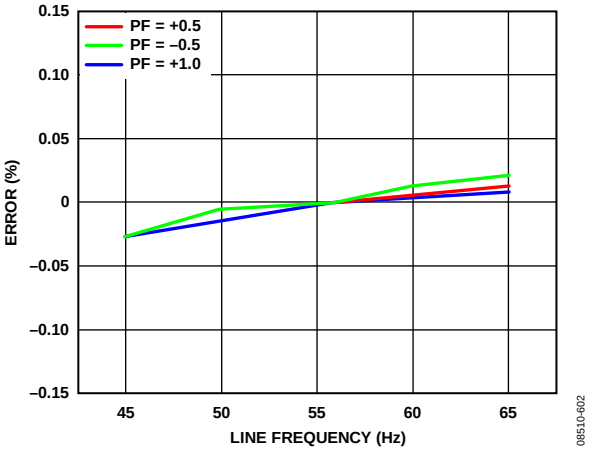

Figure 11. Total Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

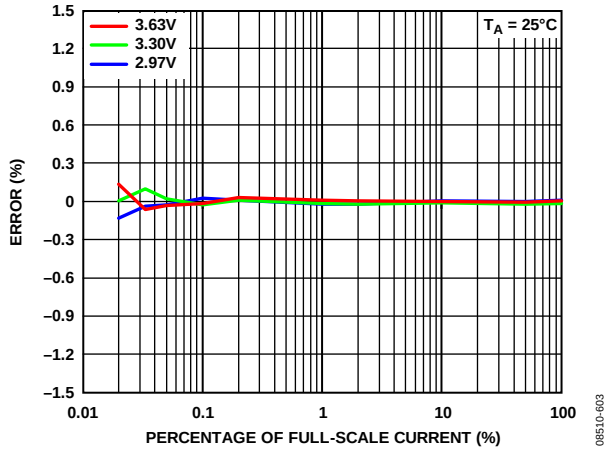

Figure 12. Total Active Energy Error As Percentage of Reading (Gain = +1, Power Factor = 1) over Power Supply with Internal Reference and Integrator Off

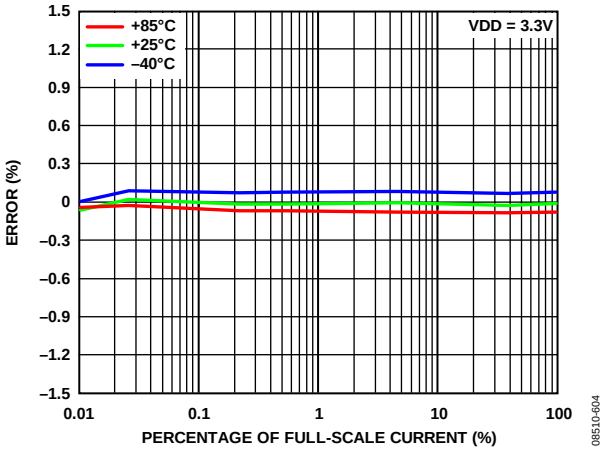

Figure 13. Total Active Energy Error As Percentage of Reading (Gain = +16, Power Factor = 1) over Temperature with Internal Reference and Integrator On

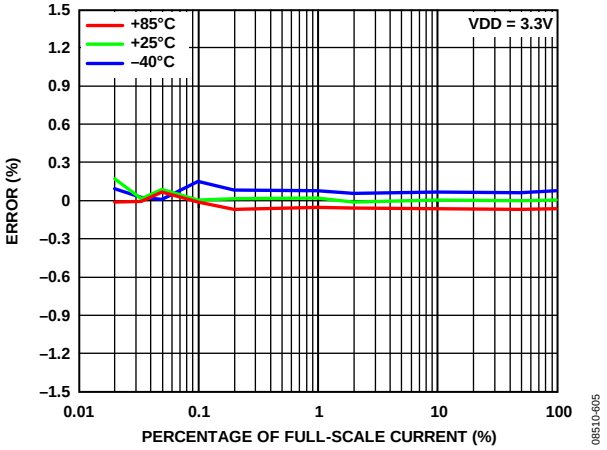

Figure 14. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Temperature with Internal Reference and Integrator Off

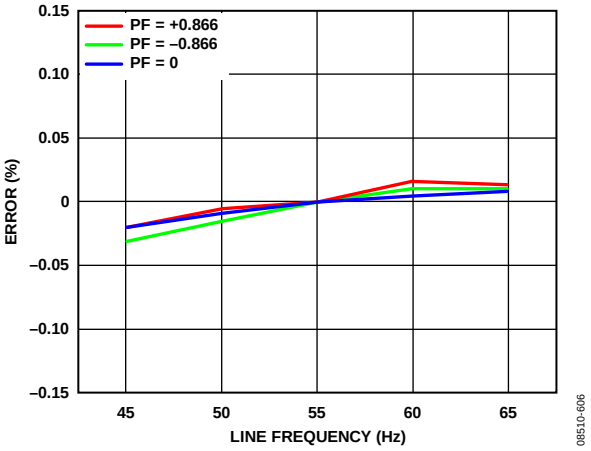

Figure 15. Total Reactive Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

Downloaded from Arrow.com.

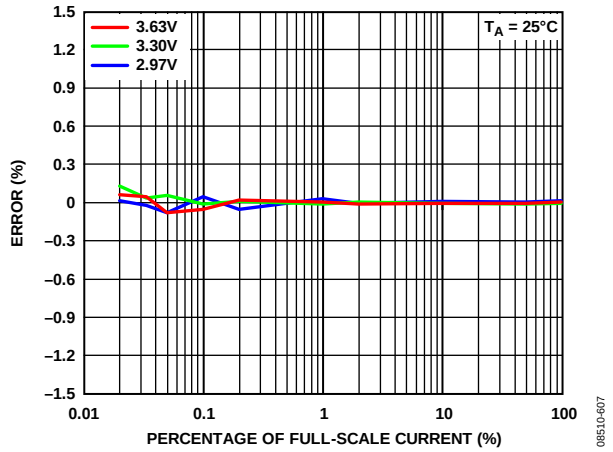

Figure 16. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Power Supply with Internal Reference and Integrator Off

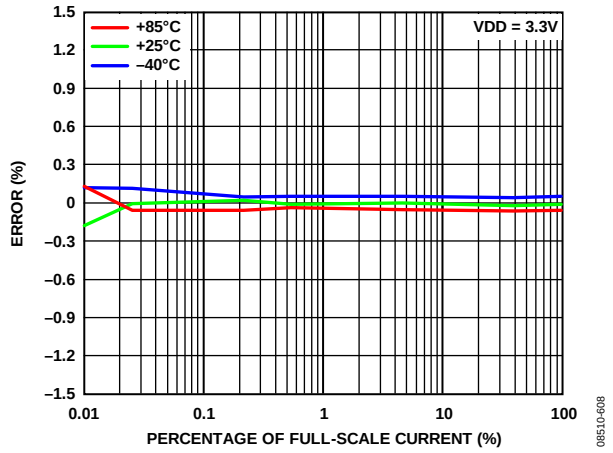

Figure 17. Total Reactive Energy Error As Percentage of Reading (Gain = +16, Power Factor = 0) over Temperature with Internal Reference and Integrator On

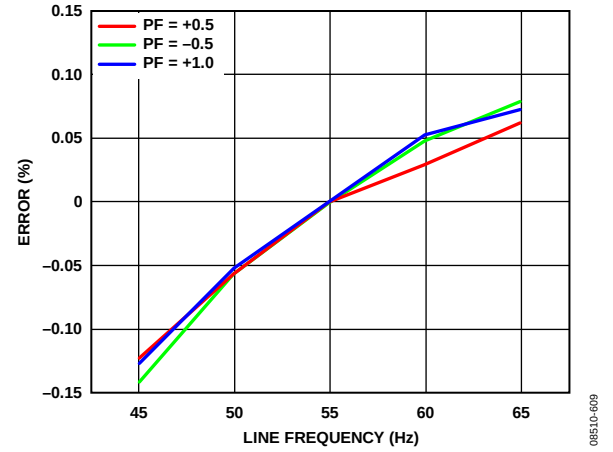

Figure 18. Fundamental Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

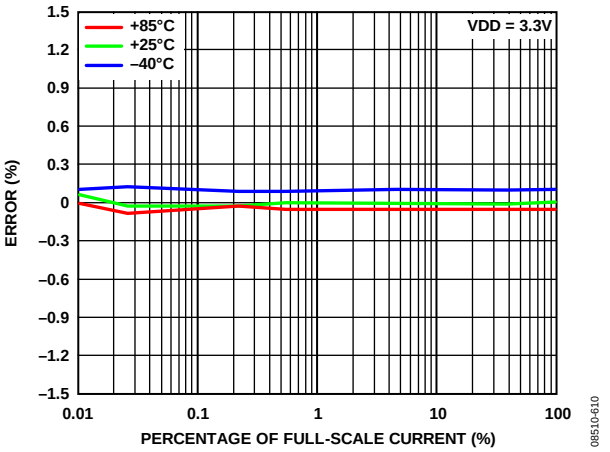

Figure 19. Fundamental Active Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

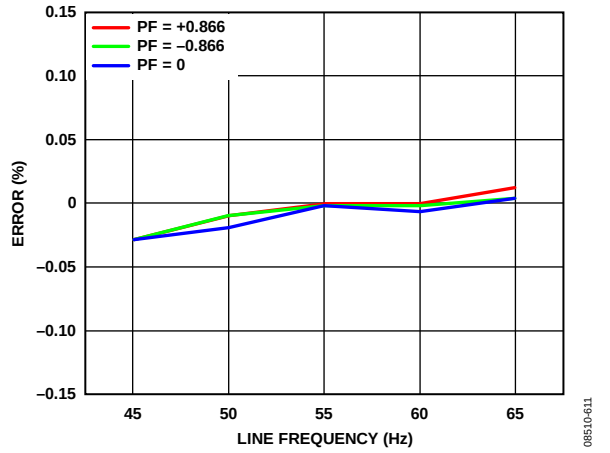

Figure 20. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

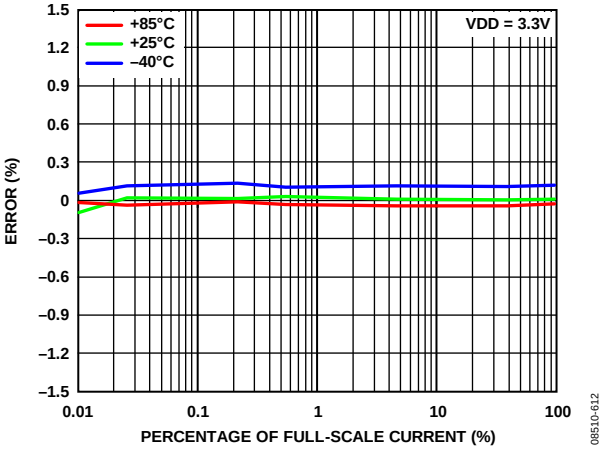

Figure 21. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

Downloaded from Arrow.com.

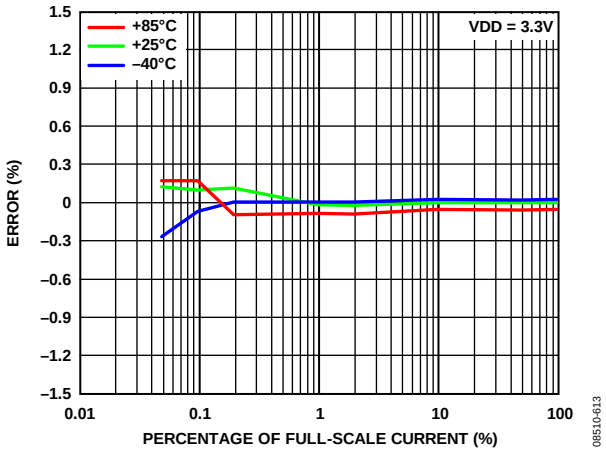

Figure 22. IRMS Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

Downloaded from Arrow.com.

TEST CIRCUIT

Note that in Figure 23, the PM1 and PM0 pins are pulled up internally to 3.3 V. Select the mode of operation by using a microcontroller to programmatically change the pin values.

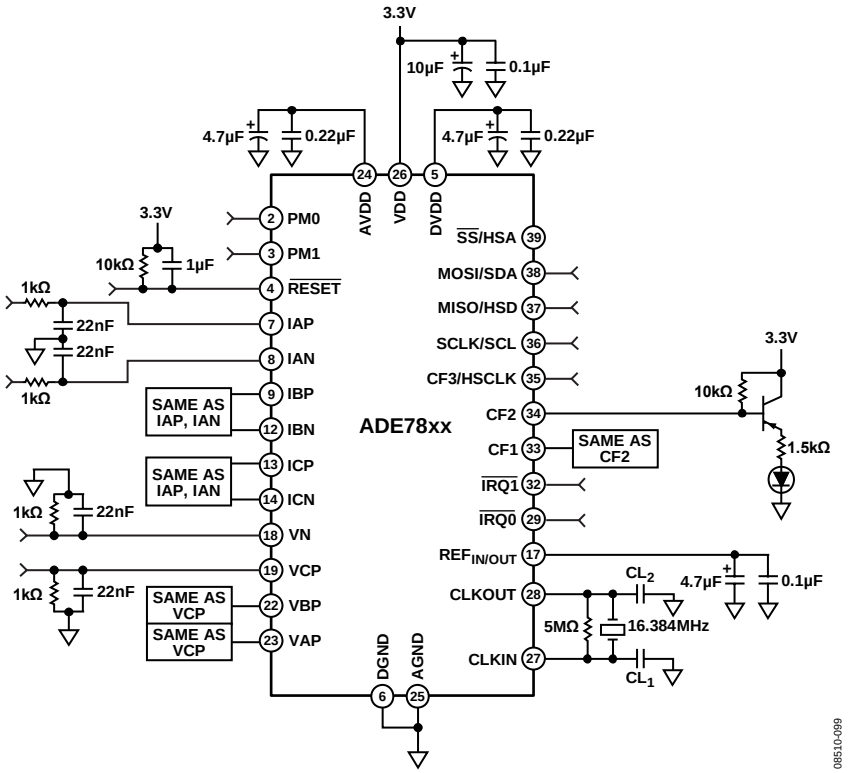

Figure 23. Test Circuit

Downloaded from Arrow.com.

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7854/ADE7858/ADE7868/ADE7878 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE78xx - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Power Supply Rejection (PSR)

This quantifies the ADE7854/ADE7858/ADE7868/ADE7878 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at twice the fundamental frequency) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection However, the HPF removes the offset from the current and voltage channels and the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7854/ADE7858/ADE7868/ADE7878 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

Signal-to-(Noise and Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

Downloaded from Arrow.com.

POWER MANAGEMENT

The ADE7868/ADE7878 have four modes of operation, determined by the state of the PM0 and PM1 pins (see Table 9). The ADE7854/ADE7858 have two modes of operation. These pins provide complete control of the ADE7854/ADE7858/ADE7868/ADE7878 operation and can easily be connected to an external microprocessor I/O. The PM0 and PM1 pins have internal pull-up resistors. See Table 11 and Table 12 for a list of actions that are recommended before and after setting a new power mode.

Table 9. Power Supply Modes

Power Supply Modes	PM1	PM0
PSM0, Normal Power Mode	0	1
PSM1, Reduced Power Mode[1]	0	0
PSM2, Low Power Mode[1]	1	0
PSM3, Sleep Mode	1	1

[1] Available in the ADE7868 and ADE7878.

PSM0—NORMAL POWER MODE (ALL PARTS)

In PSM0 mode, the ADE7854/ADE7858/ADE7868/ADE7878 are fully functional. The PM0 pin is set to high and the PM1 pin is set to low for the ADE78xx to enter this mode. If the ADE78xx is in one of PSM1, PSM2, or PSM3 modes and is switched into PSM0 mode, then all control registers take the default values with the exception of the threshold register, LPOILVL, which is used in PSM2 mode, and the CONFIG2 register, both of which maintain their values.

The ADE7854/ADE7858/ADE7868/ADE7878 signal the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the interrupt mask register does not have any functionality attached even if the $\overline{\text{IRQ1}}$ pin goes low when Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

PSM1—REDUCED POWER MODE (ADE7868, ADE7878 ONLY)

The reduced power mode, PSM1, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 measure the mean absolute values (mav) of the 3-phase currents and store the results in the AIMAV, BIMAV, and CIMAV 20-bit registers. This mode is useful in missing neutral cases in which the voltage supply of the ADE7868 or ADE7878 is provided by an external battery. The serial ports, I^2C or SPI, are enabled in this mode; the active port can be used to read the AIMAV, BIMAV, and CIMAV registers. It is not recommended to read any of the other registers because their values are not guaranteed in this mode. Similarly, a write operation is not taken into account by the ADE7868/ADE7878 in this mode.

In summary, in this mode, it is not recommended to access any register other than AIMAV, BIMAV, and CIMAV. The circuit that measures these estimates of rms values is also active during PSM0; therefore, its calibration can be completed in either PSM0 mode or in PSM1 mode. Note that the ADE7868 and ADE7878 do not provide any register to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values in connection with these measurements and uses them during PSM1 (see the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for more details on the xIMAV registers).

The 20-bit mean absolute value measurements done in PSM1, although available also in PSM0, are different from the rms measurements of phase currents and voltages executed only in PSM0 and stored in the xIRMS and xVRMS 24-bit registers. See the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for details.

If the ADE7868/ADE7878 is set in PSM1 mode while still in the PSM0 mode, the ADE7868/ADE7878 immediately begin the mean absolute value calculations without any delay. The xIMAV registers are accessible at any time; however, if the ADE7878 or ADE7868 is set in PSM1 mode while still in PSM2 or PSM3 modes, the ADE7868/ADE7878 signal the start of the mean absolute value computations by triggering the $\overline{\text{IRQ1}}$ pin low. The xIMAV registers can be accessed only after this moment.

PSM2—LOW POWER MODE (ADE7868, ADE7878 ONLY)

The low power mode, PSM2, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 compare all phase currents against a threshold for a period of 0.02 × (LPLINE[4:0] + 1) seconds, independent of the line frequency. LPLINE[4:0] are Bits[7:3] of the LPOILVL register (see Table 10).

Table 10. LPOILVL Register

Bit	Mnemonic	Default	Description
[2:0]	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8.
[7:3]	LPLINE[4:0]	00000	The measurement period is (LPLINE[4:0] + 1)/50 sec.

Downloaded from Arrow.com.

The threshold is derived from Bits[2:0] (LPOIL[2:0]) of the LPOILVL register as LPOIL[2:0]/8 of full scale. Every time one phase current becomes greater than the threshold, a counter is incremented. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, then the $\overline{\text{IRQ0}}$ pin is triggered low. If a single phase counter becomes greater or equal to LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ1}}$ pin is triggered low. Figure 24 illustrates how the ADE7868/ADE7878 behave in PSM2 mode when LPLINE[4:0] = 2 and LPOIL[2:0] = 3. The test period is three 50 Hz cycles (60 ms), and the Phase A current rises above the LPOIL[2:0] threshold three times. At the end of the test period, the $\overline{\text{IRQ1}}$ pin is triggered low.

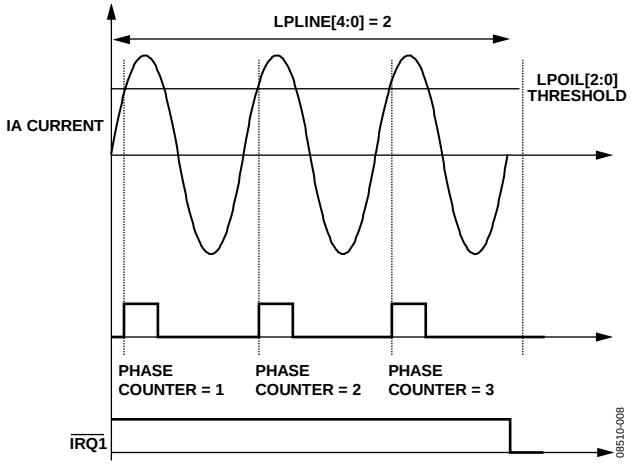

Figure 24. PSM2 Mode Triggering $\overline{\text{IRQ1}}$ Pin for LPLINE[4:0] = 2 (50 Hz Systems)

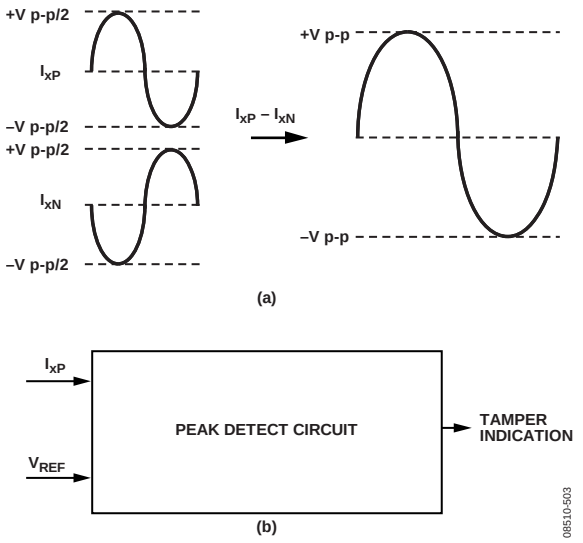

Figure 25. PSM2 Low Power Mode Peak Detection

The PSM2 level threshold comparison works based on a peak detection methodology. The peak detect circuit makes the comparison based on the positive terminal current channel input, I_{AP}, I_{BP}, and I_{CP} (see Figure 25). In case of differential inputs being applied to the current channels, Figure 25 shows the differential antiphase signals at each of the current input terminals, I_{xP} and I_{xN}, and the net differential current, $I_{xP} - I_{xN}$.

The I²C or SPI port is not functional during this mode. The PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input and the voltage supply of the ADE7868/ADE7878 is provided by an external battery. If the $\overline{\text{IRQ0}}$ pin is triggered low at the end of a measurement period, this signifies all phase currents stayed below threshold and, therefore, there is no current flowing through the system. At this point, the external microprocessor sets the ADE7868/ADE7878 into Sleep Mode PSM3. If the $\overline{\text{IRQ1}}$ pin is triggered low at the end of the measurement period, this signifies that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7868/ADE7878 pins. This situation is often called missing neutral and is considered a tampering situation, at which point the external microprocessor sets the ADE7868/ADE7878into PSM1 mode, measures the mean absolute values of phase currents, and integrates the energy based on their values and the nominal voltage.

It is recommended to use the ADE7868/ADE7878 in PSM2 mode when Bits[2:0] (PGA1[2:0]) of the gain register are equal to 1 or 2. These bits represent the gain in the current channel datapath. It is not recommended to use the ADE7868/ADE7878 in PSM2 mode when the PGA1[2:0] bits are equal to 4, 8, or 16.

PSM3—SLEEP MODE (ALL PARTS)

The sleep mode is available on all parts (ADE7854, ADE7858, ADE7868, and ADE7878). In this mode, the ADE78xx has most of its internal circuits turned off and the current consumption is at its lowest level. The I²C, HSDC, and SPI ports are not functional during this mode, and the $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins should be set high.

Downloaded from Arrow.com.

Table 11. Power Modes and Related Characteristics

Power Mode	All Registers[1]	LPOILVL, CONFIG2	I²C/SPI	Functionality
PSM0				
State After Hardware Reset	Set to default	Set to default	I²C enabled	All circuits are active and DSP is in idle mode.
State After Software Reset	Set to default	Unchanged	Active serial port is unchanged if lock-in procedure has been previously executed	All circuits are active and DSP is in idle mode.
PSM1—ADE7878, ADE7868 Only	Not available	Values set during PSM0 unchanged	Enabled	Current mean absolute values are computed and the results are stored in the AIMAV, BIMAV, and CIMAV registers. The I²C or SPI serial port is enabled with limited functionality.
PSM2—ADE7878, ADE7868 Only	Not available	Values set during PSM0 unchanged	Disabled	Compares phase currents against the threshold set in LPOILVL. Triggers $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pins accordingly. The serial ports are not available.
PSM3	Not available	Values set during PSM0 unchanged	Disabled	Internal circuits shut down and the serial ports are not available.

[1] Setting for all registers except the LPOILVL and CONFIG2 registers.

Table 12. Recommended Actions When Changing Power Modes

Initial Power Mode	Recommended Actions Before Setting Next Power Mode	Next Power Mode			
		PSM0	PSM1	PSM2	PSM3
PSM0	Stop DSP by setting the run register = 0x0000. Disable HSDC by clearing Bit 6 (HSDEN) to 0 in the CONFIG register. Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0. Erase interrupt status flags in the STATUS0 and STATUS1 registers.		Current mean absolute values (mav) computed immediately. xIMAV registers can be accessed immediately.	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly.	No action necessary.
PSM1—ADE7878, ADE7868 Only	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.		Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly.	No action necessary.
PSM2—ADE7878, ADE7868 Only	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.	Wait until the $\overline{\text{IRQ1}}$ pin triggered low. Current mean absolute values compute at this moment. xIMAV registers may be accessed from this moment.		No action necessary.
PSM3	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low. Current mav circuit begins computations at this time. xIMAV registers can be accessed from this moment.	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly.	

Downloaded from Arrow.com.

POWER-UP PROCEDURE

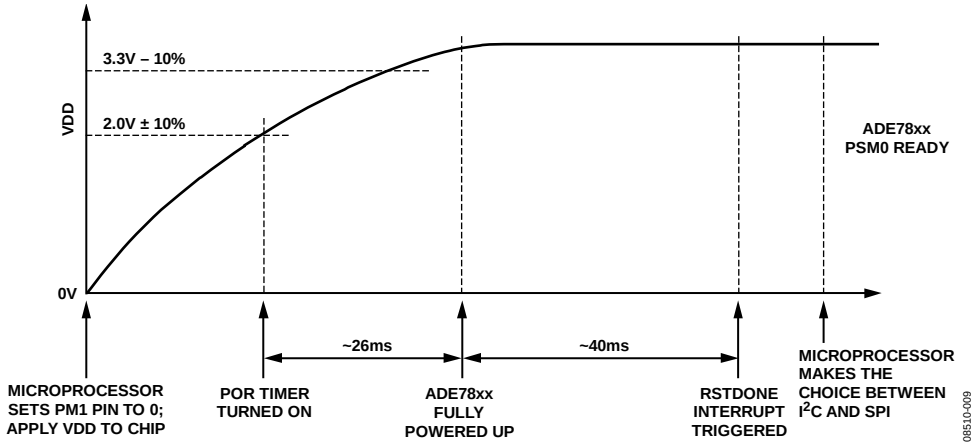

Figure 26. Power-Up Procedure

The ADE7854/ADE7858/ADE7868/ADE7878 contain an on-chip power supply monitor that supervises the power supply (VDD). At power-up, the device is inactive until VDD reaches 2 V ± 10%. When VDD crosses this threshold, the power supply monitor keeps the device in the inactive state for an additional 26 ms to allow VDD to rise to 3.3 V − 10%, the minimum recommended supply voltage.

The PM0 and PM1 pins have internal pull-up resistors, but it is necessary to set the PM1 pin to Logic 0 either through a microcontroller or by grounding the PM1 pin externally, before powering up the chip. The PM0 pin can remain open as it is held high, due to the internal pull-up resistor. This ensures that ADE7854/ADE7858/ADE7868/ADE7878 always power up in PSM0 (normal) mode. The time taken from the chip being powered up completely to the state where all functionality is enabled, is about 40 ms (see Figure 26). It is necessary to ensure that the $\overline{\text{RESET}}$ pin is held high during the entire power-up procedure.

If PSM0 mode is the only desired power mode, the PM1 pin can be tied to ground externally. When the ADE7854/ADE7858/ADE7868/ADE7878 enter PSM0 mode, the I²C port is the active serial port. To use the SPI port, toggle the $\overline{\text{SS}}$/HSA pin three times from high to low.

To lock I²C as the active serial port, set Bit 1 (I2C_LOCK) of the CONFIG2 register to 1. From this moment, the device ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and a switch to the SPI port is no longer possible.

If SPI is the active serial port, any write to the CONFIG2 register locks the port, and a switch to the I²C port is no longer possible. To use the I²C port, the ADE7854/ADE7858/ADE7868/ADE7878 must be powered down or the device must be reset by setting the $\overline{\text{RESET}}$ pin low. After the serial port is locked, the serial port selection is maintained when the device changes from one PSMx power mode to another.

Immediately after entering PSM0 mode, all registers in the ADE7854/ADE7858/ADE7868/ADE7878 are set to their default values, including the CONFIG2 and LPOILVL registers.

The ADE7854/ADE7858/ADE7868/ADE7878 signal the end of the transition period by pulling the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is cleared to 0 during the transition period and is set to 1 when the transition ends. Writing the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high. Because RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. Wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode and, therefore, does not execute any instructions. This is the moment to initialize all registers in the ADE7854, ADE7858, ADE7868, or ADE7878. See the Digital Signal Processor section for the proper procedure to initialize all registers and start the metering.

If the supply voltage, VDD, falls lower than 2 V ± 10%, the ADE7854/ADE7858/ADE7868/ADE7878 enter an inactive state, which means that no measurements or computations are executed.

Downloaded from Arrow.com.

HARDWARE RESET

The ADE7854/ADE7858/ADE7868/ADE7878 each has a $\overline{\text{RESET}}$ pin. If the ADE7854, ADE7858, ADE7868, or ADE7878 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is set low, then the ADE78xx enters the hardware reset state. The ADE78xx must be in PSM0 mode for a hardware reset to be considered. Setting the $\overline{\text{RESET}}$ pin low while the ADE78xx is in PSM1, PSM2, and PSM3 modes does not have any effect.

If the ADE7854, ADE7858, ADE7868, or ADE7878 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is toggled from high to low and then back to high after at least 10 µs, all the registers are set to their default values, including the CONFIG2 and LPOILVL registers. The ADE78xx signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned high by writing to the STATUS1 register with the corresponding bit set to 1.

After a hardware reset, the DSP is in idle mode, which means it does not execute any instruction.

Because the I²C port is the default serial port of the ADE7854/ADE7858/ADE7868/ADE7878, it becomes active after a reset state. If SPI is the port used by the external microprocessor, the procedure to enable it must be repeated immediately after the $\overline{\text{RESET}}$ pin is toggled back to high (see the Serial Interfaces section for details).

At this point, it is recommended to initialize all of the ADE78xx registers, enable data memory RAM protection, and then write 0x0001 into the run register to start the DSP. See the Digital Signal Processor section for details on data memory RAM protection and the run register.

SOFTWARE RESET FUNCTIONALITY

Bit 7 (SWRST) in the CONFIG register manages the software reset functionality in PSM0 mode. The default value of this bit is 0. If this bit is set to 1, then the ADE7854/ADE7858/ADE7868/ADE7878 enter the software reset state. In this state, almost all internal registers are set to their default values. In addition, the choice of which serial port, I²C or SPI, is in use remains unchanged if the lock-in procedure has been executed previously (see the Serial Interfaces for details). The registers that maintain their values despite the SWRST bit being set to 1 are the CONFIG2 and LPOILVL registers. When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

After a software reset ends, the DSP is in idle mode, which means it does not execute any instruction. It is recommended to initialize all the ADE7854/ADE7858/ADE7868/ADE7878 registers and then enable the data memory RAM protection and write 0x0001 into the run register to start the DSP (see the Digital Signal Processor section for details on data memory RAM protection and the run register).

Software reset functionality is not available in PSM1, PSM2, or PSM3 mode.

Downloaded from Arrow.com.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7868/ADE7878 have seven analog inputs forming current and voltage channels. The ADE7854/ADE7858 have six analog inputs, not offering the neutral current. The current channels consist of four pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, ICP and ICN, and INP and INN. These vol-tage input pairs have a maximum differential signal of ±0.5 V. In addition, the maximum signal level on analog inputs for the IxP/IxN pair is ±0.5 V with respect to AGND. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 27 presents a schematic of the input for the current channels and their relation to the maximum common-mode voltage.

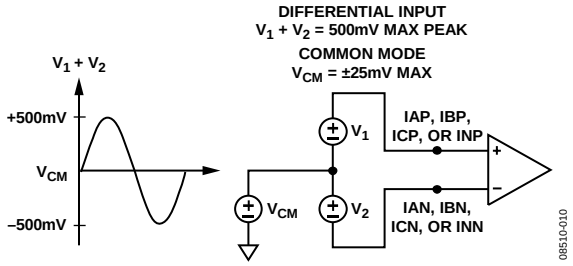

Figure 27. Maximum Input Level, Current Channels, Gain = 1

All inputs have a programmable gain amplifier (PGA) with a possible gain selection of 1, 2, 4, 8, or 16. The gain of IA, IB, and IC inputs is set in Bits[2:0] (PGA1[2:0]) of the gain register. For the ADE7868 and ADE7878 only, the gain of the IN input is set in Bits[5:3] (PGA2[2:0]) of the gain register; thus, a different gain from the IA, IB, or IC inputs is possible. See Table 44 for details on the gain register.

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. In addition, the max-imum signal level on analog inputs for VxP and VN is ±0.5 V with respect to AGND. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 28 presents a schematic of the voltage channels inputs and their relation to the maximum common-mode voltage.

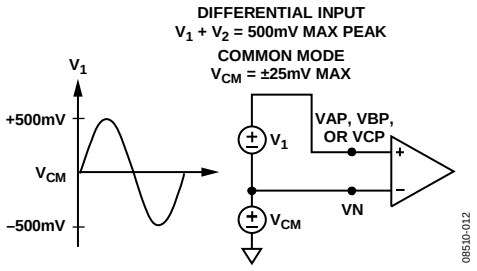

Figure 28. Maximum Input Level, Voltage Channels, Gain = 1

All inputs have a programmable gain with a possible gain selection of 1, 2, 4, 8, or 16. To set the gain, use Bits[8:6] (PGA3[2:0]) in the gain register (see Table 44).

Figure 29 shows how the gain selection from the gain register works in both current and voltage channels.

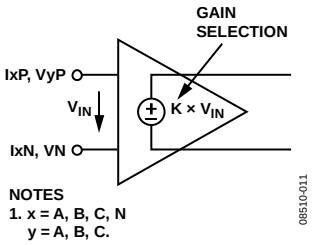

Figure 29. PGA in Current and Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7868/ADE7878 have seven sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), and the ADE7854/ADE7858 have six Σ-Δ ADCs. In PSM0 mode, all ADCs are active. In PSM1 mode, only the ADCs that measure the Phase A, Phase B, and Phase C currents are active. The ADCs that measure the neutral current and the A, B, and C phase voltages are turned off. In PSM2 and PSM3 modes, the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 30 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter.

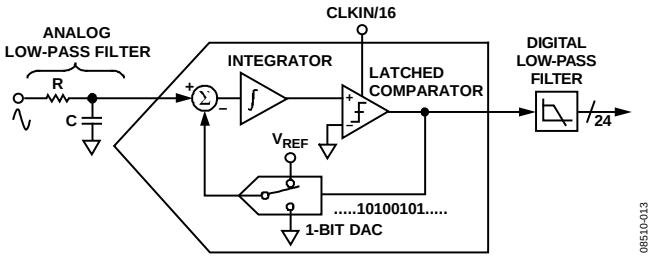

Figure 30. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7854/ADE7858/ADE7868/ADE7878, the sampling clock is equal to 1.024 MHz (CLKIN/16). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than

Downloaded from Arrow.com.

the bandwidth of interest. For example, the sampling rate in the ADE7854/ADE7858/ADE7868/ADE7878 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered, as shown in Figure 31. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required just to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 31.

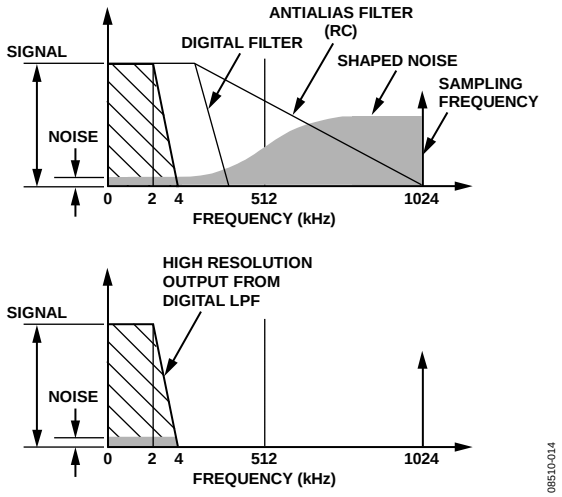

Figure 31. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialiasing Filter

Figure 30 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7854/ADE7858/ADE7868/ADE7878, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems as shown in Figure 32. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, that is, 1.024 MHz, move into the band of interest for metering, that is, 40 Hz to 2 kHz. To attenuate the high frequency (near 1.024 MHz) noise and prevent the distortion of the band of interest, a low-pass filer (LPF) must be introduced. For conventional current sensors, it is recommended to use one RC filter with a corner frequency of 5 kHz for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the 20 dB per decade attenuation produced by the LPF. Therefore, when using a di/dt sensor, take care to offset the 20 dB per decade gain. One simple approach is to cascade one additional RC filter, thereby producing a −40 dB per decade attenuation.

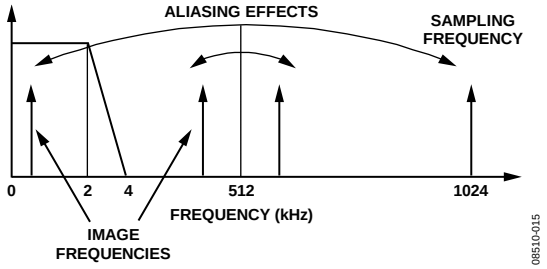

Figure 32. Aliasing Effects

ADC Transfer Function

All ADCs in the ADE7854/ADE7858/ADE7868/ADE7878 are designed to produce the same 24-bit signed output code for the same input signal level. With a full-scale input signal of 0.5 V and an internal reference of 1.2 V, the ADC output code is nominally 5,928,256 (0x5A7540). The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±0.707 V. However, for specified performance, do not exceed the nominal range of ±0.5 V; ADC performance is guaranteed only for input signals lower than ±0.5 V.

CURRENT CHANNEL ADC

Figure 33 shows the ADC and signal processing path for Input IA of the current channels (it is the same for IB and IC). The ADC outputs are signed twos complement 24-bit data-words and are available at a rate of 8 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. Figure 33 shows a full-scale voltage signal applied to the differential inputs (IAP and IAN). The ADC output swings between −5,928,256 (0xA58AC0) and +5,928,256 (0x5A7540). The input, IN, corresponds to the neutral current of a 3-phase system (available in the ADE7868 and ADE7878 only). If no neutral line is present, connect this input to AGND. The datapath of the neutral current is similar to the path of the phase currents as shown in Figure 34.

Downloaded from Arrow.com.

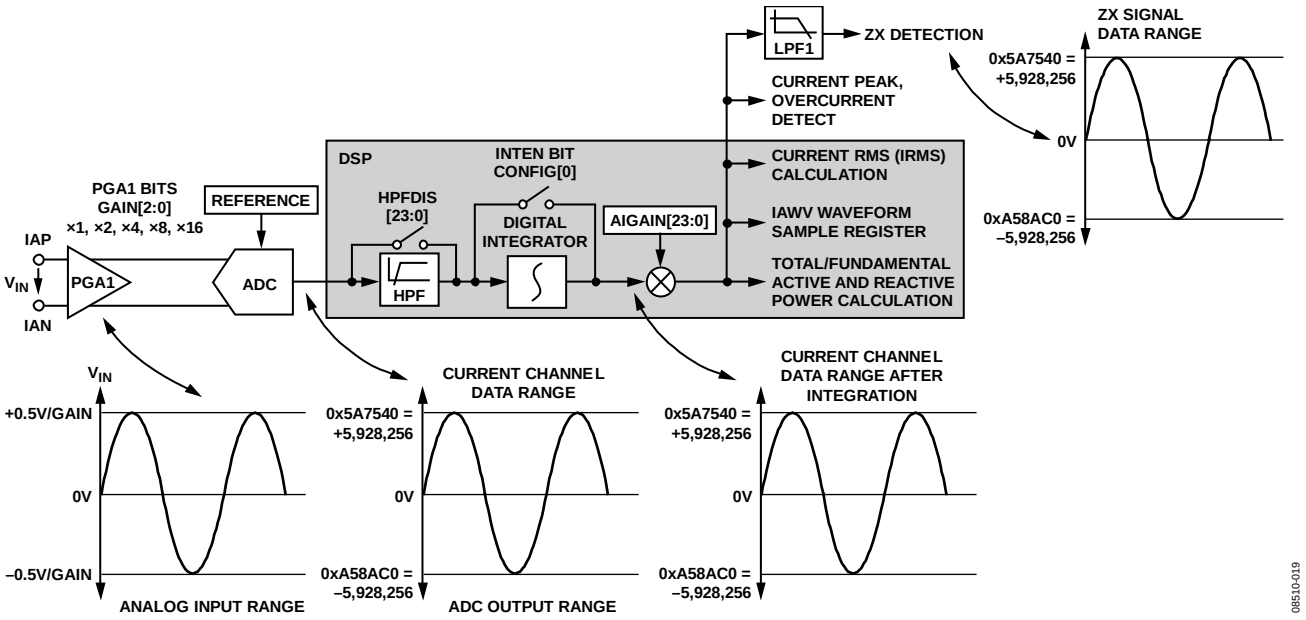

Figure 33. Current Channel Signal Path

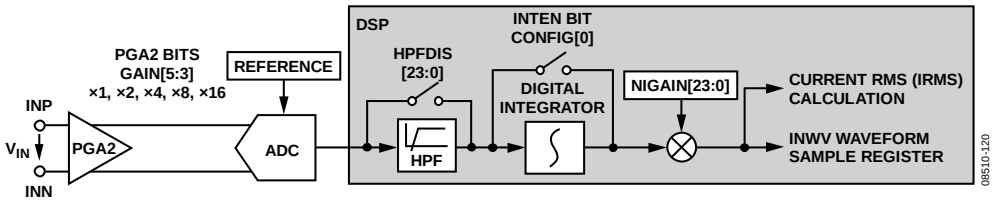

Figure 34. Neutral Current Signal Path (ADE7868, ADE7878 Only)

Current Waveform Gain Registers

There is a multiplier in the signal path of each phase and neutral current. The current waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed current waveform gain registers (AIGAIN, BIGAIN, CIGAIN, and NIGAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 3 describes mathematically the function of the current waveform gain registers.

$$Current\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Current\ Gain\ Register}{2^{23}}\right) \quad (3)$$

Changing the content of the AIGAIN, BIGAIN, CIGAIN, or INGAIN registers affects all calculations based on its current; that is, it affects the corresponding phase active/reactive/apparent energy and current rms calculation. In addition, waveform samples scale accordingly.

Note that the serial ports of the ADE7854, ADE7858, ADE7868, and/or ADE7878 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. The 24-bit AIGAIN, BIGAIN, CIGAIN, and NIGAIN registers are accessed as 32-bit registers with the four most significant bits (MSBs) padded with 0s and sign extended to 28 bits. See Figure 35 for details.

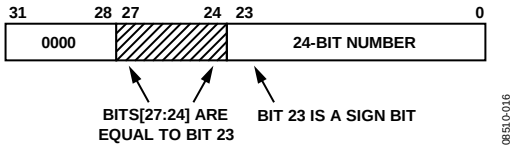

Figure 35. 24-Bit xIGAIN Transmitted as 32-Bit Words

Current Channel HPF

The ADC outputs can contain a dc offset. This offset can create errors in power and rms calculations. High-pass filters (HPFs) are placed in the signal path of the phase and neutral currents and of the phase voltages. If enabled, the HPF eliminates any dc offset on the current channel. All filters are implemented in the DSP and, by default, they are all enabled: the 24-bit HPFDIS register is cleared to 0x00000000. All filters are disabled by setting HPFDIS to any nonzero value.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. The HPFDIS register is accessed as a 32-bit register with eight MSBs padded with 0s. See Figure 36 for details.

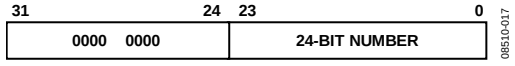

Figure 36. 24-Bit HPFDIS Register Transmitted as 32-Bit Word

Downloaded from Arrow.com.

Current Channel Sampling

The waveform samples of the current channel are taken at the output of HPF and stored in the 24-bit signed registers, IAWV, IBWV, ICWV, and INWV (ADE7868 and ADE7878 only) at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the IAWV, IBWV, ICWV, and INWV registers are available to be read using the I²C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. When the IAWV, IBWV, ICWV, and INWV 24-bit signed registers are read from the ADE78xx (INWV is available on ADE7868/ADE7878 only), they are transmitted sign extended to 32 bits. See Figure 37 for details.

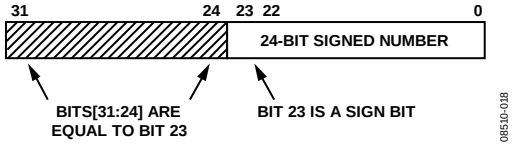

Figure 37. 24-Bit IxWV Register Transmitted as 32-Bit Signed Word

The ADE7854/ADE7858/ADE7868/ADE7878 devices each contain a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in the magnetic field caused by the ac current. Figure 38 shows the principle of a di/dt current sensor.

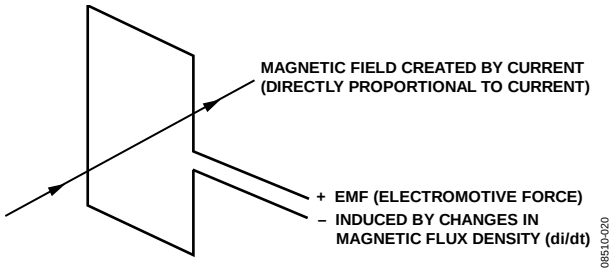

Figure 38. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

Due to the di/dt sensor, the current signal needs to be filtered before it can be used for power measurement. On each phase and neutral current datapath, there is a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator is disabled by default when the ADE78xx is powered up and after a reset. Setting Bit 0 (INTEN) of the CONFIG register turns on the integrator. Figure 39 and Figure 40 show the magnitude and phase response of the digital integrator.

Note that the integrator has a −20 dB/dec attenuation and approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. An antialiasing filter of at least the second order is needed to avoid noise aliasing back in the band of interest when the ADC is sampling (see the Antialiasing Filter section).

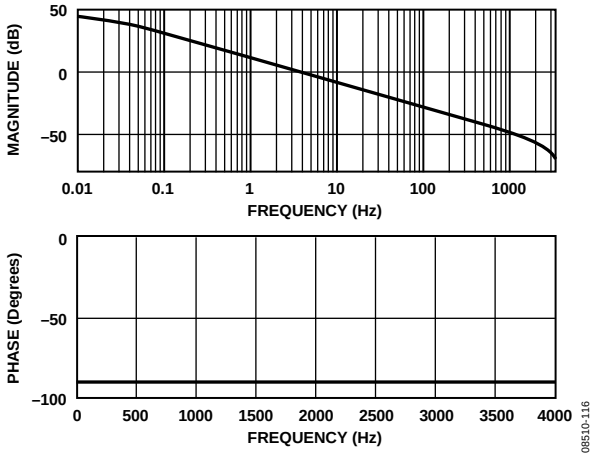

Figure 39. Combined Gain and Phase Response of the Digital Integrator

The DICOEFF 24-bit signed register is used in the digital integrator algorithm. At power-up or after a reset, its value is 0x000000. Before turning on the integrator, this register must be initialized with 0xFFF8000. DICOEFF is not used when the integrator is turned off and can remain at 0x000000 in that case.

Downloaded from Arrow.com.

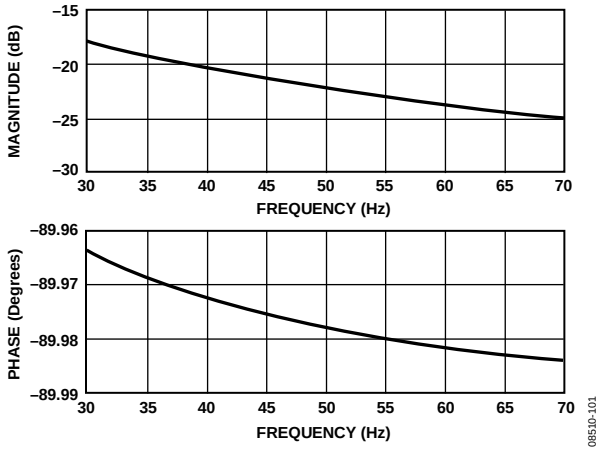

Figure 40. Combined Gain and Phase Response of the Digital Integrator (40 Hz to 70 Hz)

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words. Similar to the registers shown in Figure 35, the DICOEFF 24-bit signed register is accessed as a 32-bit register with four MSBs padded with 0s and sign extended to 28 bits, which practically means it is transmitted equal to 0xFFF8000.

When the digital integrator is switched off, the ADE7854/ ADE7858/ ADE7868/ADE7878 can be used directly with a conventional current sensor, such as a current transformer (CT).

VOLTAGE CHANNEL ADC

Figure 41 shows the ADC and signal processing chain for Input VA in the voltage channel. The VB and VC channels have similar processing chains. The ADC outputs are signed twos complement 24-bit words and are available at a rate of 8 kSPS. With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. Figure 41 shows a full-scale voltage signal being applied to the differential inputs (VA and VN). The ADC output swings between −5,928,256 (0xA58AC0) and +5,928,256 (0x5A7540).

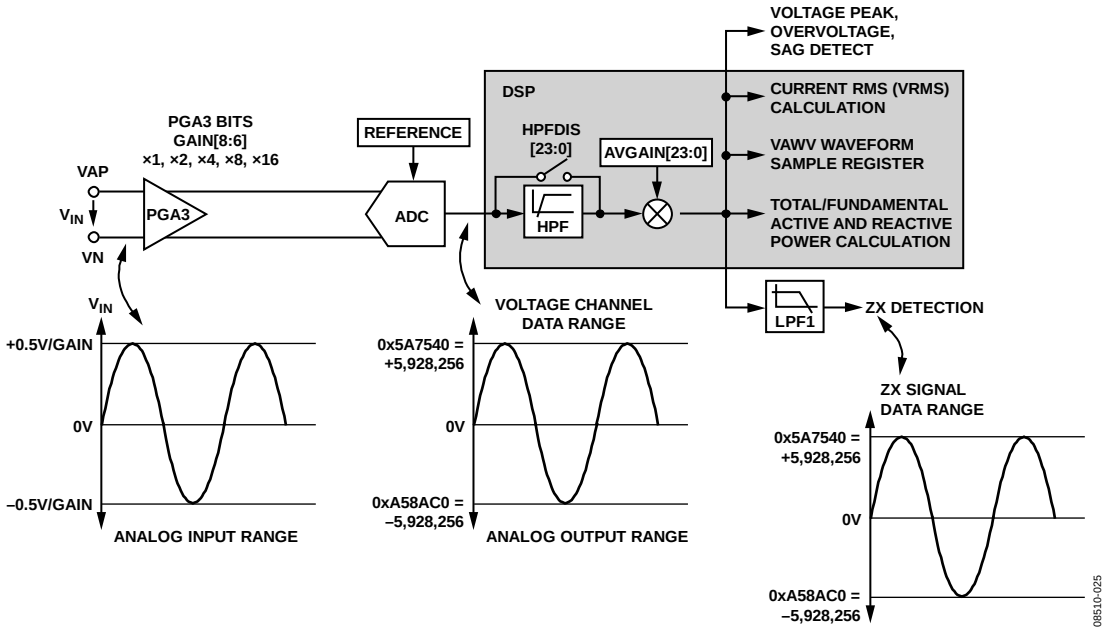

Figure 41. Voltage Channel Datapath

Downloaded from Arrow.com.

Voltage Waveform Gain Registers

There is a multiplier in the signal path of each phase voltage. The voltage waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed voltage waveform gain registers (AVGAIN, BVGAIN, and CVGAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 4 describes mathematically the function of the current waveform gain registers.

$$Voltage\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Voltage\ Gain\ Register}{2^{23}}\right) \quad (4)$$

Changing the content of the AVGAIN, BVGAIN, and CVGAIN registers affects all calculations based on its voltage; that is, it affects the corresponding phase active/reactive/apparent energy and voltage rms calculation. In addition, waveform samples are scaled accordingly.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. As presented in Figure 35, the AVGAIN, BVGAIN, and CVGAIN registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Voltage Channel HPF

As explained in the Current Channel HPF section, the ADC outputs can contain a dc offset that can create errors in power and rms calculations. HPFs are placed in the signal path of the phase voltages, similar to the ones in the current channels. The HPFDIS register can enable or disable the filters. See the Current Channel HPF section for more details.

Voltage Channel Sampling

The waveform samples of the voltage channel are taken at the output of HPF and stored into VAWV, VBWV, and VCWV 24-bit signed registers at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the VAWV, VBWV, and VCWV registers are available to be read using the I^2C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to registers presented in Figure 37, the VAWV, VBWV, and VCWV 24-bit signed registers are transmitted sign extended to 32 bits.

The ADE7854/ADE7858/ADE7868/ADE7878 each contain an HSDC port especially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

CHANGING PHASE VOLTAGE DATAPATH

The ADE7854/ADE7858/ADE7868/ADE7878 can direct one phase voltage input to the computational datapath of another phase. For example, Phase A voltage can be introduced in the Phase B computational datapath, which means all powers computed by the ADE78xx in Phase B are based on Phase A voltage and Phase B current.

Bits[9:8] (VTOIA[1:0]) of the CONFIG register manage what phase voltage is directed to Phase A computational data path. If VTOIA[1:0] = 00 (default value), the Phase A voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 01, the Phase B voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 10, the Phase C voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 11, the ADE7854/ADE7858/ADE7868/ADE7878 behaves as if VTOIA[1:0] = 00.

Bits[11:10] (VTOIB[1:0]) of the CONFIG register manage what phase voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 00 (default value), the Phase B voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 01, the Phase C voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 10, the Phase A voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 11, the ADE7854/ADE7858/ADE7868/ADE7878 behaves as if VTOIB[1:0] = 00.

Bits[13:12] (VTOIC[1:0]) of the CONFIG register manage what phase voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 00 (default value), the Phase C voltage is directed to Phase C computational data path, if VTOIC[1:0] = 01, the Phase A voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 10, the Phase B voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 11, the ADE7854/ADE7858/ADE7868/ADE7878 behaves as if VTOIC[1:0] = 00.

Downloaded from Arrow.com.

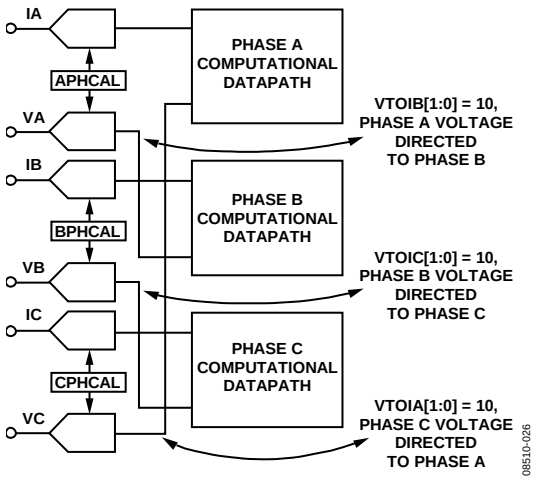

Figure 42. Phase Voltages Used in Different Datapaths

Figure 42 presents the case in which Phase A voltage is used in the Phase B datapath, Phase B voltage is used in the Phase C datapath, and Phase C voltage is used in the Phase A datapath.

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE7854/ADE7858/ADE7868/ADE7878 have a zero-crossing (ZX) detection circuit on the phase current and voltage channels. The neutral current datapath does not contain a zero-crossing detection circuit. Zero-crossing events are used as a time base for various power quality measurements and in the calibration process.

The output of LPF1 is used to generate zero crossing events. The low-pass filter is intended to eliminate all harmonics of 50 Hz and 60 Hz systems, and to help identify the zero-crossing events on the fundamental components of both current and voltage channels.

The digital filter has a pole at 80 Hz and is clocked at 256 kHz. As a result, there is a phase lag between the analog input signal (one of IA, IB, IC, VA, VB, and VC) and the output of LPF1. The error in ZX detection is 0.0703° for 50 Hz systems (0.0843° for 60 Hz systems). The phase lag response of LPF1 results in a time delay of approximately 31.4° or 1.74 ms (at 50 Hz) between its input and output. The overall delay between the zero crossing on the analog inputs and ZX detection obtained after LPF1 is about 39.6° or 2.2 ms (at 50 Hz). The ADC and HPF introduce the additional delay. The LPF1 cannot be disabled to assure a good resolution of the ZX detection. Figure 43 shows how the zero-crossing signal is detected.

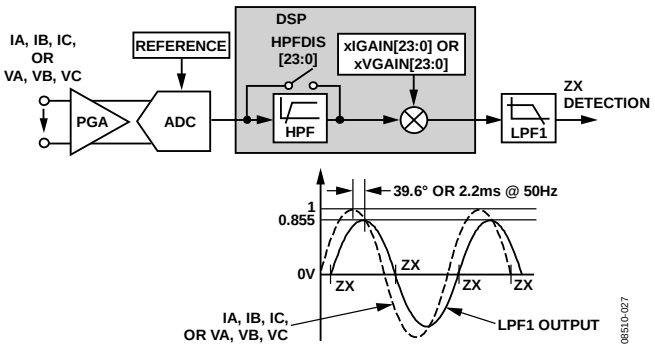

Figure 43. Zero-Crossing Detection on Voltage and Current Channels

To provide further protection from noise, input signals to the voltage channel with amplitude lower than 10% of full scale do not generate zero-crossing events at all. The Current Channel ZX detection circuit is active for all input signals independent of their amplitudes.

The ADE7854/ADE7858/ADE7868/ADE7878 contain six zero-crossing detection circuits, one for each phase voltage and current channel. Each circuit drives one flag in the STATUS1 register. If a circuit placed in the Phase A voltage channel detects one zero-crossing event, Bit 9 (ZXVA) in the STATUS1 register is set to 1.

Similarly, the Phase B voltage circuit drives Bit 10 (ZXVB), the Phase C voltage circuit drives Bit 11 (ZXVC), and circuits placed in the current channel drive Bit 12 (ZXIA), Bit 13 (ZXIB), and Bit 14 (ZXIC) in the STATUS1 register. If a ZX detection bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the corresponding status flag is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

Zero-Crossing Timeout

Every zero-crossing detection circuit has an associated timeout register. This register is loaded with the value written into the 16-bit ZXTOUT register and is decremented (1 LSB) every 62.5 µs (16 kHz clock). The register is reset to the ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, one of Bits[8:3] of the STATUS1 register is set to 1. Bit 3 (ZXTOVA), Bit 4 (ZXTOVB), and Bit 5 (ZXTOVC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the voltage channel; Bit 6 (ZXTOIA), Bit 7 (ZXTOIB), and Bit 8 (ZXTOIC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the current channel.

If a ZXTOIx or ZXTOVx bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when the corresponding status bit is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

The resolution of the ZXOUT register is 62.5 µs (16 kHz clock) per LSB. Thus, the maximum timeout period for an interrupt is 4.096 sec: 2^{16}/16 kHz.

Downloaded from Arrow.com.

Figure 44 shows the mechanism of the zero-crossing timeout detection when the voltage or the current signal stays at a fixed dc level for more than 62.5 µs × ZXTOUT µs.

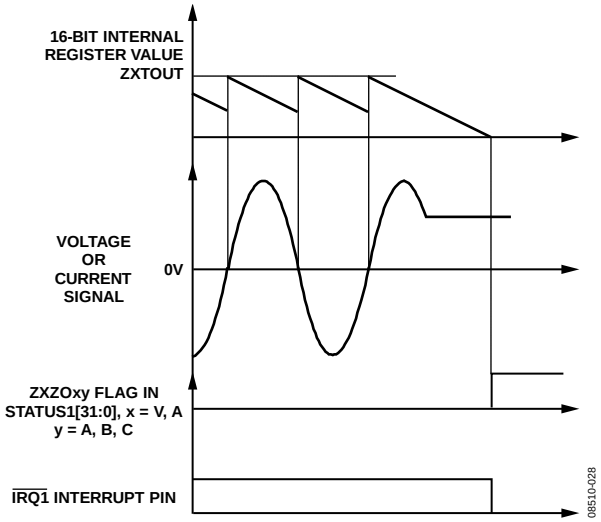

Figure 44. Zero-Crossing Timeout Detection

Phase Sequence Detection

The ADE7854/ADE7858/ADE7868/ADE7878 have on-chip phase sequence error detection circuits. This detection works on phase voltages and considers only the zero crossings determined by their negative-to-positive transitions. The regular succession of these zero-crossing events is Phase A followed by Phase B followed by Phase C (see Figure 46). If the sequence of zero-crossing events is, instead, Phase A followed by Phase C followed by Phase B, then Bit 19 (SEQERR) in the STATUS1 register is set.

If Bit 19 (SEQERR) in the MASK1 register is set to 1 and a phase sequence error event is triggered, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1 register with the Status Bit 19 (SEQERR) set to 1.

The phase sequence error detection circuit is functional only when the ADE78xx is connected in a 3-phase, 4-wire, three voltage sensors configuration (Bits[5:4], CONSEL[1:0] in the ACCMODE register, set to 00). In all other configurations, only two voltage sensors are used; therefore, it is not recommended to use the detection circuit. In these cases, use the time intervals between phase voltages to analyze the phase sequence (see the Time Interval Between Phases section for details).

Figure 45 presents the case in which Phase A voltage is not followed by Phase B voltage but by Phase C voltage. Every time a negative-to-positive zero crossing occurs, Bit 19 (SEQERR) in the STATUS1 register is set to 1 because such zero crossings on Phase C, Phase B, or Phase A cannot come after zero crossings from Phase A, Phase C, or respectively, Phase B zero crossings.

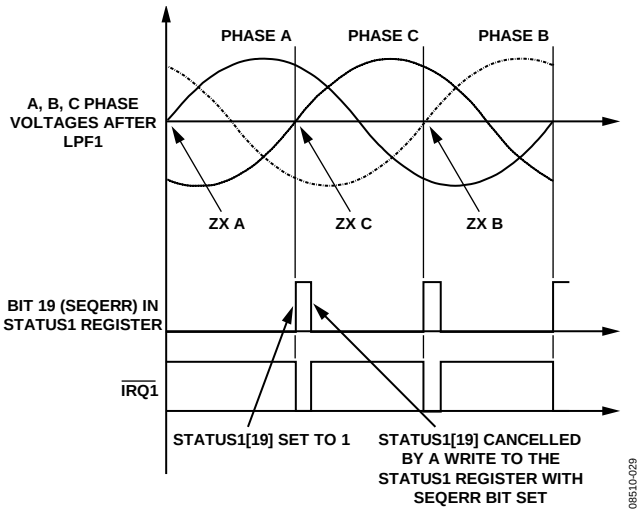

Figure 45. SEQERR Bit Set to 1 When Phase A Voltage Is Followed by Phase C Voltage

Once a phase sequence error has been detected, the time measurement between various phase voltages (see the Time Interval Between Phases section) can help to identify which phase voltage should be considered with another phase current in the computational datapath. Bits[9:8] (VTOIA[1:0]), Bits[11:10] (VTOIB[1:0]), and Bits[13:12] (VTOIC[1:0]) in the CONFIG register can be used to direct one phase voltage to the datapath of another phase. See the Changing Phase Voltage Datapath section for details.

Time Interval Between Phases

The ADE7854/ADE7858/ADE7868/ADE7878 have the capability to measure the time delay between phase voltages, between phase currents, or between voltages and currents of the same phase. The negative-to-positive transitions identified by the zero-crossing detection circuit are used as start and stop measuring points. Only one set of such measurements is available at one time, based on Bits[10:9] (ANGLESEL[1:0]) in the COMPMODE register.

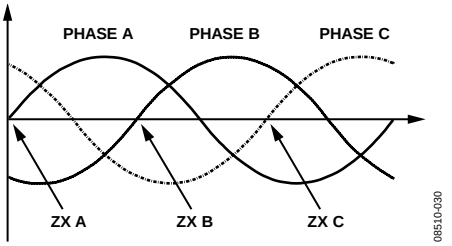

Figure 46. Regular Succession of Phase A, Phase B, and Phase C

When the ANGLESEL[1:0] bits are set to 00, the default value, the delays between voltages and currents on the same phase are measured. The delay between Phase A voltage and Phase A current is stored in the 16-bit unsigned ANGLE0 register (see Figure 47 for details). In a similar way, the delays between voltages and currents on Phase B and Phase C are stored in the ANGLE1 and ANGLE2 registers, respectively.

Downloaded from Arrow.com.

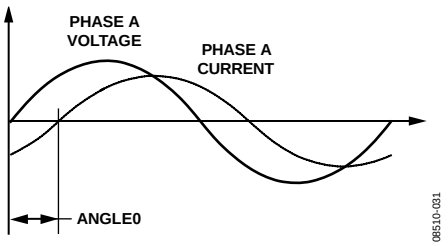

Figure 47. Delay Between Phase A Voltage and Phase A Current Is Stored in the ANGLE0 Register

When the ANGLESEL[1:0] bits are set to 01, the delays between phase voltages are measured. The delay between Phase A voltage and Phase C voltage is stored into the ANGLE0 register. The delay between Phase B voltage and Phase C voltage is stored in the ANGLE1 register, and the delay between Phase A voltage and Phase B voltage is stored in the ANGLE2 register (see Figure 48 for details).

When the ANGLESEL[1:0] bits are set to 10, the delays between phase currents are measured. Similar to delays between phase voltages, the delay between Phase A and Phase C currents is stored into the ANGLE0 register, the delay between Phase B and Phase C currents is stored in the ANGLE1 register, and the delay between Phase A and Phase B currents is stored into the ANGLE2 register (see Figure 48 for details).

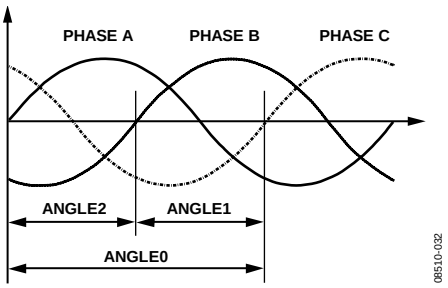

Figure 48. Delays Between Phase Voltages (Currents)

The ANGLE0, ANGLE1, and ANGLE2 registers are 16-bit unsigned registers with 1 LSB corresponding to 3.90625 µs (256 kHz clock), which means a resolution of 0.0703° (360° × 50 Hz/256 kHz) for 50 Hz systems and 0.0843° (360° × 60 Hz/256 kHz) for 60 Hz systems. The delays between phase voltages or phase currents are used to characterize how balanced the load is. The delays between phase voltages and currents are used to compute the power factor on each phase as shown in the following Equation 5:

$$\cos\varphi_x = \cos\left[ANGLEx \times \frac{360^\circ \times f_{LINE}}{256\,\text{kHz}} \right] \quad (5)$$

where f_{LINE} = 50 Hz or 60 Hz.

Period Measurement

The ADE7854/ADE7858/ADE7868/ADE7878 provide the period measurement of the line in the voltage channel. Bits[1:0] (PERSEL[1:0]) in the MMODE register select the phase voltage used for this measurement. The period register is a 16-bit unsigned register and updates every line period. Because of the LPF1 filter (see Figure 43), a settling time of 30 ms to 40 ms is associated with this filter before the measurement is stable.

The period measurement has a resolution of 3.90625 µs/LSB (256 kHz clock), which represents 0.0195% (50 Hz/256 kHz) when the line frequency is 50 Hz and 0.0234% (60 Hz/256 kHz) when the line frequency is 60 Hz. The value of the period register for 50 Hz networks is approximately 5120 (256 kHz/50 Hz) and for 60 Hz networks is approximately 4267 (256 kHz/60 Hz). The length of the register enables the measurement of line frequencies as low as 3.9 Hz (256 kHz/2^{16}). The period register is stable at ±1 LSB when the line is established and the measurement does not change.

The following expressions can be used to compute the line period and frequency using the period register:

$$T_L = \frac{PERIOD[15:0]+1}{256\text{E}3}[\text{sec}] \quad (6)$$

$$f_L = \frac{256\text{E}3}{PERIOD[15:0]+1}[\text{Hz}] \quad (7)$$

Phase Voltage Sag Detection

The ADE7854/ADE7858/ADE7868/ADE7878 can be programmed to detect when the absolute value of any phase voltage drops below a certain peak value for a number of half-line cycles. The phase where this event takes place is identified in Bits[14:12] (VSPHASE[x]) of the PHSTATUS register. This condition is illustrated in Figure 49.

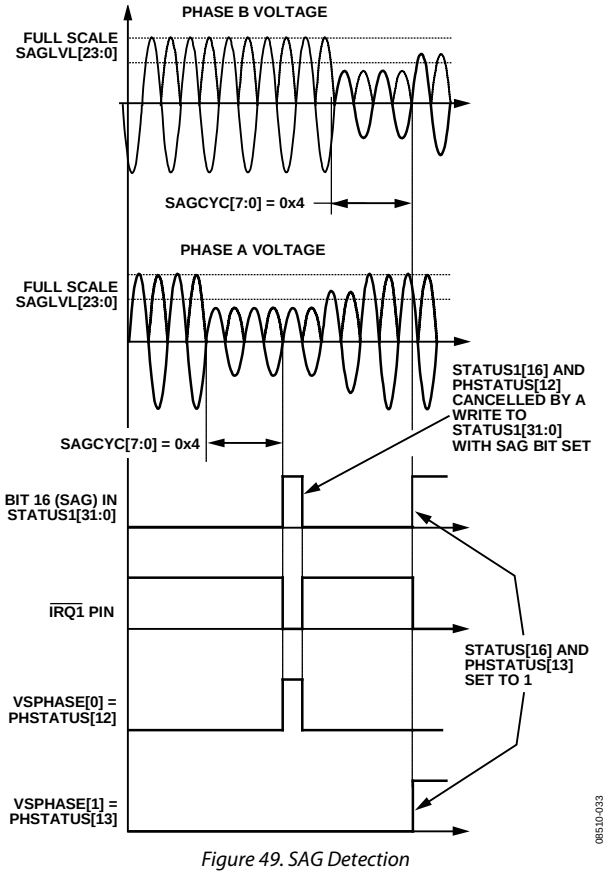

Figure 49. SAG Detection

Downloaded from Arrow.com.

Figure 49 shows Phase A voltage falling below a threshold that is set in the SAG level register (SAGLVL) for four half-line cycles (SAGCYC = 4). When Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition, Bit VSPHASE[0] in the PHSTATUS register is also set to 1 because the event happened on Phase A Bit 16 (SAG) in the STATUS1 register. All Bits[14:12] (VSPHASE[2], VSPHASE[1], and VSPHASE[0]) of the PHSTATUS register (not just the VSPHASE[0] bit) are erased by writing the STATUS1 register with the SAG bit set to 1.

The SAGCYC register represents the number of half-line cycles the phase voltage must remain below the level indicated in the SAGLVL register to trigger a SAG condition; 0 is not a valid number for SAGCYC. For example, when the SAG cycle (SAGCYC[7:0]) contains 0x07, the SAG flag in the STATUS1 register is set at the end of the seventh half line cycle for which the line voltage falls below the threshold. If Bit 16 (SAG) in MASK1 is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of a SAG event in the same moment the Status Bit 16 (SAG) in STATUS1 register is set to 1. The SAG status bit in the STATUS1 register and all Bits[14:12] (VSPHASE[2], VSPHASE[1], and VSPHASE[0]]) of the PHSTATUS register are cleared, and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

When the Phase B voltage falls below the indicated threshold into the SAGLVL register for two line cycles, Bit VSPHASE[1] in the PHSTATUS register is set to 1, and Bit VSPHASE[0] is cleared to 0. Simultaneously, Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition.

Note that the internal zero-crossing counter is always active. By setting the SAGLVL register, the first SAG detection result is, therefore, not executed across a full SAGCYC period. Writing to the SAGCYC register when the SAGLVL register is already initialized resets the zero-crossing counter, thus ensuring that the first SAG detection result is obtained across a full SAGCYC period.

The recommended procedure to manage SAG events is the following:

1. Enable SAG interrupts in the MASK1 register by setting Bit 16 (SAG) to 1.
2. When a SAG event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low and Bit 16 (SAG) in the STATUS1 is set to 1.
3. The STATUS1 register is read with Bit 16 (SAG) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases a SAG event happened.
5. The STATUS1 register is written with Bit 16 (SAG) set to 1. Immediately, the SAG bit and all Bits[14:12] (VSPHASE[2], VSPHASE[1], and VSPHASE[0]) of the PHSTATUS register are erased.

SAG Level Set

The content of the SAGLVL[23:0] SAG level register is compared to the absolute value of the output from HPF. Writing 5,928,256 (0x5A7540) to the SAGLVL register, puts the SAG detection level at full scale (see the Voltage Channel ADC section), thus; the SAG event is triggered continuously. Writing 0x00 or 0x01 puts the SAG detection level at 0, therefore, the SAG event is never triggered.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 36, the SAGLVL register is accessed as a 32-bit register with eight MSBs padded with 0s.

Peak Detection

The ADE7854/ADE7858/ADE7868/ADE7878 record the maximum absolute values reached by the voltage and current channels over a certain number of half-line cycles and stores them into the less significant 24 bits of the VPEAK and IPEAK 32-bit registers.

The PEAKCYC register contains the number of half-line cycles used as a time base for the measurement. The circuit uses the zero-crossing points identified by the zero-crossing detection circuit. Bits[4:2] (PEAKSEL[2:0]) in the MMODE register select the phases upon which the peak measurement is performed. Bit 2 selects Phase A, Bit 3 selects Phase B, and Bit 4 selects Phase C. Selecting more than one phase to monitor the peak values decreases proportionally the measurement period indicated in the PEAKCYC register because zero crossings from more phases are involved in the process. When a new peak value is determined, one of Bits[26:24] (IPPHASE[2:0] or VPPHASE[2:0]) in the IPEAK and VPEAK registers is set to 1, identifying the phase that triggered the peak detection event. For example, if a peak value has been identified on Phase A current, Bit 24 (IPPHASE[0]) in the IPEAK register is set to 1. If next time a new peak value is measured on Phase B, Bit 24 (IPPHASE[0]) of the IPEAK register is cleared to 0, and Bit 25 (IPPHASE[1]) of the IPEAK register is set to 1. Figure 50 shows the composition of the IPEAK and VPEAK registers.

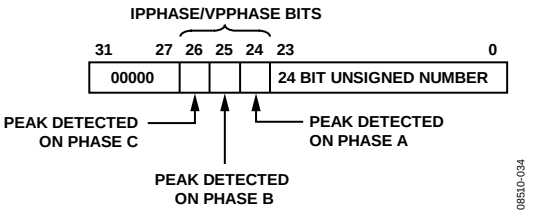

Figure 50. Composition of IPEAK[31:0] and VPEAK[31:0] Registers

Downloaded from Arrow.com.

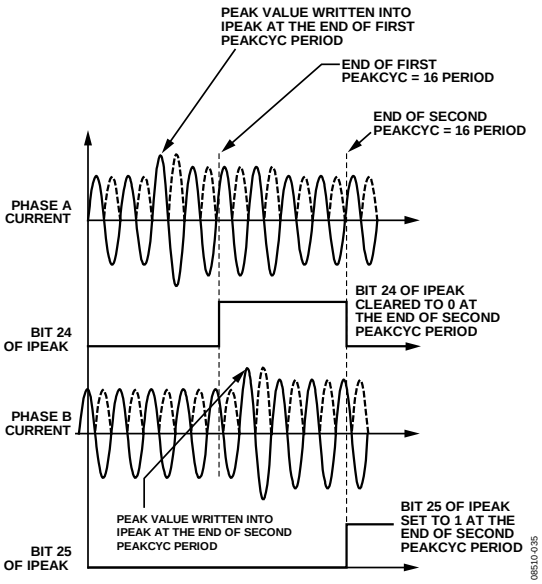

Figure 51. Peak Level Detection

Figure 51 shows how the ADE78xx records the peak value on the current channel when measurements on Phase A and Phase B are enabled (Bit PEAKSEL[2:0] in the MMODE register are 011). PEAKCYC is set to 16, meaning that the peak measurement cycle is four line periods. The maximum absolute value of Phase A is the greatest during the first four line periods (PEAKCYC = 16), so the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 24 (IPPHASE[0]) of the IPEAK register is set to 1 at the end of the period. This bit remains at 1 for the duration of the second PEAKCYC period of four line cycles. The maximum absolute value of Phase B is the greatest during the second PEAKCYC period; therefore, the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 25 (IPPHASE[1]) in the IPEAK register is set to 1 at the end of the period.

At the end of the peak detection period in the current channel, Bit 23 (PKI) in the STATUS1 register is set to 1. If Bit 23 (PKI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and Status Bit 23 (PKI) in the STATUS1 register is set to 1. In a similar way, at the end of the peak detection period in the voltage channel, Bit 24 (PKV) in the STATUS1 register is set to 1. If Bit 24 (PKV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and Status Bit 24 (PKV) in the STATUS1 register is set to 1. To find the phase that triggered the interrupt, one of either the IPEAK or VPEAK registers is read immediately after reading the STATUS1 register. Next, the status bits are cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting Bits[4:2] (PEAKSEL[2:0]) in the MMODE register, the first peak detection result is, therefore, not executed across a full PEAKCYC period. Writing to the PEAKCYC register when the PEAKSEL[2:0] bits are set resets the zero-crossing counter, thereby ensuring that the first peak detection result is obtained across a full PEAKCYC period.

Overvoltage and Overcurrent Detection

The ADE7854/ADE7858/ADE7868/ADE7878 detect when the instantaneous absolute value measured on the voltage and current channels becomes greater than the thresholds set in the OVLVL and OILVL 24-bit unsigned registers. If Bit 18 (OV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of an overvoltage event. There are two status flags set when the $\overline{\text{IRQ1}}$ interrupt pin is driven low: Bit 18 (OV) in the STATUS1 register and one of Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register to identify the phase that generated the overvoltage. The Status Bit 18 (OV) in the STATUS1 register and all Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register are cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1. Figure 52 presents overvoltage detection in Phase A voltage.

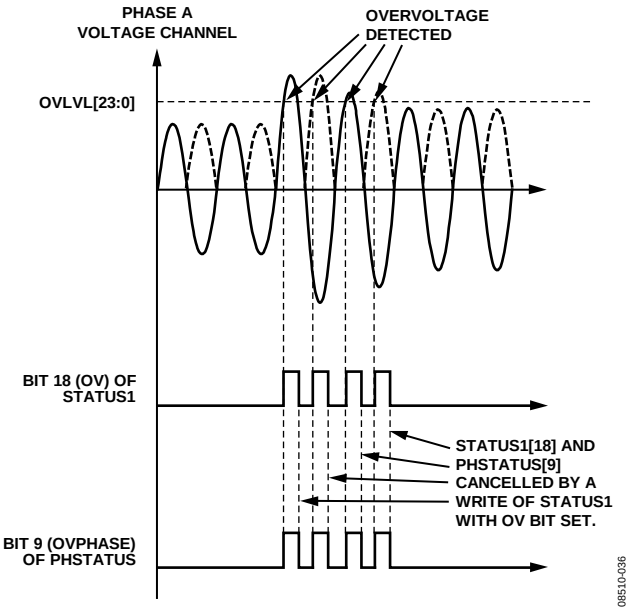

Figure 52. Overvoltage Detection

Whenever the absolute instantaneous value of the voltage goes above the threshold from the OVLVL register, Bit 18 (OV) in the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are set to 1. Bit 18 (OV) of the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are cancelled when the STATUS1 register is written with Bit 18 (OV) set to 1.

The recommended procedure to manage overvoltage events is the following:

1. Enable OV interrupts in the MASK1 register by setting Bit 18 (OV) to 1.
2. When an overvoltage event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low.
3. The STATUS1 register is read with Bit 18 (OV) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases an overvoltage event happened.

Downloaded from Arrow.com.

5. The STATUS1 register is written with Bit 18 (OV) set to 1. In this moment, Bit OV is erased and also all Bits[11:9] (OVPHASE[2:0]) of the PHSTATUS register.

In case of an overcurrent event, if Bit 17 (OI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. Immediately, Bit 17 (OI) in the STATUS1 register and one of Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register, which identify the phase that generated the interrupt, are set. To find the phase that triggered the interrupt, the PHSTATUS register is read immediately after reading the STATUS1 register. Next, Status Bit 17 (OI) in the STATUS1 register and Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register are cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1. The process is similar with overvoltage detection.

Overvoltage and Overcurrent Level Set

The content of the overvoltage (OVLVL), and overcurrent, (OILVL) 24-bit unsigned registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is the maximum value of the HPF outputs: +5,928,256 (0x5A7540). When the OVLVL or OILVL register is equal to this value, the overvoltage or overcurrent conditions are never detected. Writing 0x0 to these registers signifies the overvoltage or overcurrent conditions are continuously detected, and the corresponding interrupts are permanently triggered.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 36, OILVL and OVLVL registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

Neutral Current Mismatch—ADE7868, ADE7878

Neutral current mismatch is available in the ADE7868 and ADE7878 only. In 3-phase systems, the neutral current is equal to the algebraic sum of the phase currents

$$I_N(t) = I_A(t) + I_B(t) + I_C(t)$$

If there is a mismatch between these two quantities, then a tamper situation may have occurred in the system.

The ADE7868/ADE7878 compute the sum of the phase currents adding the content of the IAWV, IBWV, and ICWV registers, and storing the result into the ISUM 28-bit signed register: $I_{SUM}(t) = I_A(t) + I_B(t) + I_C(t)$. ISUM is computed every 125 µs (8 kHz frequency), the rate at which the current samples are available, and Bit 17 (DREADY) in the STATUS0 register is used to signal when the ISUM register can be read. See the Digital Signal Processor section for more details on Bit DREADY.

To recover $I_{SUM}(t)$ value from the ISUM register, use the following expression:

$$I_{SUM}(t) = \frac{ISUM[27:0]}{ADC_{MAX}} \times I_{FS}$$

where:

ADC_{MAX} = 5,928,256, the ADC output when the input is at full scale.
I_{FS} is the full-scale ADC phase current.

The ADE7868/ADE7878 compute the difference between the absolute values of ISUM and the neutral current from the INWV register, take its absolute value and compare it against the ISUMLVL threshold. If $\left||ISUM| - |INWV|\right| \le ISUMLVL$, then it is assumed that the neutral current is equal to the sum of the phase currents, and the system functions correctly. If $\left||ISUM| - |INWV|\right| > ISUMLVL$, then a tamper situation may have occurred, and Bit 20 (MISMTCH) in the STATUS1 register is set to 1. An interrupt attached to the flag can be enabled by setting Bit 20 (MISMTCH) in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low when Status Bit MISMTCH is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with Bit 20 (MISMTCH) set to 1.

If $\left||ISUM| - |INWV|\right| \le ISUMLVL$, then $MISMTCH = 0$

If $\left||ISUM| - |INWV|\right| > ISUMLVL$, then $MISMTCH = 1$

ISUMLVL, the positive threshold used in the process, is a 24-bit signed register. Because it is used in a comparison with an absolute value, always set ISUMLVL as a positive number, somewhere between 0x00000 and 0x7FFFFF. ISUMLVL uses the same scale of the current ADCs outputs, so writing +5,928,256 (0x5A7540) to the ISUMLVL register puts the mismatch detection level at full scale; see the Current Channel ADC section for details. Writing 0x000000, the default value, or a negative value, signifies the MISMTCH event is always triggered. The right value for the application should be written into the ISUMLVL register after power-up or after a hardware/software reset to avoid continuously triggering MISMTCH events.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7868/ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. As presented in Figure 53, ISUM, the 28-bit signed register, is accessed as a 32-bit register with the four most significant bits padded with 0s.

Figure 53. The ISUM[27:0] Register is Transmitted As a 32-Bit Word

Similar to the registers presented in Figure 35, the ISUMLVL register is accessed as a 32-bit register with four most significant bits padded with 0s and sign extended to 28 bits.

PHASE COMPENSATION

As described in the Current Channel ADC and Voltage Channel ADC sections, the datapath for both current and voltages is the same. The phase error between current and voltage signals introduced by the ADE7854/ADE7858/ADE7868/ADE7878 is negligible. However, the ADE7854/ADE7858/ADE7868/ADE7878 must work with transducers that may have inherent

Downloaded from Arrow.com.

phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE78xx provides a means of digitally calibrating these small phase errors. The ADE78xx allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are 10-bit registers that can vary the time advance in the voltage channel signal path from −374.0 µs to +61.5 µs. Negative values written to the PHCAL registers represent a time advance whereas positive values represent a time delay. One LSB is equivalent to 0.976 µs of time delay or time advance (clock rate of 1.024 MHz). With a line frequency of 60 Hz, this gives a phase resolution of 0.0211° (360° × 60 Hz/1.024 MHz) at the fundamental. This corresponds to a total correction range of −8.079° to +1.329° at 60 Hz. At 50 Hz, the correction range is −6.732° to +1.107° and the resolution is 0.0176° (360° × 50 Hz/1.024 MHz).

Given a phase error of x degrees, measured using the phase voltage as the reference, the corresponding LSBs are computed dividing x by the phase resolution (0.0211°/LSB for 60 Hz and 0.0176°/LSB for 50 Hz). Results between −383 and +63 only are acceptable; numbers outside this range are not accepted. If the current leads the voltage, the result is negative and the absolute value is written into the PHCAL registers. If the current lags the voltage, the result is positive and 512 is added to the result before writing it into xPHCAL.

$$APHCAL,\ BPHCAL,\ \text{or}\ CPHCAL = \begin{cases} \left|\dfrac{x}{phase_resolution}\right|, x \le 0 \\ \dfrac{x}{phase_resolution} + 512, x > 0 \end{cases} \quad (8)$$

Figure 55 illustrates how the phase compensation is used to remove x = −1° phase lead in IA of the current channel from the external current transducer (equivalent of 55.5 µs for 50 Hz systems). To cancel the lead (1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. Using Equation 8, APHCAL is 57 least significant bits, rounded up from 56.8. The phase lead is achieved by introducing a time delay of 55.73 µs into the Phase A current.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. As shown in Figure 54, APHCAL, BPHCAL, and CPHCAL 10-bit registers are accessed as 16-bit registers with the six MSBs padded with 0s.

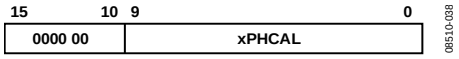

Figure 54. xPHCAL Registers Communicated As 16-Bit Registers

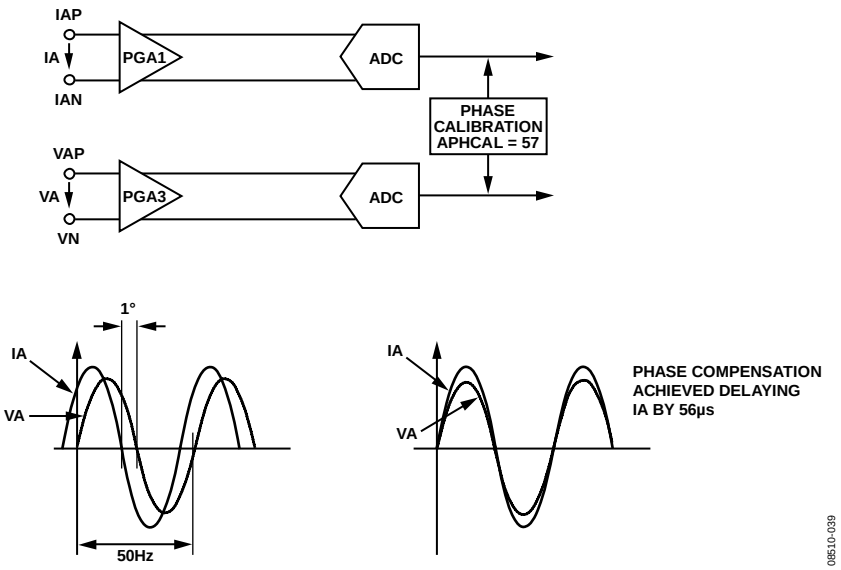

Figure 55. Phase Calibration on Voltage Channels

Downloaded from Arrow.com.

REFERENCE CIRCUIT

The nominal reference voltage at the $REF_{IN/OUT}$ pin is 1.2 V. This is the reference voltage for the ADCs in the ADE7854/ADE7858/ADE7868/ADE7878. Use a typical external reference voltage of 1.2 V to overdrive the $REF_{IN/OUT}$ pin. The temperature coefficient of the internal voltage reference is calculated based on the endpoint method. To calculate the drift over temperature, the values of the voltage reference at endpoints (−40°C and +85°C) are measured and compared to the reference value at 25°C, which in turn provides the slope of the temperature coefficient curve. Figure 56 is a typical representation of the drift over temperature. It contains two curves: Curve X and Curve Y, which are typical representations of two possible curvatures that are observed over the entire specified temperature range.

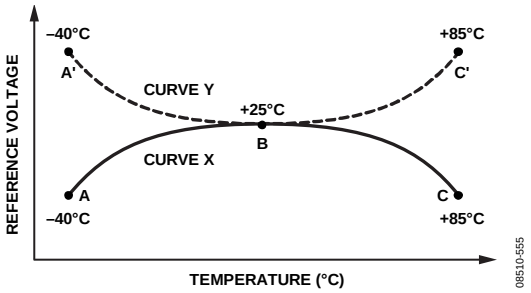

Figure 56. Internal Voltage Reference Temperature Drift

Figure 56 shows that independent consideration of two regions is necessary for accurate analysis of the drift over temperature, as follows:

- Considering the region between Point A and Point B in Curve X, the reference value increases with an increase in temperature; thus, the curve has a positive slope from A to B. This results in a positive temperature coefficient in this region.
- Considering the region between Point B and Point C in Curve X, the slope of the curve is negative because the voltage reference decreases with an increase in temperature; thus, this region of the curve has a negative temperature coefficient.
- Based on similar logic, Curve Y has a negative temperature coefficient between Point A' and PointB and a positive temperature coefficient between Point B and PointC'.

The drift curve on any particular IC can be matched with either of these sample curves. The general relationship between the absolute value of the voltage reference at a particular endpoint temperature and the temperature coefficient for that region of the curve is explained by the following two equations:

$$V_{REF\ (-40°C)} = V_{REF\ (+25°C)} \times \left(1 + \frac{\alpha_c(-40°C - 25°C)}{10^6}\right)$$

$$V_{REF\ (85°C)} = V_{REF\ (25°C)} \times \left(1 + \frac{\alpha_h(85°C - 25°C)}{10^6}\right)$$

where α_c and α_h are cold and hot temperature coefficients, respectively, calculated by

$$\alpha_c = \frac{\frac{V_{REF(-40°C)} - V_{REF(+25°C)}}{V_{REF(+25°C)}}}{(-40°C - 25°C)} \times 10^6 \text{ ppm/°C}$$

$$\alpha_h = \frac{\frac{V_{REF(85°C)} - V_{REF(25°C)}}{V_{REF(25°C)}}}{(85°C - 25°C)} \times 10^6 \text{ ppm/°C}$$

As the sign of cold and hot temperature coefficients can vary from one IC to another, the typical drift is specified for the whole range with a plus-minus sign(±). To find the typical, minimum and maximum temperature coefficients, as listed in the Specifications section, data based on the end-point method is collected on ICs spread out over different lots. The minimum and maximum temperature coefficents denote that the drift of any particular IC will be within those limits, over the specified temperature range, with reference to 25°C. See Figure 57 and Figure 58 for the device-to-device variation of the drift.

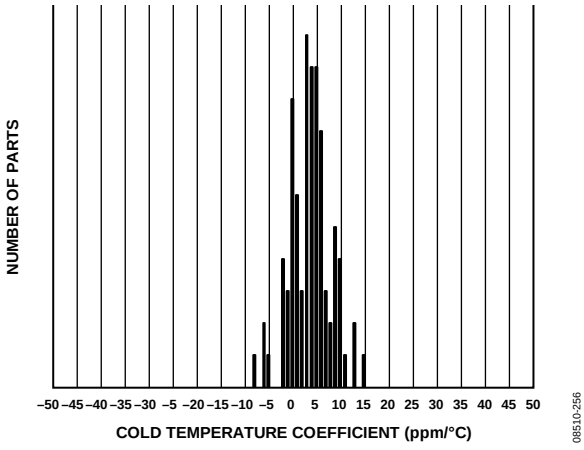

Figure 57. Histogram of the Reference Drift from −40°C to +25°C

Downloaded from Arrow.com.

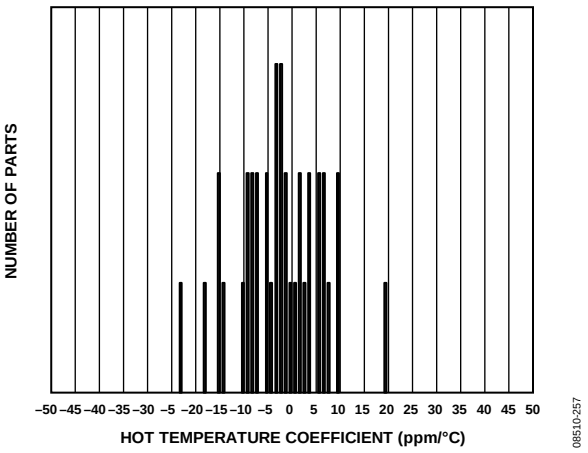

Figure 58. Histogram of the Reference Drift from 25°C to 85°C

Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and, typically, much smaller than the drift of other components on a meter.

The ADE7854/ADE7858/ADE7868/ADE7878 use the internal voltage reference when Bit 0 (EXTREFEN) in the CONFIG2 register is cleared to 0 (the default value); the external voltage reference is used when the bit is set to 1. Set the CONFIG2 register during the PSM0 mode; its value is maintained during the PSM1, PSM2, and PSM3 power modes.

DIGITAL SIGNAL PROCESSOR

The ADE7854/ADE7858/ADE7868/ADE7878 contain a fixed function digital signal processor (DSP) that computes all powers and rms values. It contains program memory ROM and data memory RAM.

The program used for the power and rms computations is stored in the program memory ROM and the processor executes it every 8 kHz. The end of the computations is signaled by setting Bit 17 (DREADY) to 1 in the STATUS0 register. An interrupt attached to this flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and Status Bit DREADY is set to 1 at the end of the computations. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with Bit 17 (DREADY) set to 1.

The registers used by the DSP are located in the data memory RAM, at addresses between 0x4380 and 0x43BE. The width of this memory is 28 bits. Within the DSP core, the DSP contains a two stage pipeline. This means that when a single register needs to be initialized, two more writes are required to ensure the value has been written into RAM, and if two or more registers need to be initialized, the last register must be written two more times to ensure the value has been written into RAM.

As explained in the Power-Up Procedure section, at power-up or after a hardware or software reset, the DSP is in idle mode. No instruction is executed. All the registers located in the data memory RAM are initialized at 0, their default values, and they can be read/written without any restriction. The run register, used to start and stop the DSP, is cleared to 0x0000. The run register needs to be written with 0x0001 for the DSP to start code execution.

To protect the integrity of the data stored in the data memory RAM of the DSP (addresses between 0x4380 and 0x43BE), a write protection mechanism is available. By default, the protection is disabled and registers placed between 0x4380 and 0x43BE can be written without restriction. When the protection is enabled, no writes to these registers is allowed. Registers can be always read, without restriction, independent of the write protection state.

To enable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.

It is recommended to enable the write protection after the registers have been initialized. If any data memory RAM based register needs to be changed, simply disable the protection, change the value and then re-enable the protection. There is no need to stop the DSP to change these registers.

To disable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3.

The recommended procedure to initialize the ADE7854/ADE7858/ADE7868/ADE7878 registers at power up is as follows:

- Initialize the AIGAIN, BIGAIN, CIGAIN, and NIGAIN registers.
- Start the DSP by setting run = 1.
- Initialize all the other data memory RAM registers. Write the last register in the queue three times to ensure its value was written into the RAM. Initialize all of the other ADE7854/ADE7858/ADE7868/ADE7878 registers with the exception of the CFMODE register.
- Read the energy registers xWATTHR, xFWATTHR, xVARHR, xFVARHR, and xVAHR to erase their content and start energy accumulation from a known state.
- Clear Bit 9 (CF1DIS), Bit 10 (CF2DIS), and Bit 11 (CF3DIS) in the CFMODE register to enable pulses at the CF1, CF2, and CF3 pins. Do this initialization last, so no spurious pulses are generated while the ADE7854/ADE7858/ADE7868/ADE7878 are initialized.
- Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
- Read back all data memory RAM registers to ensure they were initialized with the desired values.
- In the remote case that one or more registers are not initialized correctly, disable the protection by writing 0xAD to

Downloaded from Arrow.com.

an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. Reinitialize the registers. Write the last register in the queue three times. Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.

There is no obvious reason to stop the DSP if the ADE78xx is maintained in PSM0 normal mode. All ADE78xx registers, including ones located in the data memory RAM, can be modified without stopping the DSP. However, to stop the DSP, 0x0000 has to be written into run register. To restart the DSP, one of the following procedures must be followed:

- If the ADE7854/ADE7858/ADE7868/ADE7878 registers located in the data memory RAM have not been modified, write 0x0001 into the run register to start the DSP.
- If the ADE7854/ADE7858/ADE7868/ADE7878 registers located in the data memory RAM have to be modified, first execute a software or a hardware reset, and then follow the recommended procedure to initialize the registers at power up.

As mentioned in the Power Management section, when the ADE7854/ADE7858/ADE7868/ADE7878 switch out of PSM0 power mode, it is recommended to stop the DSP by writing 0x0000 into the run register (see Figure 11 and Table 12 for the recommended actions when changing power modes).

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal f(t) is defined as

$$F\,rms = \sqrt{\frac{1}{t}\int_0^t f^2(t)dt} \quad (9)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$F\,rms = \sqrt{\frac{1}{N}\sum_{N=1}^{N} f^2[n]} \quad (10)$$

Equation 10 implies that for signals containing harmonics, the rms calculation contains the contribution of all harmonics, not only the fundamental. The ADE78xx uses two different methods to calculate rms values. The first one is very accurate and is active only in PSM0 mode. The second one is less accurate, uses the estimation of the mean absolute value (mav) measurement, is active in PSM0 and PSM1 modes, and is available for the ADE7868 and ADE7878 only.

The first method is to low-pass filter the square of the input signal (LPF) and take the square root of the result (see Figure 59).

$$f(t) = \sum_{k=1}^{\infty} F_k \sqrt{2}\sin(k\omega t + \gamma_k) \quad (11)$$

Then

$$f^2(t) = \sum_{k=1}^{\infty} F_k^2 - \sum_{k=1}^{\infty} F_k^2 \cos(2k\omega t + 2\gamma_k) + \\ + 2\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} 2 \times F_k \times F_m \sin(k\omega t + \gamma_k) \times \sin(m\omega t + \gamma_m) \quad (12)$$

After the LPF and the execution of the square root, the rms value of f(t) is obtained by

$$F = \sqrt{\sum_{k=1}^{\infty} F_k^2} \quad (13)$$

The rms calculation based on this method is simultaneously processed on all seven analog input channels. Each result is available in the 24-bit registers: AIRMS, BIRMS, CIRMS, AVRMS, BVRMS, CVRMS, and NIRMS (NIRMS is available on the ADE7868 and ADE7878 only).

The second method computes the absolute value of the input signal and then filters it to extract its dc component. It computes the absolute mean value of the input. If the input signal in Equation 12 has a fundamental component only, its average value is

$$F_{DC} = \frac{1}{T}\left[\int_0^{\frac{T}{2}} \sqrt{2} \times F_1 \times \sin(\omega t)dt - \int_{\frac{T}{2}}^{T} \sqrt{2} \times F_1 \times \sin(\omega t)dt\right]$$

$$F_{DC} = \frac{2}{\pi} \times \sqrt{2} \times F_1$$

The calculation based on this method is simultaneously processed only on the three phase currents. Each result is available in the 20-bit registers, which are available on the ADE7868 and ADE7878 only: AIMAV, BMAV, and CMAV. Note that the proportionality between mav and rms values is maintained for the fundamental components only. If harmonics are present in the current channel, the mean absolute value is no longer proportional to rms.

Current RMS Calculation

This section presents the first approach to compute the rms values of all phase and neutral currents.

Figure 59 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel. The current rms values are signed 24-bit values and they are stored into the AIRMS, BIRMS, CIRMS, and NIRMS (ADE7868/ADE7878 only) registers. The update rate of the current rms measurement is 8 kHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal is 4,191,910 (0x3FF6A6), independent of the line frequency. If

Downloaded from Arrow.com.

the integrator is enabled, that is, when Bit 0 (INTEN) in the CONFIG register is set to 1, the equivalent rms value of a full-scale sinusoidal signal at 50 Hz is 4,191,910 (0x3FF6A6) and at 60 Hz is 3,493,258 (0x354D8A).

The accuracy of the current rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input when PGA = 1. Additionally, this measurement has a bandwidth of 2 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section). Table 13 shows the settling time for the I rms measurement, which is the time it takes for the rms register to reflect the value at the input to the current channel when starting from 0 to full scale. However, during the chip power-up and DSP reset cases, it would typically take about 1.2 seconds for a FS/1000 signal to be settled.

Table 13. Settling Time for I rms Measurement

Integrator Status	50 Hz Input signals	60 Hz Input signals
Integrator Off	440 ms	440 ms
Integrator On	550 ms	500 ms

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 36, the AIRMS, BIRMS, CIRMS, and NIRMS (ADE7868 and ADE7878 only) 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

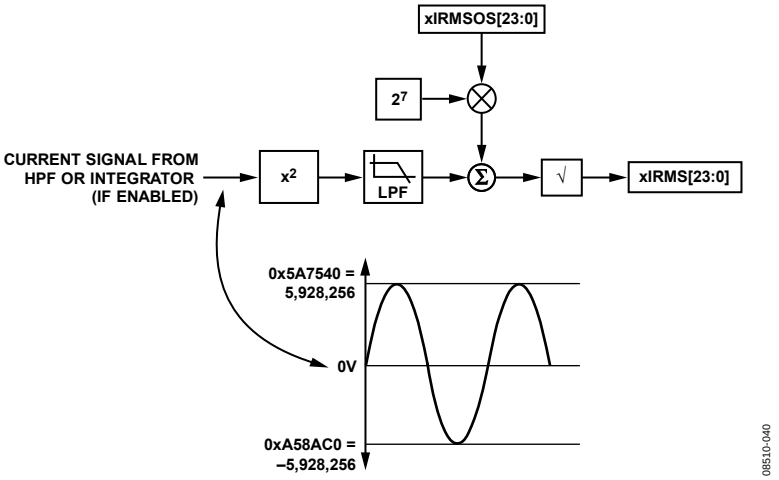

Figure 59. Current RMS Signal Processing

Downloaded from Arrow.com.

Current RMS Offset Compensation

The ADE7854/ADE7858/ADE7868/ADE7878 incorporate a current rms offset compensation register for each phase: AIRMSOS, BIRMSOS, CIRMSOS registers, and the NIRMSOS register for ADE7868 and ADE7878 only. These are 24-bit signed registers that are used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $I^2(t)$. The current rms offset register is multiplied by 128 and added to the squared current rms before the square root is executed. Assuming that the maximum value from the current rms calculation is 4,191,910 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00037% ($(\sqrt{4191^2+128}/4191 - 1) \times 100$) of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using currents equal to zero for this purpose.

$$I\,rms = \sqrt{I\,rms_0^2 + 128 \times IRMSOS} \quad (14)$$

where $I\,rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the register presented in Figure 35, the AIRMSOS, BIRMSOS, CIRMSOS, and NIRMSOS (ADE7868/ADE7878 only) 24-bit signed registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only

This section presents the second approach to estimate the rms values of all phase currents using the mean absolute value (mav) method. This approach is used in PSM1 mode, which is available to the ADE7868 and ADE7878 only, to allow energy accumulation based on current rms values when the missing neutral case demonstrates to be a tamper attack. This datapath is active also in PSM0 mode to allow for its gain calibration. The gain is used in the external microprocessor during PSM1 mode. The mav value of the neutral current is not computed using this method. Figure 60 shows the details of the signal processing chain for the mav calculation on one of the phases of the current channel.

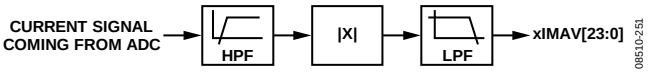

Figure 60. Current MAV Signal Processing for PSM1 Mode

The current channel mav value is processed from the samples used in the current channel waveform sampling mode. The samples are passed through a high-pass filter to eliminate the eventual dc offsets introduced by the ADCs and the absolute values are computed. The outputs of this block are then filtered to obtain the average. The current mav values are unsigned 20-bit values and they are stored in the AIMAV, BIMAV, and CIMAV registers. The update rate of this mav measurement is 8 kHz.

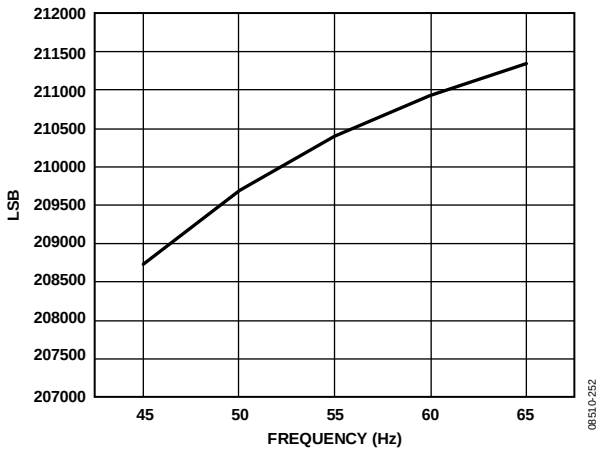

Figure 61. xIMAV Register Values at Full Scale, 45 Hz to 65 Hz Line Frequencies

The mav values of full-scale sinusoidal signals of 50 Hz and 60 Hz are 209,686 and 210,921, respectively. As seen in Figure 61, there is a 1.25% variation between the mav estimate at 45 Hz and the one at 65 Hz for full-scale sinusoidal inputs. The accuracy of the current mav is typically 0.5% error from the full-scale input down to 1/100 of the full-scale input. Additionally, this measurement has a bandwidth of 2 kHz. The settling time for the current mav measurement, that is the time it takes for the mav register to reflect the value at the input to the current channel within 0.5% error, is 500 ms. However, during the first measurement after entering this mode, it takes a longer time to settle to the correct value.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7868/ADE7878 work on 32-, 16-, or 8-bit words. As presented in Figure 62, the AIMAV, BIMAV, and CIMAV 20-bit unsigned registers are accessed as 32-bit registers with the 12 MSBs padded with 0s.

Figure 62. xIMAV Registers Transmitted as 32-Bit Registers

Current MAV Gain and Offset Compensation

The current rms values stored in the AIMAV, BIMAV, and CIMAV registers can be calibrated using gain and offset coefficients corresponding to each phase. It is recommended to calculate the gains in PSM0 mode by supplying the ADE7868/ADE7878 with nominal currents. The offsets can be estimated by supplying the ADE7868/ADE7878 with low currents, usually equal to the minimum value at which the accuracy is required. Every time the external microcontroller reads the AIMAV,

BIMAV, and CIMAV registers, it uses these coefficients stored in its memory to correct them.

Voltage Channel RMS Calculation

Figure 63 shows the detail of the signal processing chain for the rms calculation on one of the phases of the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel. The voltage rms values are signed 24-bit

Downloaded from Arrow.com.

values and they are stored into the Registers AVRMS, BVRMS, and CVRMS. The update rate of the current rms measurement is 8 kHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,928,256. The equivalent rms value of a full-scale sinusoidal signal is 4,191,910 (0x3FF6A6), independent of the line frequency.

The accuracy of the voltage rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 2 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The $\overline{\text{IRQ1}}$ interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

The settling time for the V rms measurement is 440 ms for both 50 Hz and 60 Hz input signals. The V rms measurement settling time is the time it takes for the rms register to reflect the value at the input to the voltage channel when starting from 0.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 36, the AVRMS, BVRMS, and CVRMS 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

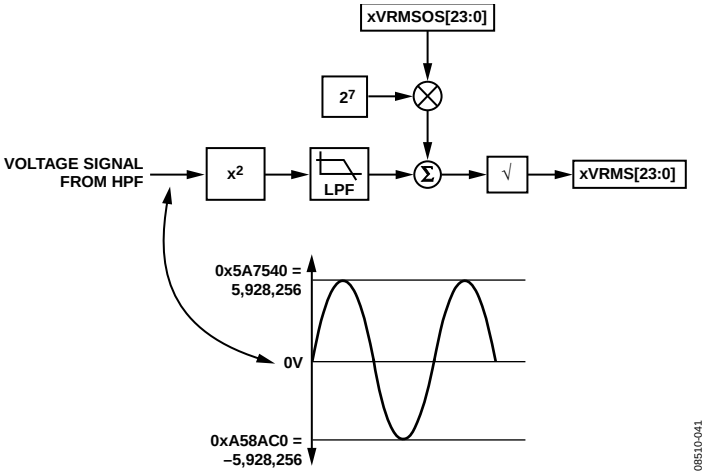

Figure 63. Voltage RMS Signal Processing

Downloaded from Arrow.com.

Voltage RMS Offset Compensation

The ADE78xx incorporates voltage rms offset compensation registers for each phase: AVRMSOS, BVRMSOS, and CVRMSOS. These are 24-bit signed registers used to remove offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The voltage rms offset register is multiplied by 128 and added to the squared current rms before the square root is executed. Assuming that the maximum value from the voltage rms calculation is 4,191,910 with full-scale ac inputs (50 Hz), one LSB of the voltage rms offset represents 0.00037% ($((\sqrt{4191^2+128}/4191-1)\times 100)$ of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using voltages equal to zero for this purpose.

$$V\ rms = \sqrt{V\ rms_0^2 + 128 \times VRMSOS} \quad (15)$$

where $V\ rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 35, the AVRMSOS, BVRMSOS, and CVRMSOS 24-bit registers are accessed as 32-bit registers with the four most significant bits padded with 0s and sign extended to 28 bits.

ACTIVE POWER CALCULATION

The ADE7854/ADE7858/ADE7868/ADE7878 compute the total active power on every phase. Total active power considers in its calculation all fundamental and harmonic components of the voltages and currents. In addition, the ADE7878 computes the fundamental active power, the power determined only by the fundamental components of the voltages and currents.

Total Active Power Calculation

Electrical power is defined as the rate of energy flow from source to load, and it is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. If an ac system is supplied by a voltage, v(t), and consumes the current, i(t), and each of them contains harmonics, then

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin(k\omega t + \varphi_k) \quad (16)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin(k\omega t + \gamma_k)$$

where:
V_k, I_k are rms voltage and current, respectively, of each harmonic.
φ_k, γ_k are the phase delays of each harmonic.

The instantaneous power in an ac system is

$$p(t) = v(t) \times i(t) = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) - \sum_{k=1}^{\infty} V_k I_k \cos(2k\omega t + \varphi_k + \gamma_k) + \sum_{\substack{k,\ m=1 \\ k \neq m}}^{\infty} V_k I_m \{\cos[(k-m)\omega t + \varphi_k - \gamma_m] - \cos[(k+m)\omega t + \varphi_k + \gamma_m]\} \quad (17)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 18.

$$P = \frac{1}{nT} \int_0^{nT} p(t)dt = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (18)$$

where:
T is the line cycle period.
P is referred to as the total active or total real power.

Note that the total active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 17, that is,

$$\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k)$$

This is the expression used to calculate the total active power in the ADE78xx for each phase. The expression of fundamental active power is obtained from Equation 18 with k = 1, as follows:

$$FP = V_1 I_1 \cos(\varphi_1 - \gamma_1) \quad (19)$$

Figure 64 shows how the ADE78xx computes the total active power on each phase. First, it multiplies the current and voltage signals in each phase. Next, it extracts the dc component of the instantaneous power signal in each phase (A, B, and C) using LPF2, the low-pass filter.

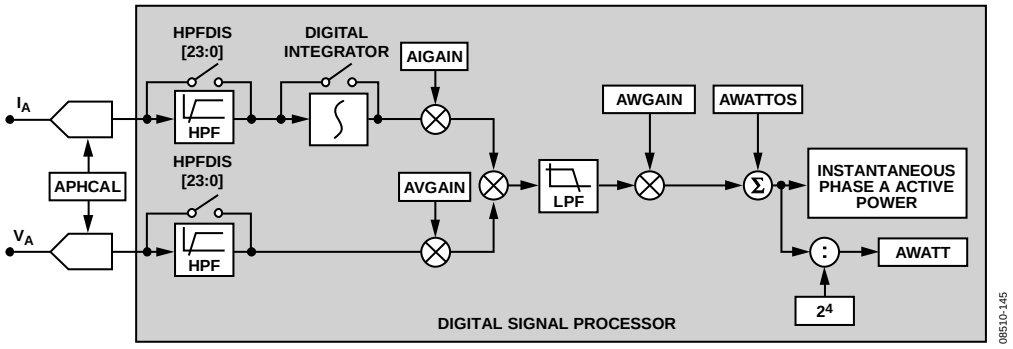

Figure 64. Total Active Power Datapath

Downloaded from Arrow.com.

If the phase currents and voltages contain only the fundamental component, are in phase (that is $\varphi_1 = \gamma_1 = 0$), and they correspond to full-scale ADC inputs, then multiplying them results in an instantaneous power signal that has a dc component, $V_1 \times I_1$, and a sinusoidal component, $V_1 \times I_1 \cos(2\omega t)$; Figure 65 shows the corresponding waveforms.

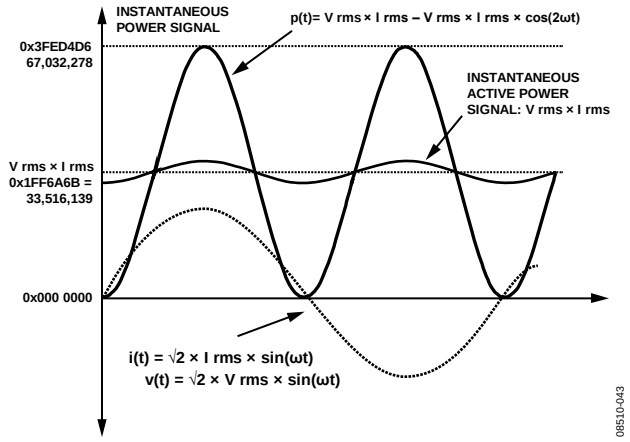

Figure 65. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response (see Figure 66), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy.

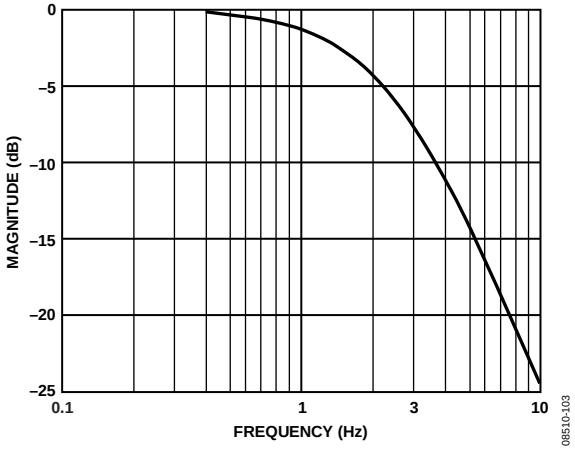

Figure 66. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase

The ADE7854/ADE7858/ADE7868/ADE7878 store the instantaneous total phase active powers into the AWATT, BWATT, and CWATT registers. Their expression is

$$xWATT = \sum_{k=1}^{\infty} \frac{V_k}{V_{FS}} \times \frac{I_k}{I_{FS}} \times \cos(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (20)$$

where:
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.

PMAX = 33,516,139; it is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xWATT[23:0] waveform registers can be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

Fundamental Active Power Calculation—ADE7878 Only

The ADE7878 computes the fundamental active power using a proprietary algorithm that requires some initializations function of the frequency of the network and its nominal voltage measured in the voltage channel. Bit 14 (SELFREQ) in the COMPMODE register must be set according to the frequency of the network in which the ADE7878 is connected. If the network frequency is 50 Hz, clear this bit to 0 (the default value). If the network frequency is 60 Hz, set this bit to 1. In addition, initialize the VLEVEL 24-bit signed register with a positive value based on the following expression:

$$VLEVEL = \frac{V_{FS}}{V_n} \times 491{,}520 \quad (21)$$

where:
V_{FS} is the rms value of the phase voltages when the ADC inputs are at full scale.
V_n is the rms nominal value of the phase voltage.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 35, the VLEVEL 24-bit signed register is accessed as a 32-bit register with four most significant bits padded with 0s and sign extended to 28 bits.

Table 14 presents the settling time for the fundamental active power measurement.

Table 14. Settling Time for Fundamental Active Power

Input Signals	
63% Full Scale	**100% Full Scale**
375 ms	875 ms

Active Power Gain Calibration

Note that the average active power result from the LPF2 output in each phase can be scaled by ±100% by writing to the phase's watt gain 24-bit register (AWGAIN, BWGAIN, CWGAIN, AFWGAIN, BFWGAIN, or CFWGAIN). The xWGAIN registers are placed in each phase of the total active power datapath, and the xFWGAIN (available for the ADE7878 only) registers are placed in each phase of the fundamental active power datapath. The watt gain registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. Equation 22 describes mathematically the function of the watt gain registers.

$$Average\ Power\ Data = LPF2\ Output \times \left(1 + \frac{Watt\ Gain\ Register}{2^{23}}\right) \quad (22)$$

Downloaded from Arrow.com.

The output is scaled by −50% by writing 0xC00000 to the watt gain registers, and it is increased by +50% by writing 0x400000 to them. These registers are used to calibrate the active power (or energy) calculation in the ADE7854/ADE7858/ADE7868/ADE7878for each phase.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. Similar to registers presented in Figure 35, AWGAIN, BWGAIN, CWGAIN, AFWGAIN, BFWGAIN, and CFWGAIN 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Active Power Offset Calibration

The ADE7854/ADE7858/ADE7868/ADE7878 incorporate a watt offset 24-bit register on each phase and on each active power. The AWATTOS, BWATTOS, and CWATTOS registers compensate the offsets in the total active power calculations, and the AFWATTOS, BFWATTOS, and CFWATTOS registers compensate offsets in the fundamental active power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the LPF2 output is PMAX = 33,516,139. At −80 dB down from the full scale (active power scaled down 10^4 times), one LSB of the active power offset register represents 0.0298% of PMAX.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 35, the AWATTOS, BWATTOS, CWATTOS, AFWATTOS, BFWATTOS, and CFWATTOS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Sign of Active Power Calculation

The average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being injected back on the grid. The ADE78xx has sign detection circuitry for active power calculations. It can monitor the total active powers or the fundamental active powers. As described in the Active Energy Calculation section, the active energy accumulation is performed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the WTHR register threshold, a dedicated interrupt is triggered. The sign of each phase active power can be read in the PHSIGN register.

Bit 6 (REVAPSEL) in the ACCMODE register sets the type of active power being monitored. When REVAPSEL is 0, the default value, the total active power is monitored. When REVAPSEL is 1, the fundamental active power is monitored.

Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register are set when a sign change occurs in the power selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Bits[2:0] (CWSIGN, BWSIGN, and AWSIGN, respectively) in the PHSIGN register are set simultaneously with the REVAPC, REVAPB, and REVAPA bits. They indicate the sign of the power. When they are 0, the corresponding power is positive. When they are 1, the corresponding power is negative.

Bit REVAPx of STATUS0 and Bit xWSIGN in the PHSIGN register refer to the total active power of Phase x, the power type being selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Interrupts attached to Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register can be enabled by setting Bits[8:6] in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is returned to high by writing to the STATUS0 register with the corresponding bit set to 1.

Active Energy Calculation

As previously stated, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$Power = \frac{dEnergy}{dt} \quad (23)$$

Conversely, energy is given as the integral of power, as follows:

$$Energy = \int p(t)dt \quad (24)$$

Total and fundamental active energy accumulations are always signed operations. Negative energy is subtracted from the active energy contents.

Downloaded from Arrow.com.

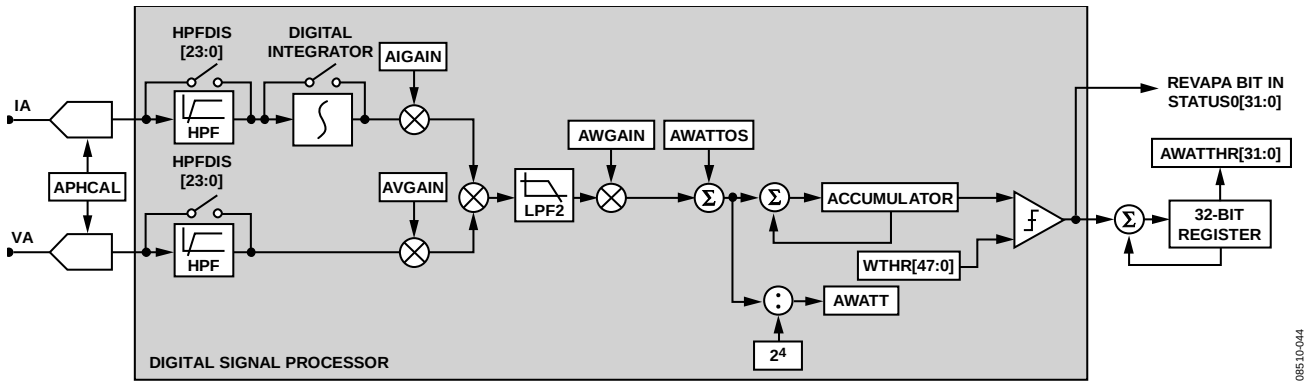

Figure 67. Total Active Energy Accumulation

The ADE7854/ADE7858/ADE7868/ADE7878 achieve the integration of the active power signal in two stages (see Figure 67). The process is identical for both total and fundamental active powers. The first stage is accomplished inside the DSP: every 125 µs (8 kHz frequency) the instantaneous phase total or fundamental active power is accumulated into an internal register. When a threshold is reached, a pulse is generated at the processor port, and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the active power (see Sign of Active Power Calculation section for details). The second stage is done outside the DSP and consists of accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to watt-hour registers, xWATTHR and xFWATTHR, when these registers are accessed.

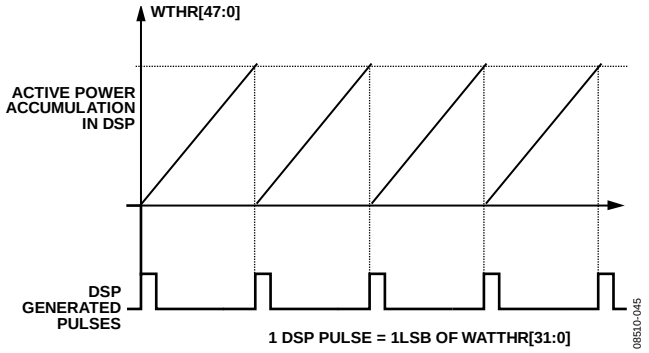

Figure 68. Active Power Accumulation Inside the DSP

Figure 68 explains this process. The WTHR 48-bit signed register contains the threshold. It is introduced by the user and is common for all phase total and fundamental active powers. Its value depends on how much energy is assigned to one LSB of watt-hour registers. When a derivative of active energy (wh) of [10^n wh], where n is an integer, is desired as one LSB of the xWATTHR register, then, the xWATTHR register can be computed using the following equation:

$$WTHR = \frac{PMAX \times f_S \times 3600 \times 10^n}{V_{FS} \times I_{FS}} \quad (25)$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B as the instantaneous power computed when the ADC inputs are at full scale.
f_S = 8 kHz, the frequency with which the DSP computes the instantaneous power.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The maximum value that can be written on WTHR is $2^{47} - 1$. The minimum value is 0x0, but it is recommended to write a number equal to or greater than PMAX. Never use negative numbers.

WTHR is a 48-bit register. As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878work on 32-, 16-, or 8-bit words. As shown in Figure 69, the WTHR register is accessed as two 32-bit registers (WTHR1 and WTHR0), each having eight MSBs padded with 0s.

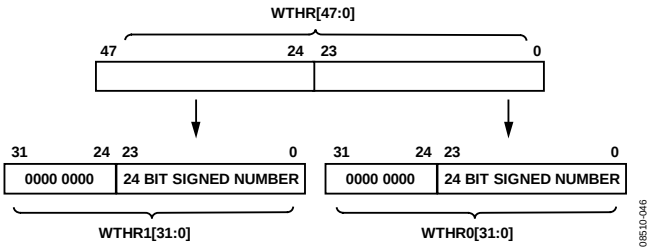

Figure 69. WTHR[47:0] Communicated As Two 32-Bit Registers

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation 26.

$$Energy = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (26)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7854/ADE7858/ADE7868/ADE7878, the total phase active powers are accumulated in the AWATTHR, BWATTHR, and CWATTHR 32-bit signed registers, and the fundamental phase active powers are accumulated in AFWATTHR, BFWATTHR, and

Downloaded from Arrow.com.

CFWATTHR 32-bit signed registers. The active energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues decreasing in value.

Bit 0 (AEHF) in the STATUS0 register is set when Bit 30 of one of the xWATTHR registers changes, signifying one of these registers is half full. If the active power is positive, the watt-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the active power is negative, the watt-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF. Similarly, Bit 1 (FAEHF) in STATUS0 register, is set when Bit 30 of one of the xFWATTHR registers changes, signifying one of these registers is half full.

Setting Bits[1:0] in the MASK0 register enable the FAEHF and AEHF interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xWATTHR (for the AEHF interrupt) or xFWATTHR (for the FAEHF interrupt), become half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to logic high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all watt-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 125 µs (8 kHz frequency). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x00000, the average word value from each LPF2 is PMAX = 33,516,139 = 0x1FF6A6B. If the WTHR register threshold is set at the PMAX level, this means the DSP generates a pulse that is added at watt-hour registers every 125 µs.

The maximum value that can be stored in the watt-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 125\ \mu s = 74\ hr\ 33\ min\ 55\ sec \quad (27)$$

Energy Accumulation Modes

The active power accumulated in each watt-hour accumulation 32-bit register (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) depends on the configuration of Bit 5 and Bit 4 (CONSEL bits) in the ACCMODE register. The various configurations are described in Table 15.

Table 15. Inputs to Watt-Hour Accumulation Registers

CONSEL	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × IA	0	VC × IC
10	VA × IA	VB × IB VB = –VA – VC	VC × IC
11	VA × IA	VB × IB VB = –VA	VC × IC

Depending on the polyphase meter service, choose the appropriate formula to calculate the active energy. The American ANSI C12.10 standard defines the different configurations of the meter. Table 16 describes which mode to choose in these various configurations.

Table 16. Meter Form Configuration

ANSI Meter Form	Configuration	CONSEL
5S/13S	3-wire delta	01
6S/14S	4-wire wye	10
8S/15S	4-wire delta	11
9S/16S	4-wire wye	00

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine how the CF frequency output can be generated as a function of the total and fundamental active powers. Whereas the watt-hour accumulation registers accumulate the active power in a signed format, the frequency output can be generated in signed mode or in absolute mode as a function of the WATTACC[1:0] bits. See the Energy-to-Frequency Conversion section for details.

Line Cycle Active Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation is synchronized to the voltage channel zero crossings such that active energy is accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation mode, the ADE7854/ADE7858/ADE7868/ADE7878 transfer the active energy accumulated in the 32-bit internal accumulation registers into the xWATTHR or xFWATTHR registers after an integral number of line cycles, as shown in Figure 70. The number of half line cycles is specified in the LINECYC register.

Downloaded from Arrow.com.

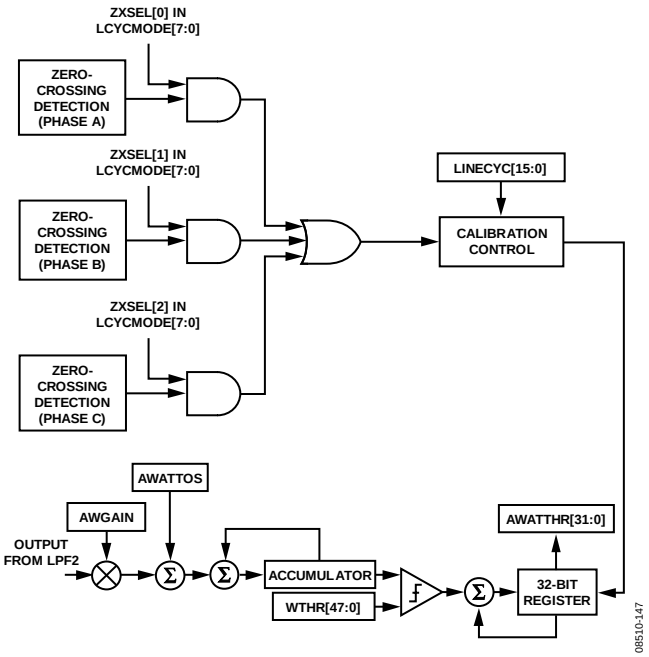

Figure 70. Line Cycle Active Energy Accumulation Mode

The line cycle energy accumulation mode is activated by setting Bit 0 (LWATT) in the LCYCMODE register. The energy accumulation over an integer number of half line cycles is written to the watt-hour accumulation registers after LINECYC number of half line cycles is detected. When using the line cycle accumulation mode, the Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because the read with reset of watt-hour registers is not available in this mode.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero crossings count during calibration.

The number of zero crossings is specified by the LINECYC 16-bit unsigned register. The ADE78xx can accumulate active power for up to 65,535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting Bit 0 (LWATT) in the LCYCMODE register, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC register when the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, Bit 5 (LENERGY) in the STATUS0 register is set. If the corresponding mask bit in the MASK0 interrupt mask register is enabled, the $\overline{\text{IRQ0}}$ pin also goes active low. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high again by writing to the STATUS0 register with the corresponding bit set to 1.

Because the active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal components are reduced to 0, eliminating any ripple in the energy calculation. Therefore, total energy accumulated using the line cycle accumulation mode is

$$e = \int_{t}^{t+nT} p(t)dt = nT\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (28)$$

where nT is the accumulation time.

Note that line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent.

REACTIVE POWER CALCULATION—ADE7858, ADE7868, ADE7878 ONLY

The ADE7858/ADE7868/ADE7878 can compute the total reactive power on every phase. Total reactive power integrates all fundamental and harmonic components of the voltages and currents. The ADE7878 also computes the fundamental reactive power, the power determined only by the fundamental components of the voltages and currents.

A load that contains a reactive element (inductor or capacitor) produces a phase difference between the applied ac voltage and the resulting current. The power associated with reactive elements is called reactive power, and its unit is VAR. Reactive power is defined as the product of the voltage and current waveforms when all harmonic components of one of these signals are phase shifted by 90°.

Equation 31 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2}\sin(k\omega t + \varphi_k) \quad (29)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2}\sin(k\omega t + \gamma_k) \quad (30)$$

$$i'(t) = \sum_{k=1}^{\infty} I_k \sqrt{2}\sin\left(k\omega t + \gamma_k + \frac{\pi}{2}\right)$$

where $i'(t)$ is the current waveform with all harmonic components phase shifted by 90°.

Next, the instantaneous reactive power, q(t), can be expressed as

$$q(t) = v(t) \times i'(t) \quad (31)$$

$$q(t) = \sum_{k=1}^{\infty} V_k I_k \times 2\sin(k\omega t + \varphi_k) \times \sin(k\omega t + \gamma_k + \frac{\pi}{2}) +$$

$$\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} V_k I_m \times 2\sin(k\omega t + \varphi_k) \times \sin(m\omega t + \gamma_m + \frac{\pi}{2})$$

Downloaded from Arrow.com.

Note that $q(t)$ can be rewritten as

$$q(t) = \sum_{k=1}^{\infty} V_k I_k \left\{\cos\left(\varphi_k - \gamma_k - \frac{\pi}{2}\right) - \cos\left(2k\omega t + \varphi_k + \gamma_k + \frac{\pi}{2}\right)\right\} + \sum_{\substack{k,m=1 \\ k \neq m}}^{\infty} V_k I_m \left\{\cos\left[(k-m)\omega t + \varphi_k - \gamma_k - \frac{\pi}{2}\right] - \cos\left[(k+m)\omega t + \varphi_k + \gamma_k + \frac{\pi}{2}\right]\right\} \quad (32)$$

The average total reactive power over an integral number of line cycles (n) is given by the expression in Equation 33.

$$Q = \frac{1}{nT}\int_0^{nT} q(t)dt = \sum_{k=1}^{\infty} V_k I_k \cos\left(\varphi_k - \gamma_k - \frac{\pi}{2}\right) \quad (33)$$

$$Q = \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k - \gamma_k)$$

where:
T is the period of the line cycle.
Q is referred to as the total reactive power. Note that the total reactive power is equal to the dc component of the instantaneous reactive power signal q(t) in Equation 32, that is,

$$\sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k - \gamma_k)$$

This is the relationship used to calculate the total reactive power in the ADE7858/ADE7868/ADE7878 for each phase. The instantaneous reactive power signal, q(t), is generated by multiplying each harmonic of the voltage signals by the 90° phase-shifted corresponding harmonic of the current in each phase.

The ADE7858/ADE7868/ADE7878 store the instantaneous total phase reactive powers into the AVAR, BVAR, and CVAR registers. Their expression is

$$xVAR = \sum_{k=1}^{\infty} \frac{V_k}{V_{FS}} \times \frac{I_k}{I_{FS}} \times \sin(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (34)$$

where:
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 33,516,139, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVAR waveform registers can be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

The expression of fundamental reactive power is obtained from Equation 33 with k = 1, as follows:

$$FQ = V_1 I_1 \sin(\varphi_1 - \gamma_1)$$

The ADE7878 computes the fundamental reactive power using a proprietary algorithm that requires some initialization function of the frequency of the network and its nominal voltage measured in the voltage channel. These initializations are introduced in the Active Power Calculation section and are common for both fundamental active and reactive powers.

Table 17 presents the settling time for the fundamental reactive power measurement, which is the time it takes the power to reflect the value at the input of the ADE7878.

Table 17. Settling Time for Fundamental Reactive Power

Input Signals	
63% Full Scale	**100% Full Scale**
375 ms	875 ms

Reactive Power Gain Calibration

The average reactive power in each phase can be scaled by ±100% by writing to one of the phase's VAR gain 24-bit registers (AVARGAIN, BVARGAIN, CVARGAIN, AFVARGAIN, BFVARGAIN, or CFVARGAIN). The xVARGAIN registers are placed in each phase of the total reactive power datapath. The xFVARGAIN registers are placed in each phase of the fundamental reactive power datapath. The xVARGAIN registers are twos complement signed registers and have a resolution of 2^{-23}/LSB. The function of the xVARGAIN registers is expressed by

$$Average\ Reactive\ Power = LPF2\,Output \times \left(1 + \frac{xVARGAIN\ Register}{2^{23}}\right) \quad (35)$$

The output is scaled by –50% by writing 0xC00000 to the xVARGAIN registers and increased by +50% by writing 0x400000 to them. These registers can be used to calibrate the reactive power (or energy) gain in the ADE78xx for each phase.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 35, the AVARGAIN, BVARGAIN, CVARGAIN, AFVARGAIN, BFVARGAIN, and CFVARGAIN 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Reactive Power Offset Calibration

The ADE7858/ADE7868/ADE7878 provide a reactive power offset register on each phase and on each reactive power. AVAROS, BVAROS, and CVAROS registers compensate the offsets in the total reactive power calculations, whereas AFVAROS, BFVAROS, and CFVAROS registers compensate offsets in the fundamental reactive power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the reactive power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset resolution of the registers is the same as for the active power offset registers (see the Active Power Offset Calibration section).

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 35, the AVAROS, BVAROS, and CVAROS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Downloaded from Arrow.com.

Sign of Reactive Power Calculation

Note that the reactive power is a signed calculation. Table 18 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting reactive power calculation.

The ADE7858/ADE7868/ADE7878 have sign detection circuitry for reactive power calculations that can monitor the total reactive powers or the fundamental reactive powers. As described in the Reactive Energy Calculation section, the reactive energy accumulation is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the VARTHR register threshold, a dedicated interrupt is triggered. The sign of each phase reactive power can be read in the PHSIGN register. Bit 7 (REVRPSEL) in the ACCMODE register sets the type of reactive power being monitored. When REVRPSEL is 0, the default value, the total reactive power is monitored. When REVRPSEL is 1, then the fundamental reactive power is monitored.

Bits[12:10] (REVRPC, REVRPB, and REVRPA, respectively) in the STATUS0 register are set when a sign change occurs in the power selected by Bit 7 (REVRPSEL) in the ACCMODE register.

Bits[6:4] (CVARSIGN, BVARSIGN, and AVARSIGN, respectively) in the PHSIGN register are set simultaneously with the REVRPC, REVRPB, and REVRPA bits. They indicate the sign of the reactive power. When they are 0, the reactive power is positive. When they are 1, the reactive power is negative.

Bit REVRPx of the STATUS0 register and Bit xVARSIGN in the PHSIGN register refer to the reactive power of Phase x, the power type being selected by Bit REVRPSEL in ACCMODE register.

Setting Bits[12:10] in the MASK0 register enables the REVRPC, REVRPB, and REVRPA interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Table 18. Sign of Reactive Power Calculation

Φ[1]	Integrator	Sign of Reactive Power
Between 0 to +180	Off	Positive
Between −180 to 0	Off	Negative
Between 0 to +180	On	Positive
Between −180 to 0	On	Negative

[1] Φ is defined as the phase angle of the voltage signal minus the current signal; that is, Φ is positive if the load is inductive and negative if the load is capacitive.

Reactive Energy Calculation

Reactive energy is defined as the integral of reactive power.

$$Reactive\ Energy = \int q(t)dt \quad (36)$$

Both total and fundamental reactive energy accumulations are always a signed operation. Negative energy is subtracted from the reactive energy contents.

Similar to active power, the ADE7858/ADE7868/ADE7878 achieve the integration of the reactive power signal in two stages (see Figure 71). The process is identical for both total and fundamental reactive powers.

- The first stage is conducted inside the DSP: every 125 µs (8 kHz frequency), the instantaneous phase total reactive or fundamental power is accumulated into an internal register. When a threshold is reached, a pulse is generated at the processor port and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the reactive power (see the Sign of Reactive Power Calculation section for details).
- The second stage is performed outside the DSP and consists in accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to the var-hour registers (xVARHR and xFVARHR) when these registers are accessed. AVARHR, BVARHR, CVARHR, AFWATTHR, BFWATTHR, and CFWATTHR represent phase fundamental reactive powers.

Figure 68 from the Active Energy Calculation section explains this process. The VARTHR 48-bit signed register contains the threshold and it is introduced by the user. It is common for both total and fundamental phase reactive powers. Its value depends on how much energy is assigned to one LSB of var-hour registers. When a derivative of reactive energy (varh) of [10^n varh], where n is an integer, is desired as one LSB of the xVARHR register; then, the xVARTHR register can be computed using the following equation:

$$VARTHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{V_{FS} \times I_{FS}}$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 8 kHz, the frequency with which the DSP computes the instantaneous power.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The maximum value that may be written on the VARTHR register is $2^{47} - 1$. The minimum value is 0x0, but it is recommended to write a number equal to or greater than PMAX. Never use negative numbers.

VARTHR is a 48-bit register. As previously stated in the Voltage Waveform Gain Registers section, the serial ports of the ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words. Similar to the WTHR register shown in Figure 69, VARTHR is accessed as two 32-bit registers (VARTHR1 and VARTHR0), each having eight MSBs padded with 0s.

Downloaded from Arrow.com.

This discrete time accumulation or summation is equivalent to integration in continuous time following the expression in Equation 37:

$$ReactiveEnergy = \int q(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} q(nT) \times T \right\} \quad (37)$$

where:
n is the discrete time sample number.
T is the sample period.

On the ADE7858/ADE7868/ADE7878, the total phase reactive powers are accumulated in the AVARHR, BVARHR, and CVARHR 32-bit signed registers. The fundamental phase reactive powers are accumulated in the AFVARHR, BFVARHR, and CFVARHR 32-bit signed registers. The reactive energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the reactive power is positive. Conversely, if the reactive power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues to decrease in value.

Bit 2 (REHF) in the STATUS0 register is set when Bit 30 of one of the xVARHR registers changes, signifying one of these registers is half full. If the reactive power is positive, the var-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the reactive power is negative, the var-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF. Analogously, Bit 3 (FREHF) in the STATUS0 register is set when Bit 30 of one of the xFVARHR registers changes, signifying one of these registers is half full.

Setting Bits[3:2] in the MASK0 register enable the FREHF and REHF interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xVARHR (for REHF interrupt) or xFVARHR (for FREHF interrupt), becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all var-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

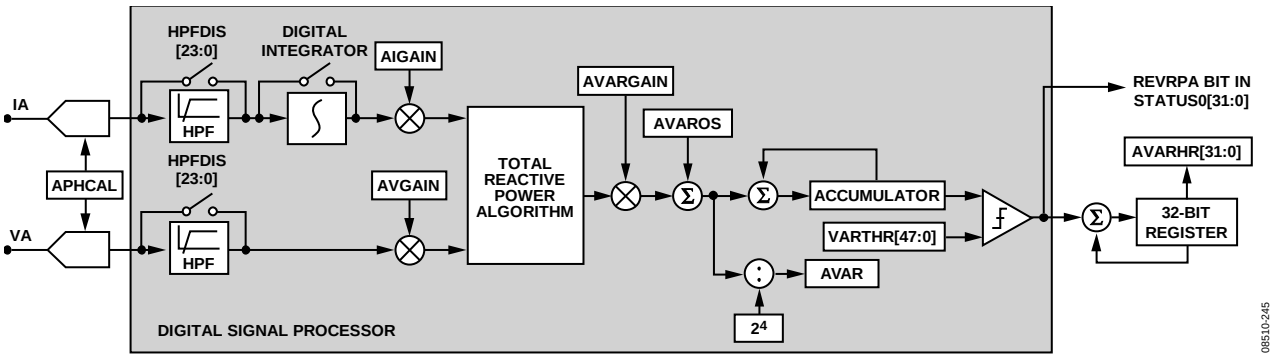

Figure 71. Total Reactive Energy Accumulation

Downloaded from Arrow.com.

Integration Time Under A Steady Load

The discrete time sample period (T) for the accumulation register is 125 µs (8 kHz frequency). With full-scale pure sinusoidal signals on the analog inputs and a 90° phase difference between the voltage and the current signal (the largest possible reactive power), the average word value representing the reactive power is PMAX = 33,516,139 = 0x1FF6A6B. If the VARTHR threshold is set at the PMAX level, this means the DSP generates a pulse that is added at the var-hour registers every 125 µs.

The maximum value that can be stored in the var-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 125\ \mu s = 74\ hr\ 33\ min\ 55\ sec \quad (38)$$

Energy Accumulation Modes

The reactive power accumulated in each var-hour accumulation 32-bit register (AVARHR, BVARHR, CVARHR, AFVARHR, BFVARHR, and CFVARHR) depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register, in correlation with the watt-hour registers. The different configurations are described in Table 19. Note that IA′/IB′/IC′ are the phase-shifted current waveforms.

Table 19. Inputs to Var-Hour Accumulation Registers

CONSEL[1:0]	AVARHR, AFVARHR	BVARHR, BFVARHR	CVARHR, CFVARHR
00	VA × IA′	VB × IB′	VC × IC′
01	VA × IA′	0	VC × IC′
10	VA × IA′	VB × IB′ VB = −VA − VC	VC × IC′
11	VA × IA′	VB × IB′ VB = −VA	VC × IC′

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine how CF frequency output can be a generated function of the total and fundamental reactive powers. While the var-hour accumulation registers accumulate the reactive power in a signed format, the frequency output can be generated in either the signed mode or the sign adjusted mode function of VARACC[1:0]. See the Energy-to-Frequency Conversion section for details.

Line Cycle Reactive Energy Accumulation Mode

As mentioned in the Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings so that reactive energy can be accumulated over an integral number of half line cycles.

In this mode, the ADE7858/ADE7868/ADE7878 transfer the reactive energy accumulated in the 32-bit internal accumulation registers into the xVARHR or xFVARHR registers after an integral number of line cycles, as shown in Figure 72. The number of half line cycles is specified in the LINECYC register.

The line cycle reactive energy accumulation mode is activated by setting Bit 1 (LVAR) in the LCYCMODE register. The total reactive energy accumulated over an integer number of half line cycles or zero crossings is available in the var-hour accumulation registers after the number of zero crossings specified in the LINECYC register is detected. When using the line cycle accumulation mode, Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because a read with the reset of var-hour registers is not available in this mode.

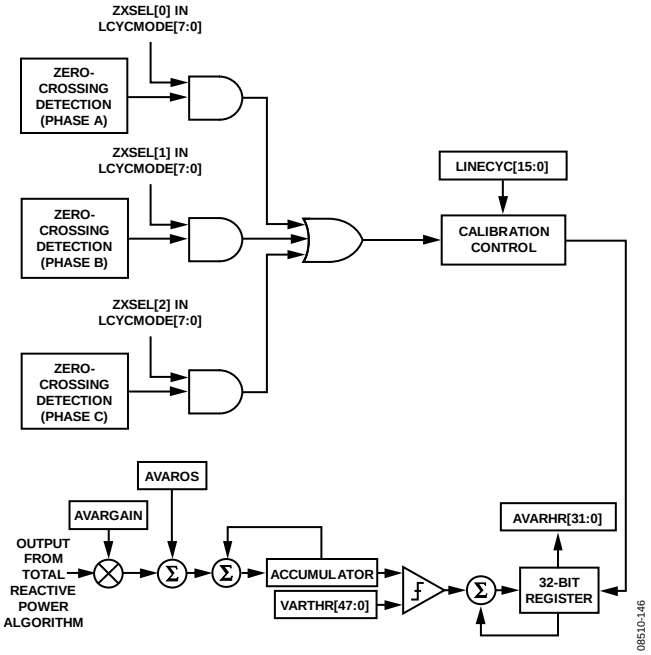

Figure 72. Line Cycle Total Reactive Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and the Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

Downloaded from Arrow.com.

APPARENT POWER CALCULATION

Apparent power is defined as the maximum power that can be delivered to a load. One way to obtain the apparent power is by multiplying the voltage rms value by the current rms value (also called the arithmetic apparent power)

$$S = V\,rms \times I\,rms \quad (39)$$

where:
S is the apparent power.
$V\,rms$ and $I\,rms$ are the rms voltage and current, respectively.

The ADE7854/ADE7858/ADE7868/ADE7878 compute the arithmetic apparent power on each phase. Figure 73 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE78xx. Because V rms and I rms contain all harmonic information, the apparent power computed by the ADE78xx is total apparent power. The ADE7878 does not compute fundamental apparent power because it does not measure the rms values of the fundamental voltages and currents.

The ADE7854/ADE7858/ADE7868/ADE7878 store the instantaneous phase apparent powers into the AVA, BVA, and CVA registers. Their expression is

$$xVA = \frac{V}{V_{FS}} \times \frac{I}{I_{FS}} \times PMAX \times \frac{1}{2^4} \quad (40)$$

where:
V, I are the rms values of the phase voltage and current.
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 33,516,139, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVA[23:0] waveform registers may be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

The ADE7854/ADE7858/ADE7868/ADE7878 can compute the apparent power in an alternative way by multiplying the phase rms current by an rms voltage introduced externally. See the Apparent Power Calculation Using VNOM section for details.

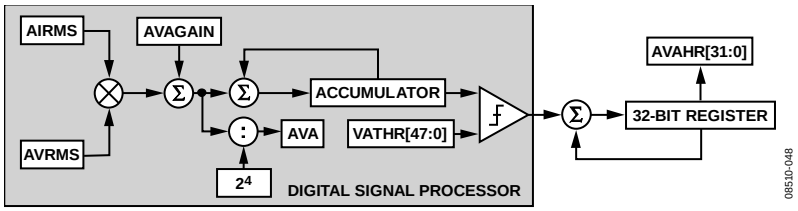

Figure 73. Apparent Power Data Flow and Apparent Energy Accumulation

Downloaded from Arrow.com.

Apparent Power Gain Calibration

The average apparent power result in each phase can be scaled by ±100% by writing to one of the phase's VAGAIN 24-bit registers (AVAGAIN, BVAGAIN, or CVAG AIN). The VAGAIN registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. The function of the xVAGAIN registers is expressed mathematically as

$$Average\ Apparent\ Power = V\ rms \times I\ rms \times \left(1 + \frac{VAGAIN\ Register}{2^{23}}\right) \quad (41)$$

The output is scaled by −50% by writing 0xC00000 to the xVAGAIN registers, and it is increased by +50% by writing 0x400000 to them. These registers calibrate the apparent power (or energy) calculation in the ADE7854/ADE7858/ADE7868/ADE7878 for each phase.

As previously stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 35, the AVAGAIN, BVAGAIN, and CVAGAIN 24-bit registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Root Mean Square Measurement section). The voltage and current rms values are multiplied together in the apparent power signal processing. As no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase is accomplished by calibrating each individual rms measurement.

Apparent Power Calculation Using VNOM

The ADE7854/ADE7858/ADE7868/ADE7878 can compute the apparent power by multiplying the phase rms current by an rms voltage introduced externally in the VNOM 24-bit signed register.

When one of Bits[13:11] (VNOMCEN, VNOMBEN, or VNOMAEN) in the COMPMODE register is set to 1, the apparent power in the corresponding phase (Phase x for VNOMxEN) is computed in this way. When the VNOMxEN bits are cleared to 0, the default value, then the arithmetic apparent power is computed.

The VNOM register contains a number determined by V, the desired rms voltage, and V_{FS}, the rms value of the phase voltage when the ADC inputs are at full scale:

$$VNOM = \frac{V}{V_{FS}} \times 4{,}191{,}910 \quad (42)$$

where V is the desired nominal phase rms voltage.

As stated in the Current Waveform Gain Registers, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 36, the VNOM 24-bit signed register is accessed as a 32-bit register with the eight MSBs padded with 0s.

Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$Apparent\ Energy = \int s(t)dt \quad (43)$$

Similar to active and reactive powers, the ADE7854/ADE7858/ADE7868/ADE7878 achieve the integration of the apparent power signal in two stages (see Figure 73). The first stage is conducted inside the DSP: every 125 µs (8 kHz frequency), the instantaneous phase apparent power is accumulated into an internal register. When a threshold is reached, a pulse is generated at the processor port and the threshold is subtracted from the internal register. The second stage is conducted outside the DSP and consists of accumulating the pulses generated by the processor into internal 32-bit accumulation registers. The content of these registers is transferred to the VA-hour registers, xVAHR, when these registers are accessed. Figure 68 from the Active Energy Calculation section illustrates this process. The VATHR 48-bit register contains the threshold. Its value depends on how much energy is assigned to one LSB of the VA-hour registers. When a derivative of apparent energy (VAh) of [10^n VAh], where n is an integer, is desired as one LSB of the xVAHR register; then, the xVATHR register can be computed using the following equation:

$$VATHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{V_{FS} \times I_{FS}}$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 8 kHz, the frequency with which the DSP computes the instantaneous power.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

VATHR is a 48-bit register. As previously stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words. Similar to the WTHR register presented in Figure 69, the VATHR register is accessed as two 32-bit registers (VATHR1 and VATHR0), each having eight MSBs padded with 0s.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation 44.

$$ApparentEnergy = \int s(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} s(nT) \times T \right\} \quad (44)$$

where:
n is the discrete time sample number.
T is the sample period.

Downloaded from Arrow.com.

In the ADE7854/ADE7858/ADE7868/ADE7878, the phase apparent powers are accumulated in the AVAHR, BVAHR, and CVAHR 32-bit signed registers. The apparent energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the apparent power is positive.

Bit 4 (VAEHF) in the STATUS0 register is set when Bit 30 of one of the xVAHR registers changes, signifying one of these registers is half full. As the apparent power is always positive and the xVAHR registers are signed, the VA-hour registers become half full when they increment from 0x3FFFFFFF to 0x4000 0000. Interrupts attached to Bit VAEHF in the STATUS0 register can be enabled by setting Bit 4 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the Energy Registers xVAHR becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all xVAHR accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period for the accumulation register is 125 µs (8 kHz frequency). With full-scale pure sinusoidal signals on the analog inputs, the average word value representing the apparent power is PMAX. If the VATHR threshold register is set at the PMAX level, this means the DSP generates a pulse that is added at the xVAHR registers every 125 µs.

The maximum value that can be stored in the xVAHR accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 125\ \mu s = 74\ hr\ 33\ min\ 55\ sec \quad (45)$$

Energy Accumulation Mode

The apparent power accumulated in each accumulation register depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register. The various configurations are described in Table 20.

Table 20. Inputs to VA-Hour Accumulation Registers

CONSEL[1:0]	AVAHR	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	0	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA – VC	CVRMS × CIRMS
11	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA	CVRMS × CIRMS

Line Cycle Apparent Energy Accumulation Mode

As described in the Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings allowing apparent energy to be accumulated over an integral number of half line cycles. In this mode, the ADE7854/ADE7858/ADE7868/ADE7878transfer the apparent energy accumulated in the 32-bit internal accumulation registers into the xVAHR registers after an integral number of line cycles, as shown in Figure 74. The number of half line cycles is specified in the LINECYC register.

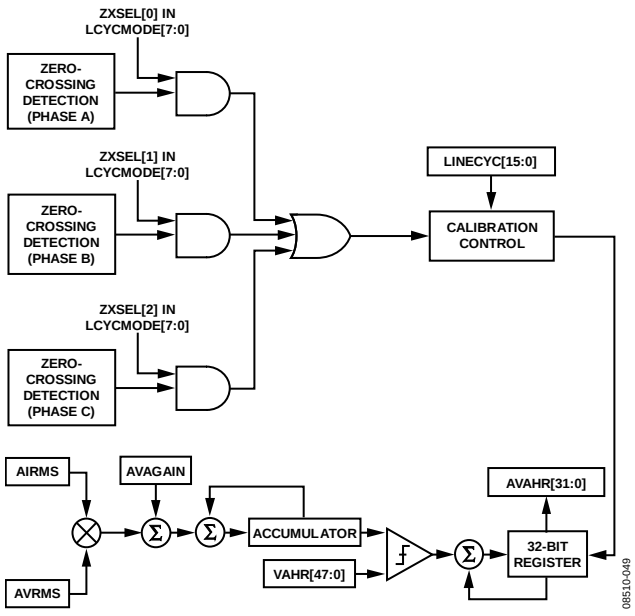

Figure 74. Line Cycle Apparent Energy Accumulation Mode

Downloaded from Arrow.com.

The line cycle apparent energy accumulation mode is activated by setting Bit 2 (LVA) in the LCYCMODE register. The apparent energy accumulated over an integer number of zero crossings is written to the xVAHR accumulation registers after the number of zero crossings specified in LINECYC register is detected. When using the line cycle accumulation mode, set Bit 6 (RSTREAD) of the LCYCMODE register to Logic 0 because a read with the reset of xVAHR registers is not available in this mode.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveform, the active, reactive, and apparent power outputs are stored every 125 µs (8 kHz rate) into 24-bit signed registers that can be accessed through various serial ports of the ADE7854/ADE7858/ADE7868/ADE7878. Table 21 provides a list of registers and their descriptions.

Table 21. Waveform Registers List

Register	Description
IAWV	Phase A current
VAWV	Phase A voltage
IBWV	Phase B current
VBWV	Phase B voltage
ICWV	Phase C current
VCWV	Phase C voltage
INWV	Neutral current, available in the ADE7868 and ADE7878 only
AVA	Phase A apparent power
BVA	Phase B apparent power
CVA	Phase C apparent power
AWATT	Phase A active power
BWATT	Phase B active power
CWATT	Phase C active power
AVAR	Phase A reactive power
BVAR	Phase B reactive power
CVAR	Phase C reactive power

Bit 17 (DREADY) in the STATUS0 register can be used to signal when the registers listed in Table 21 can be read using I²C or SPI serial ports. An interrupt attached to the flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. See the Digital Signal Processor section for more details on Bit DREADY.

The ADE7854/ADE7858/ADE7868/ADE7878 contain a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. Read the HSDC Interface section for more details.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words. All registers listed in Table 21 are transmitted signed extended from 24 bits to 32 bits (see Figure 37).

ENERGY-TO-FREQUENCY CONVERSION

The ADE7854/ADE7858/ADE7868/ADE7878 provide three frequency output pins: CF1, CF2, and CF3. The CF3 pin is multiplexed with the HSCLK pin of the HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. CF1 and CF2 pins are always available. After initial calibration at manufacturing, the manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to the active, reactive, or apparent powers under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 75 illustrates the energy-to-frequency conversion in the ADE7854/ADE7858/ADE7868/ADE7878.

The DSP computes the instantaneous values of all phase powers: total active, fundamental active, total reactive, fundamental reactive, and apparent. The process in which the energy is sign accumulated in various xWATTHR, xVARHR, and xVAHR registers has already been described in the energy calculation sections: Active Energy Calculation, Reactive Energy Calculation, and Apparent Energy Calculation. In the energy-to-frequency conversion process, the instantaneous powers generate signals at the frequency output pins (CF1, CF2, and CF3). One digital-to-frequency converter is used for every CFx pin. Every converter sums certain phase powers and generates a signal proportional to the sum. Two sets of bits decide what powers are converted.

First, Bits[2:0] (TERMSEL1[2:0]), Bits[5:3] (TERMSEL2[2:0]), and Bits[8:6] (TERMSEL3[2:0]) of the COMPMODE register decide which phases, or which combination of phases, are added.

The TERMSEL1 bits refer to the CF1 pin, the TERMSEL2 bits refer to the CF2 pin, and the TERMSEL3 bits refer to the CF3 pin. The TERMSELx[0] bits manage Phase A. When set to 1, Phase A power is included in the sum of powers at the CFx converter. When cleared to 0, Phase A power is not included. The TERMSELx[1] bits manage Phase B, and the TERMSELx[2] bits manage Phase C. Setting all TERMSELx bits to 1 means all 3-phase powers are added at the CFx converter. Clearing all TERMSELx bits to 0 means no phase power is added and no CF pulse is generated.

Downloaded from Arrow.com.

Second, Bits[2:0] (CF1SEL[2:0]), Bits[5:3] (CF2SEL[2:0]), and Bits[8:6] (CF3SEL[2:0]) in the CFMODE register decide what type of power is used at the inputs of the CF1, CF2, and CF3 converters, respectively. Table 22 shows the values that CFxSEL can have: total active, total reactive (available in the ADE7858, ADE7868, and ADE7878 only), apparent, fundamental active (available in the ADE7878 only), or fundamental reactive (available in the ADE7878 only) powers.

Table 22. CFxSEL Bits Description

CFxSEL	Description	Registers Latched When CFxLATCH = 1
000	CFx signal proportional to the sum of total phase active powers	AWATTHR, BWATTHR, CWATTHR
001	CFx signal proportional to the sum of total phase reactive powers (ADE7858/ADE7868/ADE7878)	AVARHR, BVARHR, CVARHR
010	CFx signal proportional to the sum of phase apparent powers	AVAHR, BVAHR, CVAHR
011	CFx signal proportional to the sum of fundamental phase active powers (ADE7878 only)	AFWATTHR, BFWATTHR, CFWATTHR
100	CFx signal proportional to the sum of fundamental phase reactive powers (ADE7878 only)	AFVARHR, BFVARHR, CFVARHR
101 to 111	Reserved	

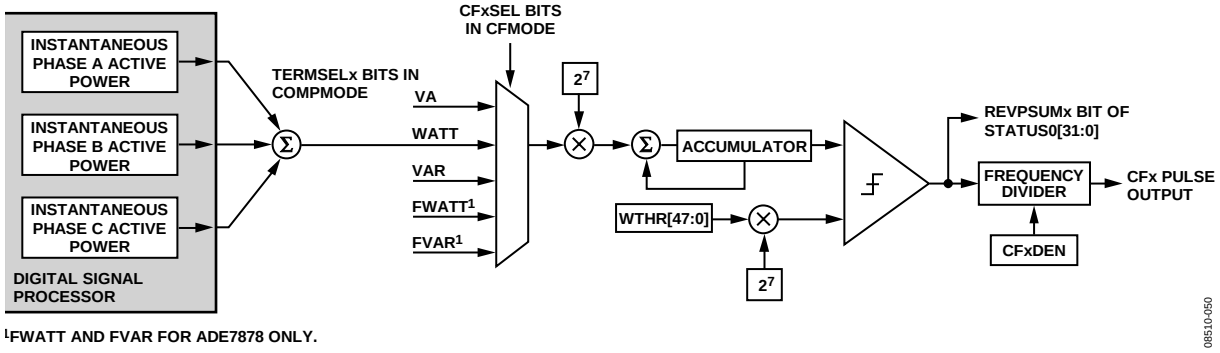

Figure 75. Energy-to-Frequency Conversion

Downloaded from Arrow.com.

By default, the TERMSELx bits are all 1 and the CF1SEL bits are 000, the CF2SEL bits are 001, and the CF3SEL bits are 010. This means that by default, the CF1 digital-to-frequency converter produces signals proportional to the sum of all 3-phase total active powers, CF2 produces signals proportional to total reactive powers, and CF3 produces signals proportional to apparent powers.

Similar to the energy accumulation process, the energy-to-frequency conversion is accomplished in two stages. In the first stage, the instantaneous phase powers obtained from the DSP at the 8 kHz rate are shifted left by seven bits and then accumulate into an internal register at a 1 MHz rate. When a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the sum of phase powers (see the Sign of Sum-of-Phase Powers in the CFx Datapath section for details). The threshold is the same threshold used in various active, reactive, and apparent energy accumulators in the DSP, such as the WTHR, VARTHR, or VATHR registers, except for being shifted left by seven bits. The advantage of accumulating the instantaneous powers at the 1 MHz rate is that the ripple at the CFx pins is greatly diminished.

The second stage consists of the frequency divider by the CFxDEN 16-bit unsigned registers. The values of CFxDEN depend on the meter constant (MC), measured in impulses/kWh and how much energy is assigned to one LSB of various energy registers: xWATTHR, xVARHR, and so forth. Supposing a derivative of wh [10^n wh], n a positive or negative integer, is desired as one LSB of xWATTHR register. Then, CFxDEN is as follows:

$$CFxDEN = \frac{10^3}{MC[\text{imp/kwh}] \times 10^n} \quad (46)$$

The derivative of wh must be chosen in such a way to obtain a CFxDEN register content greater than 1. If CFxDEN = 1, then the CFx pin stays active low for only 1 µs, therefore, avoid this number. The frequency converter cannot accommodate fractional results; the result of the division must be rounded to the nearest integer. If CFxDEN is set equal to 0, then the ADE78xx considers it to be equal to 1.

The pulse output for all digital-to-frequency converters stays low for 80 ms if the pulse period is larger than 160 ms (6.25 Hz). If the pulse period is smaller than 160 ms and CFxDEN is an even number, the duty cycle of the pulse output is exactly 50%. If the pulse period is smaller than 160 ms and CFxDEN is an odd number, the duty cycle of the pulse output is

$(1+1/CFxDEN) \times 50\%$

The pulse output is active low and preferably connected to an LED, as shown in Figure 76.

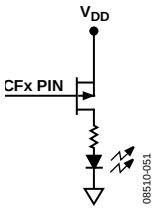

Figure 76. CFx Pin Recommended Connection

Bits[11:9] (CF3DIS, CF2DIS, and CF1DIS) of the CFMODE register decide if the frequency converter output is generated at the CF3, CF2, or CF1 pin. When Bit CFxDIS is set to 1 (the default value), the CFx pin is disabled and the pin stays high. When Bit CFxDIS is cleared to 0, the corresponding CFx pin output generates an active low signal.

Bits[16:14] (CF3, CF2, CF1) in the Interrupt Mask Register MASK0 manage the CF3, CF2, and CF1 related interrupts. When the CFx bits are set, whenever a high-to-low transition at the corresponding frequency converter output occurs, an interrupt $\overline{\text{IRQ0}}$ is triggered and a status bit in the STATUS0 register is set to 1. The interrupt is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Synchronizing Energy Registers with CFx Outputs

The ADE7854/ADE7858/ADE7868/ADE7878 contain a feature that allows synchronizing the content of phase energy accumulation registers with the generation of a CFx pulse. When a high-to-low transition at one frequency converter output occurs, the content of all internal phase energy registers that relate to the power being output at CFx pin is latched into hour registers and then resets to 0. See Table 22 for the list of registers that are latched based on the CFxSEL[2:0] bits in the CFMODE register. All 3-phase registers are latched independent of the TERMSELx bits of the COMPMODE register. The process is shown in Figure 77 for CF1SEL[2:0] = 010 (apparent powers contribute at the CF1 pin) and CFCYC = 2.

The CFCYC 8-bit unsigned register contains the number of high to low transitions at the frequency converter output between two consecutive latches. Avoid writing a new value into the CFCYC register during a high-to-low transition at any CFx pin.

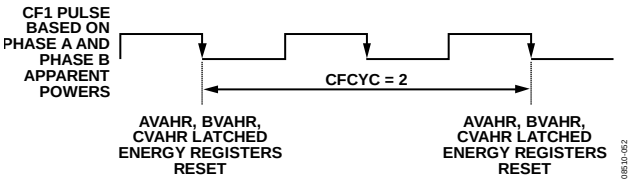

Figure 77. Synchronizing AVAHR and BVAHR with CF1

Bits[14:12] (CF3LATCH, CF2LATCH, and CF1LATCH) of the CFMODE register enable this process when set to 1. When cleared to 0, the default state, no latch occurs. The process is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Downloaded from Arrow.com.

CF Outputs for Various Accumulation Modes

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine the accumulation modes of the total active and fundamental powers when signals proportional to the active powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 000 or 011). When WATTACC[1:0] = 00 (the default value), the active powers are sign accumulated before entering the energy-to-frequency converter. Figure 78 shows how signed active power accumulation works. In this mode, the CFx pulses synchronize perfectly with the active energy accumulated in xWATTHR registers because the powers are sign accumulated in both data paths.

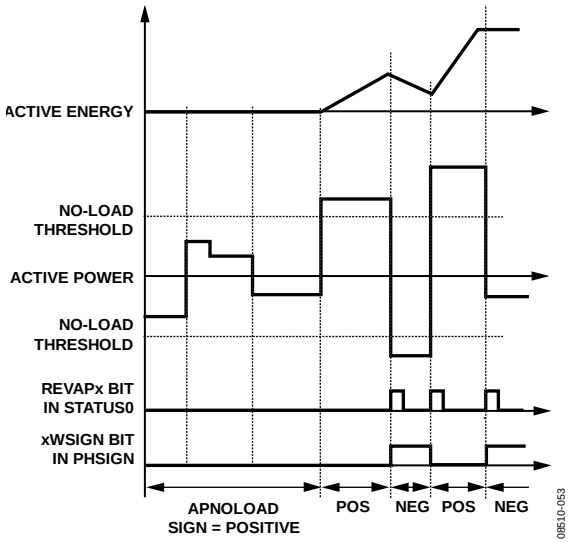

Figure 78. Active Power Signed Accumulation Mode

When WATTACC[1:0] = 11, the active powers are accumulated in absolute mode. When the powers are negative, they change sign and accumulate together with the positive power. Figure 79 shows how absolute active power accumulation works. Note that in this mode, the xWATTHR registers continue to accumulate active powers in signed mode, even if the CFx pulses are generated based on the absolute accumulation mode.

WATTACC[1:0] settings of 01 and 10 are reserved. The ADE7854/ADE7858/ADE7868/ADE7878 behave identically to the case when WATTACC[1:0] = 00.

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine the accumulation modes of the total and fundamental reactive powers when signals proportional to the reactive powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 001 or 100). When VARACC[1:0] = 00, the default value, the reactive powers are sign accumulated before entering the energy-to-frequency converter. Figure 80 shows how signed reactive power accumulation works. In this mode, the CFx pulses synchronize perfectly with the reactive energy accumulated in the xVARHR registers because the powers are sign accumulated in both datapaths.

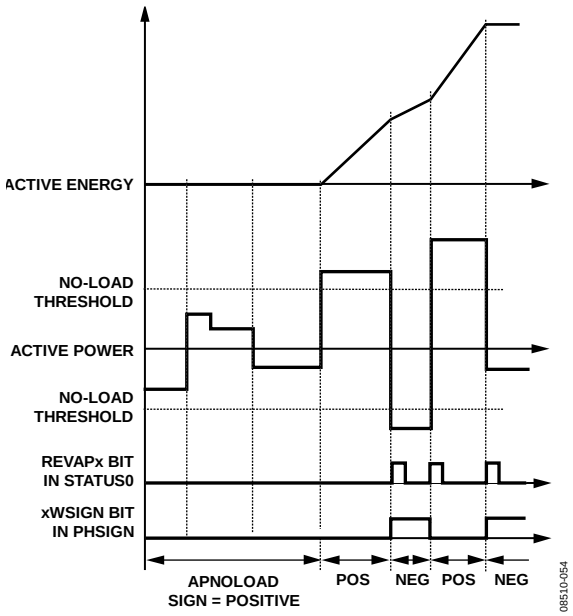

Figure 79. Active Power Absolute Accumulation Mode

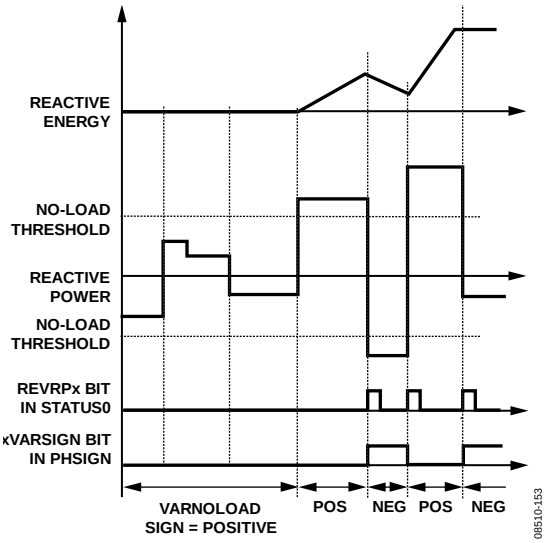

Figure 80. Reactive Power Signed Accumulation Mode

When VARACC[1:0] = 10, the reactive powers are accumulated depending on the sign of the corresponding active power. If the active power is positive, the reactive power is accumulated as is. If the active power is negative, the sign of the reactive power is changed for accumulation. Figure 81 shows how the sign adjusted reactive power accumulation mode works. In this mode, the xVARHR registers continue to accumulate reactive powers in signed mode, even if the CFx pulses are generated based on the sign adjusted accumulation mode.

VARACC[1:0] settings of 01 and 11 are reserved. The ADE7854/ADE7858/ADE7868/ADE7878 behave identically to the case when VARACC[1:0] = 00.

Downloaded from Arrow.com.

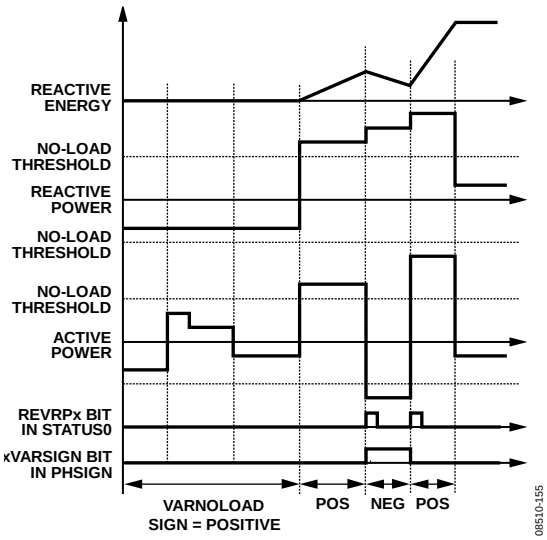

Figure 81. Reactive Power Accumulation in Sign Adjusted Mode

Sign of Sum-of-Phase Powers in the CFx Datapath

The ADE7854/ADE7858/ADE7868/ADE7878 have sign detection circuitry for the sum of phase powers that are used in the CFx datapath. As seen in the beginning of the Energy-to-Frequency Conversion section, the energy accumulation in the CFx datapath is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the accumulator reaches one of the WTHR, VARTHR, or VATHR thresholds, a dedicated interrupt can be triggered synchronously with the corresponding CFx pulse. The sign of each sum can be read in the PHSIGN register.

Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) of the STATUS0 register are set to 1 when a sign change of the sum of powers in CF3, CF2, or CF1 datapaths occurs. To correlate these events with the pulses generated at the CFx pins, after a sign change occurs, Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 are set in the same moment in which a high-to-low transition at the CF3, CF2, and CF1 pin, respectively, occurs.

Bit 8, Bit 7, and Bit 3 (SUM3SIGN, SUM2SIGN, and SUM1SIGN, respectively) of the PHSIGN register are set in the same moment with Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 and indicate the sign of the sum of phase powers. When cleared to 0, the sum is positive. When set to 1, the sum is negative.

Interrupts attached to Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) in the STATUS0 register are enabled by setting Bit 18, Bit 13, and Bit 9 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high again by writing to the STATUS0 register with the corresponding bit set to 1.

NO LOAD CONDITION

The no load condition is defined in metering equipment standards as occurring when the voltage is applied to the meter and no current flows in the current circuit. To eliminate any creep effects in the meter, the ADE7854/ADE7858/ADE7868/ADE7878contain three separate no load detection circuits: one related to the total active and reactive powers (ADE7858/ADE7868/ADE7878 only), one related to the fundamental active and reactive powers (ADE7878 only), and one related to the apparent powers.

No Load Detection Based On Total Active, Reactive Powers

This no load condition is triggered when the absolute values of both phase total active and reactive powers are less than or equal to positive thresholds indicated in the respective APNOLOAD and VARNOLOAD signed 24-bit registers. In this case, the total active and reactive energies of that phase are not accumulated and no CFx pulses are generated based on these energies. The APNOLOAD register represents the positive no load level of active power relative to PMAX, the maximum active power obtained when full-scale voltages and currents are provided at ADC inputs. The VARNOLOAD register represents the positive no load level of reactive power relative to PMAX. The expression used to compute APNOLOAD signed 24-bit value is

$$APNOLOAD = \frac{V_n}{V_{FS}} \times \frac{I_{NOLOAD}}{I_{FS}} \times PMAX \quad (47)$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B, the instantaneous power computed when the ADC inputs are at full scale.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.
V_n is the nominal rms value of phase voltage.
I_{NOLOAD} is the minimum rms value of phase current the meter starts measuring.

The VARNOLOAD register usually contains the same value as the APNOLOAD register. When APNOLOAD and VARNOLOAD are set to negative values, the no load detection circuit is disabled.

Note that the ADE7854 measures only the total active powers. To ensure good functionality of the ADE7854 no-load circuit, set the VARNOLOAD register at 0x800000.

As previously stated in the Current Waveform Gain Registers section, the serial ports of the ADE78xx work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. APNOLOAD and VARNOLOAD 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits. See Figure 35 for details.

Bit 0 (NLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[2:0] (NLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit NLOAD in the STATUS1 register. NLPHASE[0] indicates the state of Phase A, NLPHASE[1] indicates the state

Downloaded from Arrow.com.

of Phase B, and NLPHASE[2] indicates the state of Phase C. When Bit NLPHASE[x] is cleared to 0, it means the phase is out of a no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to Bit 0 (NLOAD) in the STATUS1 register can be enabled by setting Bit 0 in the MASK1 register. If enabled, the IRQ1 pin is set to low, and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the IRQ1 pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Fundamental Active and Reactive Powers—ADE7878 Only

This no load condition (available on the ADE7878 only) is triggered when the absolute values of both phase fundamental active and reactive powers are less than or equal to the respective APNOLOAD and VARNOLOAD positive thresholds. In this case, the fundamental active and reactive energies of that phase are not accumulated, and no CFx pulses are generated based on these energies. APNOLOAD and VARNOLOAD are the same no load thresholds set for the total active and reactive powers. When APNOLOAD and VARNOLOAD are set to negative values, this no load detection circuit is disabled.

Bit 1 (FNLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[5:3] (FNLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit FNLOAD in the STATUS1 register. FNLPHASE[0] indicates the state of Phase A, FNLPHASE[1] indicates the state of Phase B, and FNLPHASE[2] indicates the state of Phase C. When Bit FNLPHASE[x] is cleared to 0, it means the phase is out of the no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to the Bit 1 (FNLOAD) in the STATUS1 register can be enabled by setting Bit 1 in the MASK1 register. If enabled, the IRQ1 pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Then the status bit is cleared and the IRQ1 pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Apparent Power

This no load condition is triggered when the absolute value of phase apparent power is less than or equal to the threshold indicated in the VANOLOAD 24-bit signed register. In this case, the apparent energy of that phase is not accumulated and no CFx pulses are generated based on this energy. The VANOLOAD register represents the positive no load level of apparent power relative to PMAX, the maximum apparent power obtained when full-scale voltages and currents are provided at the ADC inputs. The expression used to compute the VANOLOAD signed 24-bit value is

$$VANOLOAD = \frac{V_n}{V_{FS}} \times \frac{I_{NOLOAD}}{I_{FS}} \times PMAX \quad (48)$$

where:
$PMAX$ = 33,516,139 = 0x1FF6A6B, the instantaneous apparent power computed when the ADC inputs are at full scale.
V_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.
V_n is the nominal rms value of phase voltage.
I_{NOLOAD} is the minimum rms value of phase current the meter starts measuring.

When the VANOLOAD register is set to negative values, the no load detection circuit is disabled.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7854/ADE7858/ADE7868/ADE7878 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 35, the VANOLOAD 24-bit signed register is accessed as a 32-bit register with the four MSBs padded with 0s and sign extended to 28 bits.

Bit 2 (VANLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[8:6] (VANLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and they are set simultaneously with Bit VANLOAD in the STATUS1 register:

- Bit VANLPHASE[0] indicates the state of Phase A.
- Bit VANLPHASE[1] indicates the state of Phase B.
- Bit VANLPHASE[2] indicates the state of Phase C.

When Bit VANLPHASE[x] is cleared to 0, it means the phase is out of no load condition. When set to 1, it means the phase is in no load condition.

An interrupt attached to Bit 2 (VANLOAD) in the STATUS1 register is enabled by setting Bit 2 in the MASK1 register. If enabled, the IRQ1 pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the IRQ1 pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

CHECKSUM REGISTER

The ADE7854/ADE7858/ADE7868/ADE7878 have a checksum 32-bit register, CHECKSUM, that ensures certain very important configuration registers maintain their desired value during Normal Power Mode PSM0.

The registers covered by this register are MASK0, MASK1, COMPMODE, gain, CFMODE, CF1DEN, CF2DEN, CF3DEN, CONFIG, MMODE, ACCMODE, LCYCMODE, HSDC_CFG, and another six 8-bit reserved internal registers that always have

Downloaded from Arrow.com.

default values. The ADE78xx computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard. The registers are introduced one-by-one into a linear feedback shift register (LFSR) based generator starting with the least significant bit (as shown in Figure 82). The 32-bit result is written in the CHECKSUM register. After power-up or a hardware/software reset, the CRC is computed on the default values of the registers giving the results presented in the Table 23.

Table 23. Default Values of CHECKSUM and of Internal Registers CRC

Part No.	Default Value of CHECKSUM	CRC of Internal Registers
ADE7854	0x44C48F8	0x391FBDDD
ADE7858	0xD6744F93	0x3E7D0FC1
ADE7868	0x93D774E6	0x23F7C7B1
ADE7878	0x33666787	0x2D32A389

Figure 83 shows how the LFSR works. The MASK0, MASK1, COMPMODE, gain, CFMODE, CF1DEN, CF2DEN, CF3DEN, CONFIG, MMODE, ACCMODE, LCYCMODE, and HSDC_CFG registers, and the six 8-bit reserved internal registers form the bits [a_{255}, a_{254},…, a_0] used by LFSR. Bit a_0 is the least significant bit of the first internal register to enter LFSR; Bit a_{255} is the most significant bit of the MASK0 register, the last register to enter LFSR. The formulas that govern LFSR are as follows:

$b_i(0) = 1$, i = 0, 1, 2, …, 31, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{31} is the most significant.

g_i, i = 0, 1, 2, …, 31 are the coefficients of the generating polynomial defined by the IEEE802.3 standard as follows:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (49)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{23} = g_{26} = 1 \quad (50)$$

All of the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{31}(j-1) \quad (51)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (52)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 31 \quad (53)$$

Equation 51, Equation 52, and Equation 53 must be repeated for j = 1, 2, …, 256. The value written into the CHECKSUM register contains the Bit $b_i(256)$, i = 0, 1, …, 31. The value of the CRC, after the bits from the reserved internal register have passed through LFSR, is obtained at Step j = 48 and is presented in the Table 23.

Two different approaches can be followed in using the CHECKSUM register. One is to compute the CRC based on the relations (47) to (53) and then compare the value against the CHECKSUM register. Another is to periodically read the CHECKSUM register. If two consecutive readings differ, it can be assumed that one of the registers has changed value and therefore, the ADE7854, ADE7858, ADE7868, or ADE7878 has changed configuration. The recommended response is to initiate a hardware/software reset that sets the values of all registers to the default, including the reserved ones, and then reinitialize the configuration registers.

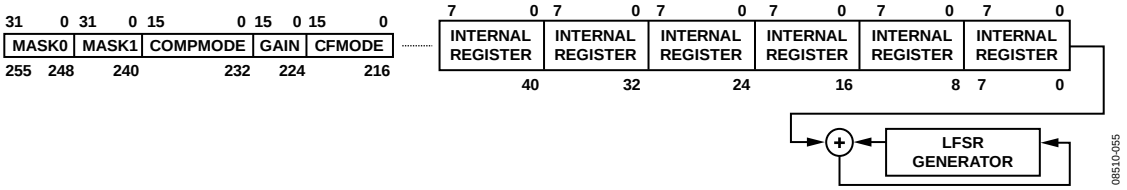

Figure 82. CHECKSUM Register Calculation

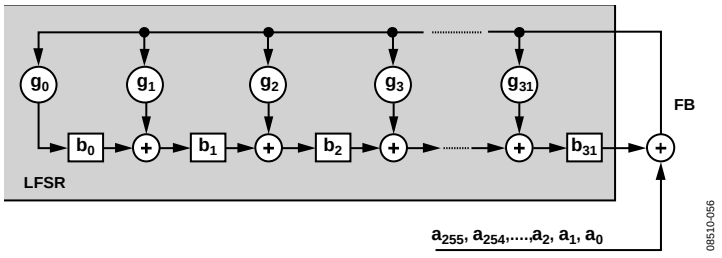

Figure 83. LFSR Generator Used in CHECKSUM Register Calculation

INTERRUPTS

The ADE7854/ADE7858/ADE7868/ADE7878 have two interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. Each of the pins is managed by a 32-bit interrupt mask register, MASK0 and MASK1, respectively. To enable an interrupt, a bit in the MASKx register must be set to 1. To disable it, the bit must be cleared to 0. Two 32-bit status registers, STATUS0 and STATUS1, are associated with the interrupts. When an interrupt event occurs in the ADE78xx, the corresponding flag in the interrupt status register is set to a Logic 1 (see Table 37 and Table 38). If the mask bit for this interrupt in the interrupt mask register is Logic 1, then the $\overline{\text{IRQx}}$ logic output

Downloaded from Arrow.com.

goes active low. The flag bits in the interrupt status register are set irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU should perform a read of the corresponding STATUSx register and identify which bit is set to 1. To erase the flag in the status register, write back to the STATUSx register with the flag set to 1. After an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back without any change to clear the status flag to 0. The $\overline{\text{IRQx}}$ pin remains low until the status flag is cancelled.

By default, all interrupts are disabled. However, the RSTDONE interrupt is an exception. This interrupt can never be masked (disabled) and, therefore, Bit 15 (RSTDONE) in the MASK1 register does not have any functionality. The $\overline{\text{IRQ1}}$ pin always goes low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1 whenever a power-up or a hardware/software reset process ends. To cancel the status flag, the STATUS1 register has to be written with Bit 15 (RSTDONE) set to 1.

Certain interrupts are used in conjunction with other status registers. The following bits in the MASK1 register work in conjunction with the status bits in the PHNOLOAD register:

- Bit 0 (NLOAD)
- Bit1 (FNLOAD), available in the ADE7878 only
- Bit 2 (VANLOAD)

The following bits in the MASK1 register work with the status bits in the PHSTATUS register:

- Bit 16, (SAG)
- Bit 17 (OI)
- Bit 18 (OV)

The following bits in the MASK1 register work with the status bits in the IPEAK and VPEAK registers, respectively:

- Bit 23 (PKI)
- Bit 24 (PKV)

The following bits in the MASK0 register work with the status bits in the PHSIGN register:

- Bits[6:8] (REVAPx)
- Bits[10:12] (REVRPx), available in the ADE7858, ADE7868, and ADE7878 only
- Bit 9, Bit 13, and Bit 18 (REVPSUMx)

When the STATUSx register is read and one of these bits is set to 1, the status register associated with the bit is immediately read to identify the phase that triggered the interrupt and only at that time can the STATUSx register be written back with the bit set to 1.

Using the Interrupts with an MCU

Figure 84 shows a timing diagram that illustrates a suggested implementation of the ADE7854/ADE7858/ADE7868/ADE7878 interrupt management using an MCU. At Time t_1, the $\overline{\text{IRQx}}$ pin goes active low indicating that one or more interrupt events have occurred in the ADE78xx, at which point the following steps should be taken:

1. Tie the $\overline{\text{IRQx}}$ pin to a negative-edge-triggered external interrupt on the MCU.
2. On detection of the negative edge, configure the MCU to start executing its interrupt service routine (ISR).
3. On entering the ISR, disable all interrupts using the global interrupt mask bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR.
4. When the MCU interrupt flag is cleared, a read from STATUSx, the interrupt status register, is carried out. The interrupt status register content is used to determine the source of the interrupt(s) and, hence, the appropriate action to be taken.
5. The same STATUSx content is written back into the ADE78xx to clear the status flag(s) and reset the $\overline{\text{IRQx}}$ line to logic high (t_2).

If a subsequent interrupt event occurs during the ISR (t_3), that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

Figure 85 shows a recommended timing diagram when the status bits in the STATUSx registers work in conjunction with bits in other registers. When the $\overline{\text{IRQx}}$ pin goes active low, the STATUSx register is read, and if one of these bits is 1, a second

Downloaded from Arrow.com.

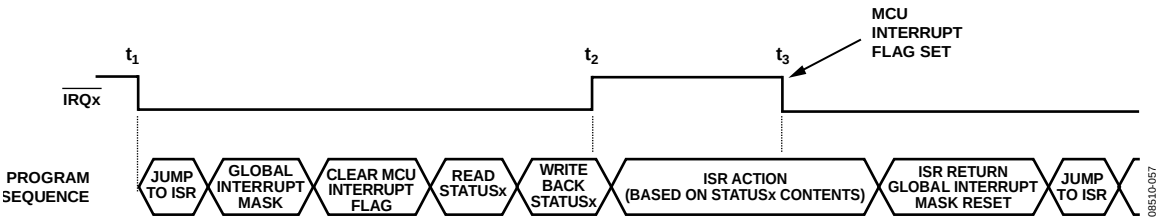

Figure 84. Interrupt Management

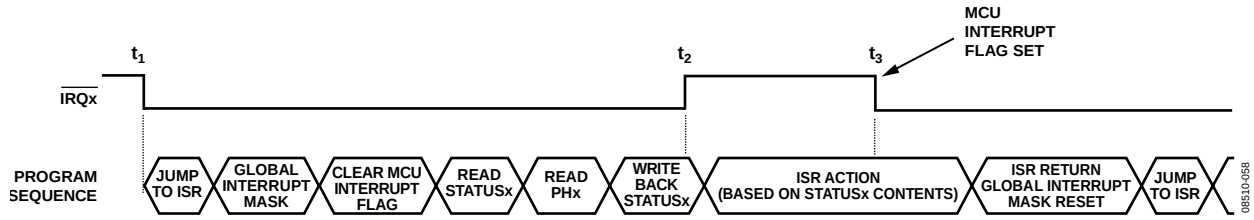

Figure 85. Interrupt Management when PHSTATUS, IPEAK, VPEAK, or PHSIGN Registers are Involved

status register is read immediately to identify the phase that triggered the interrupt. The name, PHx, in Figure 85 denotes one of the PHSTATUS, IPEAK, VPEAK, or PHSIGN registers. Then, STATUSx is written back to clear the status flag(s).

SERIAL INTERFACES

The ADE7854/ADE7858/ADE7868/ADE7878 have three serial port interfaces: one fully licensed I²C interface, one serial peripheral interface (SPI), and one high speed data capture port (HSDC). As the SPI pins are multiplexed with some of the pins of the I²C and HSDC ports, the ADE78xx accepts two configurations: one using the SPI port only and one using the I²C port in conjunction with the HSDC port.

Serial Interface Choice

After reset, the HSDC port is always disabled. Choose between the I²C and SPI ports by manipulating the $\overline{SS}$/HSA pin after power-up or after a hardware reset. If the $\overline{SS}$/HSA pin is kept high, then the ADE7854/ADE7858/ADE7868/ADE7878 use the I²C port until a new hardware reset is executed. If the $\overline{SS}$/HSA pin is toggled high to low three times after power-up or after a hardware reset, the ADE7854/ADE7858/ADE7868/ADE7878 use the SPI port until a new hardware reset is executed. This manipulation of the $\overline{SS}$/HSA pin can be accomplished in two ways. First, use the $\overline{SS}$/HSA pin of the master device (that is, the microcontroller) as a regular I/O pin and toggle it three times. Second, execute three SPI write operations to a location in the address space that is not allocated to a specific ADE78xx register (for example 0xEBFF, where eight bit writes can be executed). These writes allow the $\overline{SS}$/HSA pin to toggle three times. See the SPI Write Operation section for details on the write protocol involved.

After the serial port choice is completed, it needs to be locked. Consequently, the active port remains in use until a hardware reset is executed in PSM0 normal mode or until a power-down. If I²C is the active serial port, Bit 1 (I2C_LOCK) of the CONFIG2 register must be set to 1 to lock it in. From this moment, the ADE7854/ADE7858/ADE7868/ADE7878 ignore spurious toggling of the $\overline{SS}$ pin and an eventual switch into using the SPI port is no longer possible. If the SPI is the active serial port, any write to the CONFIG2 register locks the port. From this moment, a switch into using the I²C port is no longer possible. Once locked, the serial port choice is maintained when the ADE78xx changes PSMx power modes.

The functionality of the ADE78xx is accessible via several on-chip registers. The contents of these registers can be updated or read using either the I²C or SPI interfaces. The HSDC port provides the state of up to 16 registers representing instantaneous values of phase voltages and neutral currents, and active, reactive, and apparent powers.

I²C-Compatible Interface

The ADE7854/ADE7858/ADE7868/ADE7878 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400 kHz.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition, and the bus becomes idle.

Downloaded from Arrow.com.

I²C Write Operation

The write operation using the I²C interface of the ADE7854/ADE7858/ADE7868/ADE7878 initiate when the master generates a start condition and consists in one byte representing the address of the ADE78xx followed by the 16-bit address of the target register and by the value of the register.

The most significant seven bits of the address byte constitute the address of the ADE7854/ADE7858/ADE7868/ADE7878 and they are equal to 0111000b. Bit 0 of the address byte is a read/$\overline{\text{write}}$ bit. Because this is a write operation, it has to be cleared to 0; therefore, the first byte of the write operation is 0x70. After every byte is received, the ADE7854/ADE7858/ADE7868/ADE7878 generate an acknowledge. As registers can have 8, 16, or 32 bits, after the last bit of the register is transmitted and the ADE78xx acknowledges the transfer, the master generates a stop condition. The addresses and the register content are sent with the most significant bit first. See Figure 86 for details of the I²C write operation.

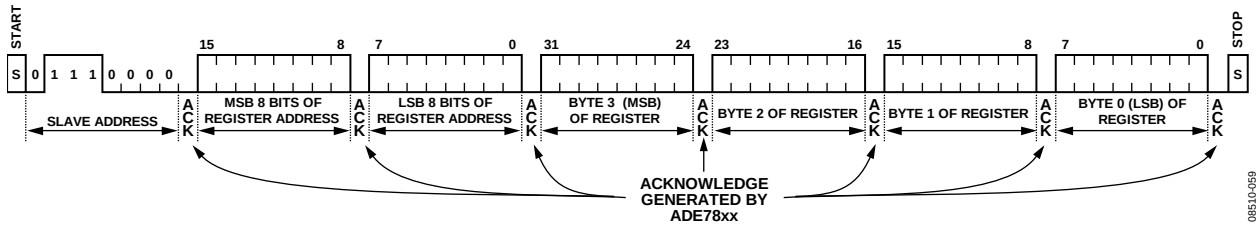

Figure 86. I²C Write Operation of a 32-Bit Register

Downloaded from Arrow.com.

I²C Read Operation

The read operation using the I²C interface of the ADE7854/ADE7858/ADE7868/ADE7878 is accomplished in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As seen in Figure 87, the first stage initiates when the master generates a start condition and consists in one byte representing the address of the ADE7854/ADE7858/ADE7868/ADE7878 followed by the 16-bit address of the target register. The ADE78xx acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I2C Write Operation section for details). After the last byte of the register address has been sent and acknowledged by the ADE7854/ADE7858/ADE7868/ADE7878, the second stage begins with the master generating a new start condition followed by an address byte. The most significant seven bits of this address byte constitute the address of the ADE78xx, and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a read operation, it must be set to 1; thus, the first byte of the read operation is 0x71. After this byte is received, the ADE78xx generates an acknowledge. Then, the ADE78xx sends the value of the register, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. Because registers can have 8, 16, or 32 bits, after the last bit of the register is received, the master does not acknowledge the transfer but generates a stop condition.

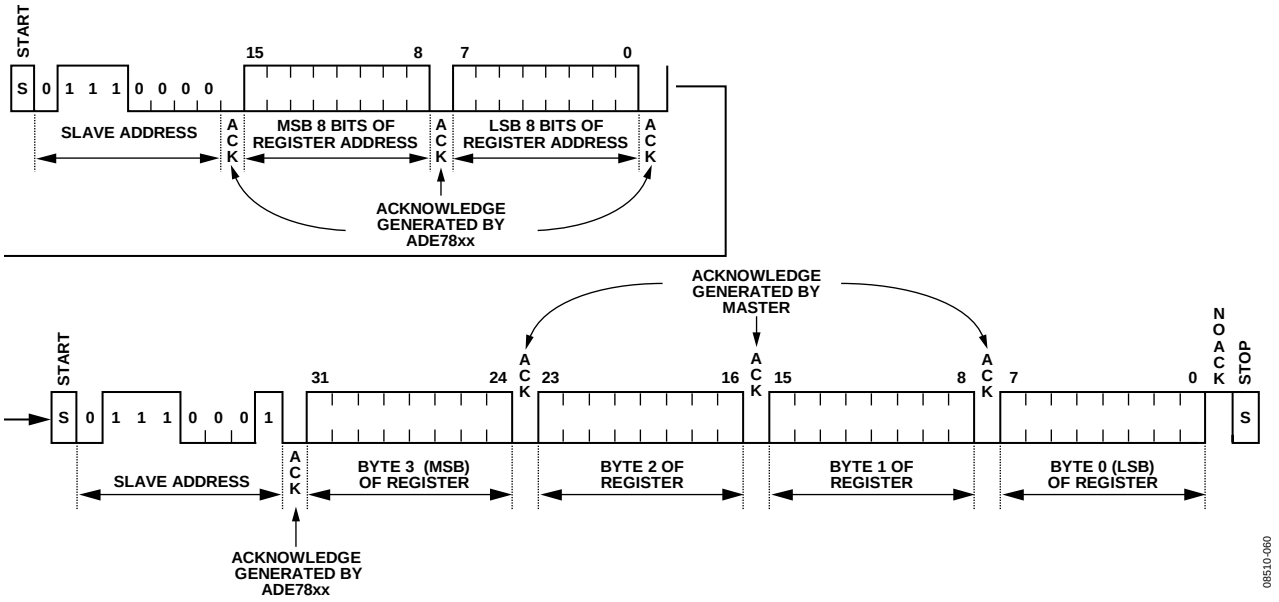

Figure 87. I²C Read Operation of a 32-Bit Register

Downloaded from Arrow.com.

SPI-Compatible Interface

The SPI of the ADE7854/ADE7858/ADE7868/ADE7878 is always a slave of the communication and consists of four pins (with dual functions): SCLK/SCL, MOSI/SDA, MISO/HSD, and $\overline{SS}$/HSA. The functions used in the SPI-compatible interface are SCLK, MOSI, MISO, and $\overline{SS}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE78xx at the MOSI logic input on the falling edge of SCLK and the ADE78xx samples it on the rising edge of SCLK. Data shifts out of the ADE7854/ADE7858/ADE7868/ADE7878 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5 MHz. MISO stays in high impedance when no data is transmitted from the ADE7854/ADE7858/ADE7868/ADE7878. See Figure 88 for details of the connection between the ADE78xx SPI and a master device containing an SPI interface.

The $\overline{SS}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. Drive the $\overline{SS}$ input low for the entire data transfer operation. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{SS}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, its value should be verified by reading it back. The protocol is similar to the protocol used in I^2C interface.

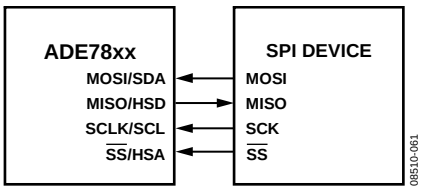

Figure 88. Connecting ADE78xx SPI with an SPI Device

SPI Read Operation

The read operation using the SPI interface of the ADE7854/ADE7858/ADE7868/ADE7878 initiate when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7854/ADE7858/ADE7868/ADE7878, on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE78xx samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, they should be different from 0111000b, the seven bits used in the I^2C protocol. Bit 0 (read/write) of the address byte must be 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE78xx receives the last bit of address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{SS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 89 for details of the SPI read operation.

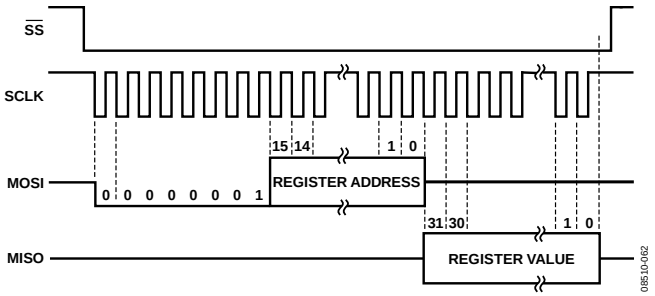

Figure 89. SPI Read Operation of a 32-Bit Register

Downloaded from Arrow.com.

SPI Write Operation

The write operation using the SPI interface of the ADE78xx initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte representing the address of the ADE7854/ADE7858/ADE7868/ADE7878 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE78xx samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, they should be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be 0 for a write operation. Next, the master sends both the 16-bit address of the register that is written and the 32-, 16-, or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 90 for details of the SPI write operation.

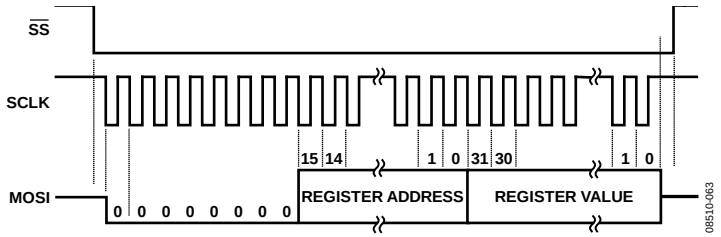

Figure 90. SPI Write Operation of a 32-Bit Register

Downloaded from Arrow.com.

HSDC Interface

The high speed data capture (HSDC) interface is disabled after default. It can be used only if the ADE7854/ADE7858/ADE7868/ADE7878 is configured with an I²C interface. The SPI interface of the ADE7854/ADE7858/ADE7868/ADE7878 cannot be used simultaneously with HSDC.

Bit 6 (HSDCEN) in the CONFIG register activates HSDC when set to 1. If Bit HSDCEN is cleared to 0, the default value, the HSDC interface is disabled. Setting Bit HSDCEN to 1 when SPI is in use does not have any effect. HSDC is an interface for sending to an external device (usually a microprocessor or a DSP) up to sixteen 32-bit words. The words represent the instantaneous values of the phase currents and voltages, neutral current, and active, reactive, and apparent powers. The registers being transmitted include IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. All are 24-bit registers that are sign extended to 32-bits (see Figure 37 for details). In the case of ADE7854 and ADE7858, the INWV register is not available. In its place, the HSDC transmits one 32-bit word always equal to 0. In addition, the AVAR, BVAR, and CVAR registers are not available in the ADE7854. In their place, the HSDC transmits three 32-bit words that are always equal to 0.

HSDC can be interfaced with SPI or similar interfaces. HSDC is always a master of the communication and consists of three pins: HSA, HSD, and HSCLK. HSA represents the select signal. It stays active low or high when a word is transmitted and it is usually connected to the select pin of the slave. HSD sends data to the slave and it is usually connected to the data input pin of the slave. HSCLK is the serial clock line that is generated by the ADE7854/ADE7858/ADE7868/ADE7878 and it is usually connected to the serial clock input of the slave. Figure 91 shows the connections between the ADE78xx HSDC and slave devices containing an SPI interface.

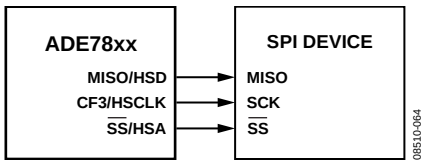

Figure 91. Connecting the ADE78xx HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG register (see Table 53). It is recommended to set the HSDC_CFG register to the desired value before enabling the port using Bit 6 (HSDCEN) in the CONFIG register. In this way, the state of various pins belonging to the HSDC port do not take levels inconsistent with the desired HSDC behavior. After a hardware reset or after power-up, the MISO/HSD and $\overline{SS}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK is 0 (the default value), the clock frequency is 8 MHz. When HCLK is 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit packages or as 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is 0 (the default value), the words are transmitted as 32-bit packages. When Bit HSIZE is 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words MSB first.

Bit 2 (HGAP) introduces a gap of seven HSCLK cycles between packages when Bit 2 (HGAP) is set to 1. When Bit HGAP is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication and a data bit is placed on the HSD line with every HSCLK high-to-low transition.

Bits[4:3] (HXFER[1:0]) decide how many words are transmitted. When HXFER[1:0] is 00, the default value, then all 16 words are transmitted. When HXFER[1:0] is 01, only the words representing the instantaneous values of phase and neutral currents and phase voltages are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and one 32-bit word that is always equal to INWV. When HXFER[1:0] is 10, only the instantaneous values of phase powers are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. The value, 11, for HXFER[1:0] is reserved and writing it is equivalent to writing 00, the default value.

Bit 5 (HSAPOL) determines the polarity of HSA function of the $\overline{SS}$/HSA pin during communication. When HSAPOL is 0 (the default value), HSA is active low during the communication. This means that HSA stays high when no communication is in progress. When a communication is executed, HSA is low when the 32-bit or 8-bit packages are transferred, and is high during the gaps. When HSAPOL is 1, the HSA function of the $\overline{SS}$/HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When a communication is executed, HSA is high when the 32-bit or 8-bit packages are transferred, and is low during the gaps.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written into these bits does not have any consequence on HSDC behavior.

Figure 92 shows the HSDC transfer protocol for HGAP = 0, HXFER[1:0] = 00 and HSAPOL = 0. Note that the HSDC interface sets a data bit on the HSD line every HSCLK high-to-low transition and the value of Bit HSIZE is irrelevant.

Downloaded from Arrow.com.

Figure 93 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 32-bit word.

Figure 94 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 8-bit word.

See Table 53 for the HSDC_CFG register and descriptions for the HCLK, HSIZE, HGAP, HXFER[1:0], and HSAPOL bits.

Table 24 lists the time it takes to execute an HSDC data transfer for all HSDC_CFG register settings. For some settings, the transfer time is less than 125 µs (8 kHz), the waveform sample registers update rate. This means the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125 µs, the HSDC port transmits data only in the first of two consecutive 8 kHz sampling cycles. This means it transmits registers at an effective rate of 4 kHz.

Table 24. Communication Times for Various HSDC Settings

HXFER[1:0]	HGAP	HSIZE[1]	HCLK	Communication Time (µs)
00	0	N/A	0	64
00	0	N/A	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	N/A	0	28
01	0	N/A	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	N/A	0	36
10	0	N/A	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

[1] N/A means not applicable.

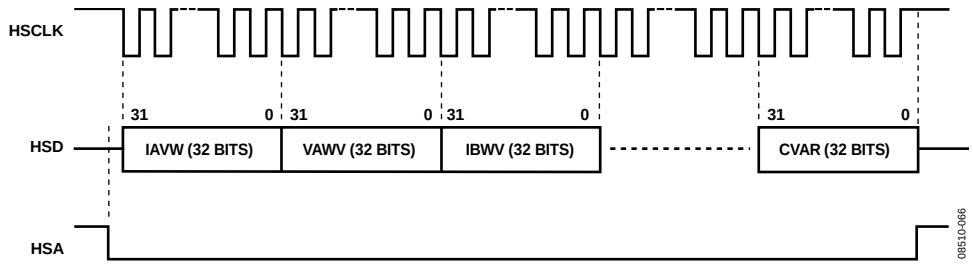

Figure 92. HSDC Communication for HGAP = 0, HXFER[1:0] = 00, and HSAPOL = 0; HSIZE Is Irrelevant

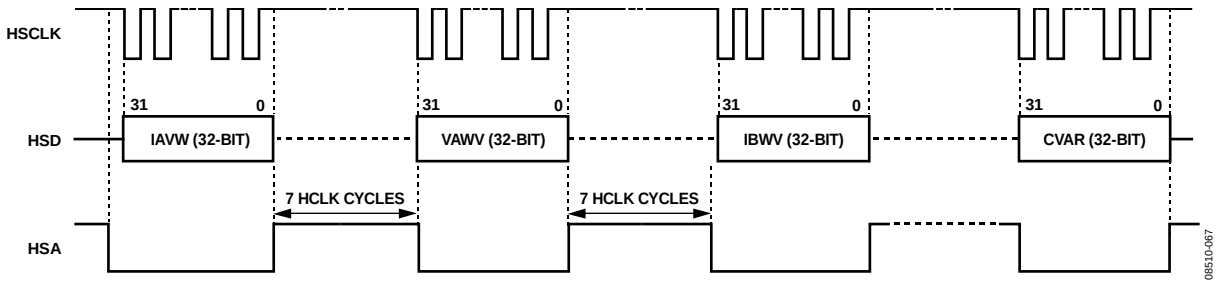

Figure 93. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

Downloaded from Arrow.com.

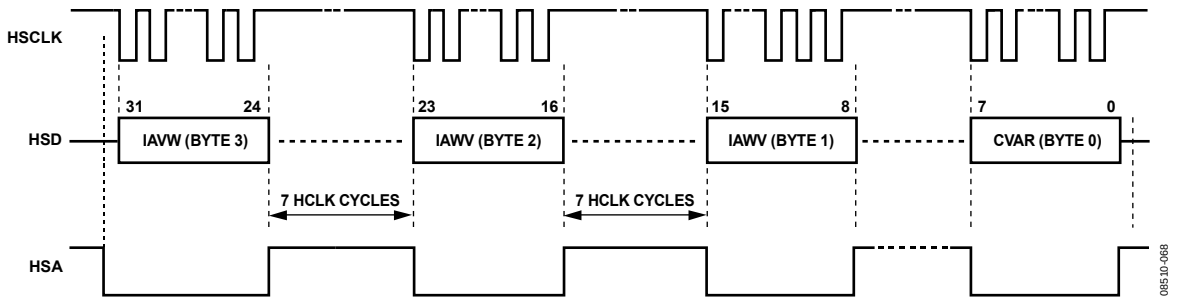

Figure 94. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

QUICK SETUP AS ENERGY METER

An energy meter is usually characterized by the nominal current I_n, nominal voltage V_n, nominal frequency f_n, and the meter constant MC.

To quickly setup the ADE7878, execute the following steps:

1. Select the PGA gains in the phase currents, voltages, and neutral current channels: Bits [2:0] (PGA1), Bits [5:3] (PGA2) and Bits [8:6] (PGA3) in the Gain register.
2. If Rogowski coils are used, enable the digital integrators in the phase and neutral currents: Bit 0 (INTEN) set to 1 in CONFIG register.
3. If f_n=60 Hz, set Bit 14 (SELFREQ) in COMPMODE register (ADE7878 only).
4. Initialize WTHR1 and WTHR0 registers based on Equation 25. Make VARTHR1 (ADE7858, ADE7868, and ADE7878 only) and VATHR1 equal to WTHR1 and VARTHR0 (ADE7858, ADE7868, and ADE7878 only) and VATHR0 equal to WTHR0.
5. Initialize CF1DEN, CF2DEN, and CF3DEN based on Equation 26.
6. Initialize VLEVEL (ADE7878 only) and VNOM registers based on Equation 21 and Equation 42.
7. Enable the data memory RAM protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
8. Start the DSP by setting Run=1.
9. Read the energy registers xWATTHR, xVARHR (ADE7858, ADE7868, and ADE7878 only), xVAHR, xFWATTHR, and xFVARHR (ADE7878 only) to erase their content and start energy accumulation from a known state.
10. Enable the CF1, CF2 and CF3 frequency converter outputs by clearing bits 9, 10 and 11 (CF1DIS, CF2DIS, and CF3DIS) to 0 in CFMODE register.

LAYOUT GUIDELINES

Figure 95 presents a basic schematic of the ADE7878 together with its surrounding circuitry: decoupling capacitors at pins VDD, AVDD, DVDD and $REF_{in/out}$, the 16.384 MHz crystal and its load capacitors. The rest of the pins are dependent on the particular application and are not shown here. The ADE7854, ADE7858 and ADE7868 have an identical approach to the decoupling capacitors, the crystal and its load capacitors.

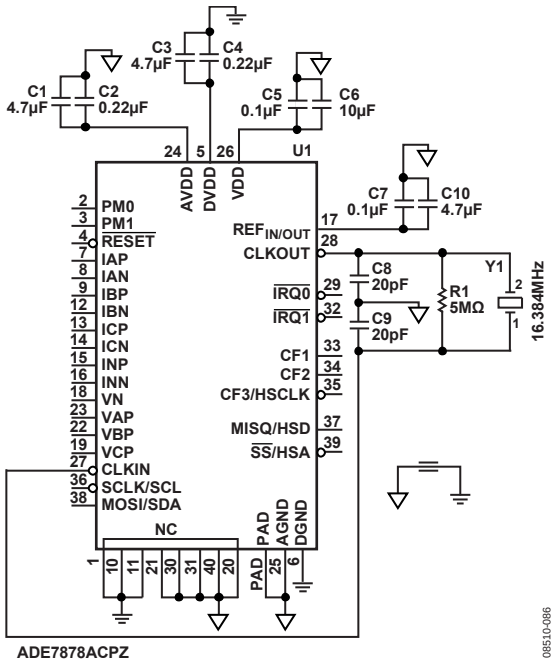

Figure 95. ADE7878 Crystal and Capacitors Connections

Figure 96 and Figure 97 present a proposed layout of a printed circuit board (PCB) with two layers that have the components placed only on the top of the board. Following these layout guidelines will help in creating a low noise design with higher immunity to EMC influences.

The VDD, AVDD, DVDD and $REF_{in/out}$ pins have each two decoupling capacitors, one of uF order and a ceramic one of 220nF or 100nF. These ceramic capacitors need to be placed the closest the the ADE7878 as they decouple high frequency noises, while the uF ones need to be placed in close proximity.

The crystal load capacitors need to be placed closest to the ADE7878, while the crystal can be placed in close proximity.

Downloaded from Arrow.com.

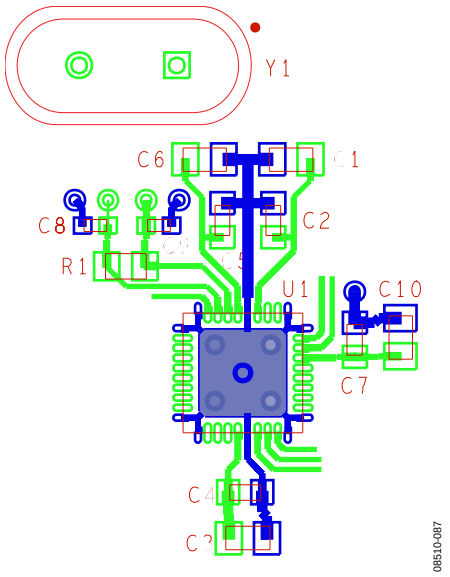

Figure 96. ADE7878 Top Layer Printed Circuit Board

The exposed pad of the ADE7878 is soldered to an equivalent pad on the PCB. The AGND and DGND traces of the ADE7878 are then routed directly into the PCB pad.

The bottom layer is composed mainly of a ground plane surrounding as much as possible the crystal traces.

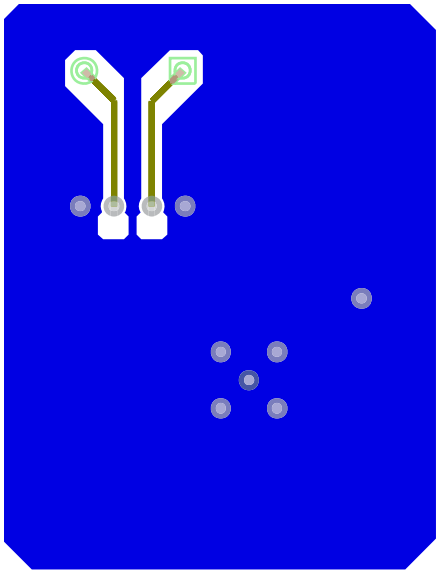

Figure 97. ADE7878 Bottom Layer Printed Circuit Board

CRYSTAL CIRCUIT

A digital clock signal of 16.384 MHz can be provided to the CLKIN pin of the ADE7854/ADE7858/ADE7868/ADE7878. Alternatively, attach a crystal of the specified frequency, as shown in Figure 98. CL_1 and CL_2 denote the capacitances of the ceramic capacitors attached to the crystal pins, whereas CP_1 and CP_2 denote the parasitic capacitances on those pins.

The recommended typical value of total capacitance at each clock pin, CLKIN and CLKOUT, is 24 pF, which means that

$$Total\ Capacitance = CP_1 + CL_1 = CP_2 + CL_2 = 24\ pF$$

Crystal manufacturer data sheets specify the load capacitance value. A total capacitance of 24 pF, per clock pin, is recommended; therefore, select a crystal with a 12 pF load capacitance. In addition, when selecting the ceramic capacitors, CL_1 and CL_2, the parasitic capacitances, CP_1 and CP_2, on the crystal pins of the IC must be taken into account. Thus, the values of CL_1 and CL_2 must be based on the following expression:

$$CL_1 = CL_2 = 2 \times Crystal\ Load\ Capacitance - CP_1$$

where $CP_1 = CP_2$.

For example, if a 12 pF crystal is chosen and the parasitic capacitances on the clock pins are $CP_1 = CP_2 = 2$ pF, the ceramic capacitors that must be used in the crystal circuit are $CL_1 = CL_2 = 22$ pF.

The Evaluation Board EVAL-ADE7878EBZ uses the crystal VM6-1D11C12-TR-16.384MHZ (maximum drive level 1 mW; maximum ESR 20 Ω; load capacitance 12 pF). It is recommended that the same crystal, or a crystal with similar specifications, be selected. Lower values of ESR and load capacitance and higher values of drive level capability of the crystal are preferable.

It is also recommended that a 5 MΩ resistor be attached in parallel to the crystal, as shown in Figure 98.

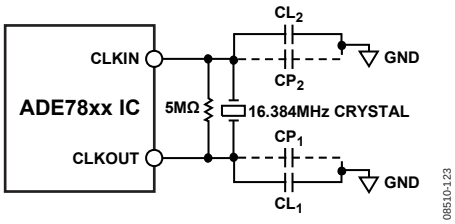

Figure 98. Crystal Circuit

ADE7878 EVALUATION BOARD

An evaluation board built upon the ADE7878 configuration supports all ADE7854, ADE7858, ADE7868, and ADE7878 components. Visit www.analog.com/ADE7878 for details.

DIE VERSION

The register named version identifies the version of the die. It is an 8-bit, read-only version register located at Address 0xE707.

Downloaded from Arrow.com.

SILICON ANOMALY

This anomaly list describes the known issues with the ADE7854, ADE7858, ADE7868, and ADE7878 silicon identified by the version register (Address 0xE707) being equal to 2, to 4, and to 5.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADE7854/ADE7858/ADE7868/ADE7878 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
Version = 2	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. A	4 (er001, er002, er003, er004)
Version = 4	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. B	1 (er005)
Version = 5	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. C	1 (er005)

FUNCTIONALITY ISSUES

Table 25. Offset RMS Registers Cannot be Set to Negative Values [er001, Version = 2 Silicon]

Background	When the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers are set to a negative value, for sufficiently small inputs, the argument of the square root used in the rms data path may become negative. In this case, the corresponding AIRMS, AVRMS, BIRMS, BVRMS, CIRMS, or CVRMS rms register is automatically set to 0.
Issue	Negative values for the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers are not supported in the silicon version identified by the version register being equal to 2.
Workaround	Do not use negative values for the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers. If further details on this issue are required, please use the following website to submit your query: www.analog.com/en/content/technical_support_page/fca.html.
Related Issues	None.

Downloaded from Arrow.com.

Table 26. Values Written to the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT Registers May Not Be Immediately Used By ADE7854, ADE7858, ADE7868, ADE7878 [er002, Version = 2 Silicon]

Background	Usually, the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT registers initialize immediately after power-up or after a hardware/software reset. After the RUN register is set to 1, the energy-to-frequency converter (for CF1DEN, CF2DEN, and CF3DEN), the phase voltage sag detector (for SAGLVL), and the zero-crossing timeout circuit (for ZXTOUT) use these values immediately.
Issue	After the CF1DEN register is initialized with a new value after power-up or a hardware/software reset, the new value may be delayed and, therefore, not immediately available for use by the energy-to-frequency converter. It is, however, used by the converter after the first high-to-low transition is triggered at t the CF1 pin using the CF1DEN default value (0x0). CF2DEN and CF3DEN registers present similar behavior at the CF2 and CF3 pins, respectively. CF1DEN, CF2DEN and CF3DEN above behavior has been corrected in Version = 4 silicon. After the SAGLVL register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the phase voltage sag detector. However, it is used by the detector after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs. After the ZXTOUT register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the zero-crossing timeout circuit. However, the circuit does use the new value after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs.
Workaround	If the behavior outlined in the Issue row does not conflict with the meter specification, then the new values of the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT registers may be written one time only. If the behavior is not acceptable, write the new value into the CF1DEN, CF2DEN, and CF3DEN registers eight consecutive times. This ensures the probability of the new value not being considered immediately by the energy-to-frequency converter becomes lower than 0.2 ppm. Usually, at least one of the phase voltages is greater than 10% of full scale after power-up or after a hardware/software reset. If this cannot be guaranteed, then the SAGLVL and ZXTOUT registers should also be written eight consecutive times to reduce the probability of not being considered immediately by the phase voltage sag detector and zero-crossing timeout circuit.
Related Issues	None.

Table 27. The Read-Only RMS Registers May Show the Wrong Value [er003, Version = 2 Silicon]

Background	The read-only rms registers (AVRMS, BVRMS, CVRMS, AIRMS, BIRMS, CIRMS, and NIRMS) can be read without restrictions at any time.
Issue	The fixed function DSP of ADE7854, ADE7858, ADE7868, and ADE7878 computes all the powers and rms values in a loop with a period of 125 µs (8 kHz frequency). If two rms registers are accessed (read) consecutively, the value of the second register may be corrupted. Consequently, the apparent power computed during that 125 µs cycle is also corrupted. The rms calculation recovers in the next 125 µs cycle, and all the rms and apparent power values compute correctly. The issue appears independent of the communication type, SPI or I^2C, when the time between the start of two consecutive rms readings is lower than 265 µs. The issue affects only the rms registers; all of the other registers of ADE7854, ADE7858, ADE7868, and ADE7878 can be accessed without any restrictions.
Workaround	The rms registers can be read one at a time with at least 265 µs between the start of the readings. DREADY interrupt at the $\overline{IRQ0}$ pin can be used to time one rms register reading every three consecutive DREADY interrupts. This ensures 375 µs between the start of the rms readings. Alternatively, the rms registers can be read interleaved with readings of other registers that are not affected by this restriction as long as the time between the start of two consecutive rms register readings is 265 µs.
Related Issues	None.

Table 28. To Obtain Best Accuracy Performance, Internal Setting Must Be Changed [er004, Version = 2 Silicon]

Background	Internal default settings provide best accuracy performance for ADE7854, ADE7858, ADE7868, and ADE7878.
Issue	It was found that if a different setting is used, the accuracy performance can be improved.
Workaround	To enable a new setting for this internal register, execute two consecutive 8-bit register write operations: The first write operation: 0xAD is written to Address 0xE7FE. The second write operation: 0x01 is written to Address 0xE7E2. The write operations must be executed consecutively without any other read/write operation in between. As a verification that the value was captured correctly, a simple 8-bit read of Address 0xE7E2 should show the 0x01 value.
Related Issues	None.

Downloaded from Arrow.com.

Table 29. Values Written to the SAGLVL and ZXTOUT Registers May Not Be Immediately Used by ADE7854, ADE7858, ADE7868, and ADE7878 [er005, Version = 4 and Version = 5 Silicons]

Background	Usually, the SAGLVL and ZXTOUT registers initialize immediately after power-up or after a hardware/software reset. After the run register is set to 1, the phase voltage sag detector (for SAGLVL), and the zero-crossing timeout circuit (for ZXTOUT) use these values immediately.
Issue	After the SAGLVL register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the phase voltage sag detector. However, it is used by the detector after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs. After the ZXTOUT register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the zero-crossing timeout circuit. However, the circuit does use the new value after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs.
Workaround	Usually, at least one of the phase voltages is greater than 10% of full scale after power-up or after a hardware/software reset. If this cannot be guaranteed, then the SAGLVL and ZXTOUT registers should be written eight consecutive times to reduce the probability of not being considered immediately by the phase voltage sag detector and zero-crossing timeout circuit below 0.2 ppm.
Related Issues	None.

SECTION 1. ADE7854/ADE7858/ADE7868/ADE7878 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Offset rms registers cannot be set to negative values.	Identified
er002	Values written to the CF1DEN, CF2DEN, CF2DEN, SAGLVL, and ZXTOUT registers may not be immediately used by ADE7854, ADE7858, ADE7868, and ADE7878.	Identified
er003	The read-only rms registers may show the wrong value.	Identified
er004	To obtain best accuracy performance, internal setting must be changed.	Identified
er005	Values written to the SAGLVL and ZXTOUT registers may not be immediately used by ADE7854, ADE7858, ADE7868, and ADE7878.	Identified

This completes the Silicon Anomaly section.

Downloaded from Arrow.com.

REGISTERS LIST

Table 30. Registers List Located in DSP Data Memory RAM

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4383	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4384	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4385	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4386	NIGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral current gain adjust (ADE7868 and ADE7878 only).
0x4387	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x4388	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x4389	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x438A	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x438B	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x438C	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x438D	NIRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset (ADE7868 and ADE7878 only).
0x438E	AVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A apparent power gain adjust.
0x438F	BVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B apparent power gain adjust.
0x4390	CVAGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C apparent power gain adjust.
0x4391	AWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A total active power gain adjust.
0x4392	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x4393	BWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B total active power gain adjust.
0x4394	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x4395	CWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C total active power gain adjust.
0x4396	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x4397	AVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A total reactive power gain adjust (ADE7858, ADE7868, and ADE7878).
0x4398	AVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A total reactive power offset adjust (ADE7858, ADE7868, and ADE7878).
0x4399	BVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B total reactive power gain adjust (ADE7858, ADE7868, and ADE7878).
0x439A	BVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B total reactive power offset adjust (ADE7858, ADE7868, and ADE7878).
0x439B	CVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C total reactive power gain adjust (ADE7858, ADE7868, and ADE7878).
0x439C	CVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C total reactive power offset adjust (ADE7858, ADE7868, and ADE7878).
0x439D	AFWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power gain adjust. Location reserved for ADE7854, ADE7858, and ADE7868.
0x439E	AFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power offset adjust. Location reserved for ADE7854, ADE7858, and ADE7868.
0x439F	BFWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power gain adjust (ADE7878 only).
0x43A0	BFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power offset adjust (ADE7878 only).
0x43A1	CFWGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power gain adjust.
0x43A2	CFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power offset adjust (ADE7878 only).

Downloaded from Arrow.com.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43A3	AFVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power gain adjust (ADE7878 only).
0x43A4	AFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power offset adjust (ADE7878 only).
0x43A5	BFVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power gain adjust (ADE7878 only).
0x43A6	BFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power offset adjust (ADE7878 only).
0x43A7	CFVARGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power gain adjust (ADE7878 only).
0x43A8	CFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power offset adjust (ADE7878 only).
0x43A9	VATHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of VATHR[47:0] threshold used in phase apparent power datapath.
0x43AA	VATHR0	R/W	24	32 ZP	U	0x000000	Less significant 24 bits of VATHR[47:0] threshold used in phase apparent power datapath.
0x43AB	WTHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of WTHR[47:0] threshold used in phase total/fundamental active power datapath.
0x43AC	WTHR0	R/W	24	32 ZP	U	0x000000	Less significant 24 bits of WTHR[47:0] threshold used in phase total/fundamental active power datapath.
0x43AD	VARTHR1	R/W	24	32 ZP	U	0x000000	Most significant 24 bits of VARTHR[47:0] threshold used in phase total/fundamental reactive power datapath (ADE7858, ADE7868, and ADE7878).
0x43AE	VARTHR0	R/W	24	32 ZP	U	0x000000	Less significant 24 bits of VARTHR[47:0] threshold used in phase total/fundamental reactive power datapath (ADE7858, ADE7868, and ADE7878).
0x43AF	Reserved	N/A[4]	N/A[4]	N/A[4]	N/A[4]	0x000000	This memory location should be kept at 0x000000 for proper operation.
0x43B0	VANOLOAD	R/W	24	32 ZPSE	S	0x0000000	No load threshold in the apparent power datapath.
0x43B1	APNOLOAD	R/W	24	32 ZPSE	S	0x0000000	No load threshold in the total/fundamental active power datapath.
0x43B2	VARNOLOAD	R/W	24	32 ZPSE	S	0x0000000	No load threshold in the total/fundamental reactive power datapath. Location reserved for ADE7854.
0x43B3	VLEVEL	R/W	24	32 ZPSE	S	0x000000	Register used in the algorithm that computes the fundamental active and reactive powers (ADE7878 only).
0x43B4	Reserved	N/A[4]	N/A[4]	N/A[4]	N/A[4]	0x000000	This location should not be written for proper operation.
0x43B5	DICOEFF	R/W	24	32 ZPSE	S	0x0000000	Register used in the digital integrator algorithm. If the integrator is turned on, it must be set at 0xFF8000. In practice, it is transmitted as 0xFFF8000.
0x43B6	HPFDIS	R/W	24	32 ZP	U	0x000000	Disables/enables the HPF in the current datapath (see Table 34).
0x43B7	Reserved	N/A[4]	N/A[4]	N/A[4]	N/A[4]	0x000000	This memory location should be kept at 0x000000 for proper operation.
0x43B8	ISUMLVL	R/W	24	32 ZPSE	S	0x000000	Threshold used in comparison between the sum of phase currents and the neutral current (ADE7868 and ADE7878 only).

Downloaded from Arrow.com.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43B9 to 0x43BE	Reserved	N/A[4]	N/A[4]	N/A[4]	N/A[4]	0x000000	These memory locations should be kept at 0x000000 for proper operation.
0x43BF	ISUM	R	28	32 ZP	S	N/A[4]	Sum of IAWV, IBWV, and ICWV registers (ADE7868 and ADE7878 only).
0x43C0	AIRMS	R	24	32 ZP	S	N/A[4]	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	N/A[4]	Phase A voltage rms value.
0x43C2	BIRMS	R	24	32 ZP	S	N/A[4]	Phase B current rms value.
0x43C3	BVRMS	R	24	32 ZP	S	N/A[4]	Phase B voltage rms value.
0x43C4	CIRMS	R	24	32 ZP	S	N/A[4]	Phase C current rms value.
0x43C5	CVRMS	R	24	32 ZP	S	N/A[4]	Phase C voltage rms value.
0x43C6	NIRMS	R	24	32 ZP	S	N/A[4]	Neutral current rms value (ADE7868 and ADE7878 only).
0x43C7 to 0x43FF	Reserved	N/A[4]	N/A[4]	N/A[4]	N/A[4]	N/A[4]	These memory locations should not be written for proper operation.

[1] R is read, and W is write.
[2] 32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits. Whereas 32 ZP = 28- or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four MSBs or eight MSBs, respectively, padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A means not applicable.

Table 31. Internal DSP Memory RAM Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	16	U	0x0000	This memory location should not be written for proper operation.
0xE228	Run	R/W	16	16	U	0x0000	Run register starts and stops the DSP. See the Digital Signal Processor section for more details.

[1] R is read, and W is write.
[2] U is unsigned register, and S is signed register in twos complement format.

Table 32. Billable Registers

Address	Register Name	R/W[1, 2]	Bit Length[2]	Bit Length During Communication[2]	Type[2, 3]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation.
0xE403	AFWATTHR	R	32	32	S	0x00000000	Phase A fundamental active energy accumulation (ADE7878 only).
0xE404	BFWATTHR	R	32	32	S	0x00000000	Phase B fundamental active energy accumulation (ADE7878 only).
0xE405	CFWATTHR	R	32	32	S	0x00000000	Phase C fundamental active energy accumulation (ADE7878 only).
0xE406	AVARHR	R	32	32	S	0x00000000	Phase A total reactive energy accumulation (ADE7858, ADE7868, and ADE7878 only).
0xE407	BVARHR	R	32	32	S	0x00000000	Phase B total reactive energy accumulation (ADE7858, ADE7868, and ADE7878 only).
0xE408	CVARHR	R	32	32	S	0x00000000	Phase C total reactive energy accumulation (ADE7858, ADE7868, and ADE7878 only).
0xE409	AFVARHR	R	32	32	S	0x00000000	Phase A fundamental reactive energy accumulation (ADE7878 only).
0xE40A	BFVARHR	R	32	32	S	0x00000000	Phase B fundamental reactive energy accumulation (ADE7878 only).
0xE40B	CFVARHR	R	32	32	S	0x00000000	Phase C fundamental reactive energy accumulation (ADE7878 only).

Downloaded from Arrow.com.

Address	Register Name	R/W[1, 2]	Bit Length[2]	Bit Length During Communication[2]	Type[2, 3]	Default Value	Description
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R is read, and W is write.
[2] N/A is not applicable.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 33. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register. See Figure 50 and Table 35 for details about its composition.
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register. See Figure 50 and Table 36 for details about its composition.
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0. See Table 37.
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1. See Table 38.
0xE504	AIMAV	R	20	32 ZP	U	N/A	Phase A current mean absolute value computed during PSM0 and PSM1 modes (ADE7868 and ADE7878 only).
0xE505	BIMAV	R	20	32 ZP	U	N/A	Phase B current mean absolute value computed during PSM0 and PSM1 modes (ADE7868 and ADE7878 only).
0xE506	CIMAV	R	20	32 ZP	U	N/A	Phase C current mean absolute value computed during PSM0 and PSM1 modes (ADE7868 and ADE7878 only).
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage SAG level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0. See Table 39.
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1. See Table 40.
0xE50C	IAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C current.
0xE50F	INWV	R	24	32 SE	S	N/A	Instantaneous value of neutral current (ADE7868 and ADE7878 only).
0xE510	VAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C voltage.
0xE513	AWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase A total active power.
0xE514	BWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase B total active power.
0xE515	CWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase C total active power.
0xE516	AVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase A total reactive power (ADE7858, ADE7868, and ADE7878 only).
0xE517	BVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase B total reactive power (ADE7858, ADE7868, and ADE7878 only).
0xE518	CVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase C total reactive power (ADE7858, ADE7868, and ADE7878 only).

Downloaded from Arrow.com.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE519	AVA	R	24	32 SE	S	N/A	Instantaneous value of Phase A apparent power.
0xE51A	BVA	R	24	32 SE	S	N/A	Instantaneous value of Phase B apparent power.
0xE51B	CVA	R	24	32 SE	S	N/A	Instantaneous value of Phase C apparent power.
0xE51F	CHECKSUM	R	32	32	U	0x33666787	Checksum verification. See the Checksum Register section for details.
0xE520	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power. When the VNOMxEN bit is set, the applied voltage input in the corresponding phase is ignored and all corresponding rms voltage instances are replaced by the value in the VNOM register.
0xE521 to 0xE52E	Reserved						These addresses should not be written for proper operation.
0xE600	PHSTATUS	R	16	16	U	N/A	Phase peak register. See Table 41.
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0. See the Time Interval Between Phases section for details.
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1. See the Time Interval Between Phases section for details.
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2. See the Time Interval Between Phases section for details.
0xE604 to 0xE606	Reserved						These addresses should not be written for proper operation.
0xE607	PERIOD	R	16	16	U	N/A	Network line period.
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no load register. See Table 42.
0xE609 to 0xE60B	Reserved						These addresses should not be written for proper operation.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation-mode register. See Table 43.
0xE60F	Gain	R/W	16	16	U	0x0000	PGA gains at ADC inputs. See Table 44.
0xE610	CFMODE	R/W	16	16	U	0x0E88	CFx configuration register. See Table 45.
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase A. See Table 46.
0xE615	BPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase B. See Table 46.
0xE616	CPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase C. See Table 46.
0xE617	PHSIGN	R	16	16	U	N/A	Power sign register. See Table 47.
0xE618	CONFIG	R/W	16	16	U	0x0000	ADE7878 configuration register. See Table 48.
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register. See Table 49.
0xE701	ACCMODE	R/W	8	8	U	0x00	Accumulation mode register. See Table 50.
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior. See Table 52.
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	SAG detection half line cycles.

Downloaded from Arrow.com.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches. See the Synchronizing Energy Registers with CFx Outputs section.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register. See Table 53.
0xE707	Version	R	8	8	U		Version of die.
0xEBFF	Reserved		8	8			This address can be used in manipulating the $\overline{SS}$/HSA pin when SPI is chosen as the active port. See the Serial Interfaces section for details.
0xEC00	LPOILVL	R/W	8	8	U	0x07	Overcurrent threshold used during PSM2 mode (ADE7868 and ADE7878 only). See Table 54 in which the register is detailed.
0xEC01	CONFIG2	R/W	8	8	U	0x00	Configuration register used during PSM1 mode. See Table 55.

[1] R is read, and W is write.
[2] 32 ZP = 24- or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, padded with 0s. 32 SE = 24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits. 16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word with six MSBs padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A is not applicable.

Table 34. HPFDIS Register (Address 0x43B6)

Bit Location	Default Value	Description
23:0	00000000	When HPFDIS = 0x00000000, then all high-pass filters in voltage and current channels are enabled. When the register is set to any nonzero value, all high-pass filters are disabled.

Table 35. IPEAK Register (Address 0xE500)

Bit Location	Bit Mnemonic	Default Value	Description
23:0	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, Phase A current generated IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, Phase B current generated IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, Phase C current generated IPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 36. VPEAK Register (Address 0xE501)

Bit Location	Bit Mnemonic	Default Value	Description
23:0	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, Phase A voltage generated VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, Phase B voltage generated VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, Phase C voltage generated VPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 37. STATUS0 Register (Address 0xE502)

Bit Location	Bit Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.
1	FAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental active energy registers, FWATTHR, BFWATTHR, or CFWATTHR, has changed. This bit is always 0 for ADE7854, ADE7858, and ADE7868.
2	REHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total reactive energy registers (AVARHR, BVARHR, or CVARHR) has changed. This bit is always 0 for ADE7854.

Downloaded from Arrow.com.

Bit Location	Bit Mnemonic	Default Value	Description
3	FREHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental reactive energy registers, AFVARHR, BFVARHR, or CFVARHR, has changed. This bit is always 0 for ADE7854, ADE7858, and ADE7868.
4	VAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it indicates the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it indicates that the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 47).
7	REVAPB	0	When this bit is set to 1, it indicates that the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN register (see Table 47).
8	REVAPC	0	When this bit is set to 1, it indicates that the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 47).
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 datapath has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 47).
10	REVRPA	0	When this bit is set to 1, it indicates that the Phase A reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 4 (AVARSIGN) of the PHSIGN register (see Table 47). This bit is always 0 for ADE7854.
11	REVRPB	0	When this bit is set to 1, it indicates that the Phase B reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 5 (BVARSIGN) of the PHSIGN register (see Table 47). This bit is always 0 for ADE7854.
12	REVRPC	0	When this bit is set to 1, it indicates that the Phase C reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 6 (CVARSIGN) of the PHSIGN register (see Table 47). This bit is always 0 for ADE7854.
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 datapath has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 47).
14	CF1		When this bit is set to 1, it indicates a high to low transition has occurred at CF1 pin; that is, an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 45).
15	CF2		When this bit is set to 1, it indicates a high-to-low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 45).
16	CF3		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF3 pin; that is, an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 45).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (at 8 kHz rate) DSP computations have finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 datapath has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 47).
31:19	Reserved	0 0000 0000 0000	Reserved. These bits are always 0.

Downloaded from Arrow.com.

Table 38. STATUS1 Register (Address 0xE503)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on total active and reactive powers. The phase is indicated in Bits[2:0] (NLPHASE[x]) in the PHNOLOAD register (see Table 42).
1	FNLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on fundamental active and reactive powers. The phase is indicated in Bits[5:3] (FNLPHASE[x]) in PHNOLOAD register (see Table 42 in which this register is described). This bit is always 0 for ADE7854, ADE7858, and ADE7868.
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on apparent power. The phase is indicated in Bits[8:6] (VANLPHASE[x]) in the PHNOLOAD register (see Table 42).
3	ZXTOVA	0	When this bit is set to 1, it indicates a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C current.
15	RSTDONE	1	In case of a software reset command, Bit 7 (SWRST) is set to 1 in the CONFIG register, or a transition from PSM1, PSM2, or PSM3 to PSM0, or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers changed value to default. The $\overline{\text{IRQ1}}$ pin goes low to signal this moment because this interrupt cannot be disabled.
16	SAG	0	When this bit is set to 1, it indicates a SAG event has occurred on one of the phases indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 41).
17	OI	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 41).
18	OV	0	When this bit is set to 1, it indicates an overvoltage event has occurred on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 41).
19	SEQERR	0	When this bit is set to 1, it indicates a negative-to-positive zero crossing on Phase A voltage was not followed by a negative-to-positive zero crossing on Phase B voltage but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it indicates $\left\|\|ISUM\| - \|INWV\right\| > ISUMLVL$, where *ISUMLVL* is indicated in the ISUMLVL register. This bit is always 0 for ADE7854 and ADE7858.
21	Reserved	1	Reserved. This bit is always set to 1.
22	Reserved	0	Reserved. This bit is always set to 0.
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. The IPEAK register contains the peak value and the phase where the peak has been detected (see Table 35).
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. VPEAK register contains the peak value and the phase where the peak has been detected (see Table 36).
31:25	Reserved	000 0000	Reserved. These bits are always 0.

Downloaded from Arrow.com.

Table 39. MASK0 Register (Address 0xE50A)

Bit Location	Bit Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) changes.
1	FAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental active energy registers (AFWATTHR, BFWATTHR, or CFWATTHR) changes. Setting this bit to1 does not have any consequence for ADE7854, ADE7858, and ADE7868.
2	REHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total reactive energy registers (AVARHR, BVARHR, CVARHR) changes. Setting this bit to1 does not have any consequence for ADE7854.
3	FREHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR) changes. Setting this bit to1 does not have any consequence for ADE7854, ADE7858, and ADE7868.
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) changes.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
8	REVAPC	0	When this bit is set to 1, it enables an interrupt when the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 datapath changes sign.
10	REVRPA	0	When this bit is set to 1, it enables an interrupt when the Phase A reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign. Setting this bit to1 does not have any consequence for ADE7854.
11	REVRPB	0	When this bit is set to 1, it enables an interrupt when the Phase B reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign. Setting this bit to1 does not have any consequence for ADE7854.
12	REVRPC	0	When this bit is set to 1, it enables an interrupt when the Phase C reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total or fundamental) changes sign. Setting this bit to1 does not have any consequence for ADE7854.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 datapath changes sign.
14	CF1		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at the CF1 pin, that is, an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 45).
15	CF2		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at CF2 pin, that is, an active low pulse is generated. The interrupt may be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 45).
16	CF3		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF3 pin, that is, an active low pulse is generated. The interrupt may be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 45).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (at 8 kHz rate) DSP computations finish.
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 datapath changes sign.
31:19	Reserved	00 0000 0000 0000	Reserved. These bits do not manage any functionality.

Downloaded from Arrow.com.

Table 40. MASK1 Register (Address 0xE50B)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on total active and reactive powers.
1	FNLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on fundamental active and reactive powers. Setting this bit to 1 does not have any consequence for ADE7854, ADE7858, and ADE7868.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached. It can be set to 1 or cleared to 0 without having any effect.
16	SAG	0	When this bit is set to 1, it enables an interrupt when a SAG event occurs on one of the phases indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 41).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 41).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overvoltage event occurs on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 41).
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative-to-positive zero crossing on Phase A voltage is not followed by a negative-to-positive zero crossing on Phase B voltage, but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it enables an interrupt when $\left\|\|ISUM\| - \|INWV\right\| > ISUMLVL$ is greater than the value indicated in ISUMLVL register. Setting this bit to1 does not have any consequence for ADE7854 and ADE7858.
22:21	Reserved	00	Reserved. These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
31:25	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Downloaded from Arrow.com.

Table 41. PHSTATUS Register (Address 0xE600)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	Reserved	000	Reserved. These bits are always 0.
3	OIPHASE[0]	0	When this bit is set to 1, Phase A current generates Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, Phase B current generates Bit 17 (OI) in the STATUS1 register.
5	OIPHASE[2]	0	When this bit is set to 1, Phase C current generates Bit 17 (OI) in the STATUS1 register.
8:6	Reserved	000	Reserved. These bits are always 0.
9	OVPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 18 (OV) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit 18 (OV) in the STATUS1 register.
12	VSPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 16 (SAG) in the STATUS1 register.
13	VSPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 16 (SAG) in the STATUS1 register.
14	VSPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit16 (SAG) in the STATUS1 register.
15	Reserved	0	Reserved. This bit is always 0.

Table 42. PHNOLOAD Register (Address 0xE608)

Bit Location	Bit Mnemonic	Default Value	Description
0	NLPHASE[0]	0	0: Phase A is out of no load condition based on total active/reactive powers. 1: Phase A is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register. The ADE7854 no load condition is based only on the total active powers.
1	NLPHASE[1]	0	0: Phase B is out of no load condition based on total active/reactive powers. 1: Phase B is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register. The ADE7854 no load condition is based only on the total active powers.
2	NLPHASE[2]	0	0: Phase C is out of no load condition based on total active/reactive powers. 1: Phase C is in no load condition based on total active/reactive powers. Bit set together with Bit 0 (NLOAD) in the STATUS1 register. The ADE7854 no load condition is based only on the total active powers.
3	FNLPHASE[0]	0	0: Phase A is out of no load condition based on fundamental active/reactive powers. This bit is always 0 for ADE7854, ADE7858, and ADE7868. 1: Phase A is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
4	FNLPHASE[1]	0	0: Phase B is out of no load condition based on fundamental active/reactive powers. This bit is always 0 for ADE7854, ADE7858, and ADE7868. 1: Phase B is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
5	FNLPHASE[2]	0	0: Phase C is out of no load condition based on fundamental active/reactive powers. This bit is always 0 for ADE7854, ADE7858, and ADE7868. 1: Phase C is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
6	VANLPHASE[0]	0	0: Phase A is out of no load condition based on apparent power. 1: Phase A is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of no load condition based on apparent power. 1: Phase B is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
8	VANLPHASE[2]	0	0: Phase C is out of no load condition based on apparent power. 1: Phase C is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Downloaded from Arrow.com.

Table 43. COMPMODE Register (Address 0xE60E)

Bit Location	Bit Mnemonic	Default Value	Description
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] to 1 signifies the sum of all three phases is included in the CF1 output. Phase A is included in the CF1 outputs calculations.
1	TERMSEL1[1]	1	Phase B is included in the CF1 outputs calculations.
2	TERMSEL1[2]	1	Phase C is included in the CF1 outputs calculations.
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] to 1 signifies the sum of all three phases is included in the CF2 output. Phase A is included in the CF2 outputs calculations.
4	TERMSEL2[1]	1	Phase B is included in the CF2 outputs calculations.
5	TERMSEL2[2]	1	Phase C is included in the CF2 outputs calculations.
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] to 1 signifies the sum of all three phases is included in the CF3 output. Phase A is included in the CF3 outputs calculations.
7	TERMSEL3[1]	1	Phase B is included in the CF3 outputs calculations.
8	TERMSEL3[2]	1	Phase C is included in the CF3 outputs calculations.
10:9	ANGLESEL[1:0]	00	00: the angles between phase voltages and phase currents are measured. 01: the angles between phase voltages are measured. 10: the angles between phase currents are measured. 11: no angles are measured.
11	VNOMAEN	0	When this bit is 0, the apparent power on Phase A is computed regularly. When this bit is 1, the apparent power on Phase A is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase A voltage input is ignored, and all Phase A rms voltage instances are replaced by the value in the VNOM register.
12	VNOMBEN	0	When this bit is 0, the apparent power on Phase B is computed regularly. When this bit is 1, the apparent power on Phase B is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase B voltage input is ignored, and all Phase B rms voltage instances are replaced by the value in the VNOM register.
13	VNOMCEN	0	When this bit is 0, the apparent power on Phase C is computed regularly. When this bit is 1, the apparent power on Phase C is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase C voltage input is ignored, and all Phase C rms voltage instances are replaced by the value in the VNOM register.
14	SELFREQ	0	When the ADE7878 is connected to 50 Hz networks, this bit should be cleared to 0 (default value). When the ADE7878 is connected to 60 Hz networks, this bit should be set to 1. This bit does not have any consequence for ADE7854, ADE7858, and ADE7868.
15	Reserved	0	This bit is 0 by default and it does not manage any functionality.

Table 44. Gain Register (Address 0xE60F)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	PGA1[2:0]	000	Phase currents gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like PGA1[2:0] = 000.
5:3	PGA2[2:0]	000	Neutral current gain selection. 000: gain = 1. These bits are always 000 for ADE7854 and ADE7858. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7868/ADE7878 behave like PGA2[2:0] = 000.

Downloaded from Arrow.com.

8:6	PGA3[2:0]	000	Phase voltages gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like PGA3[2:0] = 000.
15:9	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 45. CFMODE Register (Address 0xE610)

Bit Location	Bit Mnemonic	Default Value	Description
2:0	CF1SEL[2:0]	000	000: the CF1 frequency is proportional to the sum of total active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 001: the CF1 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854. 010: the CF1 frequency is proportional to the sum of apparent powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 011: the CF1 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 100: the CF1 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 101, 110, 111: reserved. When set, the CF1 signal is not generated.
5:3	CF2SEL[2:0]	001	000: the CF2 frequency is proportional to the sum of total active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 001: the CF2 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854. 010: the CF2 frequency is proportional to the sum of apparent powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 011: the CF2 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 100: the CF2 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 101,110,111: reserved. When set, the CF2 signal is not generated.
8:6	CF3SEL[2:0]	010	000: the CF3 frequency is proportional to the sum of total active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 001: the CF3 frequency is proportional to the sum of total reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854. 010: the CF3 frequency is proportional to the sum of apparent powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 011: CF3 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 100: CF3 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. This condition does not have any consequence for the ADE7854, ADE7858, and ADE7868. 101,110,111: reserved. When set, the CF3 signal is not generated.
9	CF1DIS	1	When this bit is set to 1, the CF1 output is disabled. The respective digital to frequency converter remains enabled even if CF1DIS = 1. When this bit is set to 0, the CF1 output is enabled.

Downloaded from Arrow.com.

Bit Location	Bit Mnemonic	Default Value	Description
10	CF2DIS	1	When this bit is set to 1, the CF2 output is disabled. The respective digital to frequency converter remains enabled even if CF2DIS = 1. When this bit is set to 0, the CF2 output is enabled.
11	CF3DIS	1	When this bit is set to 1, the CF3 output is disabled. The respective digital to frequency converter remains enabled even if CF3DIS = 1. When this bit is set to 0, the CF3 output is enabled.
12	CF1LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF1 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
13	CF2LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF2 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
14	CF3LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF3 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
15	Reserved	0	Reserved. This bit does not manage any functionality.

Table 46. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, Address 0xE616)

Bit Location	Bit Mnemonic	Default Value	Description
9:0	PHCALVAL	0000000000	If the current leads the voltage, these bits can vary only between 0 and 383. If the current lags the voltage, these bits can vary only between 512 and 575. If the PHCALVAL bits are set with numbers between 384 and 511, the compensation behaves like PHCALVAL set between 256 and 383. If the PHCALVAL bits are set with numbers between 576 and 1023, the compensation behaves like PHCALVAL bits set between 384 and 511.
15:10	Reserved	000000	Reserved. These bits do not manage any functionality.

Table 47. PHSIGN Register (Address 0xE617)

Bit Location	Bit Mnemonic	Default Value	Description
0	AWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
1	BWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
2	CWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. 1: if the active power identified by Bit 6 (REVAPSEL) bit in the ACCMODE register (total of fundamental) on Phase C is negative.
3	SUM1SIGN	0	0: if the sum of all phase powers in the CF1 datapath is positive. 1: if the sum of all phase powers in the CF1 datapath is negative. Phase powers in the CF1 datapath are identified by Bits[2:0] (TERMSEL1[x]) of the COMPMODE register and by Bits[2:0] (CF1SEL[x]) of the CFMODE register.
4	AVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. This bit is always 0 for ADE7854. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
5	BVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. This bit is always 0 for ADE7854. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
6	CVARSIGN	0	0: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. This bit is always 0 for ADE7854. 1: if the reactive power identified by Bit 7 (REVRPSEL) in the ACCMODE register (total of fundamental) on Phase C is negative.

Downloaded from Arrow.com.

Bit Location	Bit Mnemonic	Default Value	Description
7	SUM2SIGN	0	0: if the sum of all phase powers in the CF2 datapath is positive. 1: if the sum of all phase powers in the CF2 datapath is negative. Phase powers in the CF2 datapath are identified by Bits[5:3] (TERMSEL2[x]) of the COMPMODE register and by Bits[5:3] (CF2SEL[x]) of the CFMODE register.
8	SUM3SIGN	0	0: if the sum of all phase powers in the CF3 datapath is positive. 1: if the sum of all phase powers in the CF3 datapath is negative. Phase powers in the CF3 datapath are identified by Bits[8:6] (TERMSEL3[x]) of the COMPMODE register and by Bits[8:6] (CF3SEL[x]) of the CFMODE register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 48. CONFIG Register (Address 0xE618)

Bit Location	Bit Mnemonic	Default Value	Description
0	INTEN	0	Integrator enable. When this bit is set to 1, the internal digital integrator is enabled for use in meters utilizing Rogowski coils on all 3-phase and neutral current inputs. When this bit is cleared to 0, the internal digital integrator is disabled.
2:1	Reserved	00	Reserved. These bits do not manage any functionality.
3	SWAP	0	When this bit is set to 1, the voltage channel outputs are swapped with the current channel outputs. Thus, the current channel information is present in the voltage channel registers and vice versa.
4	MOD1SHORT	0	When this bit is set to 1, the voltage channel ADCs behave as if the voltage inputs were put to ground.
5	MOD2SHORT	0	When this bit is set to 1, the current channel ADCs behave as if the voltage inputs were put to ground.
6	HSDCEN	0	When this bit is set to 1, the HSDC serial port is enabled and HSCLK functionality is chosen at CF3/HSCLK pin. When this bit is cleared to 0, HSDC is disabled and CF3 functionality is chosen at CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
9:8	VTOIA[1:0]	00	These bits decide what phase voltage is considered together with Phase A current in the power path. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like VTOIA[1:0] = 00.
11:10	VTOIB[1:0]	00	These bits decide what phase voltage is considered together with Phase B current in the power path. 00 = Phase B voltage. 01 = Phase C voltage. 10 = Phase A voltage. 11 = reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like VTOIB[1:0] = 00.
13:12	VTOIC[1:0]	00	These bits decide what phase voltage is considered together with Phase C current in the power path. 00 = Phase C voltage. 01 = Phase A voltage. 10 = Phase B voltage. 11 = reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like VTOIC[1:0] = 00.
15:14	Reserved	0	Reserved. These bits do not manage any functionality.

Downloaded from Arrow.com.

Table 49. MMODE Register (Address 0xE700)

Bit Location	Bit Mnemonic	Default Value	Description
1:0	PERSEL[1:0]	00	00: Phase A selected as the source of the voltage line period measurement. 01: Phase B selected as the source of the voltage line period measurement. 10: Phase C selected as the source of the voltage line period measurement. 11: reserved. When set, the ADE7854/ADE7858/ADE7868/ADE7878 behave like PERSEL[1:0] = 00.
2	PEAKSEL[0]	1	PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all three phases simultaneously. If more than one PEAKSEL[2:0] bits are set to 1, then the peak measurement period indicated in the PEAKCYC register decreases accordingly because zero crossings are detected on more than one phase. When this bit is set to 1, Phase A is selected for the voltage and current peak registers.
3	PEAKSEL[1]	1	When this bit is set to 1, Phase B is selected for the voltage and current peak registers.
4	PEAKSEL[2]	1	When this bit is set to 1, Phase C is selected for the voltage and current peak registers.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 50. ACCMODE Register (Address 0xE701)

Bit Location	Bit Mnemonic	Default Value	Description
1:0	WATTACC[1:0]	00	00: signed accumulation mode of the total and fundamental active powers. Fundamental active powers are available in the ADE7878. 01: reserved. When set, the device behaves like WATTACC[1:0] = 00. 10: reserved. When set, the device behaves like WATTACC[1:0] = 00. 11: absolute accumulation mode of the total and fundamental active powers.
3:2	VARACC[1:0]	00	00: signed accumulation of the total and fundamental reactive powers. Total reactive powers are available in the ADE7858, ADE7868, and ADE7878. Fundamental reactive powers are available in the ADE7878. These bits are always 00 for the ADE7854. 01: reserved. When set, the device behaves like VARACC[1:0] = 00. 10: the total and fundamental reactive powers are accumulated, depending on the sign of the total and fundamental active power: if the active power is positive, the reactive power is accumulated as is, whereas if the active power is negative, the reactive power is accumulated with reversed sign. 11: reserved. When set, the device behave like VARACC[1:0] = 00.
5:4	CONSEL[1:0]	00	These bits select the inputs to the energy accumulation registers. IA', IB', and IC' are IA, IB, and IC shifted respectively by −90°. See Table 51. 00: 3-phase four wires with three voltage sensors. 01: 3-phase three wires delta connection. 10: 3-phase four wires with two voltage sensors. 11: 3-phase four wires delta connection.
6	REVAPSEL	0	0: The total active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC). This bit is always 0 for the ADE7854, ADE7858, and ADE7868. 1: The fundamental active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC).
7	REVRPSEL	0	0: The total reactive power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 10 (REVRPA), on Phase B triggers Bit 11 (REVRPB), and on Phase C triggers Bit 12 (REVRPC). This bit is always 0 for the ADE7854, ADE7858, and ADE7868. 1: The fundamental reactive power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 10 (REVRPA), on Phase B triggers Bit 11 (REVRPB), and on Phase C triggers Bit 12 (REVRPC).

Downloaded from Arrow.com.

Table 51. CONSEL[1:0] Bits in Energy Registers

Energy Registers	CONSEL[1:0] = 00	CONSEL[1:0] = 01	CONSEL[1:0] = 10	CONSEL[1:0] = 11
AWATTHR, AFWATTHR	VA × IA	VA × IA	VA × IA	VA × IA
BWATTHR, BFWATTHR	VB × IB	0	VB = −VA − VC VB × IB	VB = −VA VB × IB
CWATTHR, CFWATTHR	VC × IC	VC × IC	VC × IC	VC × IC
AVARHR, AFVARHR	VA × IA′	VA × IA′	VA × IA′	VA × IA′
BVARHR, BFVARHR	VB × IB′	0	VB = −VA − VC VB × IB′	VB = −VA VB × IB′
CVARHR, CFVARHR	VC × IC′	VC × IC′	VC × IC′	VC × IC′
AVAHR	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms
BVAHR	VB rms × IB rms	0	VB rms × IB rms	VB rms × IB rms
CVAHR	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms

Table 52. LCYCMODE Register (Address 0xE702)

Bit Location	Bit Mnemonic	Default Value	Description
0	LWATT	0	0: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed in regular accumulation mode. 1: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed into line cycle accumulation mode.
1	LVAR	0	0: the var-hour accumulation registers (AVARHR, BVARHR, and CVARHR) are placed in regular accumulation mode. This bit is always 0 for the ADE7854. 1: the var-hour accumulation registers (AVARHR, BVARHR, and CVARHR) are placed into line-cycle accumulation mode.
2	LVA	0	0: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed in regular accumulation mode. 1: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed into line-cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase A is selected for zero-crossings counts in the line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase B is selected for zero-crossings counts in the line cycle accumulation mode.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase C is selected for zero-crossings counts in the line cycle accumulation mode.
6	RSTREAD	1	0: read-with-reset of all energy registers is disabled. Clear this bit to 0 when Bits[2:0] (LWATT, LVAR, and LVA) are set to 1. 1: enables read-with-reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. This means a read of those registers resets them to 0.
7	Reserved	0	Reserved. This bit does not manage any functionality.

Table 53. HSDC_CFG Register (Address 0xE706)

Bit Location	Bit Mnemonic	Default Value	Description
0	HCLK	0	0: HSCLK is 8 MHz. 1: HSCLK is 4 MHz.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first. 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.

Downloaded from Arrow.com.

Bit Location	Bit Mnemonic	Default Value	Description
4:3	HXFER[1:0]	00	00 = for ADE7854, HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, and VCWV, one 32-bit word equal to 0, AVA, BVA, CVA, AWATT, BWATT, and CWATT, three 32-bit words equal to 0. For ADE7858, HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, and VCWV, one 32-bit word equal to 0, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. For the ADE7868 and ADE7878, HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 01 = for the ADE7854 and ADE7858, HSDC transmits six instantaneous values of currents and voltages: IAWV, VAWV, IBWV, VBWV, ICWV, and VCWV, and one 32-bit word equal to 0. For the ADE7868 and ADE7878, HSDC transmits seven instantaneous values of currents and voltages: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. 10 = for the ADE7854, HSDC transmits six instantaneous values of phase powers: AVA, BVA, CVA, AWATT, BWATT, and CWATT and three 32-bit words equal to 0. For the ADE7858, ADE7868, and ADE7878, HSDC transmits nine instantaneous values of phase powers: AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 11 = reserved. If set, the ADE7854/ADE7858/ADE7868/ADE7878 behave as if HXFER[1:0] = 00.
5	HSAPOL	0	0: $\overline{SS}$/HSA output pin is active low. 1: $\overline{SS}$/HSA output pin is active high.
7:6	Reserved	00	Reserved. These bits do not manage any functionality.

Table 54. LPOILVL Register (Address 0xEC00)[1]

Bit Location	Bit Mnemonic	Default Value	Description
2:0	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8.
7:3	LPLINE[4:0]	00000	The measurement period is (LPLINE + 1)/50 seconds.

[1] The LPOILVL register is available only for the ADE7868 and ADE7878; it is reserved for ADE7854 and ADE7858.

Table 55. CONFIG2 Register (Address 0xEC01)

Bit Location	Bit Mnemonic	Default Value	Description
0	EXTREFEN	0	When this bit is 0, it signifies that the internal voltage reference is used in the ADCs. When this bit is 1, an external reference is connected to the Pin 17 $REF_{IN/OUT}$.
1	I2C_LOCK	0	When this bit is 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From this moment on, spurious toggling of the $\overline{SS}$/HSA pin and an eventual switch into using the SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2 register locks the port. From this moment on, a switch into using I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7854/ADE7858/ADE7868/ADE7878 change PSMx power modes.
7:2	Reserved	0	Reserved. These bits do not manage any functionality.

Downloaded from Arrow.com.

OUTLINE DIMENSIONS

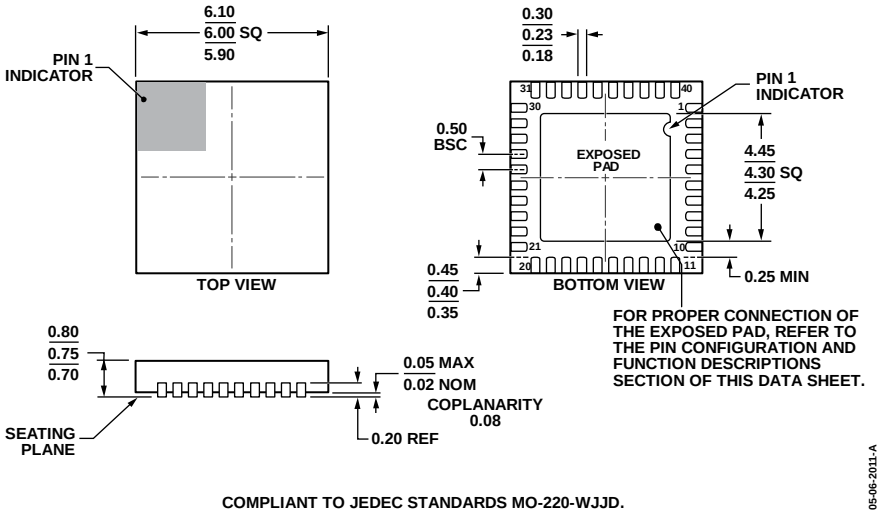

Figure 99. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm x 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE7854ACPZ	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7854ACPZ-RL	−40°C to +85°C	40-Lead LFCSP_WQ, 13”Tape and Reel	CP-40-10
ADE7858ACPZ	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7858ACPZ-RL	−40°C to +85°C	40-Lead LFCSP_WQ, 13”Tape and Reel	CP-40-10
ADE7868ACPZ	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7868ACPZ-RL	−40°C to +85°C	40-Lead LFCSP_WQ, 13”Tape and Reel	CP-40-10
ADE7878ACPZ	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7878ACPZ-RL	−40°C to +85°C	40-Lead LFCSP_WQ, 13”Tape and Reel	CP-40-10

[1] Z = RoHS Compliant Part.

Downloaded from Arrow.com.

NOTES

Downloaded from Arrow.com.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

©2010–2014 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D08510-0-4/14(H)

Downloaded from Arrow.com.