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5/03—Revision 0: Initial Version

SPECIFICATIONS

ANALOG INTERFACE

V_D = 3.3 V, V_{DD} = 3.3 V, ADC clock = maximum conversion rate, unless otherwise noted.

Table 1.

			AD9887AKS-100			AD9887AKS-140			AD9887AKS-170			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		±0.5	+1.15/−1.0		±0.5	+1.25/−1.0		±0.8	+1.25/−1.0	LSB
	Full	VI			+1.15/−1.0			+1.25/−1.0			+1.50/−1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.40		±0.5	±1.4		±1.0	±2.25	LSB
	Full	VI			±1.75			±2.5			±2.75	LSB
No Missing Codes	25°C	I		Guaranteed			Guaranteed			Guaranteed		
ANALOG INPUTS												
Voltage Range												
Minimum	Full	VI			0.5			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			1.0			V p-p
Gain Tempco	25°C	V		135			150			150		ppm/°C
Bias Current	25°C	IV			1			1			1	µA
	Full	IV			1			1			1	µA
Full-Scale Matching	Full	VI			8.0			8.0			8.0	% FS
Offset Adjustment Range	Full	VI	43	48	53	43	48	53	43	48	53	% FS
REFERENCE OUTPUTS												
Voltage Range	Full	V		1.3			1.3			1.3		V
Temperature Coefficient	Full	V		90			90			90		ppm/°C
SWITCHING PERFORMANCE[1]												
Max Conversion Rate	Full	VI	100			140			170			MSPS
Min Conversion Rate	Full	IV			10			10			10	MSPS
Clock-to-Data Skew, t_{SKEW}	Full	IV	−1.5		+2.5	−1.5		+2.5	−1.5		+2.5	ns
Serial Port Timing												
t_{BUFF}	Full	VI	4.7			4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			4.0			µs
t_{DHO}	Full	VI	250			250			250			ns
t_{DAL}	Full	VI	4.7			4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			4.0			µs
t_{DSU}	Full	VI	100			100			100			ns
t_{STASU}	Full	VI	4.7			4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	15		110	kHz
Max PLL Clock Rate	Full	VI	100			140			170			MHz
Min PLL Clock Rate	Full	IV			12			12			12	MHz
PLL Jitter	25°C	IV		500	700[2]		440	650[3]		370	500[4]	ps p-p
	Full	IV			1000[2]			700[3]			700[4]	ps p-p
Sampling Phase Tempco	Full	IV		10			10			10		ps/°C

Parameter	Temp	Test Level	AD9887AKS-100 Min	AD9887AKS-100 Typ	AD9887AKS-100 Max	AD9887AKS-140 Min	AD9887AKS-140 Typ	AD9887AKS-140 Max	AD9887AKS-170 Min	AD9887AKS-170 Typ	AD9887AKS-170 Max	Unit
DIGITAL INPUTS												
Voltage High, V_{IH}	Full	VI	2.6			2.6			2.6			V
Voltage Low, V_{IL}	Full	VI			0.8			0.8			0.8	V
Current High, V_{IH}	Full	IV			−1.0			−1.0			−1.0	µA
Current Low, V_{IL}	Full	IV			1.0			1.0			1.0	µA
Capacitance	25°C	V		3			3			3		pF
DIGITAL OUTPUTS												
Voltage High, V_{OH}	Full	VI	2.4			2.4			2.4			V
Voltage Low, V_{OL}	Full	VI			0.4			0.4			0.4	V
Duty Cycle DATACK, $\overline{DATACK}$	Full	IV	45	55	60	45	55	60	45	55	65	%
Output Coding				Binary			Binary			Binary		
POWER SUPPLIES												
V_D Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.45	2.2	3.3	3.45	2.2	3.3	3.45	V
PV_D Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
I_D Supply Current, V_D	25°C	V		167			185			230		mA
I_{DD} Supply Current, V_{DD}[5]	25°C	V		33			46			55		mA
IPV_D Supply Current, PV_D	25°C	V		43			43			60		mA
Total Supply Current[5]	Full	VI		243	330		274	360		345	390	mA
Power-Down Supply Current	Full	VI		90	120		90	120		90	120	mA
DYNAMIC PERFORMANCE												
Analog Bandwidth, Full Power	25°C	V		330			330			330		MHz
Transient Response	25°C	V		2			2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5			1.5		ns
Signal-to-Noise Ratio (SNR)[6] f_{IN} = 40.7 MHz	25°C	V		46			46			45		dB
Crosstalk	Full	V		60			60			60		dBc
THERMAL CHARACTERISTICS												
θ_{JA} Junction-to-Ambient Thermal Resistance[7]		V		37			37			37		°C/W

[1] Drive strength = 11.
[2] VCO range = 01, charge-pump current = 001, PLL divider = 1693.
[3] VCO range = 10, charge-pump current = 110, PLL divider = 1600.
[4] VCO range = 11, charge-pump current = 110, PLL divider = 2159.
[5] DEMUX = 1, DATACK and $\overline{DATACK}$ load = 10 pF, data load = 5 pF.
[6] Using external pixel clock.
[7] Simulated typical performance with package mounted to a 4-layer board.

DIGITAL INTERFACE

VD = 3.3 V, VDD = 3.3 V, clock = maximum, unless otherwise noted.

Table 2.

Parameter	Conditions	Temp	Test Level	AD9887AKS Min	Typ	Max	Unit
RESOLUTION					8		Bits
DC DIGITAL I/O SPECIFICATIONS							
High Level Input Voltage, V_{IH}		Full	VI	2.6			V
Low Level Input Voltage, V_{IL}		Full	VI			0.8	
High Level Output Voltage, V_{OH}		Full	VI	2.4			V
Low Level Output Voltage, V_{OL}		Full	VI			0.4	V
Input Clamp Voltage, V_{CINL}	I_{CL} = −18 mA		IV			GND − 0.8	V
Input Clamp Voltage, V_{CIPL}	I_{CL} = +18 mA		IV			V_{DD} + 0.8	V
Output Clamp Voltage, V_{CONL}	I_{CL} = −18 mA		IV			GND − 0.8	V
Output Clamp Voltage, V_{COPL}	I_{CL} = +18 mA		IV			V_{DD} + 0.8	V
Output Leakage Current, I_{OL}	High impedance	Full	IV	−10		+10	µA
DC SPECIFICATIONS							
Output High Drive, I_{OHD} (V_{OUT} = V_{OH})	Output drive = high	Full	IV		13		mA
	Output drive = med	Full	IV		8		mA
	Output drive = low	Full	IV		5		mA
Output Low Drive, I_{OLD} (V_{OUT} = V_{OL})	Output drive = high	Full	IV		−9		mA
	Output drive = med	Full	IV		−7		mA
	Output drive = low	Full	IV		−5		mA
DATACK High Drive, I_{OHC} (V_{OUT} = V_{OH})	Output drive = high	Full	IV		25		mA
	Output drive = med	Full	IV		12		mA
	Output drive = low	Full	IV		8		mA
DATACK Low Drive, I_{OLC} (V_{OUT} = V_{OL})	Output drive = high	Full	IV		−25		mA
	Output drive = med	Full	IV		−19		mA
	Output drive = low	Full	IV		−8		mA
Differential Input Voltage, Single-Ended Amplitude		Full	IV	75		800	mA
POWER SUPPLIES							
V_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
V_{DD} Supply Voltage	Minimum value for two pixels per clock mode	Full	IV	2.2	3.3	3.45	V
PV_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
I_D Supply Current[1]		25°C	V		350		mA
I_{DD} Supply Current[1, 2]		255°C	V		40		mA
IPV_D Supply Current[1]		255°C	IV		130		mA
Total Supply Current with HDCP[1, 2]			VI		520	560	mA
AC SPECIFICATIONS							
Intrapair (+ to −) Differential Input Skew, T_{DPS}		Full	IV			360	ps
Channel-to-Channel Differential Input Skew, T_{CCS}		Full	IV			1.0	Clock period
Low-to-High Transition Time for Data and Controls, D_{LHT}	Output drive = high; C_L = 10 pF	Full	IV			2.5	ns
	Output drive = med; C_L = 7 pF	Full	IV			3.1	ns
	Output drive = low; C_L = 5 pF	Full	IV			5.4	ns

Parameter	Conditions	Temp	Test Level	AD9887AKS Min	Typ	Max	Unit
Low-to-High Transition Time (D_{LHT}) for DATACK	Output drive = high; C_L = 10 pF	Full	IV			1.2	ns
	Output drive = med; C_L = 7 pF	Full	IV			1.6	ns
	Output drive = low; C_L = 5 pF	Full	IV			2.3	ns
High-to-Low Transition Time (D_{HLT}) for Data	Output drive = high; C_L = 10 pF	Full	IV			2.6	ns
	Output drive = med; C_L = 7 pF	Full	IV			3.0	ns
	Output drive = low; C_L = 5 pF	Full	IV			3.7	ns
High-to-Low Transition Time (D_{HLT}) for DATACK	Output drive = high; C_L =10 pF	Full	IV			1.4	ns
	Output drive = med; C_L = 7 pF	Full	IV			1.6	ns
	Output drive = low; C_L = 5 pF	Full	IV			2.4	ns
Clock-to-Data Skew, t_{SKEW}[3]		Full	IV	0		4.0	ns
Duty Cycle, DATACK, $\overline{DATACK}$[3]		Full	IV	45		55	% of period high
DATACK Frequency (f_{CIP})	1 pixel/clock	Full	VI	20		140	MHz
DATACK Frequency (f_{CIP})	2 pixels/clock	Full	IV	10		85	MHz

[1] The typical pattern contains a gray-scale area, output drive = high.
[2] DATACK and $\overline{DATACK}$ load = 10 pF, data load = 5 pF, and HDCP disabled.
[3] Drive strength = 11.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
VREFIN	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C; sample tested at specified temperatures.

III. Sample tested only.

IV. Guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

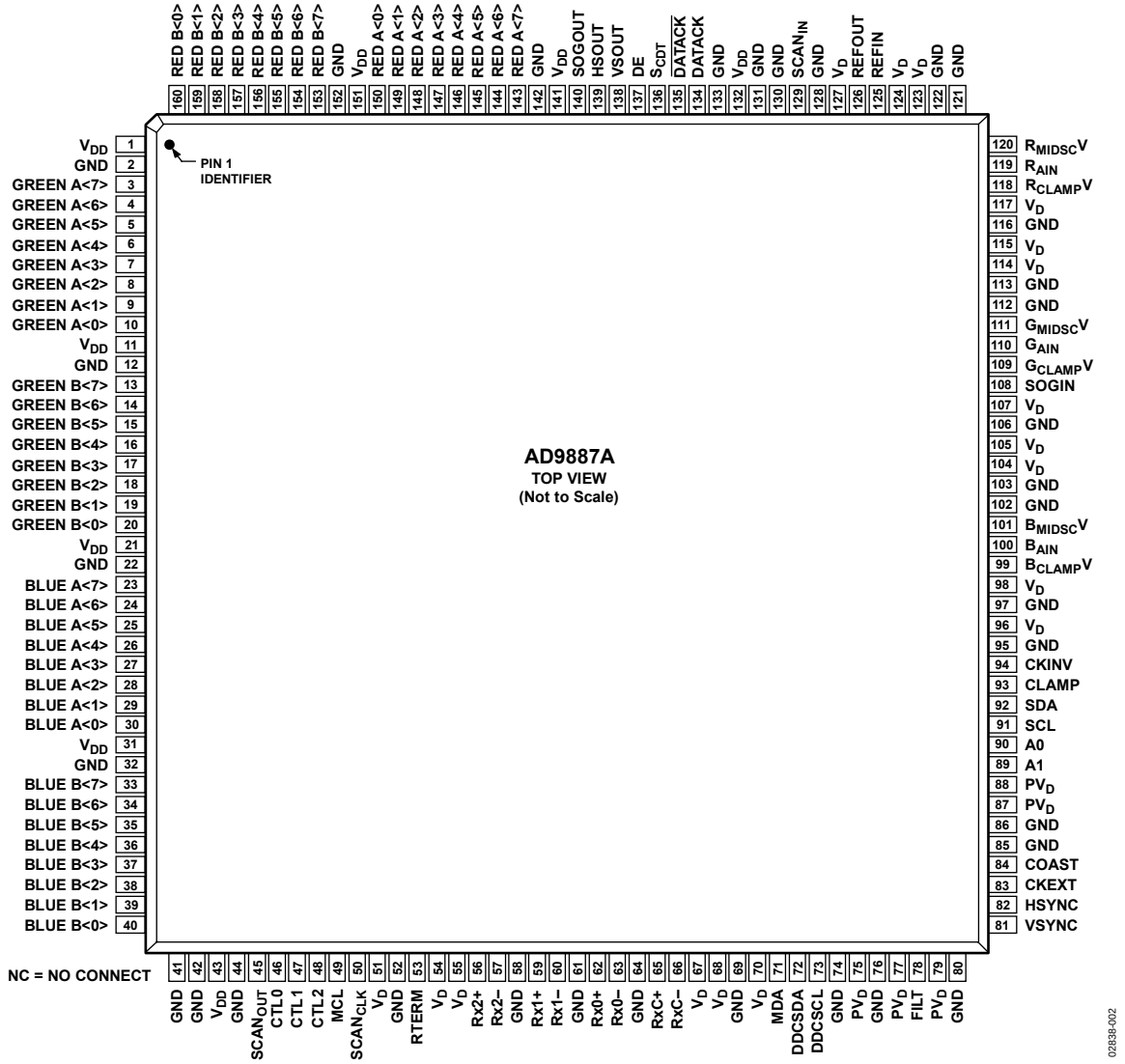

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin Type	Mnemonic	Description	Value	Pin No.	Interface
Analog Video Data Inputs	R_{AIN}	Analog Input for Red Channel	0.0 V to 1.0 V	119	Analog
	G_{AIN}	Analog Input for Green Channel	0.0 V to 1.0 V	110	Analog
	B_{AIN}	Analog Input for Blue Channel	0.0 V to 1.0 V	100	Analog
Sync/Clock Inputs	HSYNC	Horizontal Sync Input	3.3 V CMOS	82	Analog
	VSYNC	Vertical Sync Input	3.3 V CMOS	81	Analog
	SOGIN	Sync-on-Green Input	0.0 V to 1.0 V	108	Analog
	CLAMP	External Clamp Input (Optional)	3.3 V CMOS	93	Analog
	COAST	PLL Coast Signal Input (Optional)	3.3 V CMOS	84	Analog
	CKEXT	External Pixel Clock Input (to Bypass the PLL) to V_{DD} or Ground (Optional)	3.3 V CMOS	83	Analog
	CKINV	ADC Sampling Clock Invert (Optional)	3.3 V CMOS	94	Analog
Sync Outputs	HSOUT	Horizontal Sync Output	3.3 V CMOS	139	Analog/Digital
	VSOUT	Vertical Sync Output	3.3 V CMOS	138	Analog/Digital
	SOGOUT	Sync-on-Green Slicer Output or Raw Hsync	3.3 V CMOS	140	Analog
Voltage References	REFOUT	Internal Reference Output (bypass with 0.1 µF to Ground)	1.25 V	126	Analog
	REFIN	Reference Input (1.25 V ± 10%)	1.25 V ± 10%	125	Analog
Clamp Voltages	$R_{MIDSC}V$	Red Channel Midscale Clamp Voltage Output	0.5 V ± 50%	120	Analog
	$R_{CLAMP}V$	Red Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	118	Analog
	$G_{MIDSC}V$	Green Channel Midscale Clamp Voltage Output	0.5 V ± 50%	111	Analog
	$G_{CLAMP}V$	Green Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	109	Analog
	$B_{MIDSC}V$	Blue Channel Midscale Clamp Voltage Output	0.5 V ± 50%	101	Analog
	$B_{CLAMP}V$	Blue Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	99	Analog
PLL Filter	FILT	External Filter Connection (Component of PLL)		78	Analog
Power Supplies	V_D	Main Power Supply	3.3 V ± 5%	51, 54, 55, 67, 68, 70, 96, 98, 104, 105, 107, 114, 115, 117, 123, 124, 127	Analog/Digital
	V_{DD}	Output Power Supply	3.3 V ± 5%	1, 11, 21, 31, 43, 132, 141, 151	Analog/Digital
	PV_D	PLL Power Supply	3.3 V ± 5%	75, 77, 79, 87, 88	Analog/Digital
	GND	Ground	0 V	2, 12, 22, 32, 41, 42, 44, 52, 58, 61, 64, 69, 74, 76, 80, 85, 86, 95, 97, 102, 103, 106, 112, 113, 116, 121, 122, 128, 130, 131, 133, 142, 152	Analog/Digital
Serial Port	SDA	Serial Port Data I/O	3.3 V CMOS	92	Analog/Digital

Pin Type	Mnemonic	Description	Value	Pin No.	Interface
2-Wire Serial Interface	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	91	Analog/Digital
	A0	Serial Port Address Input 1	3.3 V CMOS	90	Analog/Digital
	A1	Serial Port Address Input 2	3.3 V CMOS	89	Analog/Digital
Data Outputs	RED B[7:0]	Data Output, Red Channel, Port B/Odd, Bit 7 is the MSB	3.3 V CMOS	153 to 160	Analog/Digital
	GREEN B[7:0]	Data Output, Green Channel, Port B/Odd	3.3 V CMOS	13 to 20	Analog/Digital
	BLUE B[7:0]	Data Output, Blue, Port B/Odd	3.3 V CMOS	33 to 40	Analog/Digital
	RED A[7:0]	Data Output, Red Channel, Port A/Even	3.3 V CMOS	143 to 150	Analog/Digital
	GREEN A[7:0]	Data Output, Green Channel, Port A/Even	3.3 V CMOS	3 to 10	Analog/Digital
	BLUE A[7:0]	Data Output, Blue Channel, Port A/Even	3.3 V CMOS	23 to 30	Analog/Digital
Data Clock Outputs	DATACK	Data Output Clock	3.3 V CMOS	134	Analog/Digital
	$\overline{\text{DATACK}}$	Data Output Clock Complement	3.3 V CMOS	135	Analog/Digital
Sync Detect	S_{CDT}	Sync Detect Output	3.3 V CMOS	136	Analog/Digital
Scan Function	$SCAN_{IN}$	Input for Scan Function	3.3 V CMOS	129	Analog/Digital
	$SCAN_{OUT}$	Output for Scan Function	3.3 V CMOS	45	Analog/Digital
	$SCAN_{CLK}$	Clock for Scan Function	3.3 V CMOS	50	Analog/Digital
Digital Video Data Inputs	Rx0+	Digital Differential Input Channel 0 True		62	Digital
	Rx0−	Digital Differential Input Channel 0 Complement		63	Digital
	Rx1+	Digital Differential Input Channel 1 True		59	Digital
	Rx1−	Digital Differential Input Channel 1 Complement		60	Digital
	Rx2+	Digital Differential Input Channel 2 True		56	Digital
	Rx2−	Digital Differential Input Channel 2 Complement		57	Digital
Digital Video Clock Inputs	RxC+	Digital Differential Data Clock True		65	Digital
	RxC−	Digital Differential Data Clock Complement		66	Digital
Data Enable	DE	Data Enable	3.3 V CMOS	137	Digital
Control Bit	CTL0, CTL1, CTL2	Digital Control Outputs	3.3 V CMOS	46 to 48	Digital
Termination Control	RTERM	Internal Termination Resistance Set Pin		53	Digital
HDCP	DDCSCL	HDCP Slave Serial Port Data Clock	3.3 V CMOS	73	Digital
	DDCSDA	HDCP Slave Serial Port Data I/O	3.3 V CMOS	72	Digital
	MCL	HDCP Master Serial Port Data Clock	3.3 V CMOS	49	Digital
	MDA	HDCP Master Serial Port Data I/O	3.3 V CMOS	71	Digital

PIN FUNCTION DETAILS—PINS SHARED BETWEEN DIGITAL AND ANALOG INTERFACES

Sync Outputs

HSOUT Horizontal Sync Output

The horizontal sync output is a reconstructed version of the video Hsync, phase-aligned with DATACK. The polarity of this output can be controlled via a serial bus bit. In analog interface mode, the placement and duration are variable. In digital interface mode, the placement and duration are set by the graphics transmitter.

VSOUT Vertical Sync Output

The Vsync is separated from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes are set by the graphics transmitter.

2-Wire Serial Port

SDA Serial Port Data I/O

SCL Serial Port Data Clock

A0 Serial Port Address Input 1

A1 Serial Port Address Input 2

For a full description of the 2-wire serial register and how it works, see the 2-Wire Serial Control Port section.

Data Outputs

RED A Data Output, Red Channel, Port A/Even

RED B Data Output, Red Channel, Port B/Odd

GREEN A Data Output, Green Channel, Port A/Even

GREEN B Data Output, Green Channel, Port B/Odd

BLUE A Data Output, Blue Channel, Port A/Even

BLUE B Data Output, Blue Channel, Port B/Odd

These outputs are the main data outputs. Bit 7 is the MSB. These outputs are shared between the two interfaces.

Data Clock Outputs

DATACK Data Output Clock

$\overline{\text{DATACK}}$ Data Output Clock Complement

Like the data outputs, the data clock outputs are shared between the two interfaces. They also behave differently, depending on which interface is active. See the Theory of Operation and Design Guide—Analog Interface and the Theory of Operation—Digital Interface sections for details on how these pins behave.

Sync Detect

S_{CDT} Chip Active/Inactive Detect Output

The logic for the S_{CDT} pin is analog interface HSYNC detection or digital interface DE detection. Therefore, the S_{CDT} pin switches to logic low under two conditions: when neither interface is active, or when the chip is in full power-down mode. The data outputs are automatically set to three-state when S_{CDT} is low. This pin can be read by a controller to identify periods of inactivity.

Scan Function

$SCAN_{IN}$ Data Input for Scan Function

By using the scan function, 48 bits of data can be loaded into the data outputs. Data is input serially through this pin, clocked with the $SCAN_{CLK}$ pin, and comes through the outputs as parallel words. This function is useful for loading known data into a graphics controller chip for testing purposes.

$SCAN_{OUT}$ Data Output for Scan Function

The data input serially into the $SCAN_{IN}$ register can be read through this pin. Data is read on a FIFO basis and is clocked via the $SCAN_{CLK}$ pin.

$SCAN_{CLK}$ Data Clock for Scan Function

This pin clocks the data for the scan function. It controls both data input and output.

Power Supplies

V_D Main Power Supply

These pins supply power to the main elements of the circuit. They should be filtered to be as quiet as possible.

V_{DD} Digital Output Power Supply

These supply pins are identified separately from the V_D pins; therefore, special care can be taken to minimize output noise transferred into the sensitive analog circuitry.

If the AD9887A is interfacing with lower voltage logic, V_{DD} can be connected to a lower supply voltage (as low as 2.2 V) for compatibility.

PV_D Clock Generator Power Supply

The most sensitive portion of the AD9887A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide noise-free power to these pins.

GND Ground

This is the ground return for all circuitry on the chip. It is recommended that the application circuit board have a single, solid ground plane.

PIN FUNCTION DETAILS—ANALOG INTERFACE

Analog Video Data Inputs

R_{AIN} Analog Input for Red Channel

G_{AIN} Analog Input for Green Channel

B_{AIN} Analog Input for Blue Channel

These are the high impedance inputs that accept graphics signals from the red, green, and blue channels, respectively. For RGB, the three channels are identical and can be used for any color, but colors are assigned for convenient reference. For proper 4:2:2 formatting in a YUV application, the Y channel must be connected to the G_{AIN} input, U must be connected to the B_{AIN} input, and V must be connected to the R_{AIN} input.

These pins accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.

External Inputs

HSYNC Horizontal Sync Input

This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation.

The logic sense of this pin is controlled by Serial Register 0x0F, Bit 7 (Hsync polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync polarity = 1, the rising edge is active.

The input includes a Schmitt trigger for noise immunity with a nominal input threshold of 1.5 V.

Electrostatic discharge (ESD) protection diodes conduct heavily if this pin is driven more than 0.5 V above the maximum tolerance voltage (3.3 V) or more than 0.5 V below ground.

VSYNC Vertical Sync Input

This is the input for vertical sync.

Sync/Clock Inputs

SOGIN Sync-on-Green Input

This input is provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold that is 0.15 V above the negative peak of the input signal.

When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT.

When not used, leave this input unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green Input section.

CLAMP External Clamp Input (Optional)

This logic input can be used to define the time during which the input signal is clamped to the reference dc level (ground for RGB, midscale for YUV). It should be used when the reference dc level is known to be present on the analog input channels, typically during a period called the back porch of the graphics signal following Hsync. The CLAMP pin is enabled by setting control bit EXTCLMP to 1 (the default at power-up is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting the delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by CLAMPOL. When not used, this pin must be grounded and EXTCLMP must be programmed to 0.

COAST Clock Generator Coast Input (Optional)

This input can be used to stop the pixel clock generator from synchronizing with Hsync while maintaining the clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses when in the vertical interval. The coast signal is generally not required for PC-generated signals. For applications requiring coast, it is provided through the internal coast found in the sync processing engine.

The logic sense of this pin is controlled by coast polarity. When not used, this pin can be grounded with coast polarity programmed to 1, or tied high with coast polarity programmed to 0. Coast polarity defaults to 1 at power-up.

CKEXT External Clock Input (Optional)

This pin can be used to provide an external clock to the AD9887A in place of the clock internally generated from HSYNC. It is enabled by programming CKEXT to 1. When an external clock is used, all other internal functions, including the clock phase adjustment, operate normally. When not used, this pin should be tied to V_{DD} or to ground and CKEXT should be programmed to 0.

CKINV Sampling Clock Inversion (Optional)

This pin can be used to invert the pixel sampling clock, which has the effect of shifting the sampling phase 180°. This supports the alternate pixel sampling mode, wherein higher frequency input signals (up to 340 MPPS) can be captured by sampling the odd pixels and capturing the even pixels on the subsequent frame.

This pin should be used only during blanking intervals (typically vertical blanking), because it might produce several samples of corrupted data during the phase shift.

CKINV should be grounded when not used.

Either or both signals can be used, depending on the timing mode and the interface design used.

Sync Outputs

HSOUT Horizontal Sync Output

A reconstructed, phase-aligned version of the HSYNC input. Both the polarity and duration of this output can be programmed via serial bus registers.

By maintaining alignment with DATACK, $\overline{\text{DATACK}}$, and Data, data timing with respect to horizontal sync can be determined.

SOGOUT Sync-on-Green Slicer Output

This pin can be programmed to output either the composite sync output from the sync-on-green slicer comparator or an unprocessed, but delayed, version of the HSYNC input. See the sync processing block diagram (Figure 43) to see how this pin is connected.

Voltage References

REFOUT Internal Reference Output

This is the output from the internal 1.25 V band gap reference. This output is intended to drive relatively light loads. It can drive the AD9887A reference input directly, but should be externally buffered if it is used to drive other loads, as well.

The absolute accuracy of this output is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9887A applications. If higher accuracy is required, an external reference can be used instead. When using an external reference, connect this pin to ground through a 0.1 µF capacitor.

REFIN Reference Input

The reference input accepts the master reference voltage for all AD9887A internal circuitry (1.25 V ± 10%). It can be driven directly by the REFOUT pin. Its high impedance presents a very light load to the reference source.

This pin should always be bypassed to ground with a 0.1 µF capacitor.

PLL Filter

FILT External Filter Connection

For proper operation, the pixel clock generator, PLL, requires an external filter. Connect the filter shown in Figure 11 to this pin. For optimal performance, minimize noise and parasitics on this node.

Data Outputs

RED A Data Output, Red Channel, Port A/Even

RED B Data Output, Red Channel, Port B/Odd

GREEN A Data Output, Green Channel, Port A/Even

GREEN B Data Output, Green Channel, Port B/Odd

BLUE A Data Output, Blue Channel, Port A/Even

BLUE B Data Output, Blue Channel, Port B/Odd

These are the main data outputs. Bit 7 is the MSB.

Each channel has two ports. When the part is operated in single-channel mode (DEMUX = 0), all data presented to Port A and Port B is placed in a high impedance state. Programming demux to 1 establishes the dual-channel mode, wherein alternate pixels are presented to the Port A and Port B of each channel. These appear simultaneously; two pixels are presented at the time of every second input pixel when PAR is set to 1 (parallel mode). When PAR is set to 0, pixel data appears alternately on the two ports, one new sample with each incoming pixel (interleaved mode).

In dual-channel mode, the first pixel after Hsync is routed to Port A. The second pixel goes to Port B, the third to Port A, and so on.

The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK, $\overline{\text{DATACK}}$, and HSOUT outputs are also moved; therefore, the timing relationship among the signals is maintained.

$R_{MIDSC}V$ Red Channel Midscale Clamp Voltage Output

$G_{MIDSC}V$ Green Channel Midscale Clamp Voltage Output

$B_{MIDSC}V$ Blue Channel Midscale Clamp Voltage Output

$R_{CLAMP}V$ Red Channel Midscale Clamp Voltage Input

$G_{CLAMP}V$ Green Channel Midscale Clamp Voltage Input

$B_{CLAMP}V$ Blue Channel Midscale Clamp Voltage Input

These pins are part of the circuit that provides a voltage reference for midscale clamping used in the capture of YUV and YPbPr input signals. These pins should be grounded through 0.1 µF capacitors, as shown in Figure 4.

Data Clock Outputs

DATACK Data Output Clock

$\overline{\text{DATACK}}$ Data Output Clock Complement

These differential data clock output signals are used to strobe the output data and HSOUT into external logic.

These signals are produced by the internal clock generator and are synchronous with the internal pixel sampling clock.

When the AD9887A is operated in single-channel mode, the output frequency is equal to the pixel sampling frequency. When the AD9887A is operated in dual-channel mode, the clock frequency is half the pixel frequency.

When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, $\overline{\text{DATACK}}$, and HSOUT outputs are moved; therefore, the timing relationship among the signals is maintained.

PIN FUNCTION DETAILS—DIGITAL INTERFACE

Digital Video Data Inputs

Rx0+ Digital Differential Input Channel 0 True

Rx0− Digital Differential Input Channel 0 Complement

Rx1+ Digital Differential Input Channel 1 True

Rx1− Digital Differential Input Channel 1 Complement

Rx2+ Digital Differential Input Channel 2 True

Rx2− Digital Differential Input Channel 2 Complement

These pins receive three pairs of differential, low voltage, swing input pixel data from a digital graphics transmitter.

Digital Video Clock Inputs

RxC+ Digital Differential Data Clock True

RxC− Digital Differential Data Clock Complement

These pins receive the differential, low voltage, swing input pixel clock from a digital graphics transmitter.

Termination Control

R_{TERM} Internal Termination Set Pin

This pin is used to set the termination resistance for all digital interface high speed inputs. To set this pin, place a resistor of 10 times the desired input termination resistance between this pin (Pin 53) and the ground supply. Typically, the value of this resistor should be 500 Ω.

Data Enable

DE Data Enable

This pin outputs the state of data enable (DE). The AD9887A decodes DE from the incoming stream of data. The DE signal is high during active video and low when there is no active video.

HDCP

DDCSCL HDCP Slave Serial Port Data Clock

For use in communicating with the HDCP-enabled DVI transmitter.

DDCSDA HDCP Slave Serial Port Data I/O

For use in communicating with the HDCP-enabled DVI transmitter.

MCL HDCP Master Serial Port Data Clock

Connects the EEPROM for reading the encrypted HDCP keys.

MDA HDCP Master Serial Port Data I/O

Connects the EEPROM for reading the encrypted HDCP keys.

CTL Digital Control Outputs

These pins output the control signals for the red and green channels. CTL0 and CTL1 correspond to the red channel input, and CTL2 and CTL3 correspond to the green channel input.

THEORY OF OPERATION AND DESIGN GUIDE—ANALOG INTERFACE

GENERAL DESCRIPTION

The AD9887A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The device is ideal for implementing a computer interface in HDTV monitors or for serving as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 170 MHz, or of up to 340 MHz with an alternate pixel sampling mode.

The AD9887A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

INPUT SIGNAL HANDLING

The AD9887A has three high impedance analog input pins for the red, green, and blue channels that accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-lead D connector, or BNC connectors. The AD9887A should be located as close as is practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At this point, the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9887A inputs through 47 nF capacitors. These capacitors form part of the dc-restoration circuit (see Figure 3).

In an ideal world of perfectly matched impedances, the best performance would be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9887A (330 MHz) would track the input signal continuously as it moves from one pixel level to the next and would digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise that result in excessive ringing and distortion of the input waveform. This makes it difficult to establish a sampling phase that provides good image quality. A small inductor in series with the input can be effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 high speed signal chip bead inductor in the circuit of Figure 3 provides good results in most applications.

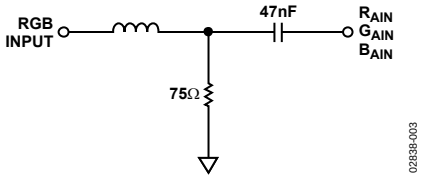

Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The AD9887A receives a horizontal sync signal and uses it to generate the pixel clock and clamp timing. It is possible to operate the AD9887A without applying Hsync (using an external clock), but several of the chip's features are unavailable. Therefore, it is recommended to provide Hsync. It can be in the form of either a sync signal directly from the graphics source or a preprocessed TTL- or CMOS-level signal.

The HSYNC input includes a Schmitt-trigger buffer and is capable of handling signals that have long rise times with superior noise immunity. In typical PC-based graphics systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required or desired.

When the VSYNC input is selected as the source for Vsync, it is used for coast generation and passed through to the VSOUT pin.

Serial Control Port

The serial control ports are designed for 3.3 V logic. If there are 5 V drivers on the bus, the serial control port pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}), but can operate with a V_{DD} as low as 2.5 V for compatibility with 2.5 V logic.

CLAMPING

RGB Clamping

To digitize the incoming signal properly, adjust the dc offset of the input to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, the black level is at 300 mV, and the white level is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal. Clamping removes this offset to allow proper capture.

The key to clamping is to identify a time when the graphics system is known to be producing a black signal. Originating from CRT displays, the electron beam is blanked by sending a black level during horizontal retrace to prevent disturbing the image. Most graphics systems maintain this format of sending a black level between active video lines.

An offset is then introduced that results in the ADCs producing a black output (Code 0x00) when the known black input is present. The offset remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync, called the back porch, when a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by using the CLAMP pin at the appropriate time (with EXTCLMP = 1). The polarity of this signal is set by the clamp polarity bit.

An easier method of clamp timing uses the AD9887A internal clamp timing generator. The clamp placement register is programmed with the number of pixel clocks that should pass after the trailing edge of Hsync before clamping starts. A second register (clamp duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync, and the back porch (black reference) always follows Hsync. To establish clamping, set the clamp placement to 0x08 (to provide eight pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x14 (to allow the clamp 20 pixel periods to re-establish the black reference).

The value of the external input coupling capacitor affects the performance of the clamp. If the value is too small, there is an amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, it takes an excessively long time for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovery from a step error of 100 mV to within ½ LSB in 10 lines, using a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping

YUV signals are slightly different from RGB signals in that the dc-reference level (black level in RGB signals) is at the midpoint of the U and V video signals. For these signals, it may be necessary to clamp to the midscale range of the ADC range (0x80), rather than to the bottom of the ADC range (0x00).

Clamping to midscale, rather than to ground, can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that it can be clamped to either midscale or ground independently. These bits (Bit 0 to Bit 2) are located in Register 0x0F.

The midscale reference voltage that each ADC clamps to is independently provided on the $R_{MIDSC}V$, $G_{MIDSC}V$, and $B_{MIDSC}V$ pins. Each converter must have its own midscale reference, because both offset adjustment and gain adjustment for each converter affect the dc level of midscale.

During clamping, the Y and V converters are clamped to their respective midscale reference inputs. These inputs are Pin $B_{CLAMP}V$ and Pin $R_{CLAMP}V$ for the U and V converters, respectively. The typical connections for both RGB and YUV clamping are shown in Figure 4. Note that even if midscale clamping is not required, all midscale voltage outputs should be connected to ground through a 0.1 µF capacitor.

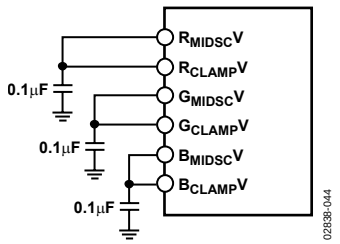

Figure 4. Typical Clamp Configuration for RGB and YUV Applications

GAIN AND OFFSET CONTROL

A block diagram of the gain and offset control integrated with each ADC is shown in Figure 5.

The AD9887A can accommodate input signals of 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (red gain, green gain, and blue gain).

Code 0 gives the minimum input range (a maximum of 0.5 V); Code 255 corresponds to the maximum input range (a minimum of 1.0 V). Increasing the gain setting results in an image with less contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (red offset, green offset, and blue offset) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range; therefore, if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 6 and Figure 7 illustrate the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, which is controlled by the gain setting. Therefore, changing the full-scale range changes the offset (see Figure 6). The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale range is not affected, but the full-scale level is shifted by the same amount as the zero-scale level.

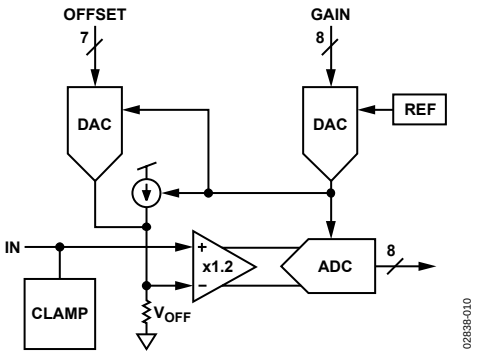

Figure 5. ADC Block Diagram (Single-Channel Output)

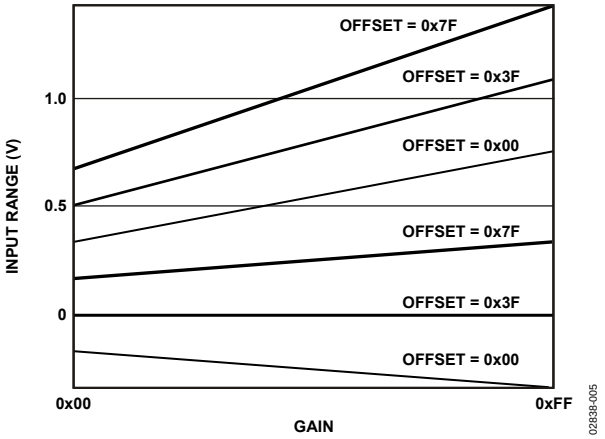

Figure 6. Gain and Offset Control

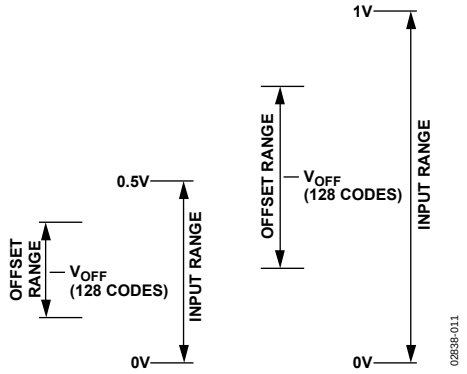

Figure 7. Relationship of Offset Range to Input Range

SYNC-ON-GREEN INPUT

The sync-on-green input operates in two steps. First, with the aid of a negative peak detector, it sets a baseline clamp level from the incoming video signal. Second, it sets the sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via Register 0x11. The sync-on-green input must be ac-coupled to the green analog input through its own capacitor, as shown in Figure 8.

The value of the capacitor must be 1 nF ± 20%. If sync-on-green is not used, this connection is not required and SOGIN should be left unconnected. (Note that the sync-on-green signal is always negative polarity.) See the Theory of Operation—Sync Processing section for more information.

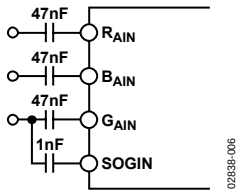

Figure 8. Typical Clamp Configuration for RGB and YUV Applications

CLOCK GENERATION

A phase-locked loop (PLL) is used to generate the pixel clock. The HSYNC input provides a reference frequency for the PLL. A voltage-controlled oscillator (VCO) generates a much higher pixel clock frequency. This is divided by the PLL divide value (MSBs in Register 0x01 and LSBs in Register 0x02) and phase compared with the HSYNC input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is important for providing the clearest, most stable image. During each pixel time, there is a period when the signal slews from the old pixel amplitude and settles at its new value. Then, the input voltage is stable until the signal slews to a new value (see Figure 9). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC, the bandwidth of the transmission system (cable and termination), and the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, the slewing and settling times are likewise fixed. Subtract these times from the total pixel period to determine the stable period. At higher pixel frequencies, both the total cycle time and stable pixel time are shorter.

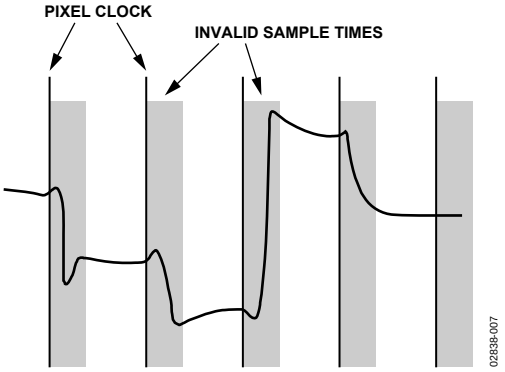

Figure 9. Pixel Sampling Times

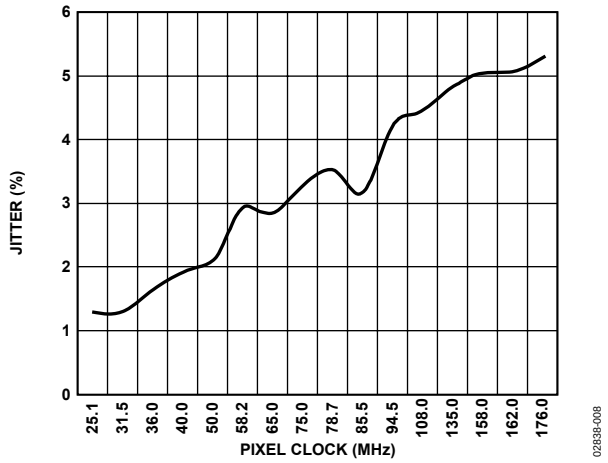

Figure 10. Pixel Clock Jitter vs. Frequency

Any jitter in the clock reduces the precision with which the sampling time can be determined and, thus, must be subtracted from the stable pixel time. The AD9887A clock generation circuit is designed to minimize jitter to less than 6% of the total pixel time in all operating modes, making its effect on valid sampling time negligible (see Figure 10).

The PLL characteristics are determined by the loop-filter design, the PLL charge-pump current, and the VCO range setting. The loop-filter design is illustrated in Figure 11. Recommended settings of VCO range and charge-pump current for VESA standard display modes are listed in Table 7.

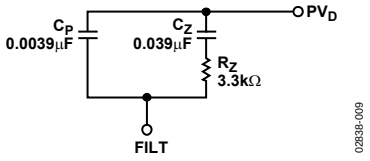

Figure 11. PLL Loop-Filter Detail

The following programmable registers are provided to optimize the performance of the PLL:

- The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 170 MHz. The divisor register controls the exact multiplication factor. This register can be set to any value between 221 and 4095. (The divide ratio used is the programmed divide ratio plus one.)
- The 2-Bit VCO Range Register. To lower the sensitivity of the output frequency to noise on the control signal, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. Because there are only three possible regions, just 2 LSBs of the VCO range register are used. The frequency ranges for the lowest and highest regions are shown in Table 5.

Table 5. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)
0	0	12 to 37
0	1	37 to 74
1	0	74 to 140
1	1	140 to 170

- The 3-Bit Charge-Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table 6.

Table 6. Charge-Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

- The 5-Bit Phase Adjust Register. The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase-adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjustment is operational even if the pixel clock is provided externally. The COAST signal allows the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal. This can be used during the vertical sync period or any other time that the Hsync signal is unavailable. The polarity of the coast signal can be set through the COAST polarity bit, and the polarity of the Hsync signal can be set through the HSYNC polarity bit. If not using automatic polarity detection, set the HSYNC and COAST polarity bits to match the polarity of their respective signals.

Table 7. Recommended VCO Range and Charge-Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	VCORNGE	CURRENT
VGA	640 × 480	60	31.5	25.175	00	011
		72	37.7	31.500	00	100
		75	3735	31.500	00	100
		85	43.3	36.000	00	101
SVGA	800 × 600	56	35.1	36.000	00	101
		60	3739	40.000	01	011
		72	4831	50.000	01	011
		75	46.9	49.500	01	011
		85	53.7	56.250	01	100
XGA	1024 × 768	60	48.4	65.000	01	101
		70	56.5	75.000	10	011
		75	60.0	78.750	10	011
		80	64.0	85.500	10	011
		85	68.3	94.500	10	100
SXGA	1280 × 1024	60	64.0	108.000	10	100
		75	80.0	135.000	10	101
		85	91.1	157.500	11	101
UXGA	1600 × 1200	60	75.0	162.000	10	101
TV	480i	60	15.75	13.51	00	001
	480p	60	31.47	27	00	100
	720p	60	45.0	74.250	10	011
	1080i	60	33.75	74.250	10	010
	1080p	60	33.75	148.5	11	011

ALTERNATE PIXEL SAMPLING MODE

Logic 1 input on CKINV (Pin 94) inverts the nominal ADC clock. CKINV can be switched between frames to implement the alternate pixel sampling mode. This allows higher effective image resolution to be achieved at lower pixel rates, but with lower frame rates.

On one frame, even pixels are digitized. On the subsequent frame, odd pixels are sampled. By reconstructing the entire frame in the graphics controller, a complete image can be reconstructed. This is very similar to the interlacing process used in broadcast television systems, but the interlacing is vertical instead of horizontal. The frame data is presented to the display at the full desired refresh rate (usually 60 Hz) so that no flicker artifacts are added.

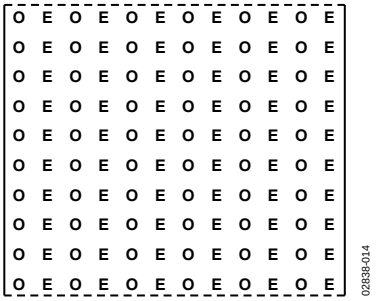

Figure 12. Odd and Even Pixels in a Frame

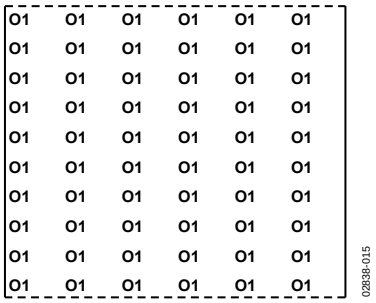

Figure 13. Odd Pixels from Frame 1

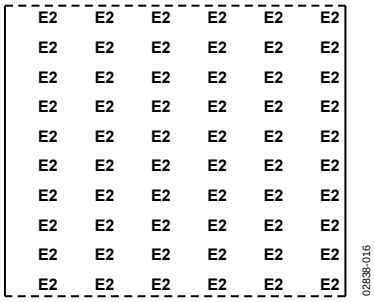

Figure 14. Even Pixels from Frame 2

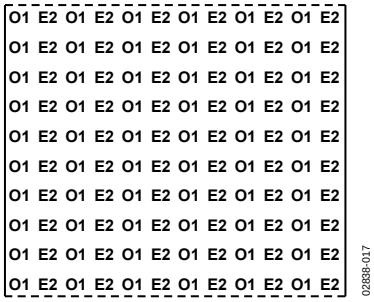

Figure 15. Combined Frame Output from Graphics Controller

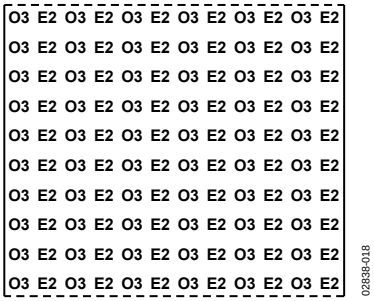

Figure 16. Subsequent Frame from Controller

TIMING—ANALOG INTERFACE

The timing diagrams (Figure 18 through Figure 27) show the operation of the AD9887A analog interface in all clock modes. The part establishes timing by sending the pixel corresponding with the leading edge of Hsync to Data Port A. In dual-channel mode, the next sample is sent to Data Port B. Subsequent samples are alternated between the A and B data ports. In single-channel mode, data is only sent to Data Port A, and Data Port B is placed in a high impedance state.

The output data clock signal is created so that its rising edge always occurs between transitions of Data Port A and can be used to latch the output data externally.

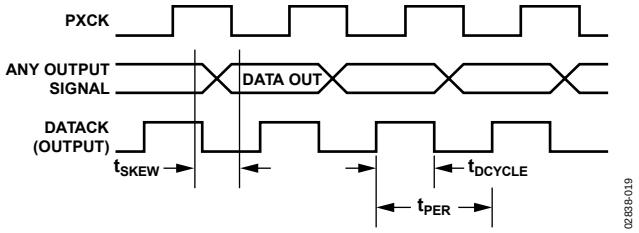

Figure 17. Analog Output Timing

Hsync Timing

Horizontal sync is processed in the AD9887A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The HSYNC input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the phase adjust register to optimize the pixel sampling time. Display systems use Hsync to align memory and display write cycles; therefore, it is important to have a stable timing relationship between the HSYNC output (HSOUT) and data clock (DATACK).

Three things happen to Hsync in the AD9887A. First, the polarity of the HSYNC input is determined and, thus, has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x04, Bit 4). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x07. Use the HSOUT signal to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the coast input and function are unnecessary and should not be used. In some systems, however, Hsync is disturbed during the vertical sync (Vsync) period, and sometimes Hsync pulses disappear. In other systems, such as those that use composite sync (Csync) signals or those that embed sync-on-green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock on to this new frequency and changes frequency by the end of the Vsync period. It then requires a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The coast input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can operate in this manner for several lines without significant frequency drift.

Coast can be provided by the graphics controller, or it can be internally generated by the AD9887A sync processing engine.

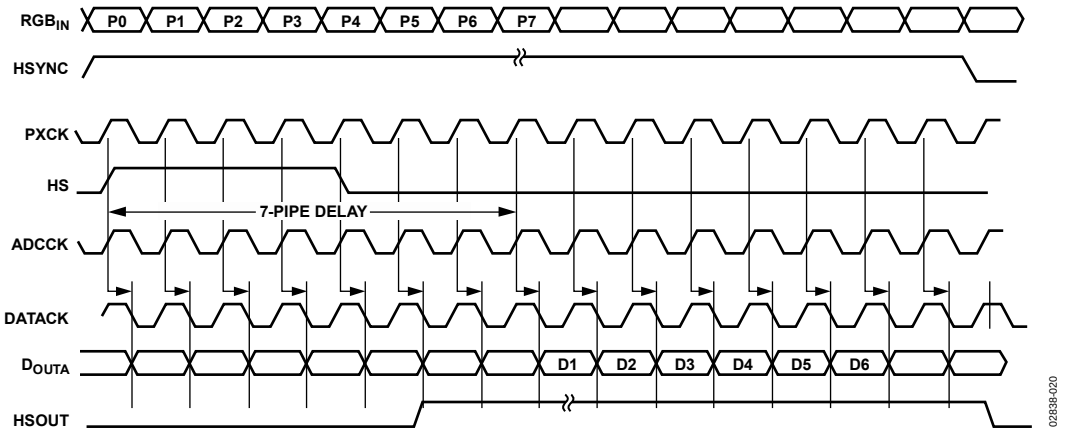

Figure 18. Single-Channel Mode (Analog Interface)

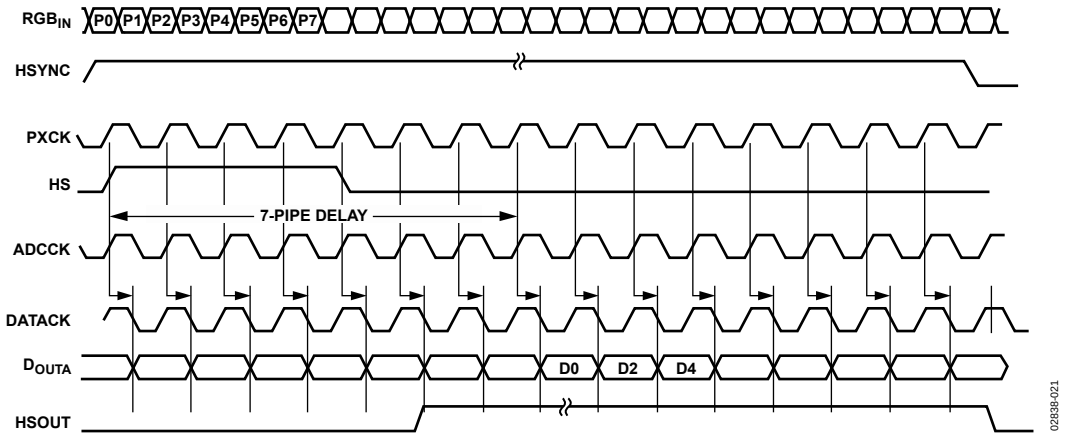

Figure 19. Single-Channel Mode, Alternate Pixel Sampling (Even Pixels, Analog Interface)

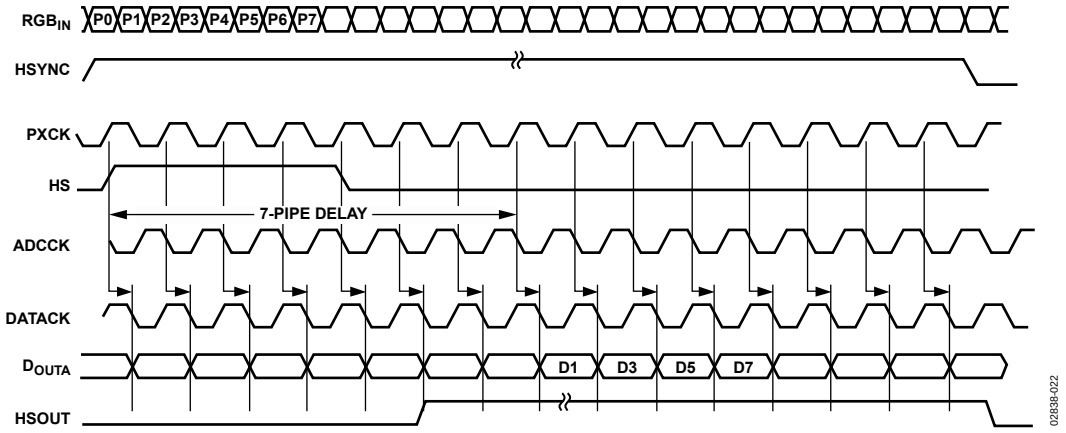

Figure 20. Single-Channel Mode, Alternate Pixel Sampling (Odd Pixels, Analog Interface)

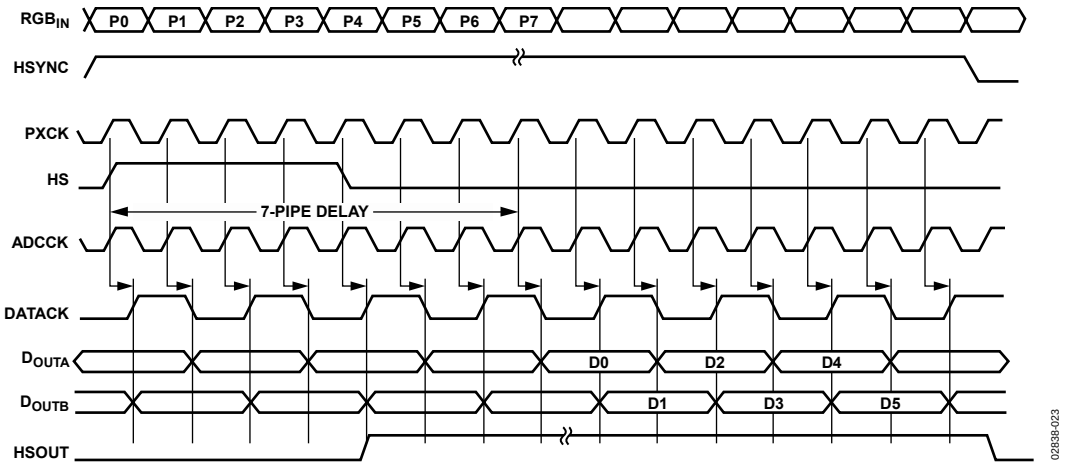

Figure 21. Dual-Channel Mode, Interleaved Outputs (Analog Interface), Outphase = 0

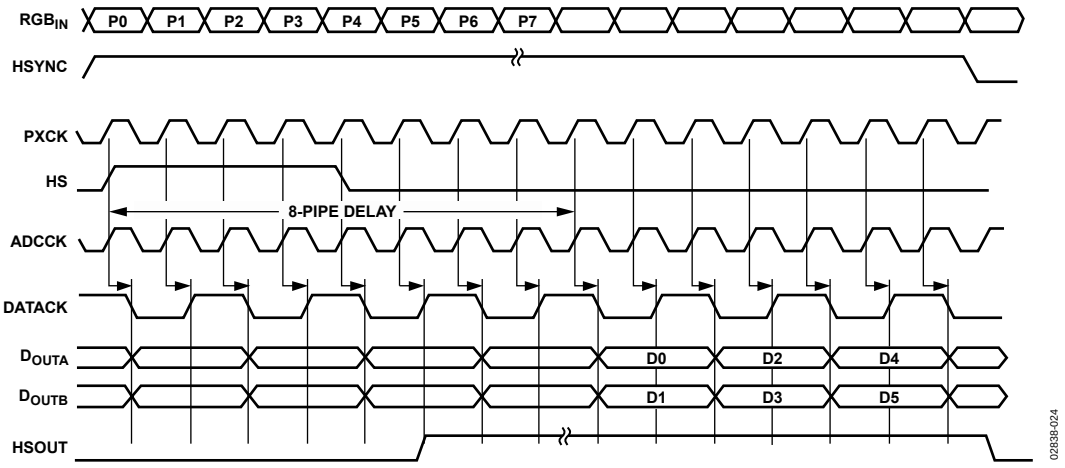

Figure 22. Dual-Channel Mode, Parallel Outputs (Analog Interface), Outphase = 0

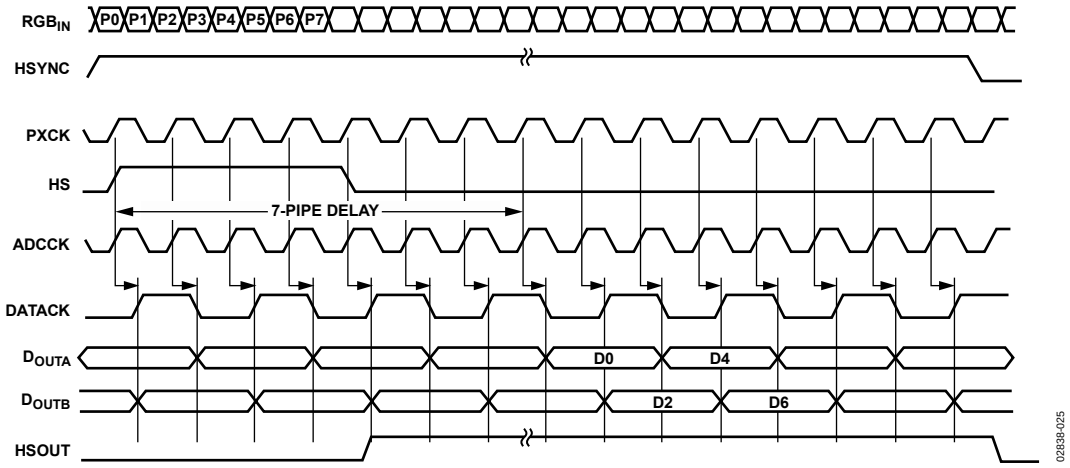

Figure 23. Dual-Channel Mode, Interleaved Outputs, Alternate Pixel Sampling (Even Pixels, Analog Interface), Outphase = 0

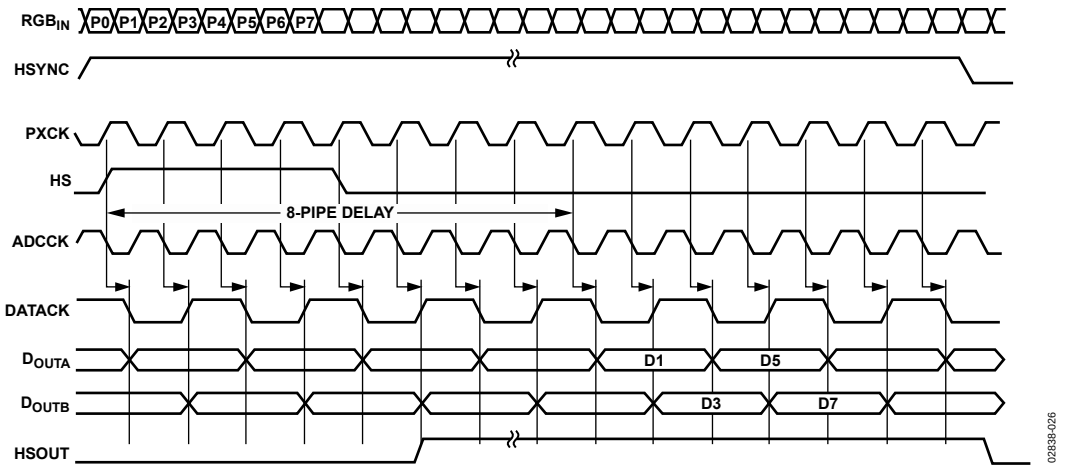

Figure 24. Dual-Channel Mode, Interleaved Outputs, Alternate Pixel Sampling (Odd Pixels, Analog Interface), Outphase = 0

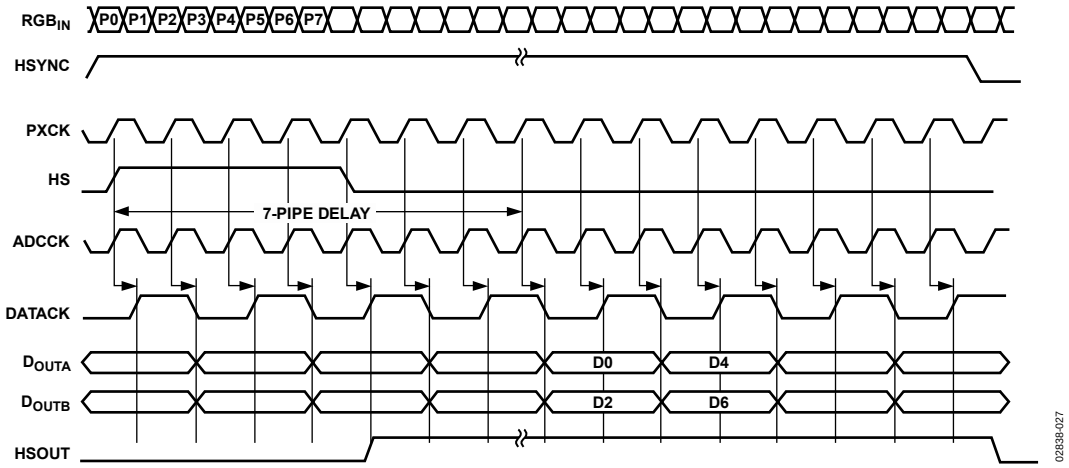

Figure 25. Dual-Channel Mode, Parallel Outputs, Alternate Pixel Sampling (Even Pixels, Analog Interface), Outphase = 0

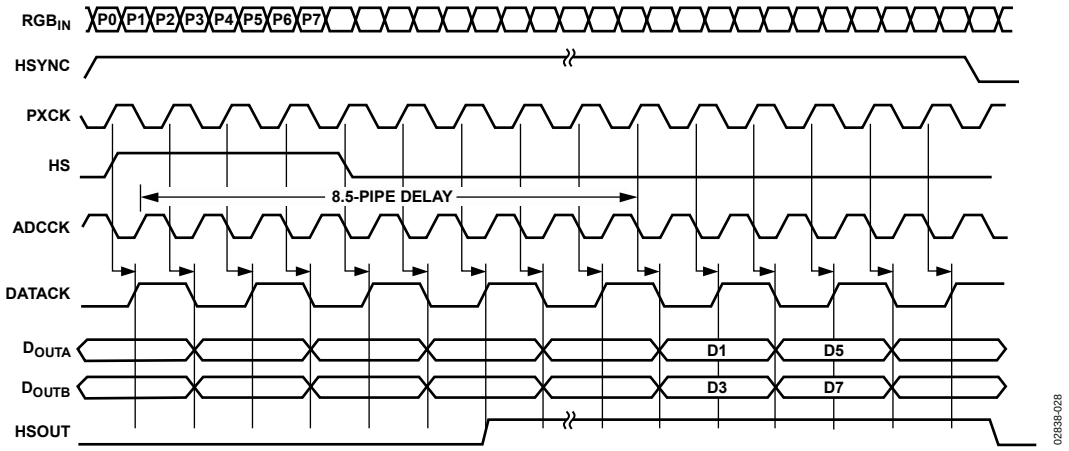

Figure 26. Dual-Channel Mode, Parallel Outputs, Alternate Pixel Sampling (Odd Pixels, Analog Interface), Outphase = 0

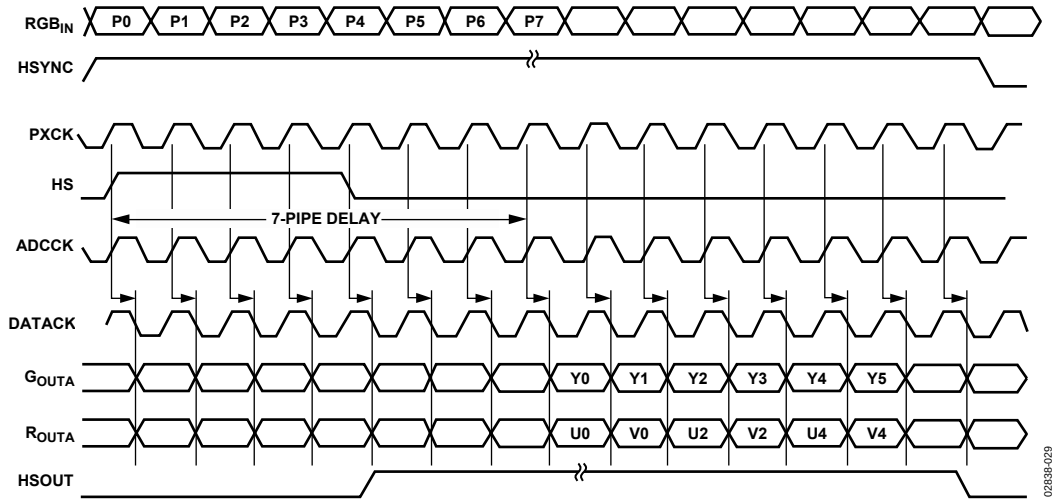

Figure 27. 4:2:2 Output Mode

THEORY OF OPERATION—INTERFACE DETECTION

ACTIVE INTERFACE DETECTION AND SELECTION

For interface detection in the AD9887A, the system should determine the correct interface and set the chip appropriately through the serial bus. An external circuit should be used to determine if the digital interface is active. A typical schematic for this detection function is shown in Figure 28.

It is recommended that the system implement the interface selection criteria, as described in Table 8. Because the digital interface clock detect bit (0x11[4]) has been unreliable in some applications, it is recommended that the active interface override bit (0x12[7]) be set to 1. This allows the system to select the interface through the serial bus register active interface select (AIS) bit (0x12[6]). This selection should be based on the analog interface detect obtained by OR'ing Bit 7, Bit 6, and Bit 5 of Register 0x11 and on the digital interface detect obtained through the external circuitry shown in Figure 28. When both interfaces are active, priority must be determined by the system and the appropriate interface must be selected via the AIS bit.

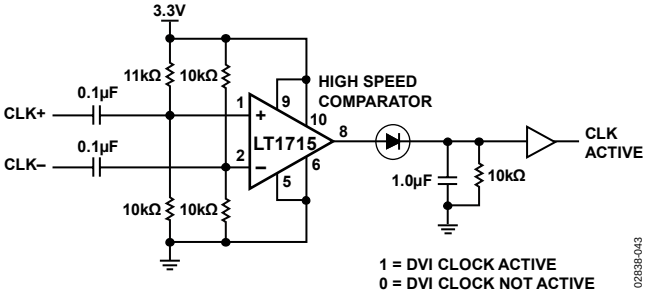

Figure 28. External Digital Interface Clock Detect Circuit

HOT-PLUG DETECT

In some HDCP-enabled applications it may be desirable to be able to switch between the analog and DVI interfaces without having an DVI plug/unplug event. In these applications, the circuit in Figure 29 should be used for the hot-plug detect connection. The FET switch should be controlled by the system-level software to force an HPD event whenever the selected interface is switched from the analog input to the DVI input.

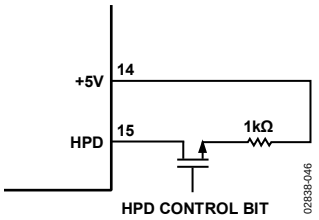

Figure 29. Manual Hot-Plug Detect

POWER MANAGEMENT

The AD9887A is a dual-interface device with shared outputs. Because only one interface can be used at a time, the unused interface should be powered down. When the analog interface is being used, most of the digital interface circuitry can be powered down and vice versa. This helps to minimize the total power dissipation of the AD9887A. In addition, if neither interface has activity on it, both interfaces should be powered down.

The correct power-down state is set by selecting an interface to be active through the serial bus when either or both interfaces are active, and by setting the power-down register bit (0x12[0]) to 0 when neither interface has activity on it. In a given power mode, not all circuitry in the inactive interface is powered down completely. When the digital interface is active, Hsync detect circuitry is not powered down. SOG, outputs, and the band gap reference are powered up if either interface is active. The serial bus stays active even if the entire chip is powered down.

Table 8. Interface Selection and Power-Down Controls

Power-Down	Active Interface Override (0x12[7])	Analog Interface Detect (0x11[7], 0x11[6], or 0x11[5])	Digital Interface Detect (from External Circuit)	AIS	Active Interface	Description
1	1	X	X	0	Analog	Force the analog interface active.
1	1	X	X	1	Digital	Force the digital interface active.
0	X	0	0	X	None	Neither interface is detected. Both interfaces are powered down and the S_{CDT} pin is set to Logic 0.
1	1	0	1	1	Digital	The digital interface is detected. Power down the analog interface.
1	1	1	0	0	Analog	The analog interface is detected. Power down the digital interface.
1	1	1	1	0	Analog	Both interfaces are detected. The analog interface has priority.
1	1	1	1	1	Digital	Both interfaces are detected. The digital interface has priority.

SCAN FUNCTION

The scan function is intended as a pseudo JTAG function for the manufacturing test of the board. The ordinary operation of the AD9887A is disabled during scanning. To enable the scan function, set Register 0x14, Bit 2, to 1. To scan data to all 48 digital outputs, apply 48 serial bits of data and 48 clock cycles (typically 5 MHz, maximum of 20 MHz) to the $SCAN_{IN}$ and $SCAN_{CLK}$ pins, respectively. The data is shifted in upon the rising edge of $SCAN_{CLK}$. The first serial bit shifted in appears at the RED A<7> output after one clock cycle.

After the next clock cycle, the first bit is shifted to RED A<6> and the next bit appears at RED A<7>. After 48 clock cycles, the first bit is shifted to the BLUE B<0> output and the 48th bit appears at the RED A<7> output. If $SCAN_{CLK}$ continues after 48 cycles, the data continues to be shifted from RED A<7> to BLUE B<0> and comes out of the $SCAN_{OUT}$ pin as serial data upon the falling edge of $SCAN_{CLK}$. This is illustrated in Figure 30. A setup time (t_{SU}) of 3 ns should be more than adequate; no hold time (t_{HOLD}) is required (0 ns). This is illustrated in Figure 31.

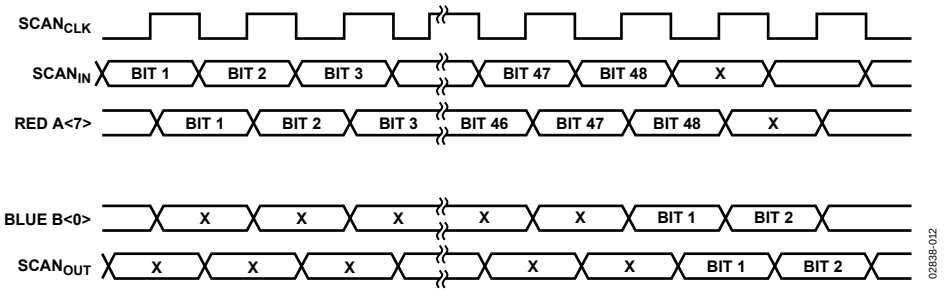

Figure 30. Scan Timing

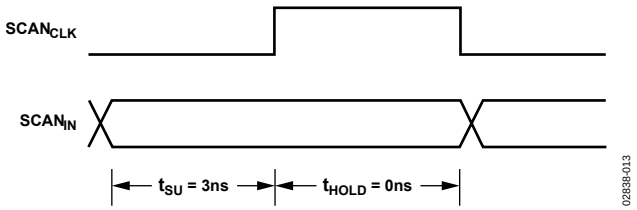

Figure 31. Scan Set-up and Hold Times

THEORY OF OPERATION—DIGITAL INTERFACE

CAPTURING ENCODED DATA

The first step in recovering encoded data is to capture the raw data. To accomplish this, the AD9887A uses a high speed, phase-locked loop (PLL) to generate clocks capable of oversampling the data at the correct frequencies. The data capture circuitry continuously monitors the incoming data during horizontal and vertical blanking periods (when DE is low) and independently selects the best sampling phase for each data channel. The phase information is stored and used until the next blanking period (one video line).

DATA FRAMES

The digital interface data is captured in groups, called data frames, of 10 bits each. During the active data period, each frame is made up of nine encoded video data bits and one dc-balancing bit. The data capture block receives this data serially, but outputs each frame in parallel, 10-bit words.

SPECIAL CHARACTERS

During periods of horizontal or vertical blanking (when DE is low), the digital transmitter transmits special characters that are used to set the video frame boundaries and the phase recovery loop for each channel. There are four special characters that can be received. They are used to identify the top, bottom, left side, and right side of each video frame. The data receiver can differentiate these special characters from active data, because the special characters have a different number of transitions per data frame.

CHANNEL RESYNCHRONIZATION

The purpose of the channel resynchronization block is to resynchronize the three data channels to a single internal data clock. Even if all three data channels are on different phases of the PLL clock (0°, 120°, and 240°), this block can resynchronize the channels from a worst-case skew of one full input period (8.93 ns at 170 MHz).

DATA DECODER

The data decoder receives frames of data and sync signals from the data capture block in 10-bit, parallel words and decodes them into groups of eight RGB/YUV bits, two control bits, and a data enable (DE) bit.

HDCP

The AD9887A contains circuitry necessary for decrypting a high-bandwidth digital content protection (HDCP) encoded DVI video stream. A typical HDCP implementation is shown in Figure 32. Several features of the AD9887A make decryption possible and ease the implementation of HDCP.

The basic components of HDCP are included in the AD9887A. A slave serial bus connects to the DDC clock and the DDC data pins on the DVI connector to allow the HDCP-enabled DVI transmitter to coordinate the HDCP algorithm with the AD9887A. A second serial port (MDA/MCL) allows the AD9887A to read the HDCP keys and key selection vector (KSV) stored in an external serial EEPROM. When transmitting encrypted video, the DVI transmitter enables HDCP through the DDC port.

The AD9887A then decodes the DVI stream using information provided by the transmitter, HDCP keys, and KSV. The AD9887A allows the MDA and MCL pins to be three-state, using the MDA/MCL three-state bit (Register 0x1B, Bit 7) in the configuration registers. The three-state feature allows the EEPROM to be programmed in-circuit. The MDA/MCL port must be three-state before attempting to program the EEPROM using an external master. The keys are stored in an I²C®-compatible 3.3 V serial EEPROM of at least 512 bytes. The EEPROM should have a device address of 0xA0.

Proprietary software licensed from Analog Devices, Inc. encrypts the keys and creates properly formatted EEPROM images for use in a production environment. Encrypting the keys helps maintain the confidentiality of the HDCP keys, as required by the HDCP v1.0 specification. The AD9887A includes hardware for decrypting the keys in the external EEPROM.

ADI provides a royalty-free license for the proprietary software needed by customers to encrypt the keys between the AD9887A and the EEPROM only after customers provide evidence of a completed HDCP *Adopter's License Agreement* and sign the *Analog Devices Software License Agreement*. The *Adopter's License Agreement* is maintained by Digital Content Protection, LLC and can be downloaded from www.digital-cp.com. To obtain the *Analog Devices Software License Agreement*, contact the Display Electronics Product Line directly by sending an email to flatpanel_apps@analog.com.

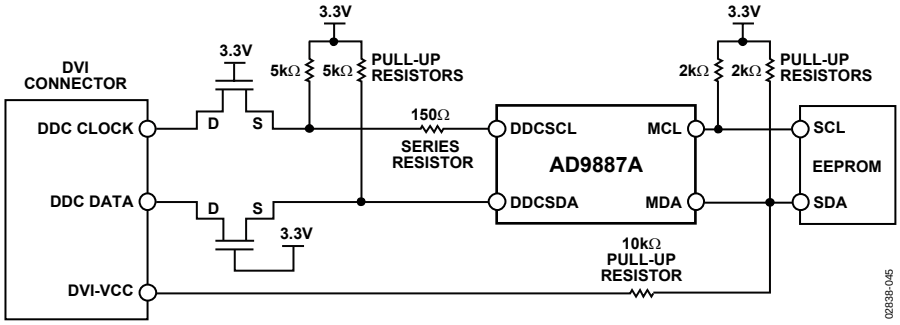

Figure 32. HDCP Implementation Using the AD9887A

GENERAL TIMING DIAGRAMS—DIGITAL INTERFACE

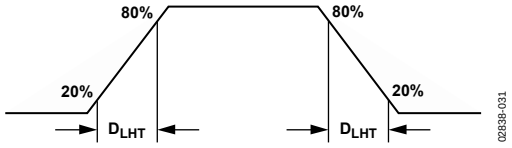

Figure 33. Digital Output Rise and Fall Times

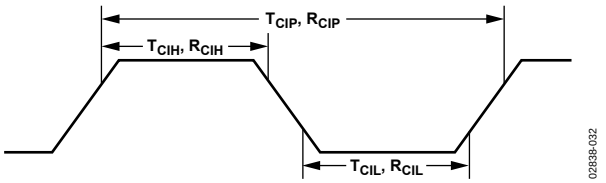

Figure 34. Clock Cycle/High/Low Times

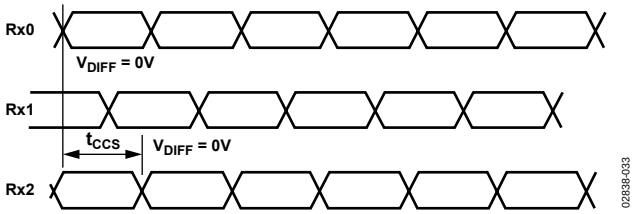

Figure 35. Channel-to-Channel Skew Timing

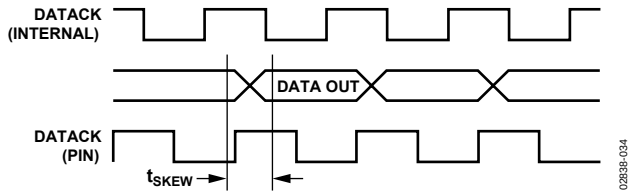

Figure 36. DVI Output Timing

TIMING MODE DIAGRAMS—DIGITAL INTERFACE

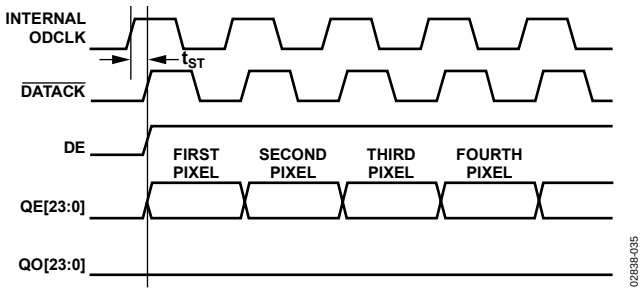

Figure 37. One Pixel per Clock (DATACK Inverted)

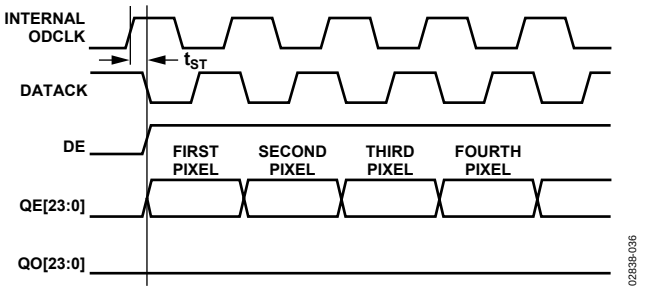

Figure 38. One Pixel per Clock (DATACK Not Inverted)

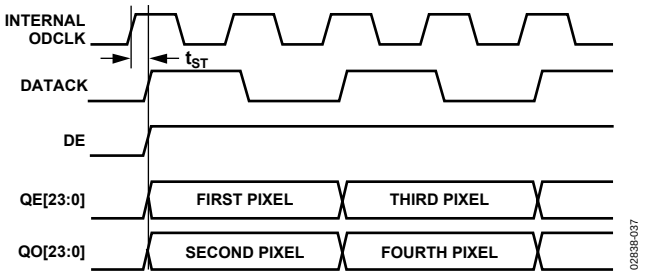

Figure 39. Two Pixels per Clock

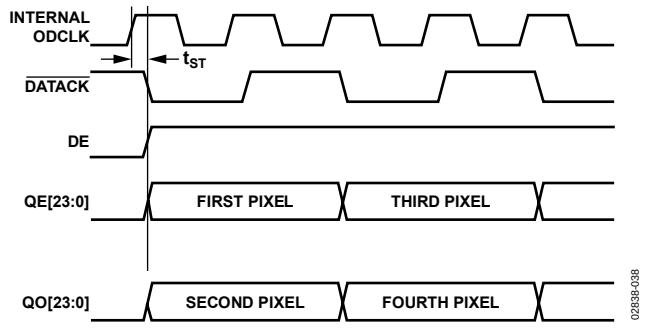

Figure 40. Two Pixels per Clock (DATACK Inverted)

2-WIRE SERIAL REGISTER MAP

The AD9887A is initialized and controlled by a set of registers that determine the operating modes. An external controller is used to write and read the control registers through the 2-line serial interface port.

Table 9. Control Register Map

Address	Read and Write, or Read Only	Bits	Default Value	Register Name	Description
0x00	RO	7:0		Chip Revision	Bit 7 through Bit 4 represent functional revisions to the analog interface. Bit 3 through Bit 0 represent nonfunctional related revisions. Revision 0 = 0000 0000.
0x01	R/W	7:0	01101001	PLL Divide Ratio MSBs	This register is for Bits[11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first when a change is needed. (This gives the PLL more time to lock.)[1]
0x02	R/W	7:4	1101****	PLL Divide Ratio LSBs	This register is for Bits[3:0] of the PLL divider. Links to the PLL divide ratio MSBs to make a 12-bit value.[1]
0x03	R/W	7:2	1******* *01***** ***001**	Clock Generator Controls	Bit 7—Must be set to 1 for proper device operation. Bits[6:5]—VCO Range Select. Selects VCO frequency range (see the PLL section). Bits[4:2]—Charge-Pump Current. Varies the current that drives the low-pass filter (see the PLL section).
0x04	R/W	7:3	10000***	Clock Phase Adjust	Clock Phase Adjust. Larger values mean more delay. (1 LSB = T/32)
0x05	R/W	7:0	10000000	Clamp Placement	Places the clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
0x06	R/W	7:0	10000000	Clamp Duration	Number of clock periods that the clamp signal is actively clamping.
0x07	R/W	7:0	00100000	Hsync Output Pulse Width	Sets the number of pixel clocks that HSOUT remains active.
0x08	R/W	7:0	10000000	REDGAIN	Controls ADC input range (contrast) of red channel. Bigger values result in less contrast.
0x09	R/W	7:0	10000000	GREENGAIN	Controls ADC input range (contrast) of green channel. Bigger values result in less contrast.
0x0A	R/W	7:0	10000000	BLUEGAIN	Controls ADC input range (contrast) of blue channel. Bigger values result in less contrast.
0x0B	R/W	7:1	1000000*	REDOFST	Controls dc offset (brightness) of red channel. Bigger values decrease brightness.
0x0C	R/W	7:1	1000000*	GREENOFST	Controls dc offset (brightness) of green channel. Bigger values decrease brightness.
0x0D	R/W	7:1	1000000*	BLUEOFST	Controls dc offset (brightness) of blue channel. Bigger values decrease brightness.
0x0E	R/W	7:3	1******* *1****** **0***** ***0**** ****0***	Mode Control 1	Bit 7—Channel Mode. Determines single-channel or dual-channel output mode. Logic 0 = single-channel mode; Logic 1 = dual-channel mode. Bit 6—Output Mode. Determines interleaved or parallel output mode. Logic 0 = interleaved mode; Logic 1 = parallel mode. Bit 5—Output Port Phase (OUTPHASE). Determines which port outputs the first data byte after Hsync. Logic 0 = B port; Logic 1 = A port. Bit 4—HSYNC Output Polarity. Logic 0 = logic high sync; Logic 1 = logic low sync. Bit 3—VSYNC Output Invert. Logic 0 = invert; Logic 1 = no invert.
0x0F	R/W	7:0	1******* *1****** **0*****	PLL and Clamp Control	Bit 7—HSYNC Input Polarity. Indicates the polarity of incoming HSYNC signal to the PLL. Logic 0 = active low; Logic 1 = active high. Bit 6—COAST Input Polarity. Changes polarity of external coast signal. Logic 0 = active low; Logic 1 = active high. Bit 5—Clamp Input Signal Source (EXTCLMP). Chooses between HSYNC for CLAMP signal and another external signal to be used for clamping. Logic 0 = HSYNC; Logic 1 = externally provided clamp signal.

Address	Read and Write, or Read Only	Bits	Default Value	Register Name	Description
			1*		Bit 4—Clamp Input Signal Polarity (name also same as Bit 6). Valid only with external CLAMP signal. Logic 0 = active low; Logic 1 = active high.
			****0***		Bit 3—External Clock Select (EXTCLK). Shuts down the PLL and allows the use of an external clock to drive the part. Logic 0 = uses internal PLL; Logic 1 = bypasses the internal PLL.
			*****0**		Bit 2—Red Clamp Select. Logic 0 selects clamp to ground; Logic 1 selects clamp to midscale. (Voltage at Pin 120 and 118)
			******0*		Bit 1—Green Clamp Select. Logic 0 selects clamp to ground; Logic 1 selects clamp to midscale. (Voltage at Pin 111 and 109)
			*******0		Bit 0—Blue Clamp Select. Logic 0 selects clamp to ground; Logic 1 selects clamp to midscale. (Voltage at Pin 101 and 99)
0x10	R/W	7:2	0*******	Mode Control 2	Bit 7—CKINV: Data Output Clock Invert. Logic 0 = not inverted; Logic 1 = inverted (digital interface only).
			*0******		Bit 6—Pixel Select. Selects either one or two pixels per clock mode. Logic 0 = one pixel/clock; Logic 1 = two pixels/clock (digital interface only).
			11**		Bit 5, 4—Output Drive. Selects among high, medium, and low output drive strength. Logic 11 or Logic 10 = high, Logic 01 = medium, and Logic 00 = low.
			****0***		Bit 3—PDO: High Impedance Outputs. Logic 0 = normal; Logic 1 = high impedance.
			*****1**		Bit 2—Sync Detect Polarity. This bit sets the polarity for the S_{CDT} pin. Logic 1 = active high; Logic 0 = active low.
0x11	RO	7:1	1*******	Sync Detection and Active Interface Control	Bit 7—Analog Interface HSYNC Detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise, it is set to Logic 0.
			*1******		Bit 6—Analog Interface Sync-on-Green Detect. It is set to Logic 1 if sync is present on the green video input; otherwise, it is set to 0.
			1***		Bit 5—Analog Interface VSYNC Detect. It is set to Logic 1 if Vsync is present on the analog interface; otherwise, it is set to Logic 0.
			1*		Bit 4—Digital Interface Clock Detect. It is set to Logic 1 if the clock is present on the digital interface; otherwise, it is set to Logic 0.
			****1***		Bit 3—Active Interface (AI). This bit indicates which interface is active. Logic 0 = analog interface; Logic 1 = digital interface.
			*****1**		Bit 2—Active Hsync (AHS). This bit indicates which analog Hsync is being used. Logic 0 = HSYNC input pin; Logic 1 = Hsync from sync-on-green.
			******1*		Bit 1—Active Vsync (AVS). This bit indicates which analog Vsync is being used. Logic 0 = VSYNC input pin; Logic 1 = Vsync from sync-on-green.
0x12	R/W	7:0	0*******	Active Interface	Bit 7—Active Interface Override (AIO). If set to Logic 1, the user can select the active interface via Bit 6. If set to Logic 0, the active interface is selected via Bit 3 in Register 0x11.
			*0******		Bit 6—Active Interface Select (AIS). Logic 0 selects the analog interface as active. Logic 1 selects the digital interface as active. Note that the indicated interface is active only if Bit 7 is set to Logic 1 or if both interfaces are active (Bit 6 or Bit 7 and Bit 4 = Logic 1 in Register 0x11).
			0***		Bit 5—Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 4. If set to Logic 0, the active interface is selected via Bit 2 in Register 0x11.
			0*		Bit 4—Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects sync-on-green as the active sync. Note that the indicated Hsync is used only if Bit 5 is set to Logic 1 or if both syncs are active (Bit 6 and Bit 7 = Logic 1 in Register 0x11).
			****0***		Bit 3—Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 2. If set to Logic 0, the active interface is selected via Bit 1 in Register 0x11.

Address	Read and Write, or Read Only	Bits	Default Value	Register Name	Description
			*****0**		Bit 2—Output Vsync Select. Logic 0 selects raw Vsync as the output Vsync. Logic 1 selects sync separator output as the active Vsync. Note that the indicated Vsync is used only if Bit 3 is set to Logic 1.
			******0*		Bit 1—COAST Select. Logic 0 selects the COAST input pin used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast.
			*******1		Bit 0—$\overline{\text{PWRDN}}$. Full Chip Power-Down, active low. Logic 0 = full chip power-down; Logic 1 = normal.
0x13	R/W	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold. Sets the number of clock cycles that the sync separator counts before toggling high or low. This should be set to a number greater than the maximum Hsync or equalization pulse width.
0x14	R/W	7:0	***1****	Control Bits	Bit 4—Must be set to 1 for proper operation.
			****0***		Bit 3—Must be set to 0 for proper operation.
			*****0**		Bit 2—Scan Enable. Logic 0 = scan function disabled; Logic 1 = scan function enabled.
			******0*		Bit 1—COAST Input Polarity Override. Logic 0 = polarity determined by chip; Logic 1 = polarity determined by user via Bit 6 in Register 0x0F.
			*******0		Bit 0—HSYNC Input Polarity Override. Logic 0 = polarity determined by chip; Logic 1 = polarity determined by user via Bit 7 in Register 0x0F.
0x15	RO	7:5	0*******	Polarity Status	Bit 7—Hsync Input Polarity Status. Logic 0 = active low; Logic 1 = active high.
			*0******		Bit 6—Vsync Output Polarity Status. Logic 0 = active high; Logic 1 = active low.
			0***		Bit 5—Coast Input Polarity Status. Logic 0 = active low; Logic 1 = active high.
0x16	R/W	7:2	10111***	Control Bits	Bits[7:3]—Sync-on-Green Slicer Threshold.
			*****1**		Bit 2—Must be set to 0 for proper operation.
0x17	R/W	7:0	00000000	Precoast	Sets the number of Hsyncs prior to Vsync before which coast goes active.
0x18	R/W	7:0	00000000	Postcoast	Sets the number of Hsyncs following Vsync before coast goes active.
0x19	R/W	7:0	00000000	Test Register	Must be set to default for proper operation.
0x1A	R/W	7:0	11111111	Test	Must be set to 01000001 for proper operation.
0x1B	R/W	7:0	00000000		Set to 0x00 for autogain mode and 0x10 for manual-gain mode
0x1C	R/W	7:0	00000***		Bits [7:3]—Set to 00000*** for autogain mode and 00101*** for manual-gain mode
			*****1**		Bit 2—CbCr Output Order.
			******1*		Bit 1—Must be set to 0 for standard input sampling.
			*******1	4:2:2 Control	Bit 0—Output Format Mode Select. Logic 1 = 4:4:4 mode; Logic 0 = 4:2:2 mode.
0x1D	RO	7:0	*_*****		HDCP Keys Detected. Logic 0 = not detected; Logic 1 = detected.
0x1E	R/W	7:0	11111111		Must set to 0xFF for proper operation.
0x1F	R/W	7:0	10000100		Must set to 0x84 for proper operation.
0x20	R/W	7:0	0*******		Bit 7—HDCP A0 Serial Address Bit. For Logic 0, Address = 0x74. For Logic 1, Address = 0x76.
			*0******		Bit 6—MDA Pin Select. For Logic 0, Pin 49 = Ctrl3 signal. For Logic 1, Pin 49 = MDA for HDCP.
			0***		Bit 5—Analog Input Bandwidth Control. Logic 0 = high.
			0*		Bit 4—MDA/MCL Three-State. Logic 0 = three-state; Logic 1 = normal operation.
			****1***		Bit 3—External Oscillator. Logic 1 = internal; Logic 0 = use external oscillator on A0.
			*****0**		Normal Operation.
0x21	R/W	7:0	00000000	TDMS Gain Control	Set to 0x00 for autogain mode and 0x64 for manual-gain mode.

Address	Read and Write, or Read Only	Bits	Default Value	Register Name	Description
0x22	R/W	7:0	00000000		Must be set to default.
0x23	R/W	7:0	00000000		Must be set to 0x2A for proper operation.
0x24	R/W	7:0	00000000		Must be set to default.
0x25	R/W	7:0	11110000		Must be set to default.
0x26	R/W	7:0	11111111		Must be set to default.
0x27			00001111		Must be set to default

[1] The AD9887A only updates the PLL divide ratio when the LSBs are written to Register 0x02.

2-WIRE SERIAL CONTROL REGISTER DETAILS

Chip Identification

0x00 7:0 Chip Revision

Bit 7 through Bit 4 represent functional revisions to the analog interface. Changes in these bits generally indicate that software and/or hardware changes are required for the chip to work properly. Bit 3 through Bit 0 represent nonfunctional related revisions and are reset to 0000 when the MSBs are changed. Changes in these bits are considered transparent to the user.

PLL Divider Control

0x01 7:0 PLL Divide Ratio MSBs

The 8 MSBs of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 221 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency. VESA has established standard timing specifications that help determine the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table 7). However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced. The power-up default of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9887A updates the full divide ratio only when the LSBs are changed. Writing to this register by itself does not trigger an update.

0x02 7:4 PLL Divide Ratio LSBs

The 4 LSBs of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9887A updates the full divide ratio only when the user writes to this register.

Clock Generator Controls

0x03 7 Test

Must be set to 1 for proper device operation.

0x03 6:5 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL provides the best jitter performance at high frequencies. To output low pixel rates while minimizing jitter, the PLL operates at a higher frequency and divides down the clock rate afterwards. Table 10 shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table 10. VCO Ranges

VCORNGE	Pixel Rate Range
00	12 to 37
01	37 to 74
10	74 to 140
11	140 to 170

The power-up default value is 01.

0x03 4–2 CURRENT Charge-Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table 11. Charge-Pump Currents

CURRENT	Current (µA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

See Table 7 for the recommended CURRENT settings. The power-up default value is CURRENT = 001.

0x04 7:3 Clock Phase Adjust

A 5-bit value that adjusts the sampling phase in 32 steps across one pixel period. Each step represents an 11.2° shift in sampling phase.

The power-up default value is 16.

Clamp Timing

0x05 7:0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When EXTCLMP = 0, a clamp signal is generated internally at a position established by the clamp placement for a duration set by the clamp duration. Clamping is started [clamp placement] pixel periods after the trailing edge of Hsync. The clamp placement can be programmed to any value between 1 and 255. A value of 0 is not supported.

The clamp should be placed during a time when the input signal presents a stable black-level reference, usually during a period between Hsync and the image called the back porch. When EXTCLMP = 1, this register is ignored.

0x06 7:0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

When EXTCLMP = 0, a clamp signal is generated internally at a position established by the clamp placement for a duration set by the clamp duration. Clamping is started [clamp placement] pixel periods after the trailing edge of Hsync and continues for [clamp duration] pixel periods. The clamp duration can be programmed to a value between 1 and 255. A value of 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen and can cause slow recovery from large changes in the average picture level (APL) or brightness.

When EXTCLMP = 1, this register is ignored.

Hsync Pulse Width

0x07 7:0 Hsync Output Pulse Width

An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9887A counts the number of pixel clock cycles set in this register. This triggers the trailing edge of the Hsync output, which is also phase adjusted.

Input Gain

0x08 7:0 Red Channel Gain Adjust (REDGAIN)

An 8-bit word that sets the gain of the red channel.

The AD9887A can accommodate input signals with a full-scale range between 0.5 V and 1.5 V p-p. Setting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that increasing REDGAIN results in the picture having less contrast because the input signal uses fewer of the available converter codes (see Figure 6).

0x09 7:0 Green Channel Gain Adjust (GREENGAIN)

An 8-bit word that sets the gain of the green channel. See REDGAIN (0x08).

0x0A 7:0 Blue Channel Gain Adjust (BLUEGAIN)

An 8-bit word that sets the gain of the blue channel. See REDGAIN (0x08).

Input Offset

0x0B 7:1 Red Channel Offset Adjust (REDOFST)

A 7-bit offset binary word that sets the dc offset of the red channel (REDOFST). An offset adjustment of 1 LSB equals approximately 1 LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel changes. A nominal setting of 63 results in the channel nominally clamping to Code 00 during the back porch clamping interval. An offset setting of 127 results in the channel clamping to Code 63 of the ADC. An offset setting of 0 clamps to Code −63 (off the bottom of the range). Increasing the value of red offset decreases the brightness of the channel.

0x0C 7:1 Green Channel Offset Adjust (GREENOFST)

A 7-bit offset binary word that sets the dc offset of the green channel. See REDOFST (0B).

0x0D 7:1 Blue Channel Offset Adjust (BLUEOFST)

A 7-bit offset binary word that sets the dc offset of the blue channel. See REDOFST (0B).

Mode Control 1

0x0E 7 Channel Mode

A bit that determines whether all pixels are presented to a single port (Port A), or if alternating pixels are demultiplexed to Port A and Port B.

Table 12. Channel Mode Settings

DEMUX	Function
0	All data goes to Port A
1	Alternate pixels go to Port A and Port B

When DEMUX = 0, Port B outputs are in a high impedance state. The maximum data rate for single-port mode is 100 MHz. The timing diagrams show the effects of this option.

The power-up default value is 1.

0x0E 6 Output Mode

A bit that determines whether all pixels are simultaneously presented to Port A and Port B upon every second DATACK rising edge or alternately presented to Port A and Port B upon successive DATACK rising edges.

Table 13. Output Mode Settings

PARALLEL	Function
0	Data is interleaved
1	Data is simultaneous upon every other data clock

When in single-port mode (DEMUX = 0), this bit is ignored. The timing diagrams (Figure 18 through Figure 27 and Figure 37 through Figure 39) show the effects of this option.

The power-up default value is PARALLEL = 1.

0x0E 5 Output Port Phase

One bit that determines whether even or odd pixels go to Port A.

Table 14. Output Port Phase (OUTPHASE) Settings

OUTPHASE	First Pixel After Hsync
1	Port B
0	Port A

In normal operation (OUTPHASE = 0) when operating in dual-port output mode (DEMUX = 1), the first sample after the Hsync leading edge is presented to Port A, every subsequent odd sample goes to Port A, and all even samples go to Port B.

When OUTPHASE = 1, these ports are reversed and the first sample goes to Port B.

When DEMUX = 0, this bit is ignored because data always comes out of only Port A.

0x0E 4 HSYNC Output Polarity

One bit that determines the polarity of the HSYNC output and the SOG output. Table 15 shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table 15. HSYNC Output Polarity Settings

Setting	HSYNC
0	Logic 1 (negative polarity)
1	Logic 0 (positive polarity)

The default setting for this register is 1. This option works on both the analog and digital interfaces.

0x0E 3 VSYNC Output Invert

One bit that inverts the polarity of the VSYNC output. Table 16 shows the effect of this option.

Table 16. VSYNC Output Polarity Settings

Setting	VSYNC Output
0	Invert
1	No invert

The default setting for this register is 1. This option works on both the analog and digital interfaces.

0x0F 7 HSYNC Input Polarity

A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL HSYNC input.

Table 17. HSYNC Input Polarity (HSPOL) Settings

HSPOL	Function
0	Active low
1	Active high

Active low is the traditional negative-going Hsync pulse. All timing is based on the leading edge of Hsync, which is the falling edge. The rising edge has no effect.

Active high is inverted from the traditional Hsync, with a positive-going pulse; therefore, timing is based on the leading edge of Hsync, which is now the rising edge.

The device operates if this bit is set incorrectly, but the internally generated clamp position, as established by CLPOS, will not be placed as expected, which might generate clamping errors.

The power-up default value is HSPOL = 1.

0x0F 6 COAST Input Polarity

A bit to indicate the polarity of the COAST signal that is applied to the PLL COAST input.

Table 18. COAST Input Polarity (CSTPOL) Settings

CSTPOL	Function
0	Active low
1	Active high

Active low means that the clock generator ignores HSYNC inputs when coast is low and continues operating at the same nominal frequency until coast goes high.

Active high means that the clock generator ignores HSYNC inputs when coast is high and continues operating at the same nominal frequency until coast goes low.

This function must be used with the COAST polarity override bit (Register 0x14, Bit 1).

The power-up default value is CSTPOL = 1.

0x0F 5 Clamp Input Signal Source

A bit that determines the source of clamp timing.

Table 19. Clamp Input Signal Source (EXTCLMP) Settings

EXTCLMP	Function
0	Internally generated clamp
1	Externally provided clamp signal

Logic 0 enables the clamp timing circuitry controlled by CLPLACE and CLDUR. The clamp position and duration is counted from the trailing edge of Hsync.

Logic 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the CLAMPOL bit.

The power-up default value is EXTCLMP = 0.

0x0F 4 CLAMP Input Signal Polarity

A bit that determines the polarity of the externally provided CLAMP signal.

Table 20. CLAMP Input Signal Polarity (EXTCLMP) Settings

EXTCLMP	Function
0	Active low
1	Active high

Logic 0 means that the circuit clamps when CLAMP is high and passes the signal to the ADC when CLAMP is low.

Logic 1 means that the circuit clamps when CLAMP is low and passes the signal to the ADC when CLAMP is high.

The power-up default value is CLAMPOL = 1.

0x0F 3 External Clock Select

A bit that determines the source of the pixel clock.

Table 21. External Clock Select (EXTCLK) Settings

EXTCLK	Function
0	Internally generated clock
1	Externally provided clock signal

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided Hsync.

A Logic 1 enables the external CKEXT input pin. In this mode, the PLL divide ratio (PLLDIV) is ignored and the clock phase adjust (PHASE) is still functional.

The power-up default value is EXTCLK = 0.

0x0F 2 Red Clamp Select

A bit that determines whether the red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YCbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 118, $R_{CLAMP}V$.

Table 22. Red Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 118)

The default setting for this register is 0.

0x0F 1 Green Clamp Select

A bit that determines whether the green channel is clamped to ground or to midscale.

Table 23. Green Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 109)

The default setting for this register is 0.

0x0F 0 Blue Clamp Select

A bit that determines whether the blue channel is clamped to ground or to midscale.

Table 24. Blue Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 99)

The default setting for this register is 0.

Mode Control 2

0x10 7 Data Output Clock Invert (CKINV)

A control bit for the inversion of the output data clocks (Pin 134 and Pin 135). This function only works for the digital interface. When not inverted, data is output upon the trailing edge of the data clock. See Figure 37 through Figure 40 for how this affects timing.

Table 25. Data Output Clock Invert (CKINV) Settings

CKINV	Function
0	Not inverted
1	Inverted

The default for this register is 0.

0x10 6 Pixel Select

This bit selects either one or two pixels per clock mode for the digital interface. It determines whether the output is from a single port (even port only) at the full data rate, or from two ports (both even and odd ports) at half the full data rate per port. Logic 0 selects one pixel per clock (even port only). Logic 1 selects two pixels per clock (both ports). See the Digital Interface Timing Diagrams (Figure 37 through Figure 40) for visual representations of this function. Note that this function operates exactly like the demux function on the analog interface.

Table 26. Pixel Select Settings

Pixel Select	Function
0	One pixel per clock
1	Two pixels per clock

The default for this register is 0.

0x10 5, 4 Output Drive

These two bits select the drive strength for the high speed digital outputs (all data output and clock output pins). Higher drive strength results in faster rise/fall times and enables easier capture of data in general. Lower drive strength results in slower rise/fall times and reduces EMI and digitally generated power supply noise. The exact timing specifications for each of these modes are specified in Table 7.

Table 27. Output Drive Strength Settings

Bit 5	Bit 4	Result
1	X	High drive strength
0	1	Medium drive strength
0	0	Low drive strength

The default for this register is 11. This option works on both the analog and digital interfaces.

0x10 3 Power-Down Outputs (PDO)

This bit can put the outputs into a high impedance mode. This applies to all outputs except SOGOUT and REFOUT.

Table 28. Power-Down Output (PDO) Settings

PDO	Function
0	Normal operation
1	Three-state

The default for this register is 0. This option works on both the analog and digital interfaces.

0x10 2 Sync Detect Polarity

This pin controls the polarity of the sync detect output pin (Pin 136).

Table 29. Sync Detect Polarity Settings

Polarity	Function
0	Activity = Logic 1 output
1	Activity = Logic 0 output

The default for this register is 0. This option works on both the analog and digital interfaces.

SYNC Detection/Active Interface Control

0x11 7 Analog Interface HSYNC Detect

This bit is used to indicate when activity is detected on the HSYNC input pin (Pin 82). If HSYNC is held high or low, activity is not detected.

Table 30. Analog Interface HSYNC Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 43 shows where this function is implemented.

0x11 6 Analog Interface Sync-on-Green Detect

This bit is used to indicate when sync activity is detected on the sync-on-green input pin (Pin 108).

Table 31. Analog Interface Sync-on-Green Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 43 shows where this function is implemented. Warning: Even if no sync is present on the green video input, normal video might trigger activity.

0x11 5 Analog Interface VSYNC Detect

This bit indicates when activity is detected on the VSYNC input pin (Pin 81). If VSYNC is held high or low, activity is not detected.

Table 32. Analog Interface VSYNC Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 43 shows where this function is implemented.

0x11 4 Digital Interface Clock Detect

This indicates when activity is detected on the digital interface clock input. Because this register is unreliable in certain applications, an external DVI clock detect shown in Figure 28 is recommended.

Table 33. Digital Interface Clock Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 43 shows where this function is implemented.

0x11 3 Active Interface (AI)

This bit indicates which interface should be active, analog or digital. It checks for activity on the analog and digital interfaces, then determines which should be active according to the conditions outlined in Table 34. Specifically, analog interface detection is determined by OR'ing Bit 7, Bit 6, and Bit 5 from this register.

Digital interface detection is determined by Bit 4 in this register. If both interfaces are detected, the user can determine which has priority via Bit 6 in Register 0x12. The user can override this function via Bit 7 in Register 0x12. If the override bit is set to Logic 1, this bit is forced to the set state of Bit 6 in Register 0x12.

Table 34. Active Interface Results

Bits 7, 6, or 5 (Analog Detection)	Bit 4 (Digital Detection)	Override[1]	AI[2, 3]
0	0	0	Soft power-down (seek mode)
0	1	0	1
1	0	0	0
1	1	0	Bit 6 in Register 0x12
X	X	1	Bit 6 in Register 0x12

[1] The override bit is Bit 7 in Register 0x12.
[2] AI = 0 means analog interface.
[3] AI = 1 means digital interface.

0x11 2 Active Hsync (AHS)

This bit determines which Hsync to use for the analog interface, the HSYNC input or the sync-on-green. It uses Bit 7 and Bit 6 in this register for inputs when determining which should be active. Similar to the previous bit, if both Hsync and sync-on-green are detected, the user can determine which has priority via Bit 4 in Register 0x12. The user can override this function via Bit 5 in Register 0x12. If the override bit is set to Logic 1, this bit is forced to the set state of Bit 4 in Register 0x12.

Table 35. Active Hsync Results

Bit 7 (HSYNC Detect)	Bit 6 (SOG Detect)	Override[1]	AHS[2, 3]
0	0	0	Bit 4 in Register 0x12
0	1	0	1
1	0	0	0
1	1	0	Bit 4 in Register 0x12
X	X	1	Bit 4 in Register 0x12

[1] The override bit is Bit 5 in Register 0x12.
[2] AHS = 0 means HSYNC input.
[3] AHS = 1 means SOG input.

0x11 1 Active VSYNC (AVS)

This bit determines which VSYNC to use for the analog interface, the VSYNC input or the sync separator output. If both VSYNC and composite SOG are detected, VSYNC is selected. The user can override this function via Bit 3 in Register 0x12. If the override bit is set to Logic 1, this bit is forced to the set state of Bit 2 in Register 0x12.

Table 36. Active VSYNC Results

Bit 5 (VSYNC Detect)	Override[1]	AVS[2, 3]
0	0	0
1	0	1
X	1	Bit 2 in Register 0x12

[1] The override bit is Bit 3 in Register 0x12.
[2] AVS = 0 means VSYNC input.
[3] AVS = 1 means sync separator.

0x12 7 Active Interface Override (AIO)

Set this bit (Bit 3 in Register 0x11) to Logic 1 to override the automatic interface selection. When overriding the automatic interface selection, the active interface is set via Bit 6 in this register.

Table 37. Active Interface Override Settings

AIO	Result
0	Autodetermines the active interface
1	Override, Bit 6 determines the active interface

The default for this register is 0.

12 6 Active Interface Select (AIS)

This bit is used under two conditions. It is used to select the active interface when the override bit (Bit 7) is set. Alternately, it is used to determine the active interface when the override bit is not set, but both interfaces are detected.

Table 38. Active Interface Select Settings

AIS	Result
0	Analog interface
1	Digital interface

The default for this register is 0.

0x12 5 Active HSYNC Override

This bit is used to override the automatic HSYNC selection (Bit 2 in Register 0x11). To initiate, set this bit to Logic 1. When overriding the automatic HSYNC selection, the active HSYNC is set via Bit 4 in this register.

Table 39. Active HSYNC Override Settings

Override	Result
0	Autodetermines the active interface
1	Override, Bit 4 determines the active interface

The default for this register is 0.

0x12 4 Active Hsync Select

This bit is used under two conditions. It is used to select the active Hsync when the override bit (Bit 5) is set. Alternately, it is used to determine the active Hsync when the override bit is not set, but both Hsyncs are detected.

Table 40. Active Hsync Select Settings

Select	Result
0	HSYNC input
1	Sync-on-green input

The default for this register is 0.

0x12 3 Active Vsync Override

This bit is used to override the automatic Vsync selection (Bit 1 in Register 0x11). To initiate this, set this bit to Logic 1. When overriding the automatic Vsync selection, the active interface is set via Bit 2 in this register.

Table 41. Active VSYNC Override Settings

Override	Result
0	Autodetermines the active Vsync
1	Override, Bit 2 determines the active Vsync

The default for this register is 0.

0x12 2 Active Vsync Select

This bit is used to select the active Vsync when the override bit (Bit 3) is set.

Table 42. Active VSYNC Select Settings

Select	Result
0	VSYNC input
1	Sync separator output

The default for this register is 0.

0x12 1 Coast Select

This bit is used to select which coast source is active, the COAST input pin or Vsync. If Vsync is selected, users must decide whether to use the VSYNC input pin or the output from the sync separator (Bit 3 and Bit 2).

Table 43. Coast Select Settings

Select	Result
0	COAST input pin
1	Vsync (see above text)

0x12 0 $\overline{\text{PWRDN}}$

This bit can be used to fully power down both interfaces of the chip. See the Power Management section for details on which blocks are actually powered down. Note that the chip is unable to detect incoming activity while fully powered down.

Table 44. Power-Down Settings

Select	Result
0	Power down
1	Normal operation

The default for this register is 1.

Digital Control

0x13 7:0 Sync Separator Threshold

This register is used to set the responsiveness of the sync separator. It sets the number of 5 MHz clock pulses the sync separator counts before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to a number greater than the maximum Hsync pulse width.

The default for this register is 32.

Control Bits

0x14 2 Scan Enable

This register is used to enable the scan function. When this function is enabled, data can be loaded into the AD9887A outputs serially. The scan function utilizes three pins: $SCAN_{IN}$, $SCAN_{OUT}$, and $SCAN_{CLK}$. These pins are described in the Scan Function section.

Table 45. Scan Enable Settings

Scan Enable	Result
0	Scan function disabled
1	Scan function enabled

The default for scan enable is 0 (disabled).

0x14 1 COAST Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL.

Table 46. COAST Input Polarity Override Settings

Override Bit	Result
0	Coast polarity determined by chip
1	Coast polarity determined by user

The default for coast polarity override is 0.

0x14 0 HSYNC Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table 47. HSYNC Input Polarity Override Setting

Override Bit	Result
0	HSYNC input polarity determined by chip
1	HSYNC input polarity determined by user

The default for HSYNC input polarity override is 0.

0x15 7 HSYNC Input Polarity Status

This bit reports the status of the HSYNC input polarity detection circuit. It can be used to determine the polarity of the HSYNC input. The location of the detection circuit is shown in the Figure 43.

Table 48. Detected HSYNC Input Polarity Status

Status	Result
0	HSYNC input polarity is negative.
1	HSYNC input polarity is positive.

0x15 6 VSYNC Output Polarity Status

This bit reports the status of the VSYNC output polarity detection circuit. It can be used to determine the polarity of the VSYNC input. The location of the detection circuit is shown in the Figure 43.

Table 49. Detected Vsync Input Polarity Status

Status	Result
0	Vsync input polarity is active low.
1	Vsync input polarity is active high.

0x15 5 COAST Input Polarity Status

This bit reports the status of the COAST input polarity detection circuit. It can be used to determine the polarity of the coast input. The location of the detection circuit is shown in the Figure 43.

Table 50. Detected COAST Input Polarity Status

Status	Result
0	Coast input polarity is negative.
1	Coast input polarity is positive.

0x16 7–3 Sync-on-Green Slicer Threshold

This register allows the comparator threshold of the sync-on-green slicer to be adjusted. This register adjusts the comparator threshold in 10 mV steps. A setting of 0 results in a 330 mV threshold; a setting of 31 results in a 10 mV threshold. The default setting is 23, which corresponds to a threshold value of 70 mV.

0x17 7:0 Precoast

This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. This register defines the number of edges that are filtered before Vsync on a composite sync.

The default is 0.

0x18 7:0 Postcoast

This register allows the coast signal to be applied following the Vsync signal. This is necessary when postequalization pulses are present. This register defines the number of edges that are filtered after Vsync on a composite sync.

The default is 0.

0x19 7:0 Test

Must be set to default.

0x1A 7:0 Test

Must be set to 0x41 for proper operation.

0x1B 7:0 Test

Must be set to 0x00 for autogain mode and 0x10 for manual-gain mode.

0x1C 7:3 Test

Must be set to 00000*** for autogain mode and 00101*** for manual-gain mode.

0x1C 2 CbCr Output Order

In 4:2:2 mode, the red and blue channels can be interchanged to help satisfy board layout or timing requirements, but the green channel must be configured for Y. Register 0x1C, Bit 2, controls the order that the U/V (CbCr) data is output. If this bit is high, the red channel data precedes the blue channel data. If this bit is low, the blue channel data precedes the red channel data. See the example in Table 51.

Table 51. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	Y	V/U if 0x1C Bit 2 = 1; U/V if 0x1C Bit 2 = 0
Green	Y	Y
Blue	U	High impedance

0x1C 1 Test Bits

Must be set to 0 for standard input sampling.

0x1C 0 4:2:2 Output Mode Select

4:2:2 mode can be used to reduce the number of data lines used from 24 to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. See Figure 27 for a timing diagram for this mode.

Table 52. 4:2:2 Output Mode Select

Select	Output Mode
1	4:4:4
0	4:2:2

0x1D 6 HDCP Keys Detected

This bit indicates the presence of HDCP keys read from the external EEPROM.

Table 53. HDCP Key Status

Select	HDCP Key Status
1	HDCP keys present
0	HDCP keys not present

0x1E 7:0 Test Register

Must be set to 0xFF for proper operation.

0x1F 7:0 Test Register

Must be set to 0x84 for proper operation.

0x20 7 HDCP A0 Serial Address Bit

This bit sets the value of the A0 bit for the DDC serial port.

Table 54. HDCP A0 Serial Address

Select	Serial Address
1	A0 bit = 1, address = 0x76
0	A0 bit = 0, address = 0x74

The default setting is 0.

0x20 6 MDA Pin Select

This bit sets the function of Pin 49 to MDA when set at 1.

Table 55. MDA Pin Select

Select	Output Mode
1	Pin 49 = MDA for HDCP
0	Pin 49 = CTL3 signal

The default setting is 0.

0x20 5 Analog Input Bandwidth Control

This bit controls the analog input bandwidth.

Table 56. Analog Input Bandwidth Control

Select	Input Bandwidth
0	High analog input bandwidth
1	Low analog input bandwidth

The default setting 0.

0x20 4 MDA/MCL Three-State

This bit allows the MDA/MCL lines to be three-stated so that the HDCP key EEPROM can be programmed in-circuit.

Table 57. MDA/MCL Three-State

Select	MDA/MCL Output
1	Normal operation
0	MDA/MCL set to three-state

The default setting is 0.

0x20 3 External Oscillator

This bit allows use of either the internal oscillator or an external one supplied on the A0 pin.

Table 58. External Oscillator Select

Select	Oscillator
1	Use internal oscillator
0	Use external oscillator on A0 pin

The default setting is 0.

0x20 2 View HDCP Mask

This bit allows the HDCP mask to be output on the RGB channels.

Table 59. View HDCP Mask

Select	Output Mode
1	HDCP mask output to RGB channel
0	Normal operation

0x21 7:0 Test Register

Set to 0x00 for autogain mode and 0x64 for manual-gain mode.

0x22 7:0 Test Register

Must be set to 0x00 for proper operation.

0x23 7:0 Test Register

Must be set to 0x2A for proper operation.

0x24 7:0 Test Register

Must be set to 0x00 for proper operation.

0x25 7:0 Test Register

Must be set to 0xF0 for proper operation.

0x26 7:0 Test Register

Must be set to 0xFF for proper operation.

0x27 7:0 Test Register

Must be set to 0x0F for proper operation.

2-Wire Serial Control Port

A 2-wire serial interface control port is provided. Up to four AD9887A devices can be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communication is initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer, reading from (1) or writing to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the A1 and A0 input pins listed in Table 60), the AD9887A acknowledges it by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9887A does not acknowledge it.

Table 60. Serial Port Addresses

Bit 7 A_6 (MSB)	Bit 6 A_5	Bit 5 A_4	Bit 4 A_3	Bit 3 A_2	Bit 2 A_1	Bit 1 A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1
1	0	0	1	1	1	0
1	0	0	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9887A does not acknowledge the master device during a write sequence, the SDA remains high so that the master can generate a stop signal. If the master device does not acknowledge the AD9887A during a read sequence, the AD9887A interprets this as the end of the data. The SDA remains high so that the master can generate a stop signal.

Writing data to a specific control register of the AD9887A requires writing to its 8-bit address after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address is established. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value of 0x1D. Any base address higher than 0x1D does not produce an acknowledge signal.

Data is read from the control registers of the AD9887A in a similar manner. Reading requires two data transfer operations.

The base address must be written with the R/$\overline{W}$ bit of the slave address byte low to set up a sequential read operation.

Reading begins at the previously established base address with the R/$\overline{W}$ bit of the slave address byte high. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9887A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high. The timing for the read/write operations is shown in Figure 41; a typical byte transfer is shown in Figure 42.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

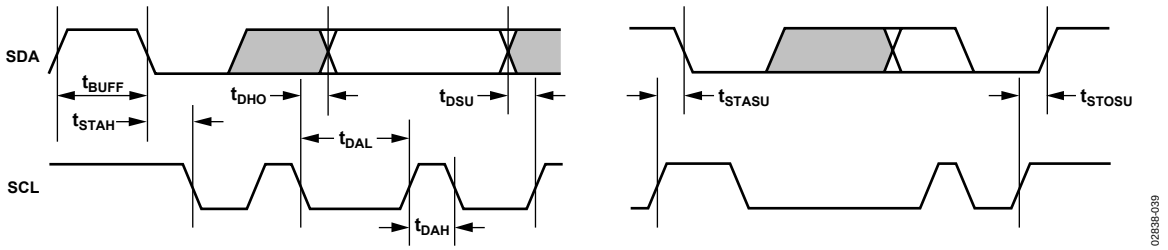

Figure 41. Serial Port R/$\overline{W}$ Timing

Figure 42. Serial Interface—Typical Byte Transfer

Serial Interface Read/Write Examples

Write to one of the following control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Data byte to base address
- Stop signal

Write to four of the following consecutive control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one of the following control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = high)
- Data byte from base address
- Stop signal

Read from four of the following consecutive control registers:

- Start signal
- Slave address byte (R/$\overline{W}$ bit = low)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

Table 61. Control of Sync Block Muxes via the Serial Register

Mux No.	Serial Bus, Control Bit	Control Bit State	Result
1 and 2	0x12, Bit 4	0	Pass Hsync
		1	Pass sync-on-green
3	0x12, Bit 1	0	Pass coast
		1	Pass Vsync
4	0x12, Bit 2	0	Pass Vsync
		1	Pass sync separator signals
5, 6, and 7	0x11, Bit 3	0	Pass digital interface signals
		1	Pass analog interface signals

THEORY OF OPERATION—SYNC PROCESSING

SYNC STRIPPER

The purpose of the sync stripper is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics systems, only those with sync-on-green. The sync signal is extracted from the green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a trigger level that is 0.15 V above the clamped level. The output signal is typically a composite sync signal containing both Hsync and Vsync.

SYNC SEPARATOR

A sync separator extracts the Vsync signal from a composite sync signal by using a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active much longer than the Hsync signal. Therefore, it rejects any signal shorter than a threshold value, which is somewhere in the range between an Hsync pulse width and a Vsync pulse width.

The sync separator on the AD9887A is simply an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.)

The basic idea is that the counter counts up when Hsync pulses are present. Since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down, eventually reaching 0 before the next Hsync pulse arrives. The specific value of N varies among video modes, but is always less than 255. For example, with a 1 µs width Hsync, the counter only reaches 5 (1 µs/200 ns = 5). When Vsync is present on the composite sync, the counter also counts up. Because the Vsync signal is much longer, it counts to a higher number M. For most video modes, M is at least 255. Therefore, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection, the threshold count (T), can be programmed through the serial Register 0x0F. Once Vsync is detected, there is a similar process to detect when it becomes inactive. Upon detection, the counter first resets to 0, then counts up when Vsync disappears. Similar to the previous case, it detects the absence of Vsync when the counter reaches T. In this way, it rejects noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

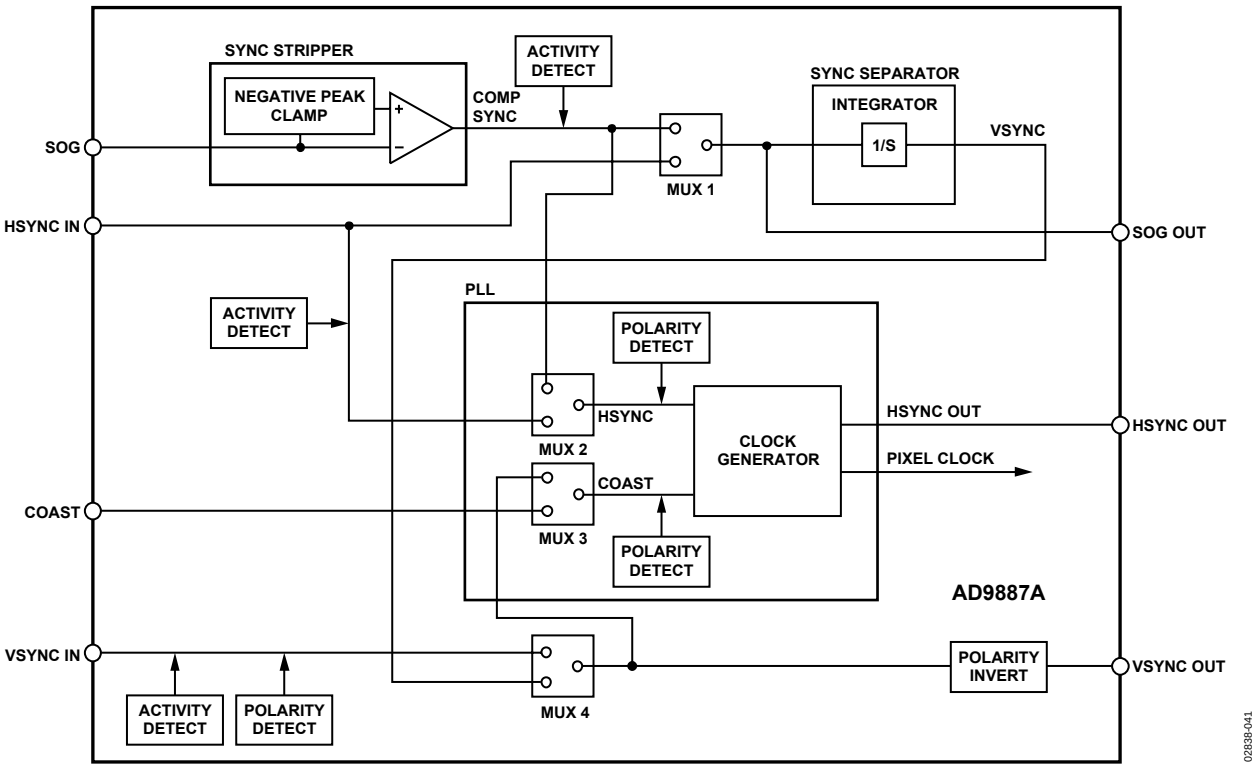

Figure 43. Sync Processing Block Diagram

PCB LAYOUT RECOMMENDATIONS

The AD9887A is a high performance, high speed analog device. To optimize its performance, it is important to have a well laid out board. The following is a guide for designing a board using the AD9887A.

ANALOG INTERFACE INPUTS

Using the following layout techniques on the graphics inputs is extremely important.

- Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9887A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up noise from the board and other external sources.
- Place the 75 Ω termination resistors as close to the AD9887A chip as possible. Any additional trace length between the termination resistors and the input of the AD9887A increases the magnitude of reflections, which corrupts the graphics signal.
- Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω also increase the chance of reflections.

The AD9887A has very high input bandwidth (330 MHz). Although this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it also captures any high frequency noise present. Therefore, it is important to reduce the amount of noise coupled to the inputs. Avoid running any digital traces near the analog inputs. Due to the high bandwidth of the AD9887A, sometimes low-pass filtering the analog inputs can help reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead in front of the 75 Ω termination resistor can filter out excess noise. Specifically, the part used was the #2508051217Z0 from Fair-Rite, but each application might work best with a different bead value. Alternatively, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also be beneficial.

DIGITAL INTERFACE INPUTS

Each differential input pair (Rx0+, Rx0−, RxC+, RxC−, and so on) should be routed together using 50 Ω strip line routing techniques kept as short as possible. No other components should be placed on these inputs (for example, no clamping diodes). Every effort should be made to route these signals on a single layer (component layer) with no vias.

POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1 µF capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor.

The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the side of the PC board opposite from the AD9887A, because this interposes resistive vias in the path.

The bypass capacitors should physically be located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphics controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner power source (for example, from a 12 V supply).

It is recommended to use a single ground plane for the entire board. Experience shows that noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller and can result in long ground loops.

In some cases, using separate ground planes is unavoidable. For these cases, it is recommended to place at least a single ground plane under the AD9887A. The location of the split should be at the receiver of the digital outputs. For these cases, it is even more important to place components wisely because the current loops are much longer, and current takes the path of least resistance. An example of a current loop follows.

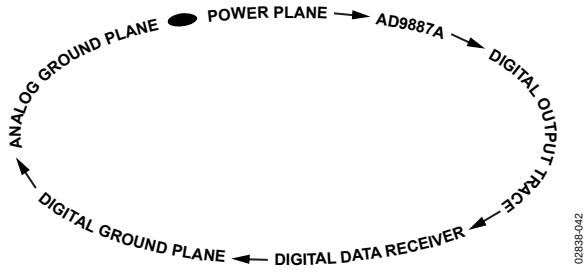

Figure 44. Example of a Current Loop

PLL

Place the PLL loop filter components as close as possible to the FILT pin. Do not place any digital or other high frequency traces near these components. Use the values suggested in the Specifications section with 10% tolerances or less.

OUTPUTS—BOTH DATA AND CLOCKS

Try to minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor with a value of 22 Ω to 100 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9887A. However, if 50 Ω traces are used on the PCB, the data outputs should not need these resistors. A 22 Ω resistor on the DATACK output should provide good impedance matching that further reduces reflections. If EMI or current spiking is a concern, it is recommended to use a lower drive strength setting. If series resistors are used, place them as close as possible to the AD9887A pins, but try not to add vias or extra length to the output trace.

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can be accomplished easily by keeping traces short and connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the AD9887A, creating digital noise on the power supplies.

DIGITAL INPUTS

The digital inputs on the AD9887A are designed to work with 3.3 V signals.

Any noise in the HSYNC input trace produces jitter in the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

VOLTAGE REFERENCE

The voltage reference should be bypassed with a 0.1 µF capacitor. Place it as close as possible to the AD9887A pin. Make the ground connection as short as possible.

REFOUT is easily connected to REFIN with a short trace. Avoid making this trace longer than necessary.

When using an external reference, the REFOUT output, although unused, still needs to be bypassed with a 0.1 µF capacitor to avoid ringing.

OUTLINE DIMENSIONS

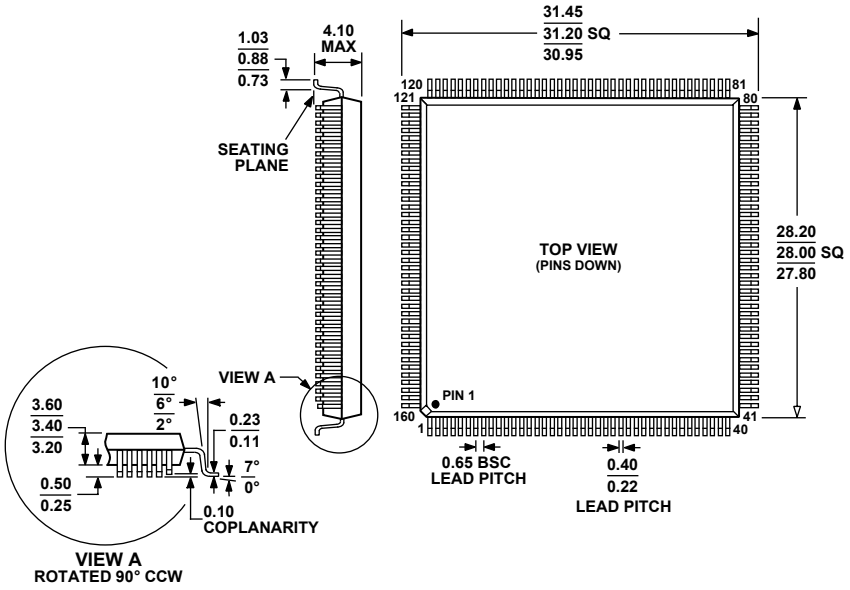

Figure 45. 160-Lead Metric Quad Flat Package [MQFP]
(S-160)
Dimension shown in millimeters

ORDERING GUIDE

Model	Max Speed (MHz) Analog	DVI	Temperature Range	Package Description	Package Option
AD9887AKS-100	100	100	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887AKSZ-100[1]	100	100	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887AKS-140	140	140	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887AKSZ-140[1]	140	140	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887AKS-170	170	170	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887AKSZ-170[1]	170	170	0°C to 70°C	160-Lead Metric Quad Flatpack	S-160
AD9887A/PCB				Evaluation Kit	

[1] Z = RoHS Compliant Part.

NOTES

C02838-0-3/07(B)