AD826–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	10	20		MHz
		±15 V	25	55		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = –1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
	0 V–10 V Step, A_V = –1	±15 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		70		ns
	0 V–10 V Step, A_V = –1	±15 V		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		–78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
Differential Gain Error	NTSC	±15 V		0.07	0.1	%
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	%
		0, +5 V		0.15		%
Differential Phase Error	NTSC	±15 V		0.11	0.15	Degrees
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	Degrees
		0, +5 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V to ±15 V		0.5	2	mV
	T_{MIN} to T_{MAX}				3	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
Input Offset Current		±5 V, ±15 V		25	300	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open-Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		3.5	6		V/mV
	T_{MIN} to T_{MAX}		2	5		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		2	4		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}	±5 V	80	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
	T_{MIN} to T_{MAX}	±15 V	80	100		dB

Parameter	Conditions	V_S	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	f = 5 MHz	±15 V		–80		dB
Gain Flatness Match	G = +1, f = 40 MHz	±15 V		0.2		dB
Slew Rate Match	G = –1	±15 V		10		V/µs
DC						
Input Offset Voltage Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.5	2	mV
Input Bias Current Match	T_{MIN}–T_{MAX}	±5 V to ±15 V		0.06	0.8	µA
Open-Loop Gain Match	V_O = ±10 V, R_{LOAD} = 1 kΩ, T_{MIN}–T_{MAX}	±15 V	0.15	0.01		mV/V
Common-Mode Rejection Ratio Match	V_{CM} = ±12 V, T_{MIN}–T_{MAX}	±15 V	80	100		dB
Power Supply Rejection Ratio Match	±5 V to ±15 V, T_{MIN}–T_{MAX}		80	100		dB
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current/Amplifier		±5 V		6.6	7.5	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
		±15 V			7.5	mA
	T_{MIN} to T_{MAX}	±15 V		6.8	7.5	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		75	86		dB

NOTES
[1]Full power bandwidth = slew rate/2 π V_{PEAK}.
Specifications subject to change without notice.

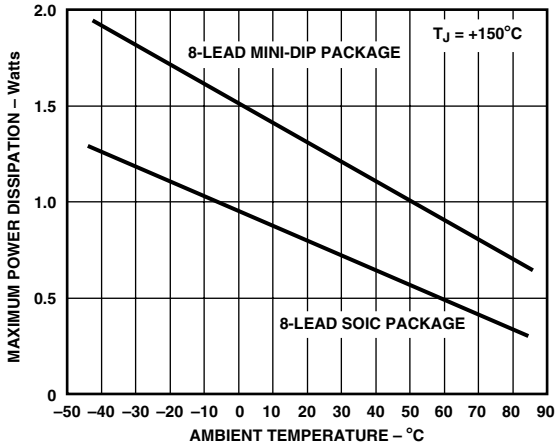
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . See Derating Curves
Small Outline (R) . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . ±V_S
Differential Input Voltage . . . . . ±6 V
Output Short Circuit Duration . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability .
[2]Specification is for device in free air: 8-lead plastic package, θ_{JA} = 100°C/watt; 8-lead SOIC package, θ_{JA} = 155°C/watt.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD826 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.



Maximum Power Dissipation vs. Temperature for Different Package Types

AD826 – Typical Characteristics

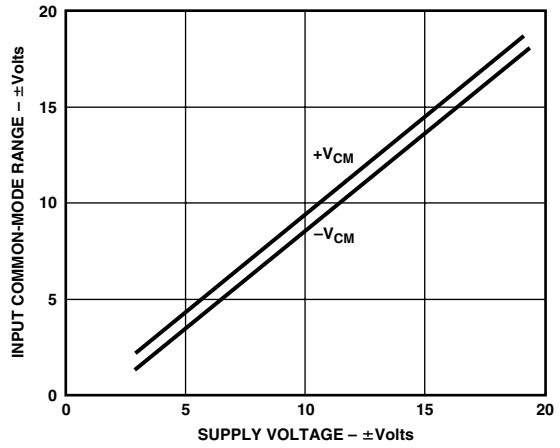


Figure 1. Common-Mode Voltage Range vs. Supply

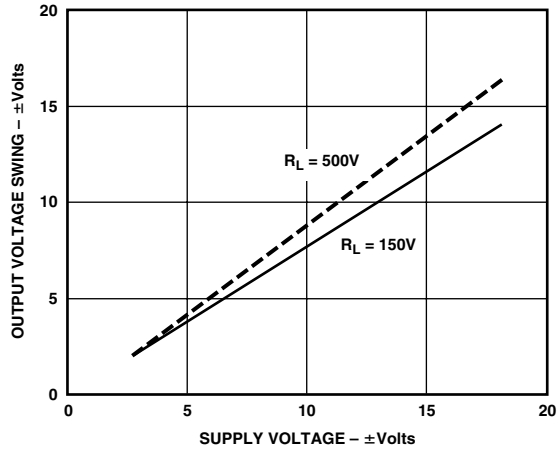


Figure 2. Output Voltage Swing vs. Supply

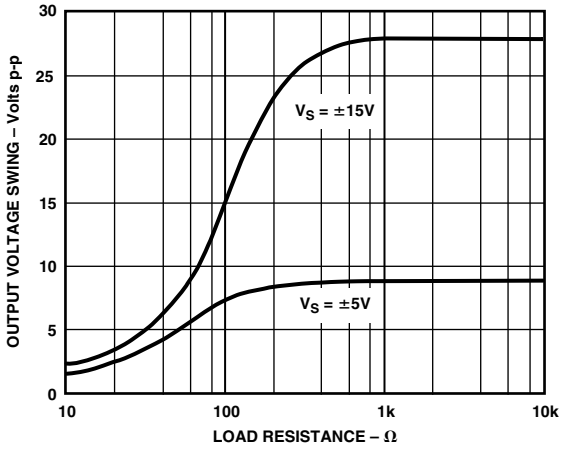


Figure 3. Output Voltage Swing vs. Load Resistance

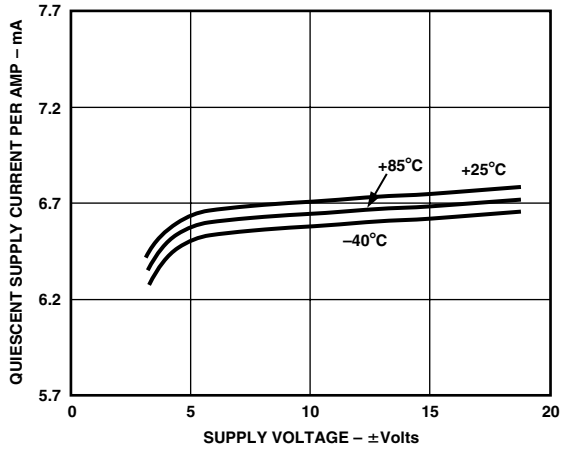


Figure 4. Quiescent Supply Current per Amp vs. Supply Voltage for Various Temperatures

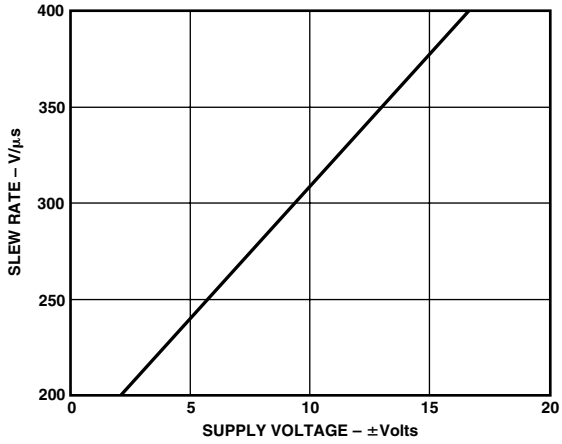


Figure 5. Slew Rate vs. Supply Voltage

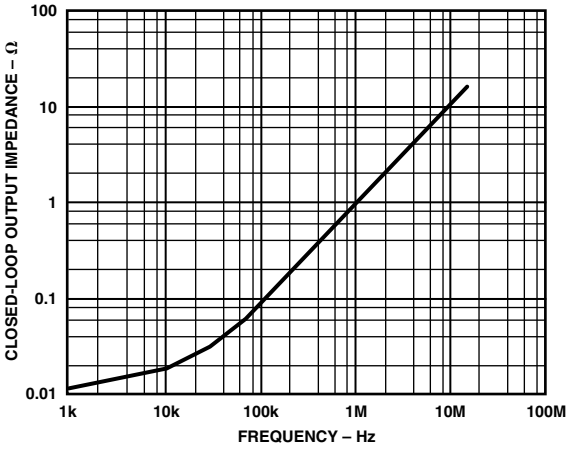


Figure 6. Closed-Loop Output Impedance vs. Frequency

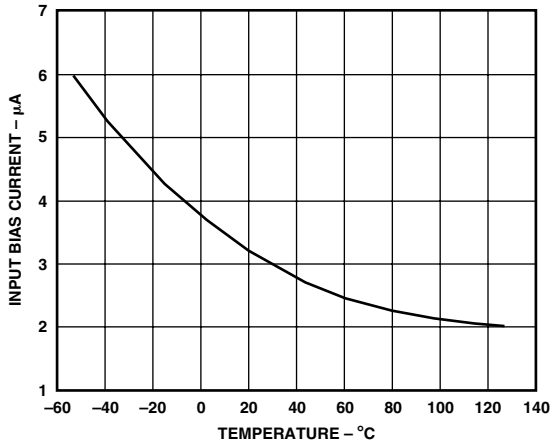


Figure 7. Input Bias Current vs. Temperature

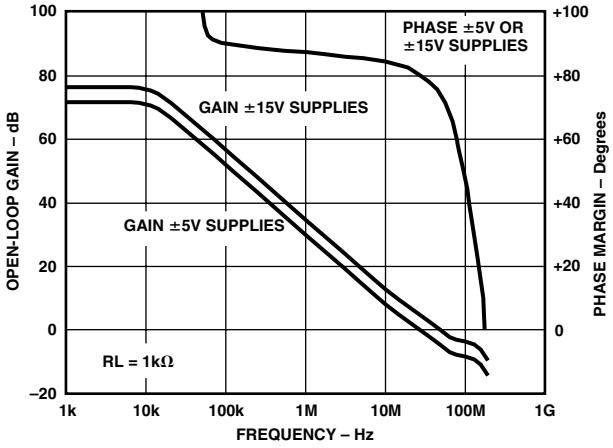


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

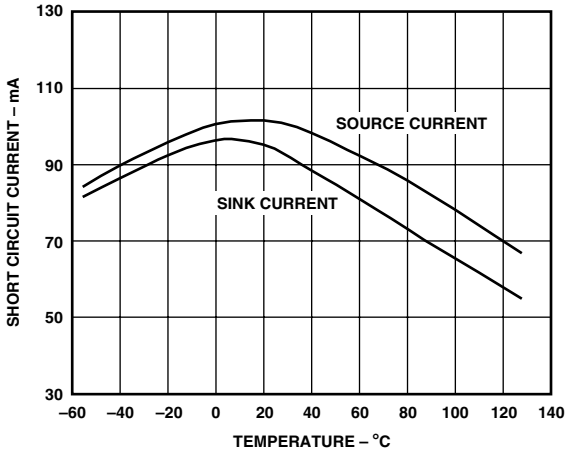


Figure 8. Short Circuit Current vs. Temperature

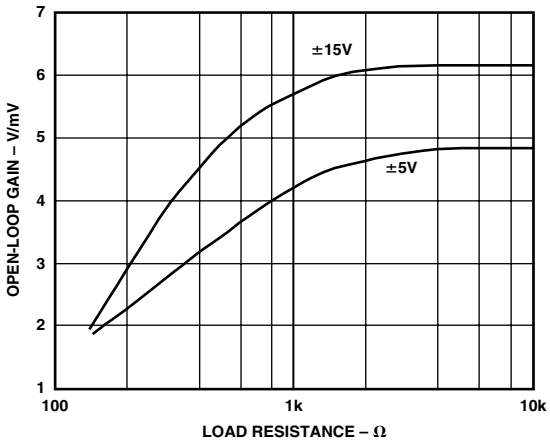


Figure 11. Open-Loop Gain vs. Load Resistance

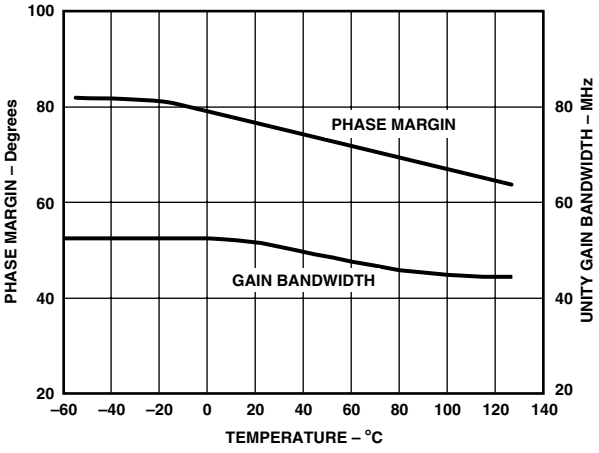


Figure 9. Unity Gain Bandwidth and Phase Margin vs. Temperature

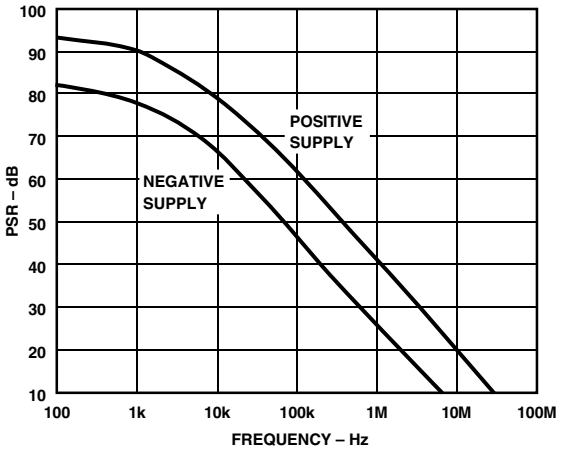


Figure 12. Power Supply Rejection vs. Frequency

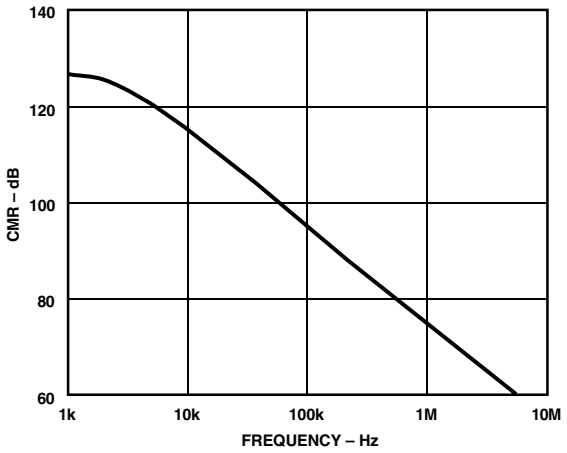


Figure 13. Common-Mode Rejection vs. Frequency

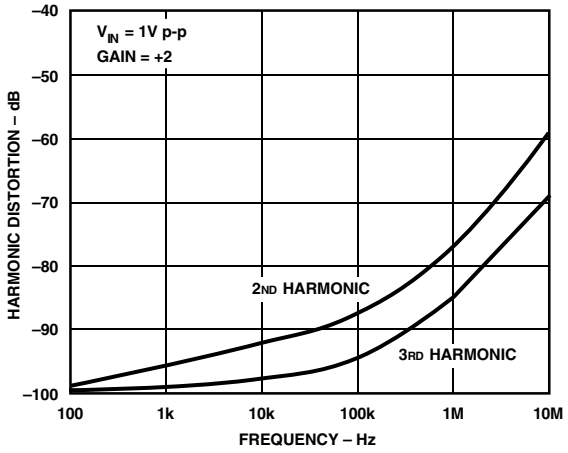


Figure 16. Harmonic Distortion vs. Frequency

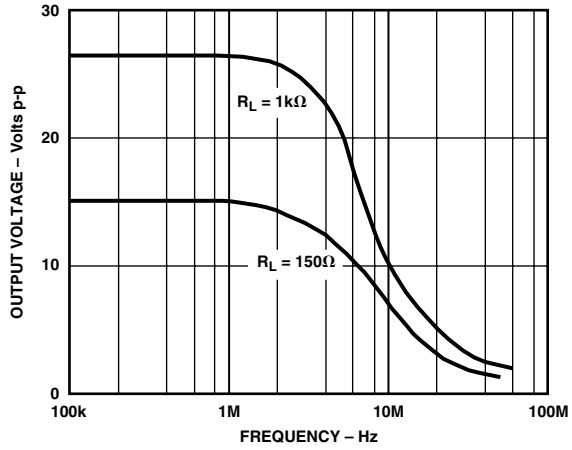


Figure 14. Large Signal Frequency Response

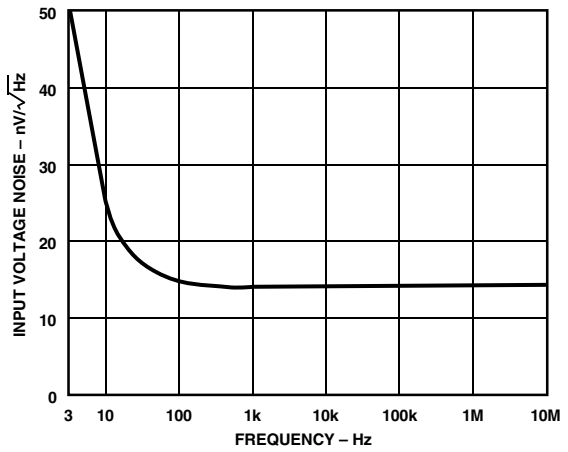


Figure 17. Input Voltage Noise Spectral Density

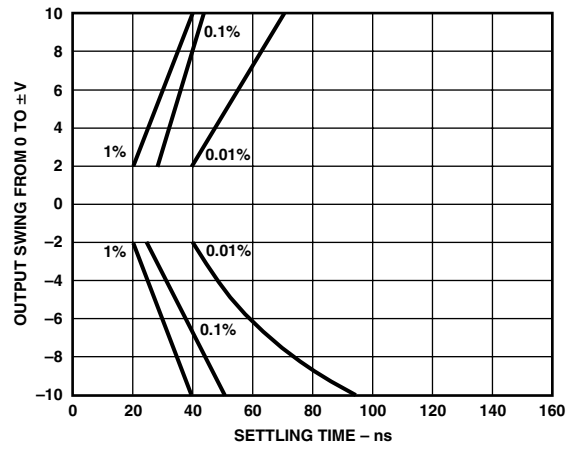


Figure 15. Output Swing and Error vs. Settling Time

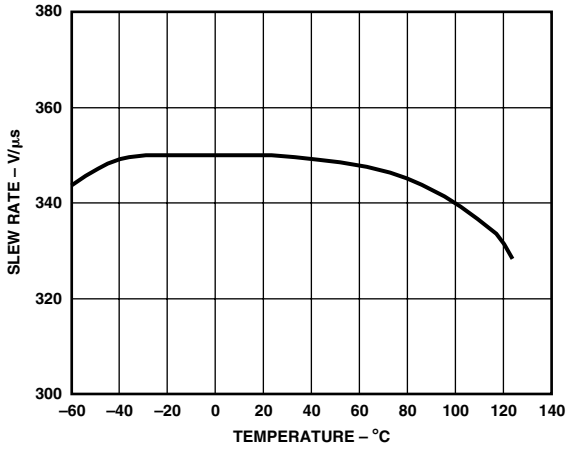


Figure 18. Slew Rate vs. Temperature

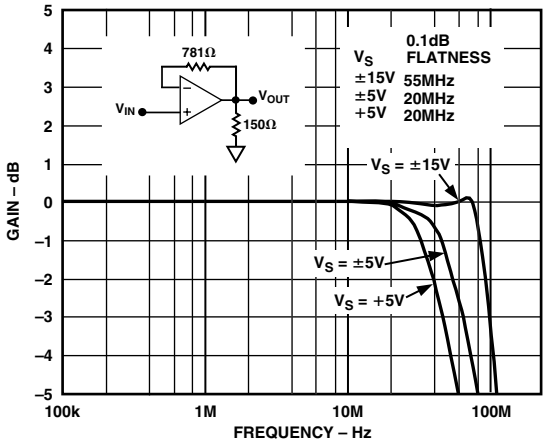


Figure 19. Closed-Loop Gain vs. Frequency

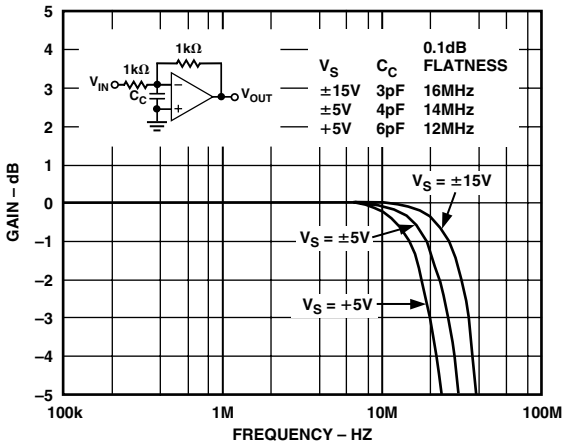


Figure 22. Closed-Loop Gain vs. Frequency, Gain = –1

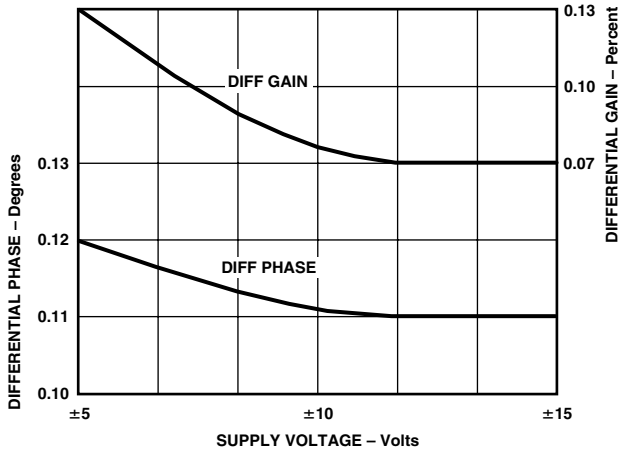


Figure 20. Differential Gain and Phase vs. Supply Voltage

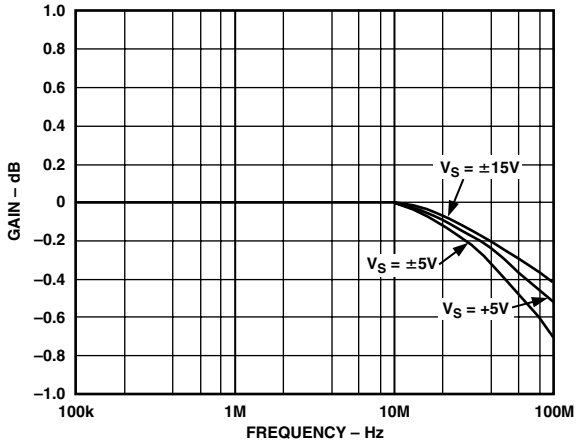


Figure 23. Gain Flatness Matching vs. Supply, G = +1

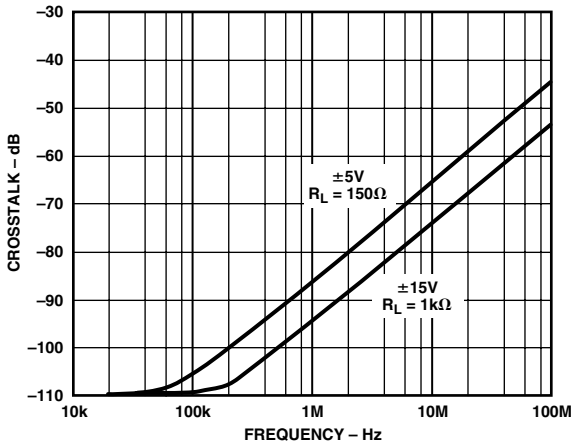


Figure 21. Crosstalk vs. Frequency

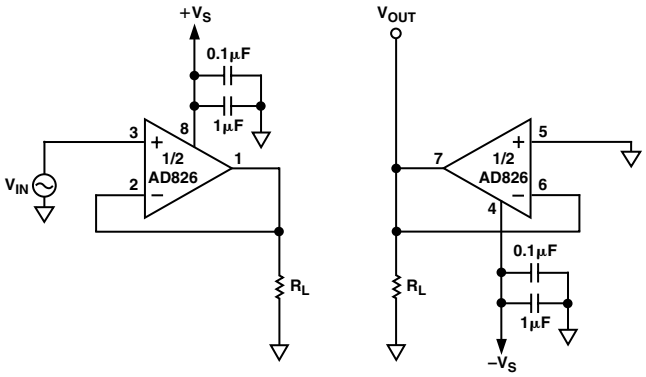


Figure 24. Crosstalk Test Circuit

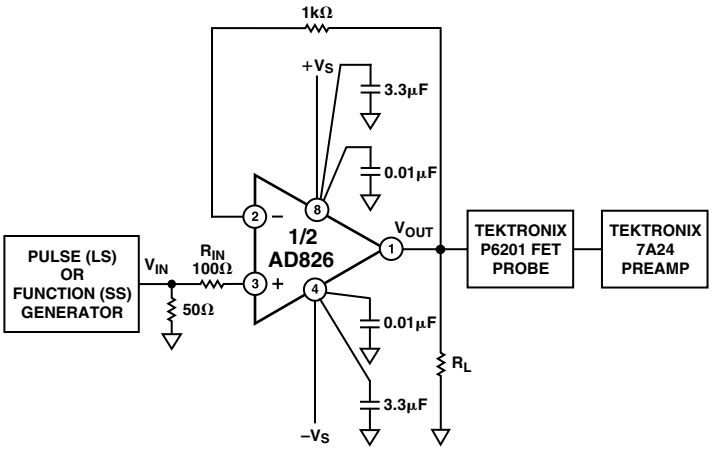


Figure 25. Noninverting Amplifier Configuration

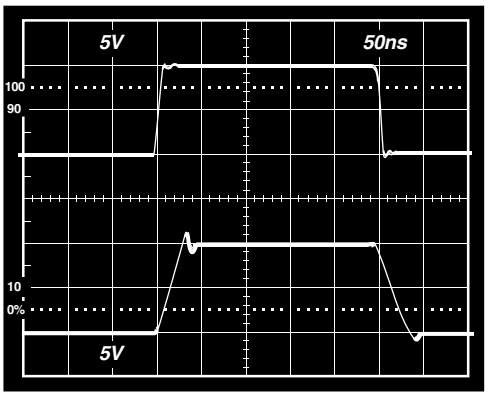


Figure 26. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

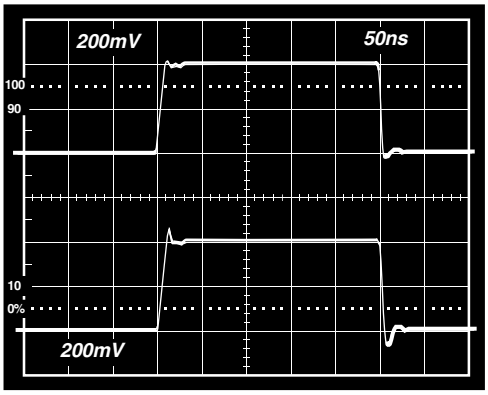


Figure 28. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

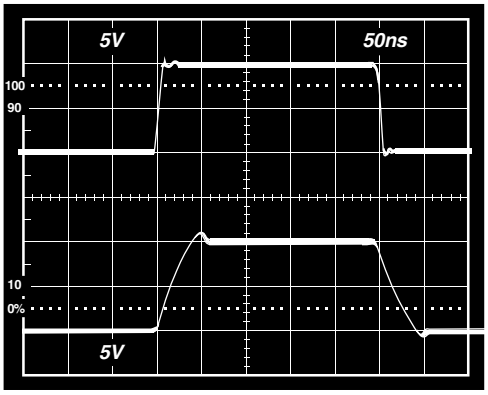


Figure 27. Noninverting Large Signal Pulse Response, R_L = 150 Ω

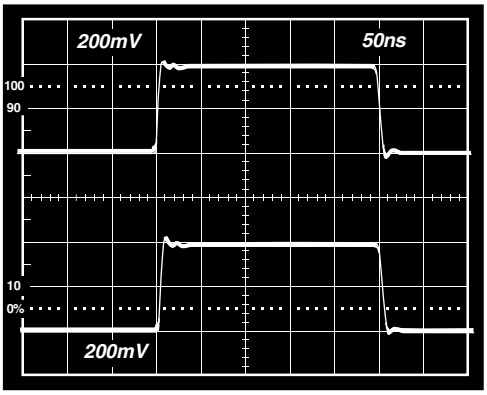


Figure 29. Noninverting Small Signal Pulse Response, R_L = 150 Ω

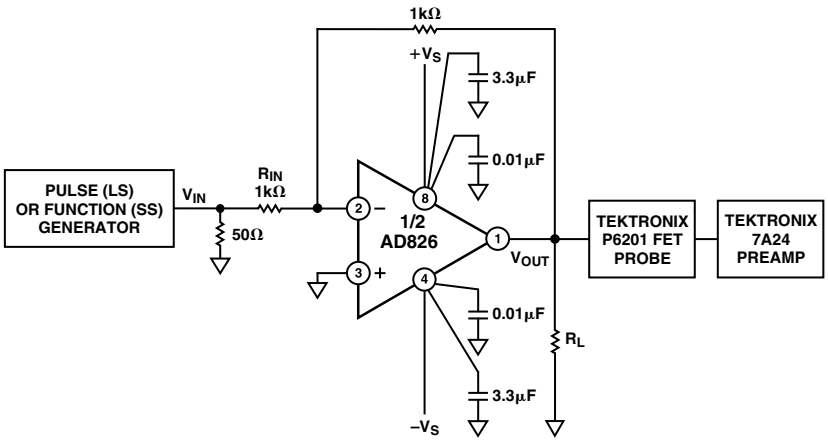


Figure 30. Inverting Amplifier Configuration

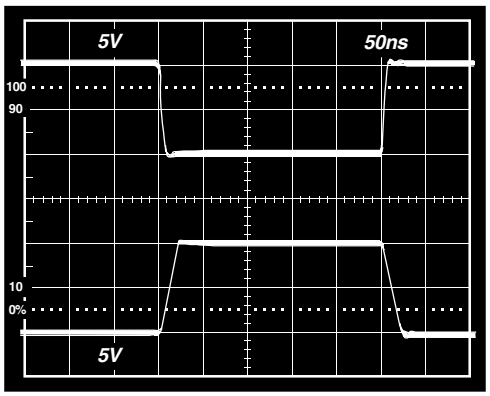


Figure 31. Inverting Large Signal Pulse Response, R_L = 1 kΩ

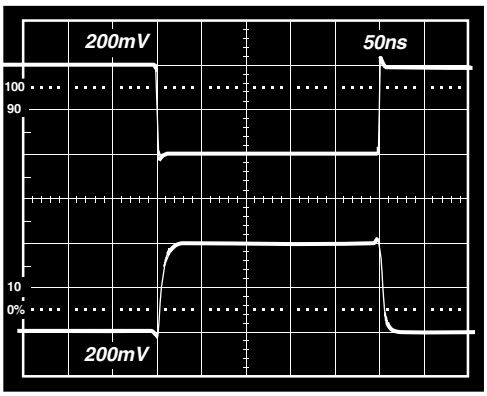


Figure 33. Inverting Small Signal Pulse Response, R_L = 1 kΩ

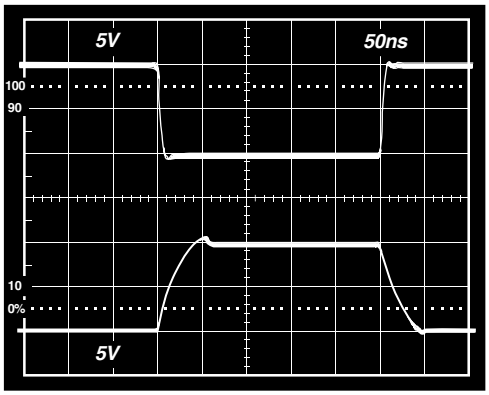


Figure 32. Inverting Large Signal Pulse Response, R_L = 150 Ω

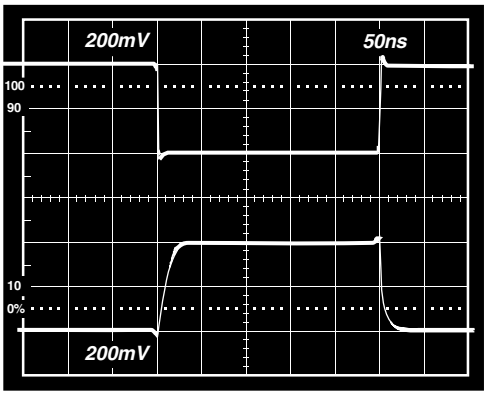


Figure 34. Inverting Small Signal Pulse Response, R_L = 150 Ω

THEORY OF OPERATION

The AD826 is a low cost, wide band, high performance dual operational amplifier which can drive heavy capacitive and resistive loads. It also achieves a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD826 (Figure 35) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

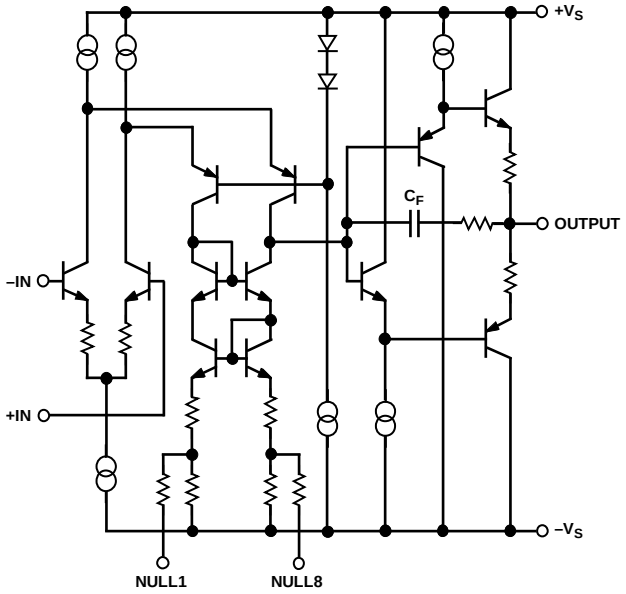


Figure 35. Simplified Schematic

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. With low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining the stability of the amplifier.

INPUT CONSIDERATIONS

An input protection resistor (R_{IN} in Figure 25) is required in circuits where the input to the AD826 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of R_{IN} and R_F and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

APPLYING THE AD826

The AD826 is a breakthrough dual amp that delivers precision and speed at low cost with low power consumption. The AD826 offers excellent static and dynamic matching characteristics, combined with the ability to drive heavy resistive and capacitive loads. As with all high frequency circuits, care should be taken to maintain overall device performance as well as their matching. The following items are presented as general design considerations.

Circuit Board Layout

Input and output runs should be laid out so as to physically isolate them from remaining runs. In addition, the feedback resistor of each amplifier should be placed away from the feedback resistor of the other amplifier, since this greatly reduces inter-amp coupling.

Choosing Feedback and Gain Resistors

In order to prevent the stray capacitance present at each amplifier's summing junction from limiting its performance, the feedback resistors should be ≤1 kΩ. Since the summing junction capacitance may cause peaking, a small capacitor (1 pF–5pF) maybe paralleled with R_F to neutralize this effect. Finally, sockets should be avoided, because of their tendency to increase interlead capacitance.

Power Supply Considerations

To ensure the proper operation of the AD826, connect the positive supply before the negative supply. Also, proper power supply decoupling is critical to preserve the integrity of high frequency signals. In carefully laid out designs, decoupling capacitors should be placed in close proximity to the supply pins, while their lead lengths should be kept to a minimum. These measures greatly reduce undesired inductive effects on the amplifier's response.

Though two 0.1 µF capacitors will typically be effective in decoupling the supplies, several capacitors of different values can be paralleled to cover a wider frequency range.

±SINGLE SUPPLY OPERATION

An exciting feature of the AD826 is its ability to perform well in a single supply configuration (see Figure 37). The AD826 is ideally suited for applications that require low power dissipation and high output current and those which need to drive large capacitive loads, such as high speed buffering and instrumentation.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: (R1 + R3)‖R2 combine with C1 to form a low frequency corner of approximately 30 Hz.

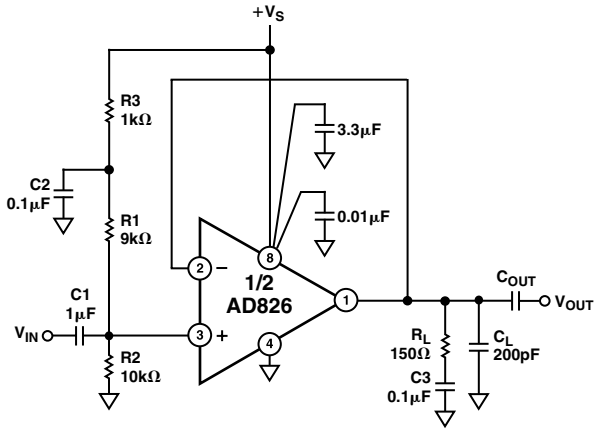


Figure 36. Single Supply Amplifier Configuration

R3 and C2 reduce the effect of the power supply changes on the output by low-pass filtering with a corner at $\frac{1}{2\pi R_3 C_2}$.

The values for R_L and C_L were chosen to demonstrate the AD826's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with R_L.

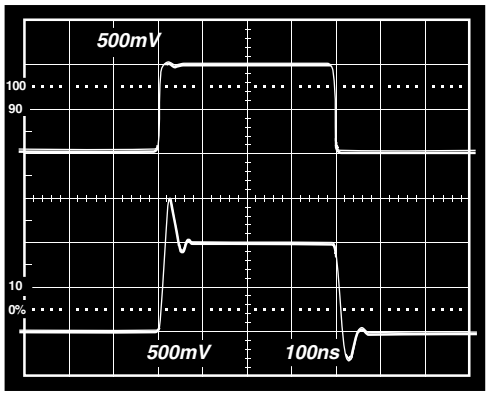


Figure 37. Single Supply Pulse Response, G = +1, R_L = 150 Ω, C_L = 200 pF

PARALLEL AMPS PROVIDE 100 mA TO LOAD

By taking advantage of the superior matching characteristics of the AD826, enhanced performance can easily be achieved by employing the circuit in Figure 38. Here, two identical cells are paralleled to obtain even higher load driving capability than that of a single amplifier (100 mA min guaranteed). R1 and R2 are included to limit current flow between amplifier outputs that would arise in the presence of any residual mismatch.

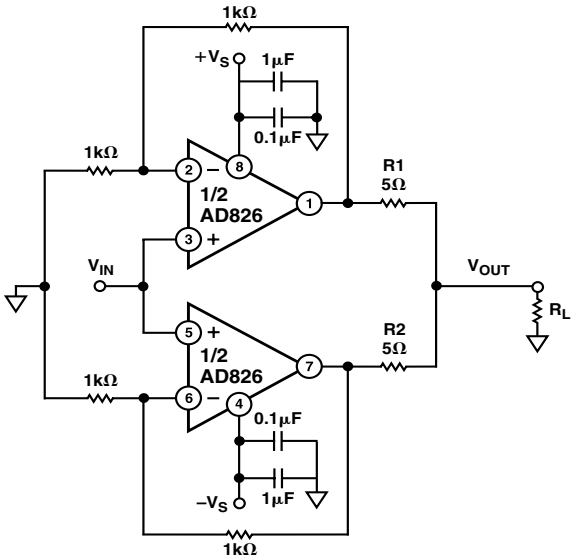


Figure 38. Parallel Amp Configuration

SINGLE-ENDED TO DIFFERENTIAL LINE DRIVER

Outstanding CMRR (> 80 dB @ 5 MHz), high bandwidth, wide supply voltage range, and the ability to drive heavy loads, make the AD826 an ideal choice for many line driving applications. In this application, the AD830 high speed video difference amp serves as the differential line receiver on the end of a back terminated, 50 ft., twisted-pair transmission line (see Figure 40). The overall system is configured in a gain of +1 and has a –3 dB bandwidth of 14 MHz. Figure 39 is the pulse response with a 2 V p-p, 1 MHz signal input.

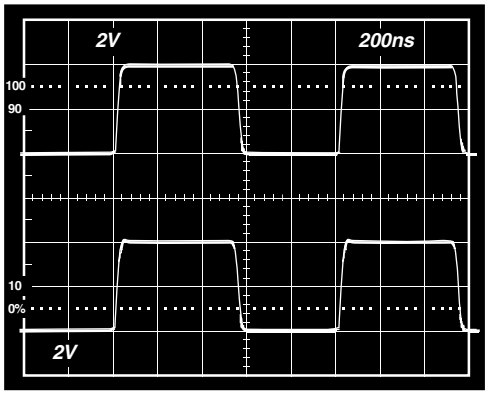


Figure 39. Pulse Response

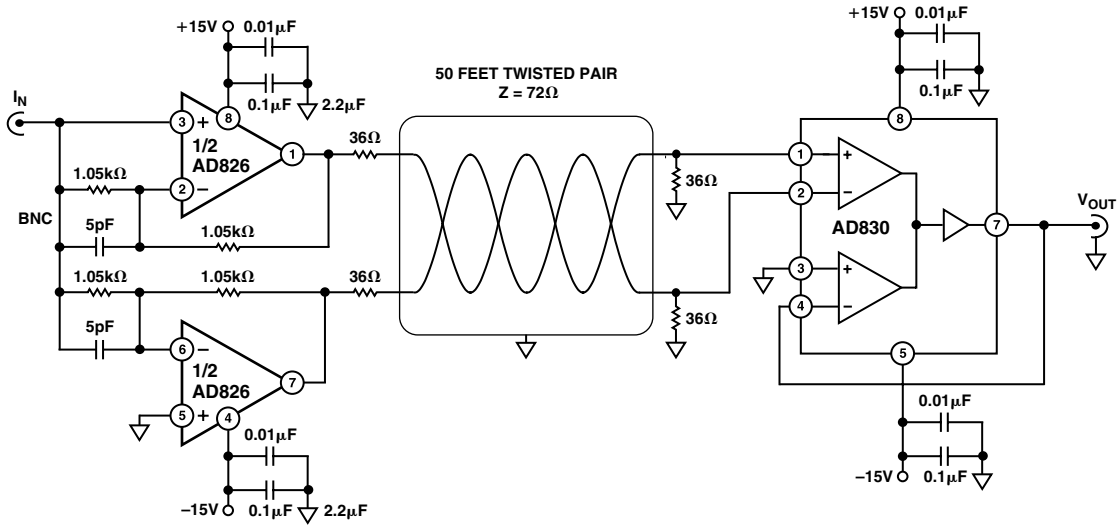


Figure 40. Differential Line Driver

LOW DISTORTION LINE DRIVER

The AD826 can quickly be turned into a powerful, low distortion line driver (see Figure 41). In this arrangement the AD826 can comfortably drive a 75 Ω back-terminated cable, with a 5 MHz, 2 V p-p input; all of this while achieving the harmonic distortion performance outlined in the following table.

Configuration	2nd Harmonic
1. No Load	–78.5 dBm
2. 150 Ω R_L Only	–63.8 dBm
3. 150 Ω R_L 7.5 Ω R_C	–70.4 dBm

In this application one half of the AD826 operates at a gain of 2.1 and supplies the current to the load, while the other provides the overall system gain of 2. This is important for two reasons: the first is to keep the bandwidth of both amplifiers the same, and the second is to preserve the AD826's ability to operate from low supply voltages. R_C varies with the load and must be chosen to satisfy the following equation:

$$R_C = MR_L$$

where M is defined by [(M+ 1) G_S = G_D] and G_D = Driver's Gain, G_S = System Gain.

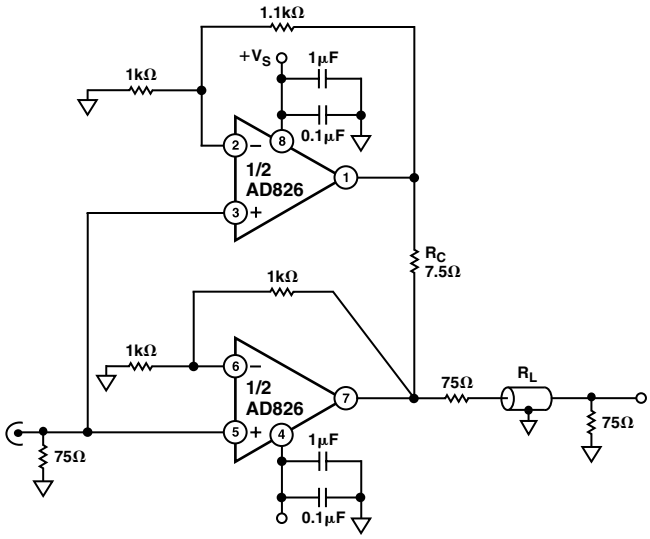


Figure 41. Low Distortion Amplifier

HIGH PERFORMANCE ADC BUFFER

Figure 42 is a schematic of a 12-bit high speed analog-to-digital converter. The AD826 dual op amp takes a single ended input and drives the AD872 A/D converter differentially, thus reducing 2nd harmonic distortion. Figure 43 is a FFT of a 1 MHz input, sampled at 10 MHz with a THD of –78 dB. The AD826 can be used to amplify low level signals so that the entire range of the converter is used. The ability of the AD826 to perform on a ±5 volt supply or even with a single 5 volts combined with its rapid settling time and ability to deliver high current to complicated loads make it a very good flash A/D converter buffer as well as a very useful general purpose building block.

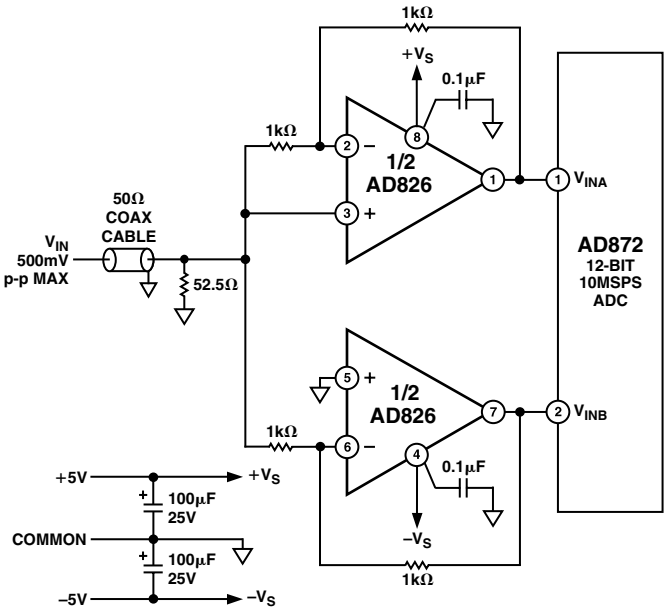


Figure 42. A Differential Input Buffer for High Bandwidth ADCs

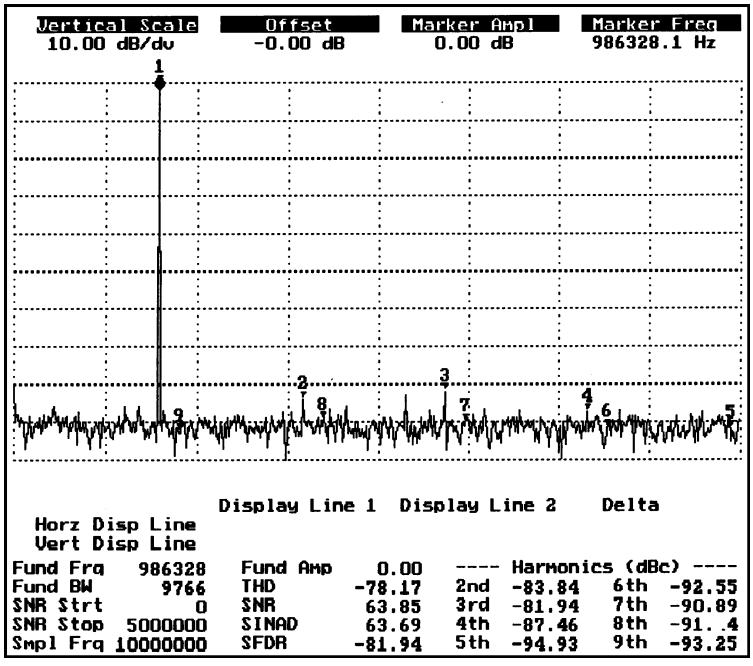
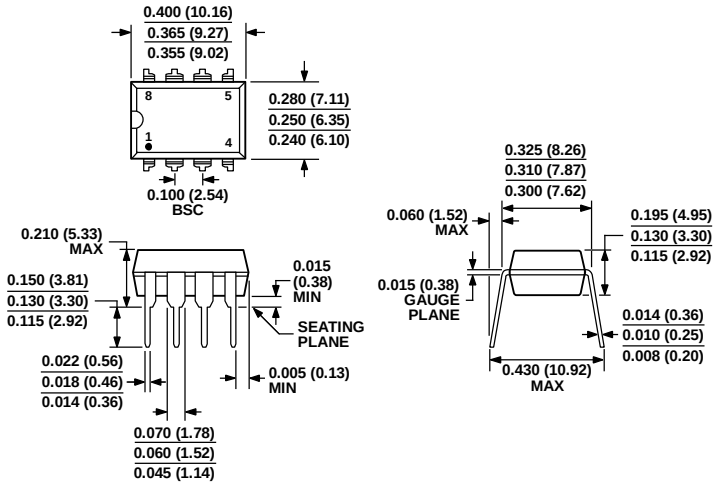


Figure 43. FFT, Buffered A/D Converter

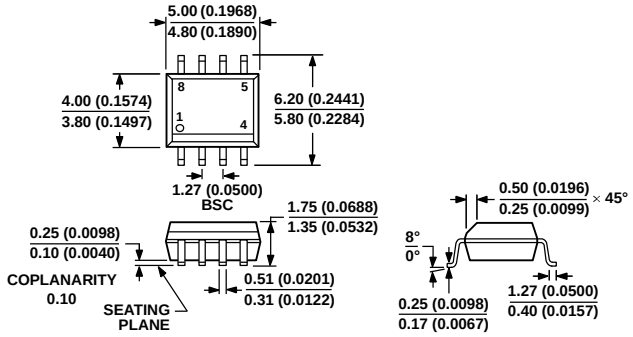
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 44. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 45. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD826AN	−40°C to +85°C	8-Lead PDIP	N-8
AD826ANZ	−40°C to +85°C	8-Lead PDIP	N-8
AD826AR	−40°C to +85°C	8-Lead SOIC_N	R-8
AD826AR-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD826AR-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8
AD826ARZ	−40°C to +85°C	8-Lead SOIC_N	R-8
AD826ARZ-REEL	−40°C to +85°C	8-Lead SOIC_N	R-8
AD826ARZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

REVISION HISTORY

Changed Power Supply Bypassing Section to Power Supply Considerations Section....10
Changes to Power Supply Considerations Section 10
Updated Outline Dimensions....14
Changes to Ordering Guide....14

D08950-0-4/10(C)