AD8013—SPECIFICATIONS (@ T_A = +25°C, R_{LOAD} = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD8013A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Bandwidth (3 dB)	No Peaking, G = +2	+5 V	100	125		MHz
	No Peaking, G = +2	±5 V	110	140		MHz
Bandwidth (0.1 dB)	No Peaking, G = +2	+5 V		50		MHz
	No Peaking, G = +2	±5 V		60		MHz
Slew Rate	2 V Step	+5 V		400		V/µs
	6 V Step	±5 V	600	1000		V/µs
Settling Time to 0.1%	0 V to +2 V	±5 V		18		ns
	4.5 V Step, C_{LOAD} = 200 pF	±6 V		40		ns
	R_{LOAD} > 1 kΩ, R_{FB} = 4 kΩ					
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 5 MHz, R_L = 1 k	±5 V		–76		dBc
	f_C = 5 MHz, R_L = 150 Ω	±5 V		–66		dBc
Input Voltage Noise	f = 10 kHz	+5 V, ±5 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz ($-I_{IN}$)	+5 V, ±5 V		12		pA/√Hz
Differential Gain (R_L = 150 Ω)	f = 3.58 MHz, G = +2	+5 V[1]		0.05		%
		±5 V		0.02	0.05	%
Differential Phase (R_L = 150 Ω)	f = 3.58 MHz, G = +2	+5 V[1]		0.06		Degrees
		±5 V		0.06	0.12	Degrees
DC PERFORMANCE						
Input Offset Voltage	T_{MIN} to T_{MAX}	+5 V, ±5 V		2	5	mV
Offset Drift				7		µV/°C
Input Bias Current (–)		+5 V, ±5 V		2	10	µA
Input Bias Current (+)	T_{MIN} to T_{MAX}	+5 V, ±5 V		3	15	µA
Open-Loop Transresistance		+5 V	650	800		kΩ
	T_{MIN} to T_{MAX}		550			kΩ
		±5 V	800 k	1.1 M		Ω
	T_{MIN} to T_{MAX}			650		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	±5 V		200		kΩ
	–Input	±5 V		150		Ω
Input Capacitance		±5 V		2		pF
Input Common-Mode Voltage Range		±5 V		3.8		±V
		+5 V	1.2		3.8	+V
Common-Mode Rejection Ratio						
Input Offset Voltage		+5 V	52	56		dB
Input Offset Voltage		±5 V	52	56		dB
–Input Current		+5 V, ±5 V		0.2	0.4	µA/V
+Input Current		+5 V, ±5 V		5	7	µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
R_L = 1 kΩ	V_{OL}–V_{EE}			0.8	1.0	V
	V_{CC}–V_{OH}			0.8	1.0	V
R_L = 150 Ω	V_{OL}–V_{EE}			1.1	1.3	V
	V_{CC}–V_{OH}			1.1	1.3	V
Output Current		+5 V		30		mA
		±5 V	25	30		mA
Short-Circuit Current		±5 V		95		mA
Capacitive Load Drive		±5 V		1000		pF
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, ±5 V		70		dB
Gain Flatness Match	f = 20 MHz	±5 V		0.1		dB
DC						
Input Offset Voltage		+5 V, ±5 V		0.3		mV
–Input Bias Current		+5 V, ±5 V		1.0		µA

Model	Conditions	V_S	AD8013A Min	Typ	Max	Units
POWER SUPPLY						
Operating Range	Single Supply		+4.2		+13	V
	Dual Supply		±2.1		±6.5	V
Quiescent Current/Amplifier		+5 V		3.0	3.5	mA
		±5 V		3.4	4.0	mA
		±6.5 V		3.5		mA
Quiescent Current/Amplifier	Power Down	+5 V		0.25	0.35	mA
		±5 V		0.3	0.4	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±2.5 V to ±5 V		70	76		dB
–Input Current		+5 V, ±5 V		0.03	0.2	µA/V
+Input Current		+5 V, ±5 V		0.07	1.0	µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 6 MHz	+5 V, ±5 V		–70		dB
Off Output Impedance	G = +1	+5 V, ±5 V		12		pF
Turn-On Time				50		ns
Turn-Off Time				30		ns
Switching Threshold		$–V_S$ + xV	1.3	1.6	1.9	V

NOTES
[1]The test circuit for differential gain and phase measurements on a +5 V supply is ac coupled.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 13.2 V Total
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.6 Watts (Observe Derating Curves)
Small Outline (R) . . . . 1.0 Watts (Observe Derating Curves)
Input Voltage (Common Mode) . . Lower of ±V_S or ±12.25 V
Differential Input Voltage . . . . . Output ±6 V (Clamped)
Output Voltage Limit
Maximum . . . . . Lower of (+12 V from $–V_S$) or ($+V_S$)
Minimum . . . . . Higher of (–12.5 V from $+V_S$) or ($–V_S$)
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range
N and R Package . . . . . –65°C to +125°C
Operating Temperature Range
AD8013A . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Pin Plastic DIP Package: θ_{JA} = 75°C/Watt
14-Pin SOIC Package: θ_{JA} = 120°C/Watt

ORDERING GUIDE

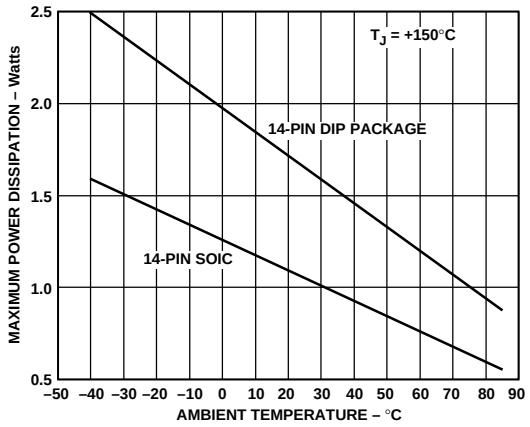
Model	Temperature Range	Package Description	Package Options
AD8013AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD8013AR-14	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013AR-14-REEL	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013AR-14-REEL7	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013ACHIPS	–40°C to +85°C	Die Form	

Maximum Power Dissipation

The maximum power that can be safely dissipated by the AD8013 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8013 is internally short circuit protected, this may not be enough to guarantee that the maximum junction temperature is not exceeded under all conditions. To ensure proper operation, it is important to observe the derating curves.

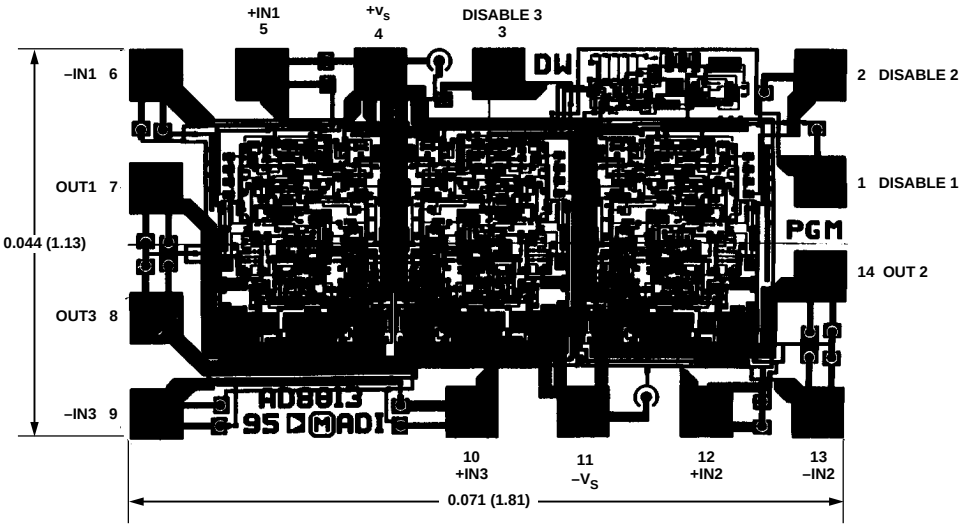
It must also be noted that in (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.



Maximum Power Dissipation vs. Ambient Temperature

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8013 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

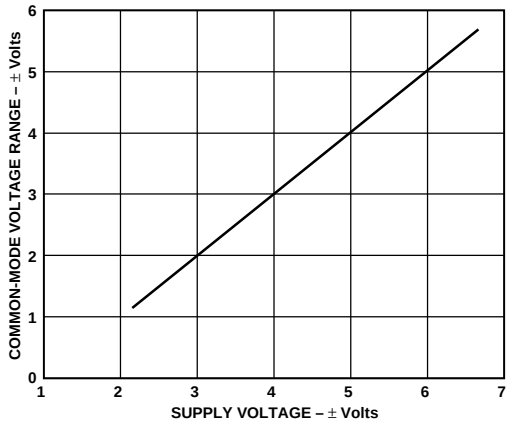


Figure 1. Input Common-Mode Voltage Range vs. Supply Voltage

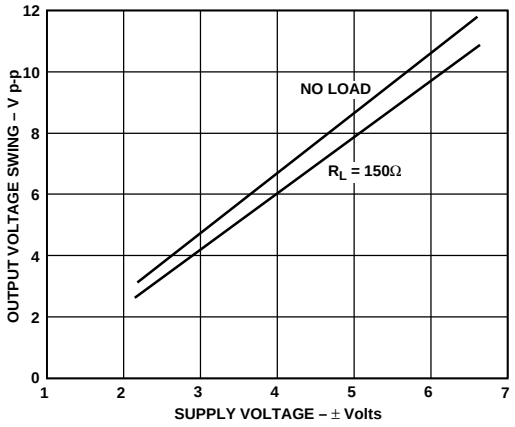


Figure 2. Output Voltage Swing vs. Supply Voltage

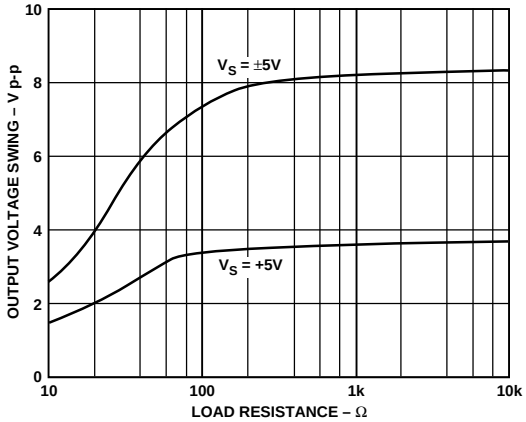


Figure 3. Output Voltage Swing vs. Load Resistance

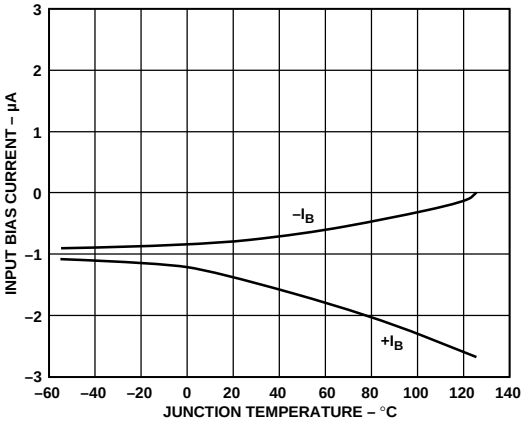


Figure 6. Input Bias Current vs. Junction Temperature

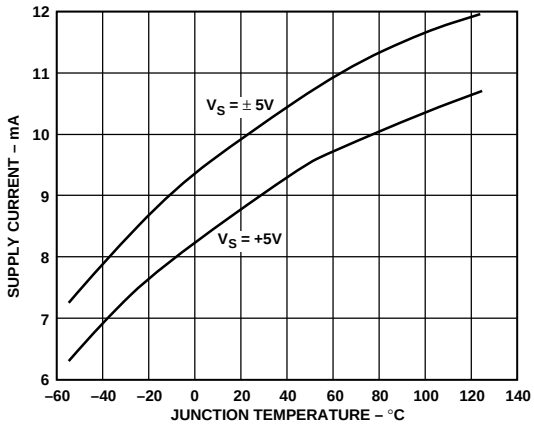


Figure 4. Total Supply Current vs. Junction Temperature

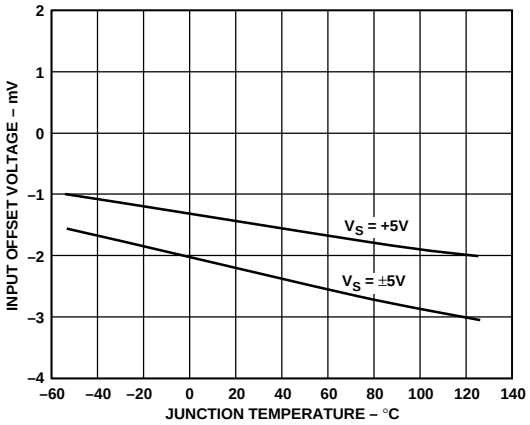


Figure 7. Input Offset Voltage vs. Junction Temperature

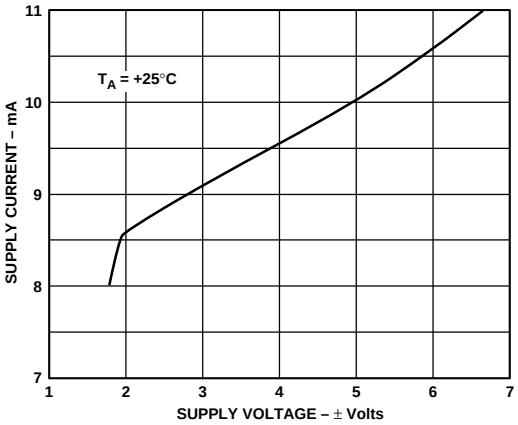


Figure 5. Supply Current vs. Supply Voltage

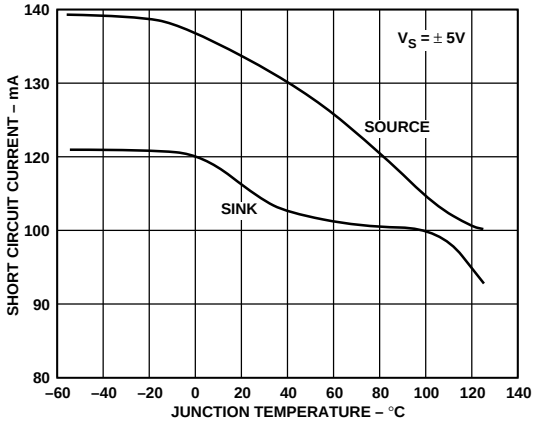


Figure 8. Short Circuit Current vs. Junction Temperature

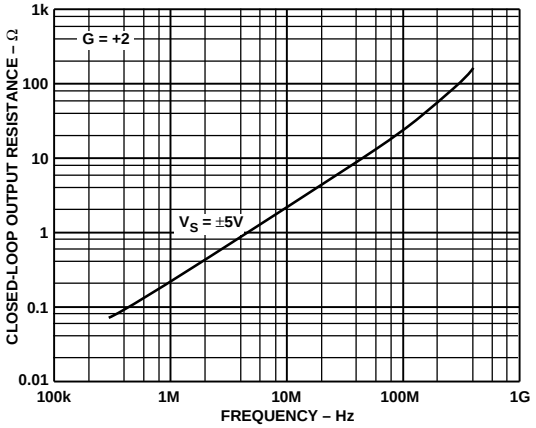


Figure 9. Closed-Loop Output Resistance vs. Frequency

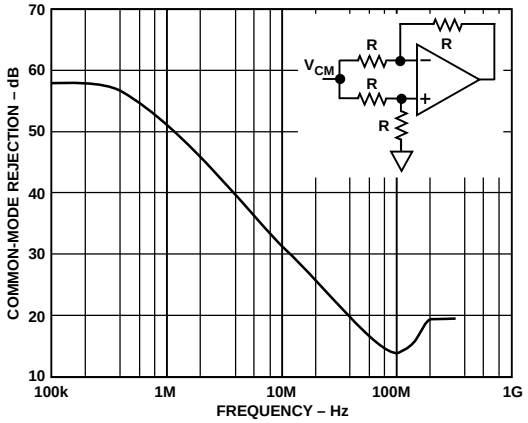


Figure 12. Common-Mode Rejection vs. Frequency

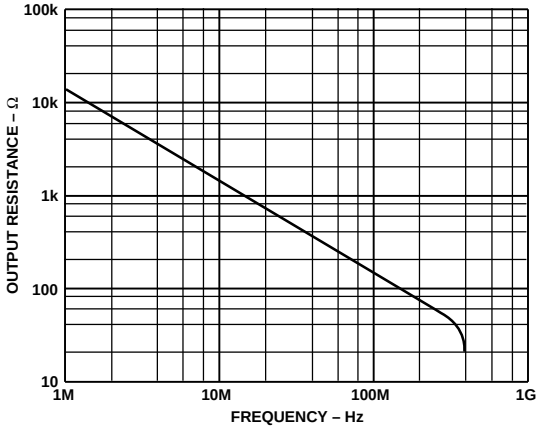


Figure 10. Output Resistance vs. Frequency, Disabled State

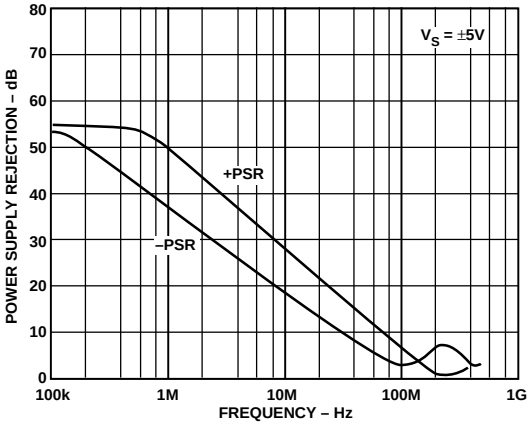


Figure 13. Power Supply Rejection Ratio vs. Frequency

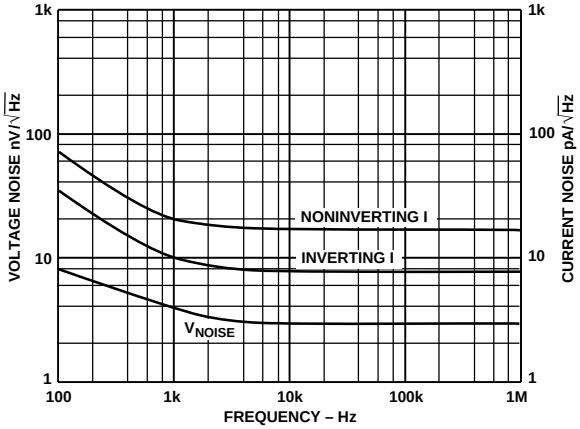


Figure 11. Input Current and Voltage Noise vs. Frequency

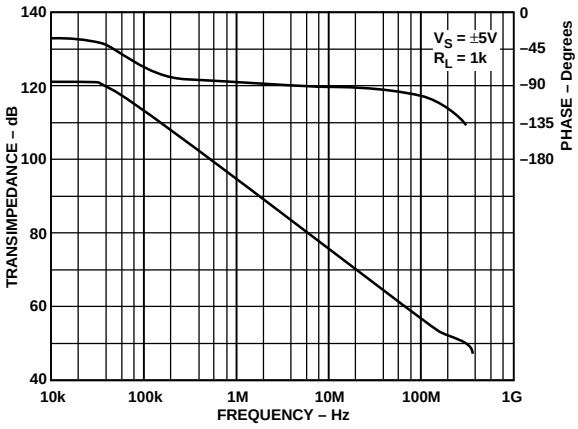


Figure 14. Open-Loop Transimpedance vs. Frequency (Relative to 1 Ω)

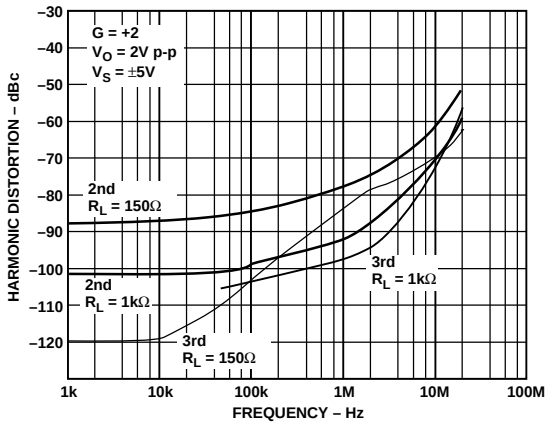


Figure 15. Harmonic Distortion vs. Frequency

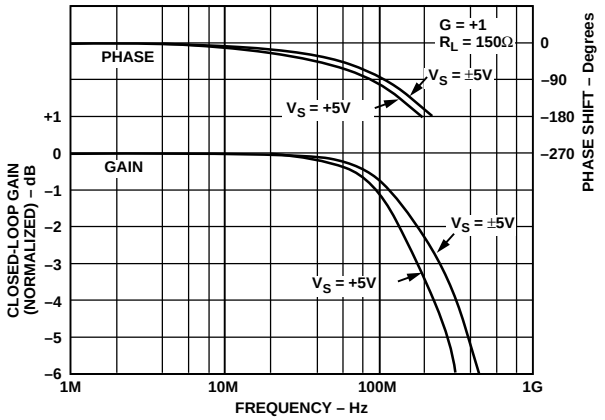


Figure 18. Closed-Loop Gain and Phase vs. Frequency, G = +1, R_L = 150 Ω

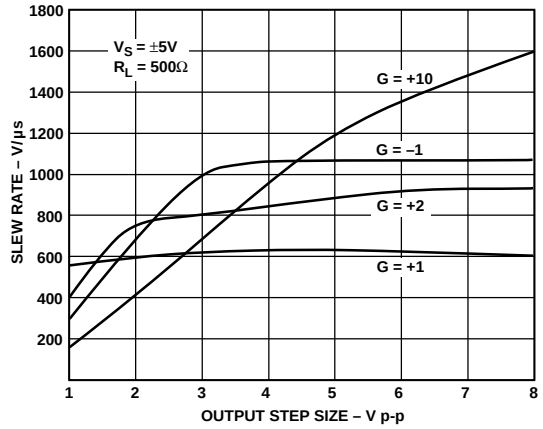


Figure 16. Slew Rate vs. Output Step Size

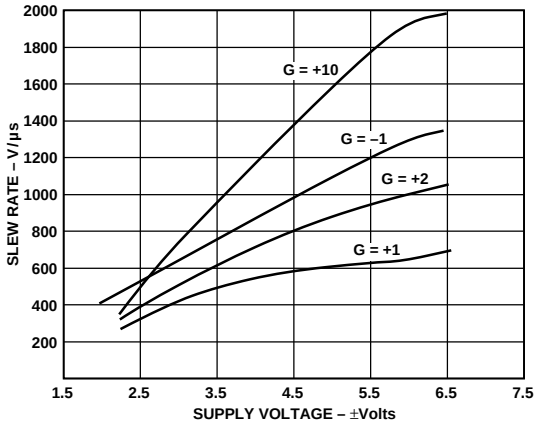


Figure 19. Maximum Slew Rate vs. Supply Voltage

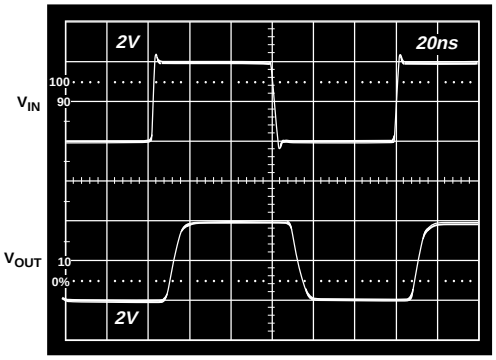


Figure 17. Large Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±5 V)

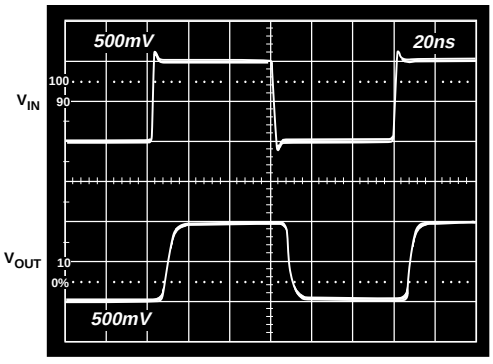


Figure 20. Small Signal Pulse Response, Gain = +1, (R_F = 2 kΩ, R_L = 150 Ω, V_S = ±5 V)

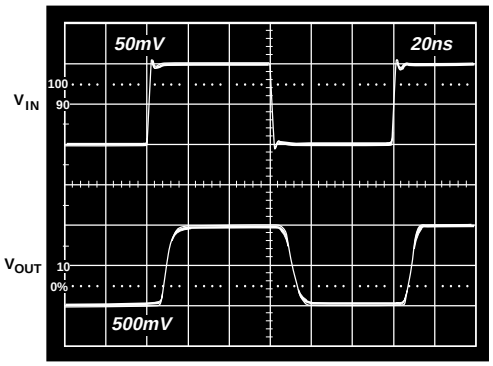


Figure 21. Large Signal Pulse Response, Gain = +10, R_F = 301 Ω, R_L = 150 Ω, V_S = ±5 V)

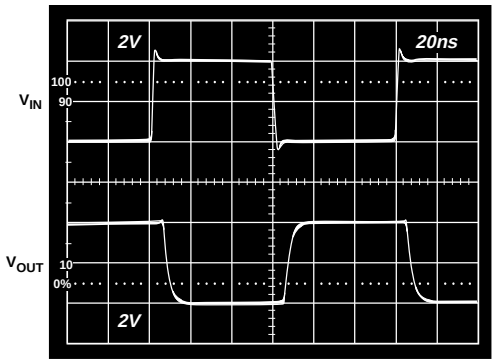


Figure 24. Large Signal Pulse Response, Gain = –1, (R_F = 698 Ω, R_L = 150 Ω, V_S = ±5 V)

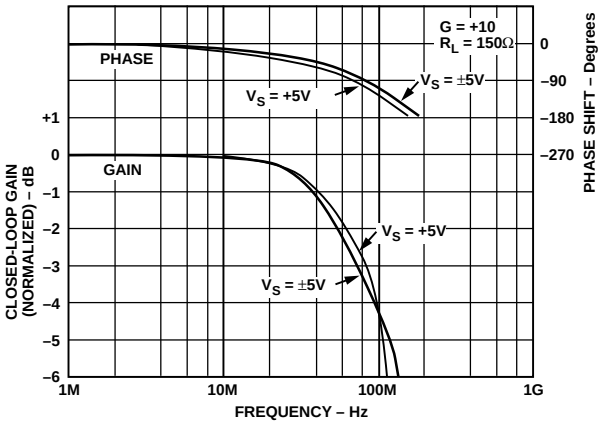


Figure 22. Closed-Loop Gain and Phase vs. Frequency, G = +10, R_L = 150 Ω

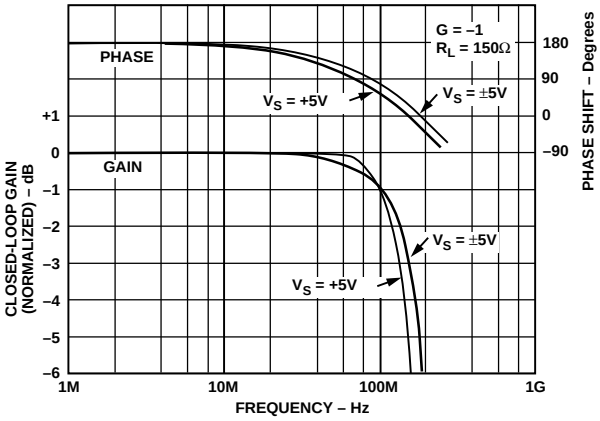


Figure 25. Closed-Loop Gain and Phase vs. Frequency, G = –1, R_L = 150 Ω

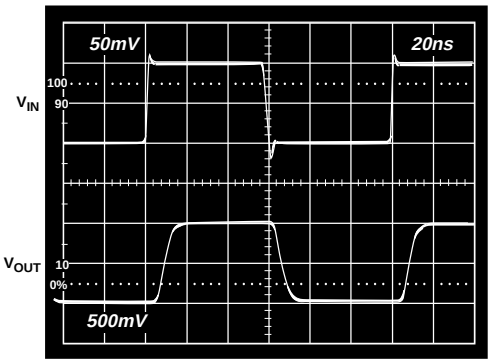


Figure 23. Small Signal Pulse Response, Gain = +10, (R_F = 301 Ω, R_L = 150 Ω, V_S = ±5 V)

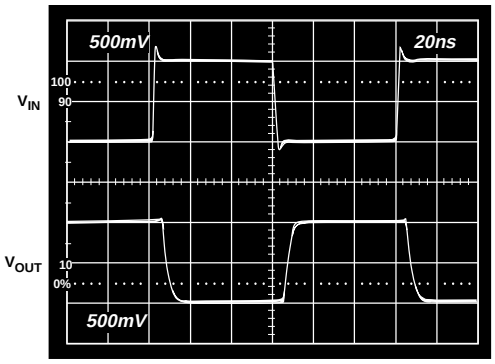


Figure 26. Small Signal Pulse Response, Gain = –1, (R_F = 698 Ω, R_L = 150 Ω, V_S = ±5 V)

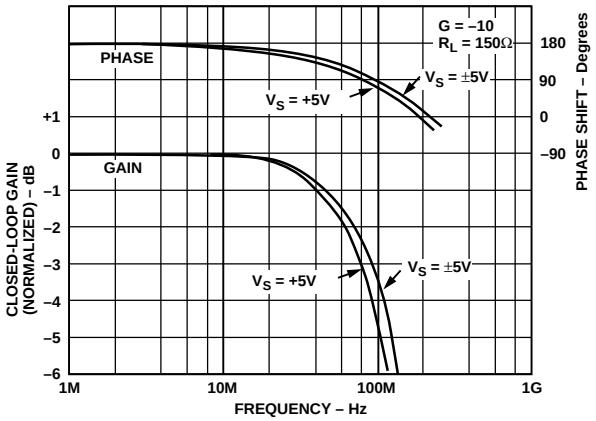


Figure 27. Closed-Loop Gain and Phase vs. Frequency, G = –10, R_L = 150 Ω

General

The AD8013 is a wide bandwidth, triple video amplifier that offers a high level of performance on less than 4.0 mA per amplifier of quiescent supply current. The AD8013 uses a proprietary enhancement of a conventional current feedback architecture, and achieves bandwidth in excess of 200 MHz with low differential gain and phase errors, making it an extremely efficient video amplifier.

The AD8013's wide phase margin coupled with a high output short circuit current make it an excellent choice when driving any capacitive load. High open-loop gain and low inverting input bias current enable it to be used with large values of feedback resistor with very low closed-loop gain errors.

It is designed to offer outstanding functionality and performance at closed-loop inverting or noninverting gains of one or greater.

Choice of Feedback & Gain Resistors

Because it is a current feedback amplifier, the closed-loop bandwidth of the AD8013 may be customized using different values of the feedback resistor. Table I shows typical bandwidths at different supply voltages for some useful closed-loop gains when driving a load of 150 Ω.

The choice of feedback resistor is not critical unless it is important to maintain the widest, flattest frequency response. The resistors recommended in the table are those (chip resistors) that will result in the widest 0.1 dB bandwidth without peaking. In applications requiring the best control of bandwidth, 1% resistors are adequate. Package parasitics vary between the 14-pin plastic DIP and the 14-pin plastic SOIC, and may result in a slight difference in the value of the feedback resistor used to achieve the optimum dynamic performance. Resistor values and widest bandwidth figures are shown in parenthesis for the SOIC where they differ from those of the DIP. Wider bandwidths than those in the table can be attained by reducing the magnitude of the feedback resistor (at the expense of increased peaking), while peaking can be reduced by increasing the magnitude of the feedback resistor.

Increasing the feedback resistor is especially useful when driving large capacitive loads as it will increase the phase margin of the closed-loop circuit. (Refer to the section on driving capacitive loads for more information.)

To estimate the –3 dB bandwidth for closed-loop gains of 2 or greater, for feedback resistors not listed in the following table, the following single pole model for the AD8013 may be used:

$$ACL \simeq \frac{G}{1+SC_T\,(R_F+Gn\,rin)}$$

where: C_T = transcapacitance ≅ 1 pF
R_F = feedback resistor
G = ideal closed loop gain

$$Gn = \left(1+\frac{R_F}{R_G}\right) = \text{noise gain}$$

rin = inverting input resistance ≅ 150 Ω
ACL = closed loop gain

The –3 dB bandwidth is determined from this model as:

$$f_3 \simeq \frac{1}{2\,\pi\,C_T(R_F+Gn\,rin)}$$

This model will predict –3 dB bandwidth to within about 10% to 15% of the correct value when the load is 150 Ω and V_S = ±5 V. For lower supply voltages there will be a slight decrease in bandwidth. The model is not accurate enough to predict either the phase behavior or the frequency response peaking of the AD8013.

It should be noted that the bandwidth is affected by attenuation due to the finite input resistance. Also, the open-loop output resistance of about 12 Ω reduces the bandwidth somewhat when driving load resistors less than about 250 Ω. (Bandwidths will be about 10% greater for load resistances above a few hundred ohms.)

Table I. –3 dB Bandwidth vs. Closed-Loop Gain and Feedback Resistor, R_L = 150 Ω (SOIC)

V_S – Volts	Gain	R_F – Ohms	BW – MHz
±5	+1	2000	230
	+2	845 (931)	150 (135)
	+10	301	80
	–1	698 (825)	140 (130)
	–10	499	85
+5	+1	2000	180
	+2	887 (931)	120 (130)
	+10	301	75
	–1	698 (825)	130 (120)
	–10	499	80

Driving Capacitive Loads

When used in combination with the appropriate feedback resistor, the AD8013 will drive any load capacitance without oscillation. The general rule for current feedback amplifiers is that the higher the load capacitance, the higher the feedback resistor required for stable operation. Due to the high open-loop transresistance and low inverting input current of the AD8013, the use of a large feedback resistor does not result in large closed-loop gain errors. Additionally, its high output short circuit current makes possible rapid voltage slewing on large load capacitors.

For the best combination of wide bandwidth and clean pulse response, a small output series resistor is also recommended. Table II contains values of feedback and series resistors which result in the best pulse responses. Figure 29 shows the AD8013 driving a 300 pF capacitor through a large voltage step with virtually no overshoot. (In this case, the large and small signal pulse responses are quite similar in appearance.)

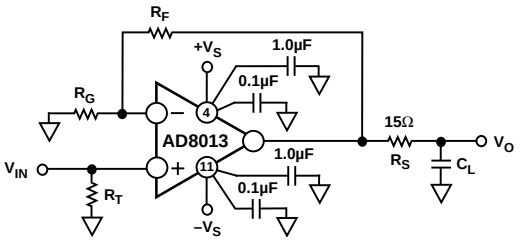


Figure 28. Circuit for Driving a Capacitive Load

Table II. Recommended Feedback and Series Resistors vs. Capacitive Load and Gain

C_L – pF	R_F – Ohms	R_S – Ohms G = 2	R_S – Ohms G ≥ 3
20	2k	25	15
50	2k	25	15
100	3k	20	15
200	4k	15	15
300	6k	15	15
≥500	7k	15	15

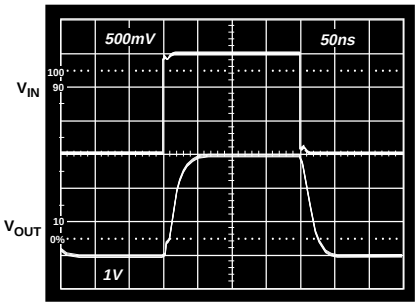


Figure 29. Pulse Response Driving a Large Load Capacitor. C_L = 300 pF, G = +2, R_F = 6k, R_S = 15 Ω

Overload Recovery

The three important overload conditions are: input common-mode voltage overdrive, output voltage overdrive, and input current overdrive. When configured for a low closed-loop gain, the amplifier will quickly recover from an input common-mode voltage overdrive; typically in under 25 ns. When configured for a higher gain, and overloaded at the output, the recovery time will also be short. For example, in a gain of +10, with 15% overdrive, the recovery time of the AD8013 is about 20 ns (see Figure 30). For higher overdrive, the response is somewhat slower. For 6 dB overdrive, (in a gain of +10), the recovery time is about 65 ns.

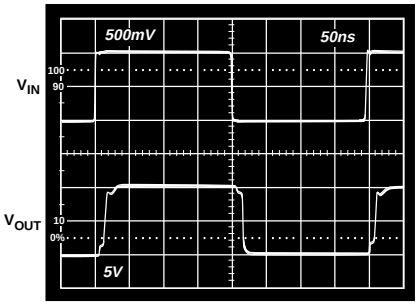


Figure 30. 15% Overload Recovery, G = +10 (R_F = 300 Ω, R_L = 1 kΩ, V_S = ±5 V)

As noted in the warning under "Maximum Power Dissipation," a high level of input overdrive in a high noninverting gain circuit can result in a large current flow in the input stage. Though this current is internally limited to about 30 mA, its effect on the total power dissipation may be significant.

High Performance Video Line Driver

At a gain of +2, the AD8013 makes an excellent driver for a back terminated 75 Ω video line (Figures 31, 32, and 33). Low differential gain and phase errors and wide 0.1 dB bandwidth can be realized. The low gain and group delay matching errors ensure excellent performance in RGB systems. Figures 34 and 35 show the worst case matching.

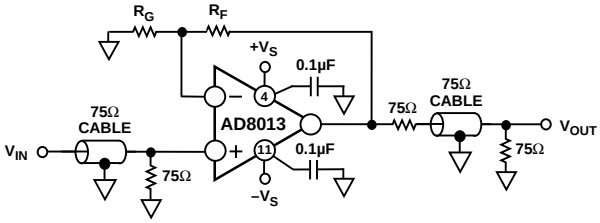


Figure 31. A Video Line Driver Operating at a Gain of +2 (R_F = R_G from Table I)

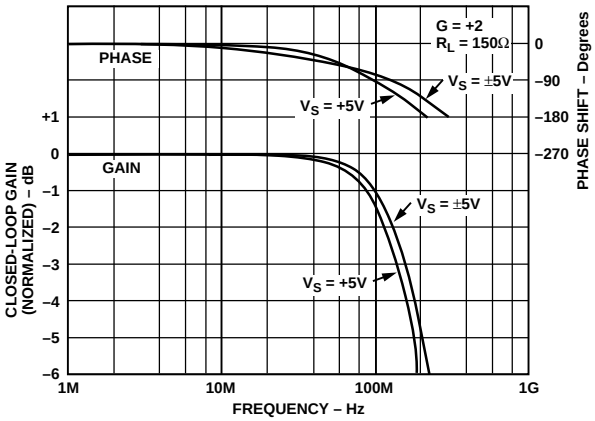


Figure 32. Closed-Loop Gain & Phase vs. Frequency for the Line Driver

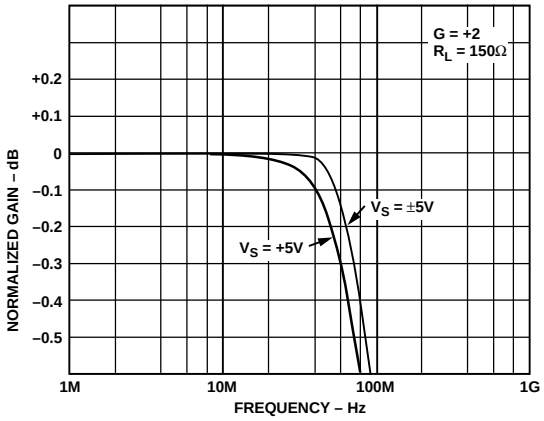


Figure 33. Fine-Scale Gain Flatness vs. Frequency, G = +2, R_L = 150 Ω

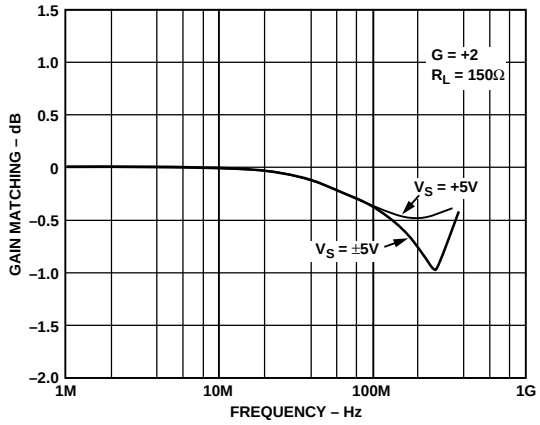


Figure 34. Closed-Loop Gain Matching vs. Frequency

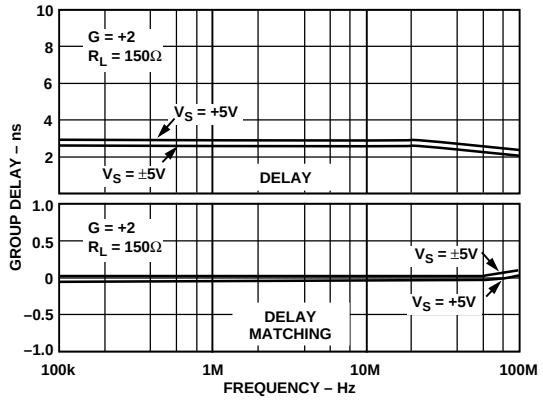


Figure 35. Group Delay and Group Delay Matching vs. Frequency, G = +2, R_L = 150 Ω

Disable Mode Operation

Pulling the voltage on any one of the Disable pins about 1.6 V up from the negative supply will put the corresponding amplifier into a disabled, powered down, state. In this condition, the amplifier's quiescent current drops to about 0.3 mA, its output becomes a high impedance, and there is a high level of isolation from input to output. In the case of the gain of two line driver for example, the impedance at the output node will be about the same as for a 1.6 kΩ resistor (the feedback plus gain resistors) in parallel with a 12 pF capacitor and the input to output isolation will be about 66 dB at 5 MHz.

Leaving the Disable pin disconnected (floating) will leave the corresponding amplifier operational, in the enabled state. The input impedance of the disable pin is about 40 kΩ in parallel with a few picofarads. When driven to 0 V, with the negative supply at –5 V, about 100 μA flows into the disable pin.

When the disable pins are driven by complementary output CMOS logic, on a single 5 V supply, the disable and enable times are about 50 ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the Disable pins. Figure 36 shows one possible method which results in a negligible increase in switching time.

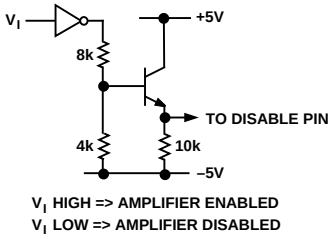


Figure 36. Level Shifting to Drive Disable Pins on Dual Supplies

The AD8013's input stages include protection from the large differential input voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3 V. The high input to output isolation will be maintained for voltages below this limit.

3:1 Video Multiplexer

Wiring the amplifier outputs together will form a 3:1 mux with excellent switching behavior. Figure 37 shows a recommended configuration which results in –0.1 dB bandwidth of 35 MHz and OFF channel isolation of 60 dB at 10 MHz on ±5 V supplies. The time to switch between channels is about 50 ns. Switching time is virtually unaffected by signal level.

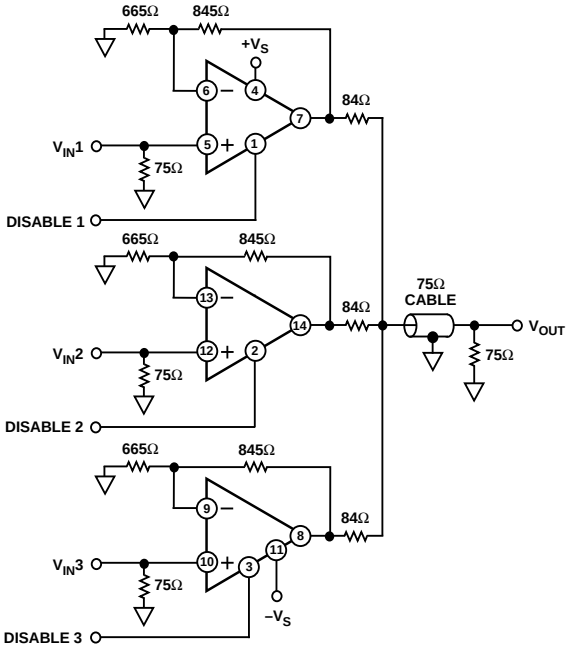


Figure 37. A Fast Switching 3:1 Video Mux (Supply Bypassing Not Shown)

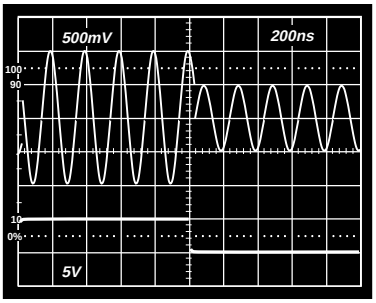


Figure 38. Channel Switching Characteristic for the 3:1 Mux

2:1 Video Multiplexer

Configuring two amplifiers as unity gain followers and using the third to set the gain results in a high performance 2:1 mux (Figures 39 and 40). This circuit takes advantage of the very low crosstalk between Channels 2 and 3 to achieve the OFF channel isolation shown in Figure 40. This circuit can achieve differential gain and phase of 0.03% and 0.07° respectively.

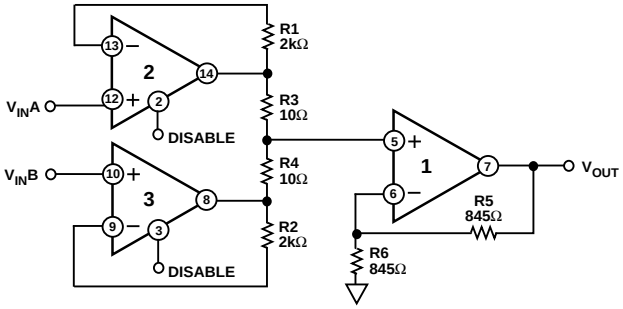


Figure 39. 2:1 Mux with High Isolation and Low Differential Gain and Phase Errors

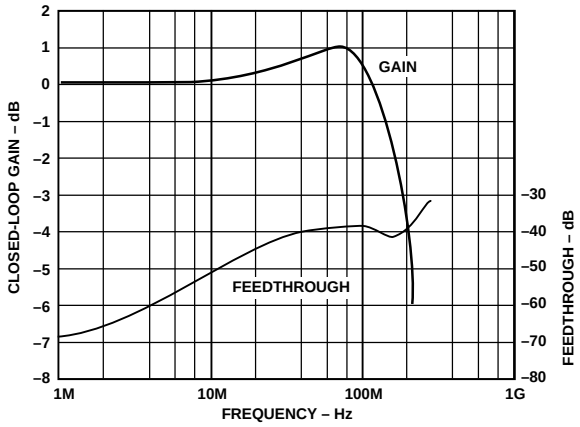


Figure 40. 2:1 Mux ON Channel Gain and Mux OFF Channel Feedthrough vs. Frequency

Gain Switching

The AD8013 can be used to build a circuit for switching between any two arbitrary gains while maintaining a constant input impedance. The example of Figure 41 shows a circuit for switching between a noninverting gain of 1 and an inverting gain of 1. The total time for channel switching and output voltage settling is about 80 ns.

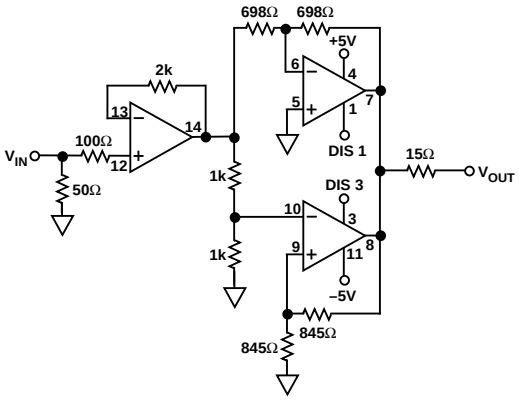


Figure 41. Circuit to Switch Between Gains of –1 and +1

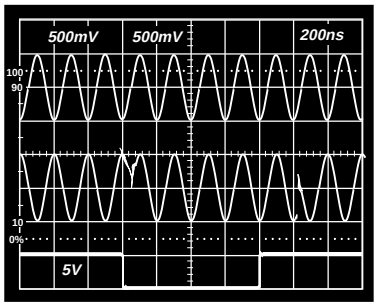


Figure 42. Switching Characteristic for Circuit of Figure 41

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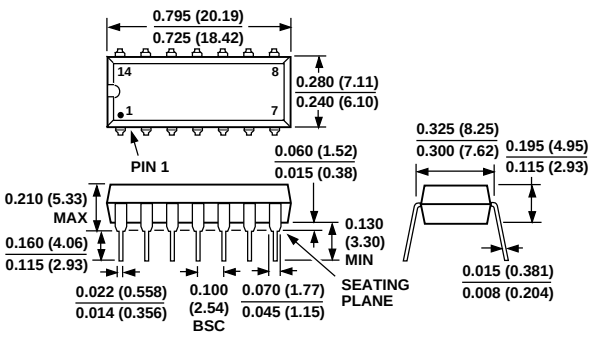
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP (N-14)



14-Lead SOIC (R-14)