

AD7543* PRODUCT PAGE QUICK LINKS

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Data Sheet

- AD7543: CMOS Serial Input 12-Bit DAC Scanned Data Sheet

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Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

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AD7543—SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted.)

Parameter	Limit At T _A = +25°C	Limit At ¹ T _A = -40°C to +85°C	Limit At ¹ T _A = -55°C & +125°C	Units	Conditions/Comments	
ACCURACY						
Resolution	12	12	12	Bits		
Relative Accuracy ²						
J, A, S Versions	±1	±1	±1	LSB max		
K, B, T Versions	±1/2	±1/2	±1/2	LSB max		
GK, GB, GT Versions	±1/2	±1/2	±1/2	LSB max		
Differential Nonlinearity ²						
J, A, S Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T _{min} to T _{max}	
K, B, T Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T _{min} to T _{max}	
GK, GB, GT Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T _{min} to T _{max}	
Gain Error ²						
J, K, A, B, S, T	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be	
GK, GB, GT	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 6 & 7)	
Gain Temperature Coefficient						
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C	
Power Supply Rejection						
ΔGain/ΔV _{DD}	0.005	0.01	0.01	% per % max	V _{DD} = +4.75V to +5.25V	
Output Leakage Current						
I _{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s	
I _{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s	
DYNAMIC PERFORMANCE						
Current Settling Time ³	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{\text{LD1}}$ and $\overline{\text{LD2}}$, see Figure 5.	
Multiplying Feedthrough Error ³	2.5	2.5	2.5	mV p-p max	V _{REF} = ±10V, 10kHz sine wave	
REFERENCE INPUT						
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is -300ppm/°C	
ANALOG OUTPUTS						
Output Capacitance						
C _{OUT1} ³	75	75	75	pF max	Register B loaded to 0000 0000 0000	
C _{OUT1} ³	260	260	260	pF max	Register B loaded to 1111 1111 1111	
C _{OUT2} ³	75	75	75	pF max	Register B loaded to 1111 1111 1111	
C _{OUT2} ³	260	260	260	pf max	Register B loaded to 0000 0000 0000	
LOGIC INPUTS						
V _{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	V _{IN} = 0V or V _{DD}	
V _{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max		
I _{IN} ⁴	1	1	1	μA max		
C _{IN} (Input Capacitance) ³	8	8	8	pF max		
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 6 and 7), serial load (MSB First)					
SWITCHING CHARACTERISTICS ⁵						
t _{DS1}	50	100	100	ns min	(Serial Input to Strobe Setup Time)	STB1 used as a strobe
t _{DS4}	0	0	0	ns min		STB4 used as a strobe
t _{DS3}	0	0	0	ns min		STB3 used as a strobe
t _{DS2}	20	40	40	ns min		STB2 used as a strobe
t _{DH1}	30	60	60	ns min	(Serial Input to Strobe Hold Time)	STB1 used as a strobe
t _{DH4}	80	160	160	ns min		STB4 used as a strobe
t _{DH3}	80	160	160	ns min		STB3 used as a strobe
t _{DH2}	60	120	120	ns min		STB2 used as a strobe
t _{SRI}	80	160	160	ns min	SRI data pulse width	
t _{STB1}	80	160	160	ns min	STB1 pulse width	
t _{STB4}	100	200	200	ns min	STB4 pulse width	
t _{STB3}	100	200	200	ns min	STB3 pulse width	
t _{STB2}	80	160	160	ns min	STB2 pulse width	
t _{LD1} , t _{LD2}	150	300	300	ns min	Load pulse width	
t _{ASB}	0	0	0	ns min	Min time between strobing LSB into Register A and loading Register B	
t _{CLR}	200	400	400	ns min	CLR pulse width	
POWER SUPPLY						
V _{DD} (Supply Voltage)	+5	+5	+5	V	Digital Inputs = V _{INH} or V _{INL}	
I _{DD} (Supply Current)	2.5	2.5	2.5	mA max		

NOTES

¹Temperature ranges as follows: JN, KN, GKN Version: -40°C to +85°C
AQ, BQ, GBQ Versions: -40°C to +85°C
SQ, TQ, GTQ Versions: -55°C to +125°C

²See Terminology on following page.

³Guaranteed but not tested.

⁴Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

⁵Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*(T_A = +25°C unless otherwise noted)**ORDERING GUIDE**

		Model	Temperature Range	Relative Accuracy	Gain Error	Package Option*
V _{DD} to AGND	0V, +7V	AD7543JN	−40°C to +85°C	±1LSB	±12.3LSB	N-16
V _{DD} to DGND	0V, +7V	AD7543KN	−40°C to +85°C	±1/2LSB	±12.3LSB	N-16
AGND to DGND	V _{DD} + 0.3V	AD7543GKN	−40°C to +85°C	±1/2LSB	±1LSB	N-16
DGND to AGND	V _{DD} + 0.3V	AD7543JP	−40°C to +85°C	±1LSB	±12.3LSB	P-20A
Digital Input Voltage to DGND	−0.3V, V _{DD} + 0.3V	AD7543KP	−40°C to +85°C	±1/2LSB	±12.3LSB	P-20A
V _{OUT1} , V _{OUT2} to AGND	−0.3V, V _{DD} to +0.3V	AD7543GKP	−40°C to +85°C	±1/2LSB	±1LSB	P-20A
V _{REF} to AGND	±25V	AD7543JR	−40°C to +85°C	±1LSB	±12.3LSB	R-16
V _{RFB} to AGND	±25V	AD7543KR	−40°C to +85°C	±1/2LSB	±12.3LSB	R-16
Power Dissipation (Package)		AD7543GKR	−40°C to +85°C	±1/2LSB	±1LSB	R-16
Plastic		AD7543AQ	−40°C to +85°C	±1LSB	±12.3LSB	Q-16
To +70°C	670mW	AD7543BQ	−40°C to +85°C	±1/2LSB	±12.3LSB	Q-16
Derates above +70°C by	8.3mW/°C	AD7543GBQ	−40°C to +85°C	±1/2LSB	±1LSB	Q-16
Cerdip		AD7543SQ	−55°C to +125°C	±1LSB	±12.3LSB	Q-16
To +75°C	450mW	AD7543TQ	−55°C to +125°C	±1/2LSB	±12.3LSB	Q-16
Derates above +75°C by	6mW/°C	AD7543GTQ	−55°C to +125°C	±1/2LSB	±1LSB	Q-16
Operating Temperature Range		AD7543SE	−55°C to +125°C	±1LSB	±12.3LSB	E-20A
Commercial (J, K, GK Versions)	−40°C to +85°C	AD7543TE	−55°C to +125°C	±1/2LSB	±12.3LSB	E-20A
Industrial (A, B, GB Versions)	−40°C to +85°C	AD7543GTE	−55°C to +125°C	±1/2LSB	±1LSB	E-20A
Extended (S, T, GT Versions)	−55°C to +125°C					
Storage Temperature	−65°C to +150°C					
Lead Temperature (Soldering, 10secs)	+300°C					

*E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC).

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table II
5	LD1	DAC Register B Load 1 input. When LD1 and LD2 go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table II
9	LD2	DAC Register B Load 2 input. When LD1 and LD2 go low the contents of Register A are loaded into DAC Register B
10	STB3	Register A Strobe 3 input, see Table II
11	STB4	Register A Strobe 4 input, see Table II
12	DGND	Digital Ground
13	CLR	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V _{DD}	+5V Supply Input
15	V _{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R _F B	DAC Feedback Resistor

Table 1. Pin Function Description, DIP Configuration

AD7543

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of $-4095/4096$. Gain error is adjustable using external trims as shown in Figures 6 and 7.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

GENERAL CIRCUIT INFORMATION

The AD7543, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

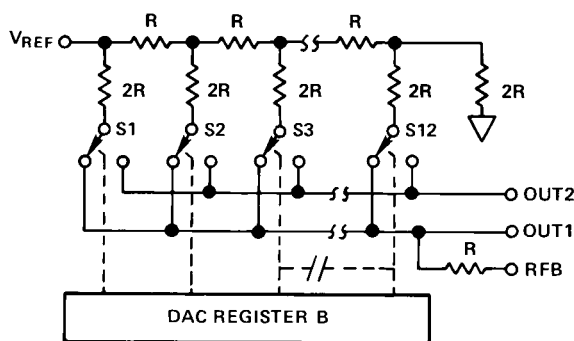


Figure 1. AD7543 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the $R/2R$ ladder characteristic resistance and is equal to value "R"). The reference terminal can be driven

by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.

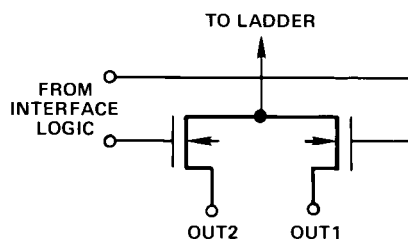


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $1/4096$ current source represents a constant 1 least significant bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

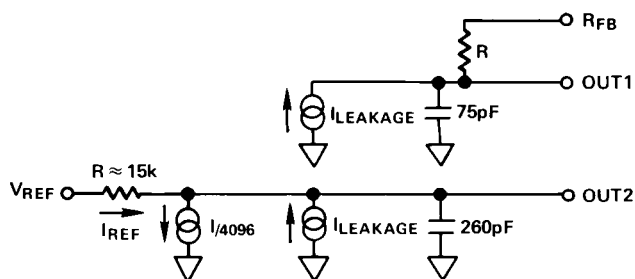


Figure 3. AD7543 DAC Equivalent Circuit All Digital Inputs LOW

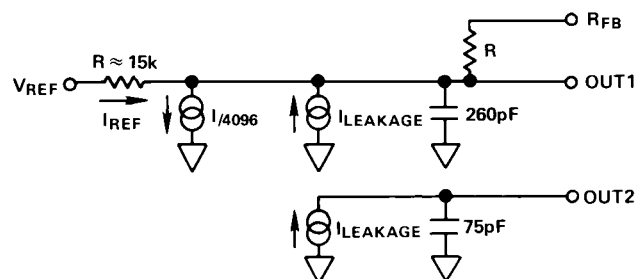


Figure 4. AD7543 DAC Equivalent Circuit All Digital Inputs HIGH

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0		X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1		0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0		0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:

1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown $\uparrow$ is positive edge $\downarrow$ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table II. AD7543 Truth Table

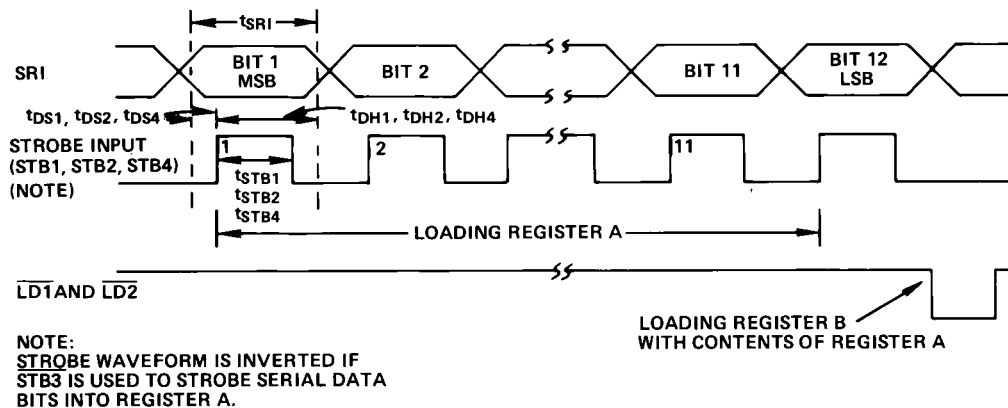


Figure 5. Timing Diagram

INTERFACE LOGIC INFORMATION

Shown in the AD7543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SR1 is clocked into the shift register on the leading (rising) edge of STB1, STB2 or STB4 or on the leading (falling) edge of STB3. Table II defines the various logic states required on the Register A control inputs, while Figure 5 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing LD1 and LD2 momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing CLR momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit of Figure 6, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit of Figure 7, a CLEAR causes the DAC output to equal $-V_{REF}$.

APPLYING THE AD7543

UNIPOLAR BINARY OPERATION
(2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current (again of + or - polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table III.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10pF to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

AD7543

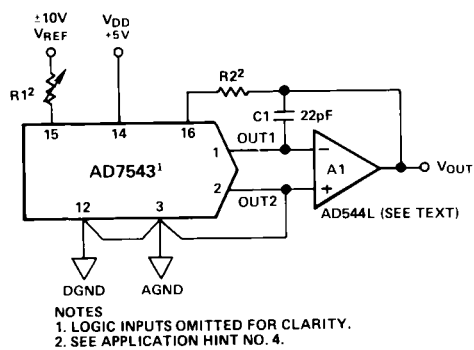


Figure 6. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT}
MSB	LSB	
1111 1111 1111		$-V_{REF} \left(\frac{4095}{4096} \right)$
1000 0000 0000		$-V_{REF} \left(\frac{2048}{4096} \right) = -1/2 V_{REF}$
0000 0000 0001		$-V_{REF} \left(\frac{1}{4096} \right)$
0000 0000 0000		0V

Table III. Unipolar Binary Code Table for Circuit of Figure 6

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT} . Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally $15k\Omega$). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS} .

BIPOLAR OPERATION
(4-QUADRANT MULTIPLICATION)

Figure 7 and Table IV illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B . R3, R4 and R5 must be selected for matching and tracking. Mismatch of $2R3$ to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 to $2R3$ causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

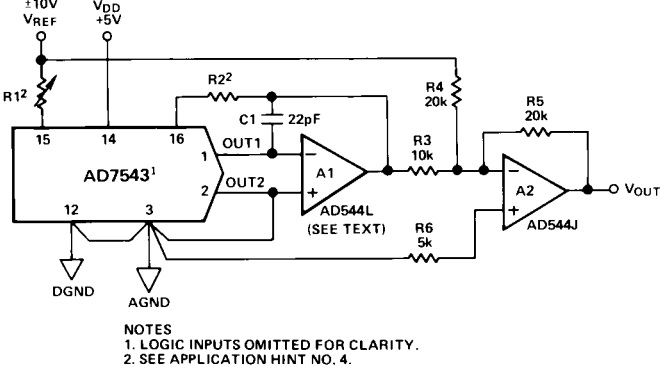


Figure 7. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT}
MSB	LSB	
1111 1111 1111		$+V_{REF} \left(\frac{2047}{2048} \right)$
1000 0000 0001		$+V_{REF} \left(\frac{1}{2048} \right)$
1000 0000 0000		0V
0111 1111 1111		$-V_{REF} \left(\frac{1}{2048} \right)$
0000 0000 0000		$-V_{REF} \left(\frac{2048}{2048} \right)$

Table IV. Bipolar Code Table for Offset Binary Circuit of Figure 7

APPLICATION HINTS

The AD7543 is a precision 12-bit multiplying DAC designed for serial interface. To ensure system performance consistent with AD7543 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7543. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7543 AGND and DGND pins to prevent possible device damage.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the $R/2R$ differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF} 2^{-n}$ where n is the number of bits exercised].

3. **HIGH FREQUENCY CONSIDERATIONS:** AD7543 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. **GAIN TEMPERATURE COEFFICIENTS:** The gain temperature coefficient of the AD7543 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 6 and 7 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to } R_1 = -\frac{R_1}{R_{IN}} (\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to } R_2 = +\frac{R_2}{R_{IN}} (\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wire-wound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN} , their contribution to gain temperature coefficient will also be small. For the standard AD7543 gain error specification of ± 12.3 LSBs it is recommended that $R_1 = 120\Omega$ and $R_2 = 60\Omega$. With $\gamma = 50$ these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7} (50 + 300) = 8\text{ppm/}^\circ\text{C}$$

However, if the AD7543GTD is used which has a specified gain error of ± 1 LSB, then with $R_1 = 10\Omega$ and $R_2 = 5\Omega$ the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630-10-6/81 available from Analog Devices.

5. For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479-15-8/78, available from Analog Devices.

AD7543 INTERFACE TO MC6800

In this example, it is assumed that the 12-bit data is contained in two memory locations (0000 and 0001). The four most significant bits are assumed to occupy the lower half of memory location 0000. The eight least significant bits occupy memory location 0001. The data is presented bit by bit on the D7 line and strobed into the AD7543 by executing memory write instructions. In this case the strobe signal (STB1) is supplied by decoding address 2000, $R/\bar{W}$ and ϕ_2 . A memory write instruction to a different address (4000) loads the data from Register A to the DAC register.

Figure 8 shows the interface circuitry and Table V gives a listing of the procedure.

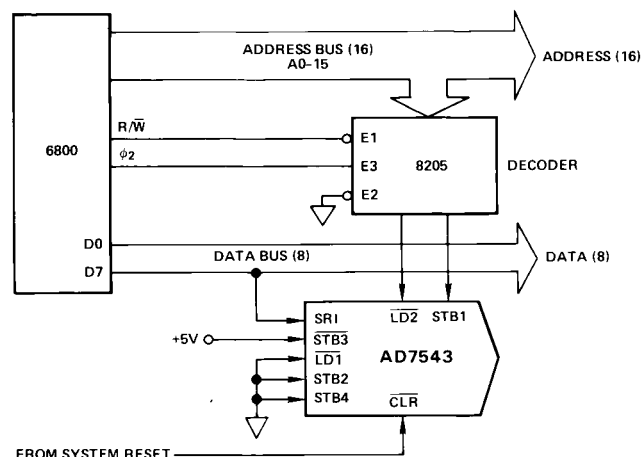


Figure 8. AD7543-MC6800 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
LOOP	LDA	B, 04	
	LDA	A, 0000	Load 4 Most Significant Bits
	ROL	A	Reposition in the Data
	DEC	B	in ACC A
	BNE	LOOP	
	LDA	B, 04	
	BSR	SHIFT	Output Data
SHIFT	LDA	B, 08	
	LDA	A, 0001	Load 8 Least Significant Bits
	BSR	SHIFT	Output Data
	STA	A, 4000	Load DAC Register
	RTS		Return to Main Program
	STA	A, 2000	Strobe Data
	ROL	A	into AD7543
	DEC	B	
	BNE	SHIFT	
	RTS		

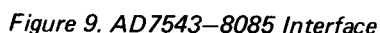
Table V. Sample Routine for AD7543-MC6800 Interface

AD7543 INTERFACE TO MCS-85

Figure 9 shows the AD7543 interfaced to the 8085. This system makes use of the serial output facility (SOD) on the 8085.

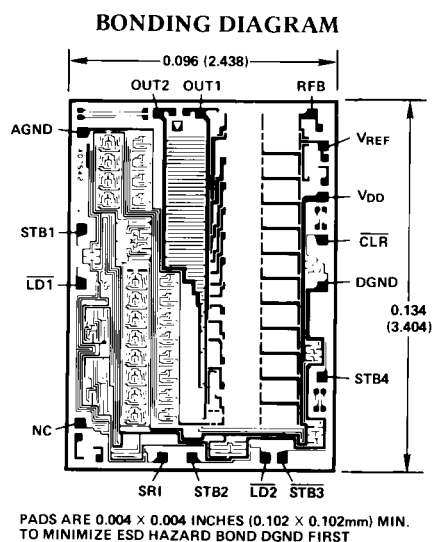
The data is presented serially on the SOD line and strobed into the AD7543 by executing memory write instructions. In this example the strobe signal (STB2) is supplied by decoding address 8000 and $\bar{W}R$. A memory write instruction to a different address (A000) loads the DAC Register with Register

A data. Table VI gives a listing of this procedure. Note, it is assumed that the required serial data is already present in right-justified format in Registers H and L when this procedure is implemented. Note that the sample routine of Table VI can be speeded up by replacing the SHIFT routine with a DAD H instruction.



LABEL	MNEMONIC	OPERAND	COMMENT
LOOP	MVI	B, 05	Shift Data Up to Most Significant Segment of HL with MSB as Carry
	CALL	SHIFT	
	DCR	B	
	JNZ	LOOP	
LUP	MVI	B, 0C	SOD Enable in ACC Shift in MSB of H Set Interrupt Mask Strobe Data into AD7543 Get Next Bit into Carry Go Back if Not Finished Load DAC Register of AD7543
	MVI	A, 80	
	RAR		
	SIM		
	STA	8000	
	CALL	SHIFT	
	DCR	B	
	JNZ	LUP	
SHIFT	STA	A000	Return to Main Program Shift H and L Left One Place and Leave Uppermost Bit of H in Carry
	RET		
	MOV	A, L	
	RAL		
	MOV	L, A	
	MOV	A, H	
	RAL		
	MOV	H, A	
	RET		

Table VI. Sample Routine for AD7543-8085 Interface



**PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm) MIN.
TO MINIMIZE ESD HAZARD BOND DGND FIRST**

Dimensions shown in inches and (mm).

Figure 1: Dimensions of Lead No. 1. The diagram shows three views of a lead: a top view, a side view, and an end view. The top view shows a rectangular lead with a central slot and two side slots. The side view shows the lead's profile with a 15-degree angle. The end view shows the lead's cross-section with a central slot and two side slots. Dimensions are given in inches and millimeters.

View	Dimension	Value (inches)	Value (millimeters)
Top View	Overall Width	0.26	6.61
	Slot Width	0.24	6.1
	Slot Depth	0.755	19.18
	Slot Depth	0.745	18.93
	Slot Depth	0.17	4.32
	Slot Depth	MAX	
	Slot Depth	0.065	1.66
	Slot Depth	0.02	0.508
	Slot Depth	0.105	2.67
	Slot Depth	0.045	1.16
Side View	Overall Width	0.306	7.78
	Slot Width	0.294	7.47
	Slot Depth	0.14	3.56
	Slot Depth	0.12	3.05
	Slot Depth	15°	
	Slot Depth	0°	
	Slot Depth	0.012	0.305
	Slot Depth	0.008	0.203
	Slot Depth	0.175	4.45
	Slot Depth	0.12	3.05
End View	Overall Width	0.065	1.66
	Slot Width	0.02	0.508
	Slot Depth	0.105	2.67
	Slot Depth	0.045	1.16
	Slot Depth	0.015	0.381
	Slot Depth	0.095	2.42
	Slot Depth	0.012	0.305
	Slot Depth	0.008	0.203
	Slot Depth	0.175	4.45
	Slot Depth	0.12	3.05

LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
 2. LEADS WILL BE EITHER GOLD OR TIN PLATED
 IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

Technical drawing showing the bottom view of a square component. The drawing includes the following dimensions and tolerances:

- Top horizontal dimension: 0.082 ± 0.018 (2.085 $\pm$ 0.455)
- Top horizontal dimension: 0.350 ± 0.008 (8.89 $\pm$ 0.20)
- Top horizontal dimension: $0.040 \times 45^\circ$ (1.02 $\times$ 45°) REF 3 PLCS
- Right vertical dimension: 0.025 ± 0.003 (0.635 $\pm$ 0.075)
- Right vertical dimension: $0.020 \times 45^\circ$ (0.51 $\times$ 45°) REF
- Bottom horizontal dimension: 0.050 (1.27)
- Internal feature: NO. 1 PIN INDEX
- Feature: SQ
- View label: BOTTOM VIEW