AD7249–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V, REFIN = +5 V, R_L = 2 kΩ, C_L = 100 pF to AGND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[2]	B Version[2]	S Version[2]	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±5	±5	±6	LSB max	V_{SS} = 0 V or –12 V to –15 V[1]; DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±5	±7	LSB max	V_{SS} = –12 V to –15 V[1] DAC Latch Contents All 0s
Full-Scale Error[3, 4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔV_{REFOUT} vs. I_L)	–1	–1	–1	mV max	Reference Load Current (I_L) Change (0 μA–100 μA)
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current	5	5	5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN}	±1	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistor, R_{OFSA} & R_{OFSB}	15/30	15/30	15/30	kΩ min/ max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = –12 V or –15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	10	μs max	Typically 3 μs
Negative Full-Scale Change	10	10	10	μs max	Typically 5 μs
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	1 LSB Change Around Major Carry
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	10	10	10	nV secs typ	
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range (Dual Supplies)	–10.8/–16.5	–11.4/–15.75	–11.4/–15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded; Typically 11 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded; Typically 3 mA

NOTES
[1]Power supply tolerance, A Version: ±10%; B, S Versions: ±5%.
[2]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[3]See Terminology.
[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.
[5]Guaranteed by design not production tested.
[6]0 V to 10 V output range available only with $V_{DD} \geq 14.25$ V.
Specifications subject to change without notice.

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TIMING CHARACTERISTICS[1, 2] (V_{DD} = +12 V to +15 V,[3] V_{SS} = 0 V or –12 V to –15 V,[3] AGND = DGND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (All Versions)	Unit	Conditions/Comments
t_1[4]	200	ns min	SCLK Cycle Time
t_2	15	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_3	50	ns min	$\overline{SYNC}$ to SCLK Hold Time
t_4	0	ns min	Data Setup Time
t_5	150	ns min	Data Hold Time
t_6	0	ns min	$\overline{SYNC}$ High to $\overline{LDAC}$ Low
t_7	20	ns min	$\overline{LDAC}$ Pulsewidth
t_8	0	ns min	$\overline{LDAC}$ High to $\overline{SYNC}$ Low
t_9	50	ns min	$\overline{CLR}$ Pulsewidth
t_{10}	20	ns min	$\overline{SYNC}$ High Time

NOTES
[1]Timing specifications guaranteed by design not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]See Figure 8.
[3]Power supply tolerance, A Version: ±10%; B, S Versions: ±5%.
[4]SCLK Mark/Space Ratio range is 45/55 to 55/45.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND, DGND . . . . . –0.3 V to +17 V
V_{SS} to AGND, DGND . . . . . +0.3 V to –17 V
AGND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
$V_{OUTA, B}$[2] to AGND . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
REFOUT to AGND . . . . . 0 V to V_{DD}
REFIN to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (A, B Versions) . . . . . –40°C to +85°C
  Extended (S Version) . . . . . –55°C to +125°C
Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Power Dissipation Plastic DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . +117°C/W
  Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation, Cerdip . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 76°C/W
  Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation, SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 75°C/W
  Lead Temperature (Soldering)
    Vapor Phase (60 secs) . . . . . +215°C
    Infrared (15 secs) . . . . . +220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any time.
[2]The outputs may be shorted to voltages in this range provided the power dissipation of the package is not exceeded.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7249 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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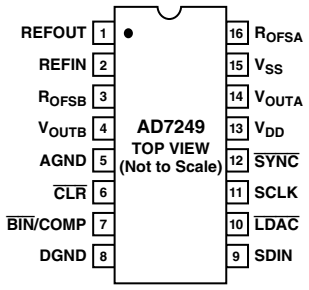
PIN FUNCTION DESCRIPTION (DIP & SOIC PIN NUMBERS)

Pin	Mnemonic	Description
1	REFOUT	Voltage Reference Output. The internal 5 V analog reference is provided at this pin. To operate the part using its internal reference, REFOUT should be connected to REFIN.
2	REFIN	Voltage Reference Input. It is internally buffered before being applied to both DACs. The nominal reference voltage for specified operation of the AD7249 is 5 V.
3	R_{OFSB}	Output Offset Resistor for the amplifier of DAC B. It is connected to V_{OUTB} for the +5 V range, to AGND for the +10 V range and to REFIN for the –5 V to +5 V range.
4	V_{OUTB}	Analog Output Voltage of DAC B. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and –5 V to +5 V.
5	AGND	Analog Ground. Ground reference for all analog circuitry.
6	$\overline{CLR}$	Clear, Logic Input. Taking this input low clears both DACs. It sets V_{OUTA} and V_{OUTB} to 0 V in both unipolar ranges and the twos complement bipolar range and to –REFIN in the offset binary bipolar range.
7	$\overline{BIN}$/COMP	Logic Input. This input selects the data format to be either binary or twos complement. In both unipolar ranges natural binary format is selected by connecting this input to a Logic "0". In the bipolar configuration offset binary format is selected with a Logic "0" while a Logic "1" selects twos complement.
8	DGND	Digital Ground. Ground reference for all digital circuitry.
9	SDIN	Serial Data In, Logic Input. The 16-bit serial data word is applied to this input.
10	$\overline{LDAC}$	Load DAC, Logic Input. Updates both DAC outputs. The DAC outputs are updated on the falling edge of this signal or alternatively if this line is permanently low, an automatic update mode is selected whereby both DACs are updated on the 16th falling SCLK pulse.
11	SCLK	Serial Clock, Logic Input. Data is clocked into the input register on each falling SCLK edge.
12	$\overline{SYNC}$	Data Synchronization Pulse, Logic Input. Taking this input low initializes the internal logic in readiness for a new data word.
13	V_{DD}	Positive Power Supply.
14	V_{OUTA}	Analog Output Voltage of DAC A. This is the buffer amplifier output voltage. Three different output voltage ranges can be chosen: 0 V to +5 V, 0 V to +10 V and –5 V to +5 V.
15	V_{SS}	Negative Power Supply (used for the output amplifier only) may be connected to 0 V for single supply operation or –12 V to –15 V for dual supplies.
16	R_{OFSA}	Output Offset Resistor for the amplifier of DAC A. It is connected to V_{OUTA} for the +5 V range, to AGND for the +10 V range and to REFIN for the –5 V to +5 V range.

PIN CONFIGURATIONS
(DIP and SOIC)



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TERMINOLOGY

Bipolar Zero Error

Bipolar Zero Error is the voltage measured at V_{OUT} when the DAC is configured for bipolar output and loaded with all 0s (Twos Complement Coding) or with 1000 0000 0000 (Offset Binary Coding). It is due to a combination of offset errors in the DAC, amplifier and mismatch between the internal gain resistors around the amplifier.

Full-Scale Error

Full-Scale Error is a measure of the output error when the amplifier output is at full scale (for the bipolar output range full scale is either positive or negative full scale). It is measured with respect to the reference input voltage and includes the offset errors.

Digital-to-Analog Glitch Impulse

This is the voltage spike that appears at V_{OUT} when the digital code in the DAC Latch changes, before the output settles to its final value. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is changed by 1 LSB at the major carry transition (0111 1111 1111 to 1000 0000 0000 or 1000 0000 0000 to 0111 1111 1111).

Digital Feedthrough

This is a measure of the voltage spike that appears on V_{OUT} as a result of feedthrough from the digital inputs on the AD7249. It is measured with $\overline{LDAC}$ held high.

Relative Accuracy (Linearity)

Relative Accuracy, or endpoint linearity, is a measure of the maximum deviation of the DAC transfer function from a straight line passing through the endpoints of the transfer function. It is measured after allowing for zero and full-scale errors and is expressed in LSBs or as a percentage of full-scale reading.

Single Supply Linearity and Gain Error

The output amplifier on the AD7249 can have true negative offsets even when the part is operated from a single +15 V supply. However, because the negative supply rail (V_{SS}) is 0 V, the output cannot actually go negative. Instead, when the output offset voltage is negative, the output voltage sits at 0 V, resulting in the transfer function shown in Figure 1.

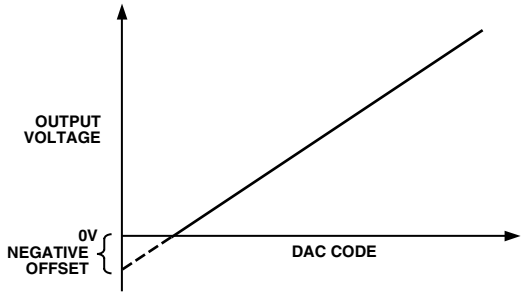

Figure 1. Effect of Negative Offset (Single Supply)

This "knee" is an offset effect, not a linearity error, and the transfer function would have followed the dotted line if the output voltage could have gone negative.

Normally, linearity is measured between zero (all 0s input code) and full scale (all 1s input code) after offset and full scale have been adjusted out or allowed for, but this is not possible in single supply operation if the offset is negative, due to the knee in the transfer function. Instead, linearity of the AD7249 in the unipolar mode is measured between full scale and the lowest code which is guaranteed to produce a positive output voltage. This code is calculated from the maximum specification for negative offset. For the A and B versions, the linearity is measured between Codes 3 and 4095. For the S grade, linearity is measured between Code 5 and Code 4095.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB or less over the operating temperature range ensures monotonicity.

Unipolar Offset Error

Unipolar Offset Error is the measured output voltage from V_{OUT} with all zeros loaded into the DAC latch, when the DAC is configured for unipolar output. It is due to a combination of the offset errors in the DAC and output amplifier.

CIRCUIT INFORMATION

D/A Section

The AD7249 contains two 12-bit voltage-mode D/A converters consisting of highly stable thin film resistors and high-speed NMOS single-pole, double-throw switches. The simplified circuit diagram for the DAC section is shown in Figure 2. The output voltage from the converter has the same polarity as the reference voltage, REFIN, allowing single supply operation.

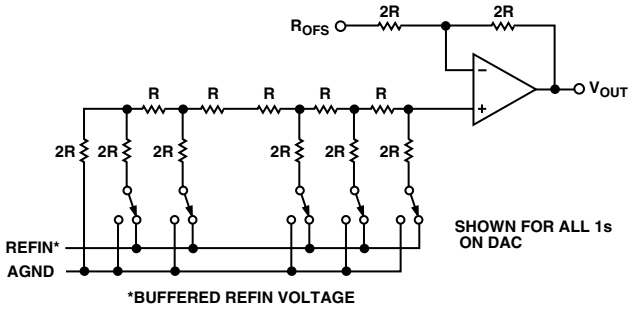

Figure 2. D/A Simplified Circuit Diagram

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Internal Reference

The AD7249 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 5 V ± 50 mV. The reference voltage is provided at the REFOUT pin. This reference can be used to provide the reference voltage for the D/A converter by connecting the REFOUT pin to the REFIN pin.

The reference voltage can also be used as a reference for other components and is capable of providing up to 500 μA to an external load. The maximum recommended capacitance on REFOUT for normal operation is 50 pF. If the reference output is required to drive a capacitive load greater than 50 pF, then a 200 Ω resistor should be placed in series with the capacitive load. Figure 3 shows the suggested REF OUT decoupling scheme, a 200 Ω resistor and the parallel combination of a 10 μF tantalum and a 0.1 μF ceramic capacitor. This decoupling scheme reduces the noise spectral density of the reference.

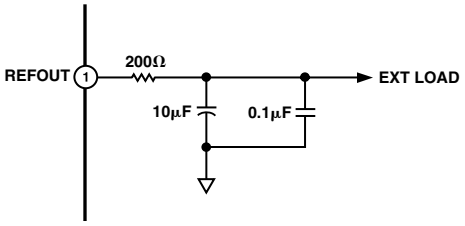

Figure 3. Reference Decoupling Scheme

External Reference

In some applications, the user may require a system reference or some other external reference to drive the AD7249. References such as the AD586 provide an ideal external reference source (See Figure 10). The REFIN voltage is internally buffered by a unity gain amplifier before being applied to the D/A converter. The D/A converter is scaled for a 5 V reference and the device is tested with 5 V applied to REFIN. Other reference voltages may be used with degraded performance. Figure 4 shows the degradation in linearity vs. REFIN.

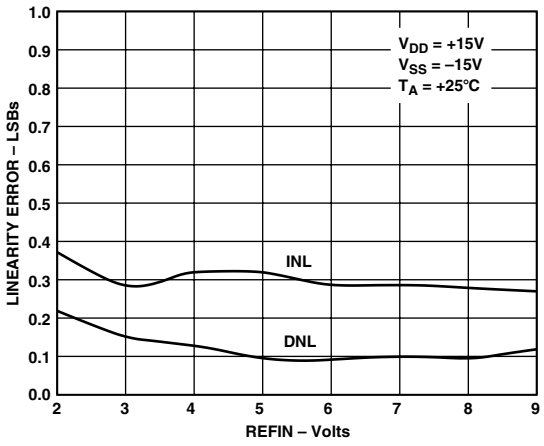

Figure 4. Linearity vs. REFIN Voltage

Op Amp Section

The output of the voltage-mode D/A converter is buffered by a noninverting CMOS amplifier. The R_{OFS} input allows three output voltage ranges to be selected. The buffer amplifier is capable of developing +10 V across a 2 kΩ load to AGND.

The output amplifier can be operated from a single +15 V supply by tying V_{SS} = 0 V.

The amplifier can also be operated from dual supplies to allow an additional bipolar output range of –5 V to +5 V. Dual supplies are necessary for the bipolar output range but can also be used for the unipolar ranges to give faster settling time to voltages near 0 V, to allow full sink capability of 2.5 mA over the entire output range and to eliminate the effects of negative offsets on the transfer characteristic (outlined previously). A plot of the output sink capability of the amplifier is shown in Figure 5.

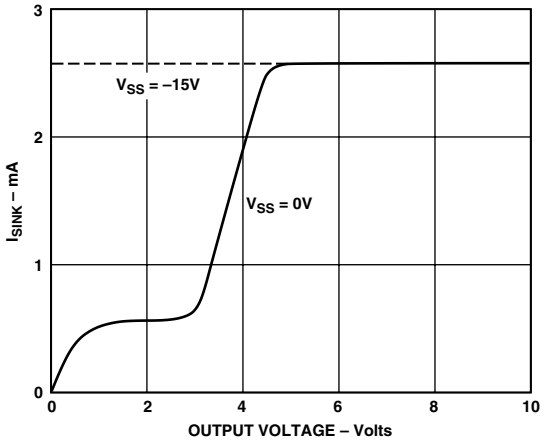

Figure 5. Amplifier Sink Current

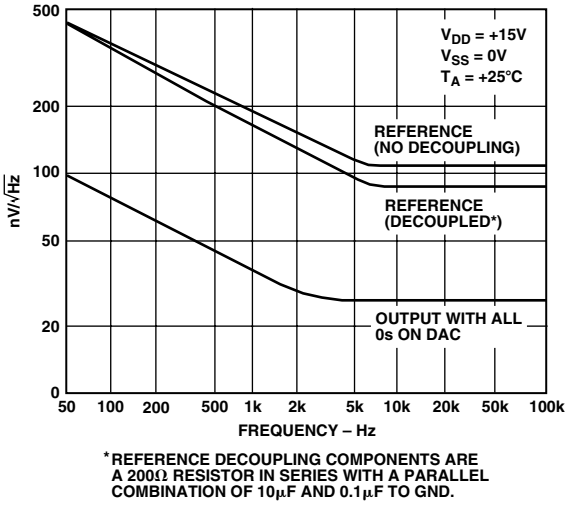

Figure 6. Noise Spectral Density vs. Frequency

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DIGITAL INTERFACE

The AD7249 contains an input serial to parallel shift register and a DAC latch for both DAC A and DAC B. A simplified diagram of the input loading circuitry is shown in Figure 7. Serial data on the SDIN input is loaded to the input register under control of $\overline{SYNC}$ and SCLK. The $\overline{SYNC}$ input provides the frame synchronization signal which tells the AD7249 that valid serial data on the SDIN input will be available for the next 16 falling edges of SCLK. An internal counter/decoder circuit provides a low gating signal so that only 16 data bits are clocked into the input shift register. After 16 SCLK pulses the internal gating signal goes inactive (high) thus locking out any further clock pulses. Therefore either a continuous clock or a burst clock source may be used to clock in the data. The $\overline{SYNC}$ input is taken high after the complete 16-bit word is loaded in.

DAC selection is accomplished using the thirteenth bit (DB12) of the serial data input stream. A zero in DB12 will select DAC A while a one in this position selects DAC B. Although 16 bits of data are clocked into the input register, only 12 bits get transferred into the DAC latch. The relevant DAC latch is determined by the value of the thirteenth bit and the first three bits in the 16-bit stream are don't cares. Therefore, the data format is three don't cares followed by the DAC selection bit and the 12-bit data word with the LSB as the last bit in the serial stream.

There are two ways in which a DAC latches and hence the analog outputs may be updated. The status of the $\overline{LDAC}$ input is examined after $\overline{SYNC}$ is taken low. Depending on its status, one of two update modes are selected.

If $\overline{LDAC}$ = 0, then the automatic update mode is selected. In this mode the DAC latch and analog output are updated automatically when the last bit in the serial data stream is clocked in. The update thus takes place on the sixteenth falling SCLK edge.

If $\overline{LDAC}$ = 1, then the automatic update is disabled and both DAC latches are updated by taking $\overline{LDAC}$ low any time after the 16-bit data transfer is complete. The update now occurs on the falling edge of $\overline{LDAC}$. Note that the $\overline{LDAC}$ input must be taken back high again before the next data transfer is initiated. When a complete word is held in the shift register it may then be loaded into the DAC latch under control of $\overline{LDAC}$.

Clear Function ($\overline{CLR}$)

The clear function clears the contents of the input shift register and loads both DAC latches with all 0s. It is activated by taking $\overline{CLR}$ low. In all ranges except the Offset Binary bipolar range (–5 V to +5 V) the output voltage is reset to 0 V. In the offset binary bipolar range the output is set to –REFIN. The clear function is especially useful at power-up as it enables the output to be reset to a known state.

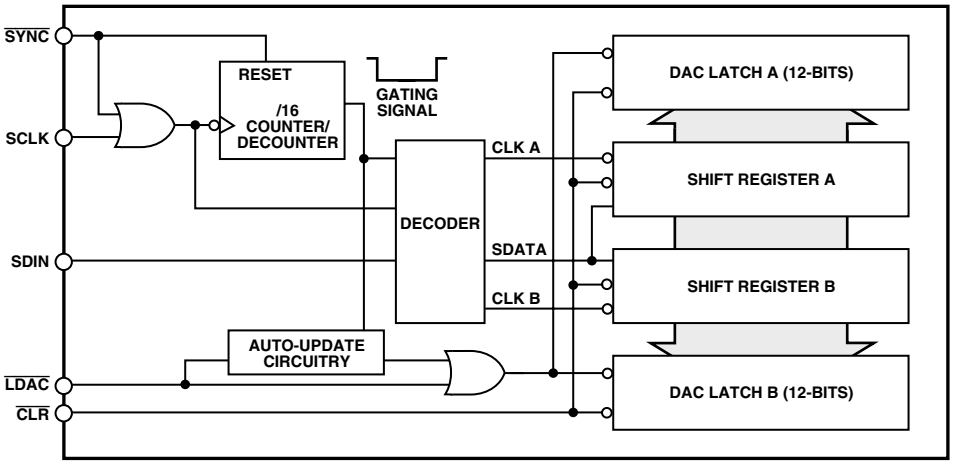

Figure 7. Simplified Loading Structure

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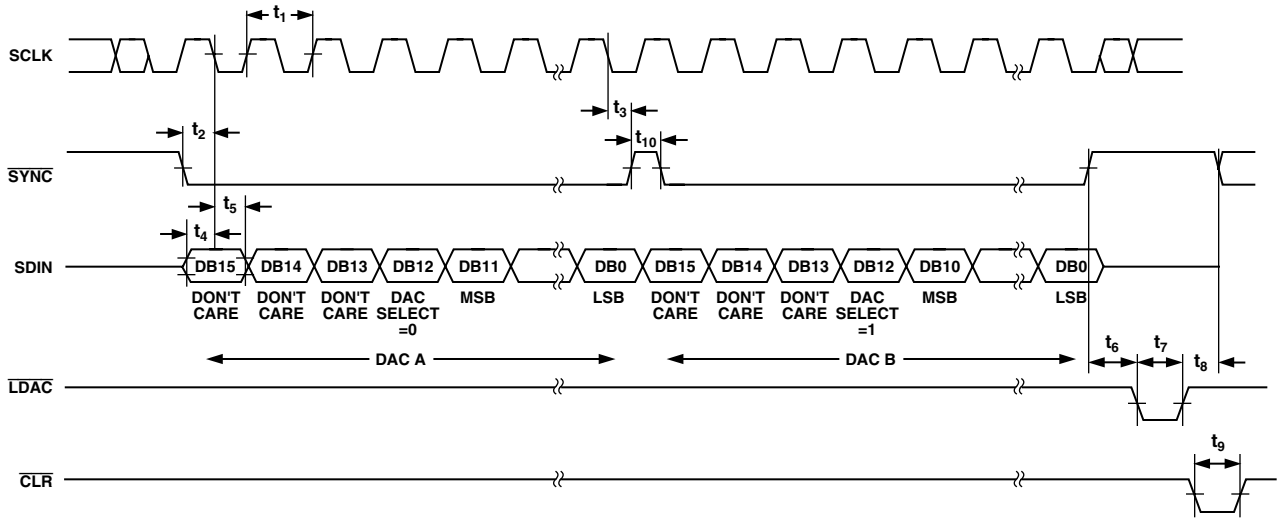

Figure 8. Timing Diagram

TRANSFER FUNCTION

The internal scaling resistors provided on the AD7249 allow several output voltage ranges. The part can produce unipolar output ranges of 0 V to +5 V or 0 V to +10 V and a bipolar output range of ±5 V. Connections for the various ranges are outlined below. Since each DAC has its own R_{OFS} input the two DACs can be set up for different output ranges.

Unipolar (0 V to +10 V) Configuration

The first of the configurations provides an output voltage range of 0 V to +10 V. This is achieved by connecting the output offset resistor R_{OFSA}, R_{OFSB} (Pin 3, 16) to AGND. Natural Binary data format is selected by connecting $\overline{BIN}$/COMP (Pin 7) to DGND. In this configuration, the AD7249 can be operated using either single or dual supplies. Note that the V_{DD} supply is restricted to +15 V ± 10% for this range in order to maintain sufficient amplifier headroom. Dual supplies may be used to improve settling time and give increased current sink capability for the amplifier. Figure 9 shows the connection diagram for unipolar operation of the AD7249. Table I shows the digital code vs. analog output for this configuration.

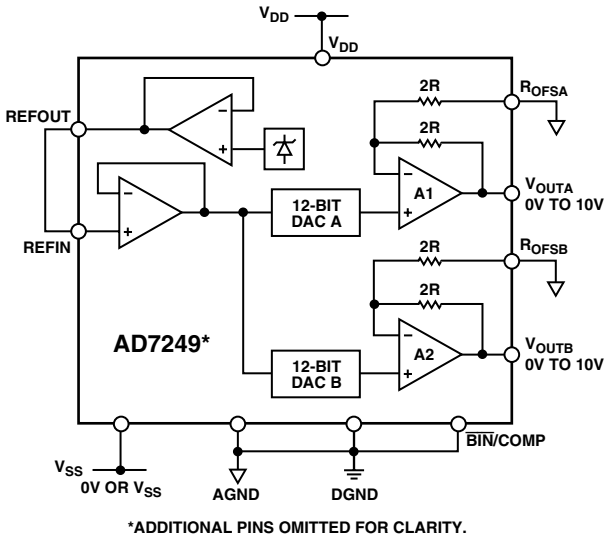

Figure 9. Unipolar (0 V to +10 V) Configuration

Unipolar (0 V to +5 V) Configuration

The 0 V to +5 V output voltage range is achieved by tying R_{OFSA} to V_{OUTA} or R_{OFSB} to V_{OUTB}. Once again, the AD7249 can be operated using either single or dual supplies. The table for output voltage versus digital code is as in Table I, with 2REFIN replaced by REFIN. Note, for this range, 1 LSB = REFIN × (2^{-12}) = (REFIN/4096).

Table I. Unipolar Code Table (0 V to +10 V Range)

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXY 1111 1111 1111	+2REFIN × (4095/4096)
XXXY 1000 0000 0001	+2REFIN × (2049/4096)
XXXY 1000 0000 0000	+2REFIN × (2048/4096) = +REFIN
XXXY 0111 1111 1111	+2REFIN × (2047/4096)
XXXY 0000 0000 0001	+2REFIN × (1/4096)
XXXY 0000 0000 0000	0 V

X = Don't Care.
Y = DAC Select Bit, 0 = DAC A, 1= DAC B.
Note: 1 LSB = 2REFIN/4096.

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Bipolar (±5 V) Configuration
The bipolar configuration for the AD7249, which gives an output range of –5 V to +5 V, is achieved by connecting R_{OFSA}, R_{OFSB} to V_{REFIN}. The AD7249 must be operated from dual supplies to achieve this output voltage range. Either offset binary or twos complement coding may be selected. Figure 10 shows the connection diagram for bipolar operation. An AD586 provides the reference voltage for the DAC but this could be provided by the on-chip reference by connecting REFOUT to REFIN.

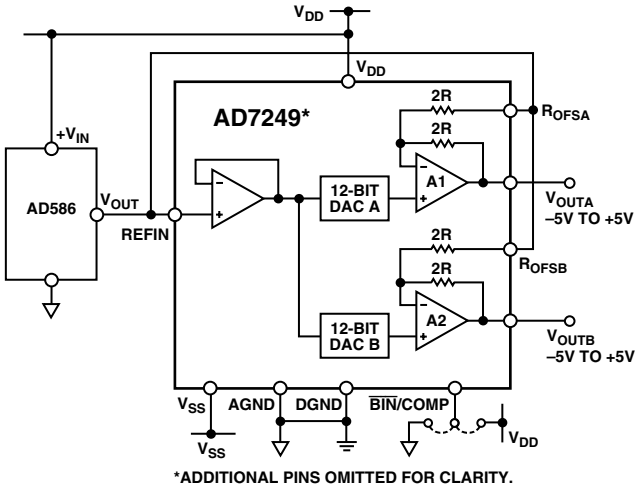

Figure 10. Bipolar Configuration with External Reference

Bipolar Operation (Twos Complement Data Format)
The AD7249 is configured for twos complement data format by connecting $\overline{\text{BIN}}$/COMP (Pin 7) high. The analog output vs. digital code is shown in Table II.

Table II. Twos Complement Bipolar Code Table

Input Data Word MSB LSB	Analog Output, V_{OUT}
XXXY 0111 1111 1111	+REFIN × (2047/2048)
XXXY 0000 0000 0001	+REFIN × (1/2048)
XXXY 0000 0000 0000	0 V
XXXY 1111 1111 1111	–REFIN × (1/2048)
XXXY 1000 0000 0001	–REFIN × (2047/2048)
XXXY 1000 0000 0000	–REFIN × (2048/2048) = –REFIN

X = Don't Care.
Y = DAC Select Bit, 0 = DAC A, 1 = DAC B.
Note: 1 LSB = REFIN/2048.

Bipolar Operation (Offset Binary Data Format)
The AD7249 is configured for Offset Binary data format by connecting $\overline{\text{BIN}}$/COMP (Pin 7) low. The analog output vs. digital code may be obtained by inverting the MSB in Table II.

APPLYING THE AD7249
Good printed circuit board layout is as important as the overall circuit design itself in achieving high speed converter performance. The AD7249 works on an LSB size of 2.44 mV for the unipolar 0 V to 10 V range and the bipolar ±5 V range, when using the unipolar 0 V to 5 V range the LSB size is 1.22 mV. Therefore the designer must be conscious of minimizing noise in both the converter itself and in the surrounding circuitry. Switching mode power supplies are not recommended as switching spikes can feedthrough to the on-chip amplifier. Other causes of concern are ground loops and feedthrough from microprocessors. These are factors which influence any high performance converter, and proper printed circuit board layout which minimizes these effects is essential to obtain high performance.

LAYOUT HINTS
Ensure that the layout has the digital and analog tracks separated as much as possible. Take care not to run any digital track alongside an analog signal track. Establish a single point analog ground separate from the logic system ground. Place this star ground as close as possible to the AD7249. Connect all analog grounds to this star point and also connect the AD7249 DGND pin to this point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential for low noise operation of high performance converters. To accomplish this track widths should be kept a wide as possible and also the use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

NOISE
Keep the signal leads on the V_{OUTA} and V_{OUTB} signals and the signal return leads to AGND as short as possible to minimize noise coupling. In applications where this is not possible use a shielded cable between the DAC outputs and their destination. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the DAC and its destination device appears as an error voltage in series with the DAC output.

Power Supply Decoupling
To achieve optimum performance when using the AD7249, the V_{DD} and V_{SS} lines should be decoupled to AGND using 0.1 µF capacitors. In noisy environments it is recommended that 10 µF capacitors be connected in parallel with the 0.1 µF capacitors.

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MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD7249 is via a serial bus which uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a three-wire interface consisting of a clock signal, a data signal and a synchronization signal. The AD7249 requires a 16-bit data word with data valid on the falling edge of SCLK. For all the interfaces, the DAC update may be done automatically when all the data is clocked in or it may be done under control of $\overline{\text{LDAC}}$.

Figures 11 to 15 show the AD7249 configured for interfacing to a number of popular DSP processors and microcontrollers.

AD7249–ADSP-2101/ADSP-2102 Interface

Figure 11 shows a serial interface between the AD7249 and the ADSP-2101/ADSP-2102 DSP processor. The ADSP-2101/ ADSP-2102 contains two serial ports and either port may be used in the interface. The data transfer is initiated by $\overline{\text{TFS}}$ going low. Data from the ADSP-2101/ADSP-2102 is clocked into the AD7249 on the falling edge of SCLK. DB12 of the 16-bit serial data stream selects the DAC to be updated. Both DACs can be updated by holding $\overline{\text{LDAC}}$ high while performing two write cycles to the DAC. $\overline{\text{TFS}}$ must be taken high after each 16 bit write cycle. $\overline{\text{LDAC}}$ is brought low at the end of the second cycle and both DAC outputs are updated together. In the interface shown the DAC is updated using an external timer which generates an $\overline{\text{LDAC}}$ pulse. This could also be done using a control or decoded address line from the processor. Alternatively, if the $\overline{\text{LDAC}}$ input is hardwired low the output update takes place automatically on the 16th falling edge of SCLK.

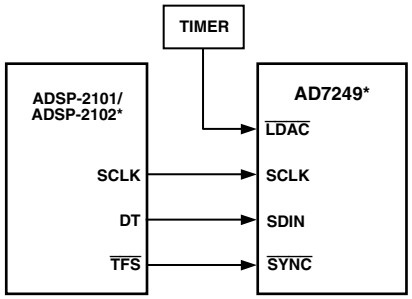

Figure 11. AD7249–ADSP-2101/ADSP-2102 Interface

AD7249–DSP56000 Interface

A serial interface between the AD7249 and the DSP56000 is shown in Figure 12. The DSP56000 is configured for Normal Mode Asynchronous operation with Gated Clock. It is also set up for a 16-bit word with SCK and SC2 as outputs and the FSL control bit set to a "0." SCK is internally generated on the DSP56000 and applied to the AD7249 SCLK input. Data from the DSP56000 is valid on the falling edge of SCK. The SC2 output provides the framing pulse for valid data. This line must be inverted before being applied to the $\overline{\text{SYNC}}$ input of the AD7249.

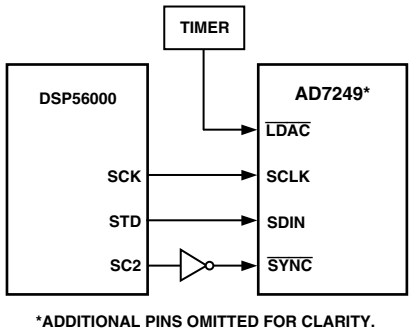

Figure 12. AD7249–DSP56000 Interface

In this interface an external $\overline{\text{LDAC}}$ pulse generated from an external timer is used to update the outputs of the DACs. This update can also be produced using a bit programmable control line from the DSP56000.

AD7249–TMS32020 Interface

Figure 13 shows a serial interface between the AD7249 and the TMS32020 DSP processor. In this interface, the CLKX and FSX signals for the TMS32020 should be generated using external clock/timer circuitry. The FSX pin of the TMS32020 must be configured as an input. Data from the TMS32020 is valid on the falling edge of CLKX.

The clock/timer circuitry generates the $\overline{\text{LDAC}}$ signal for the AD7249 to synchronize the update of the output with the serial transmission. Alternatively, the automatic update mode may be selected by connecting $\overline{\text{LDAC}}$ to DGND.

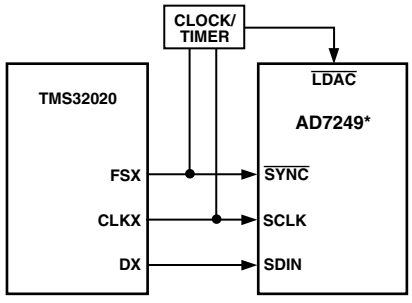

Figure 13. AD7249–TMS32020 Interface

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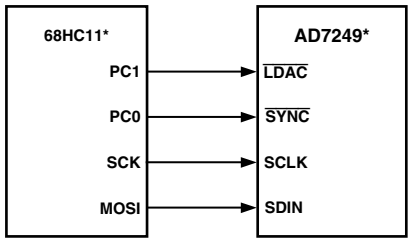
AD7249–68HC11 Interface

Figure 14 shows a serial interface between the AD7249 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7249 while the MOSI output drives the serial data line of the AD7249. The $\overline{SYNC}$ signal is derived from a port line (PC0 shown).

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transmitted to the part, PC0 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7249, PC0 is left low after the first eight bits are transferred and a second byte of data is then transferred serially to the AD7249. When the second serial transfer is complete, the PC0 line is taken high.

Figure 14 shows the $\overline{LDAC}$ input of the AD7249 being driven from another bit programmable port line (PC1). As a result, both DACs can be updated simultaneously by taking $\overline{LDAC}$ low after both DACs latches have updated.



*ADDITIONAL PINS OMITTED FOR CLARITY.

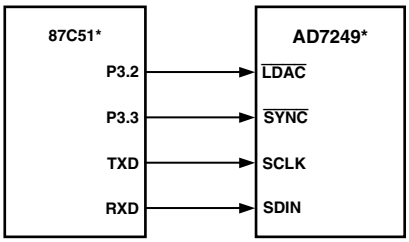
Figure 14. AD7249–68HC11 Interface

AD7249–87C51 Interface

A serial interface between the AD7249 and the 87C51 microcontroller is shown in Figure 15. TXD of the 87C51 drives SCLK of the AD7249 while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is derived from the port line P3.3 and the $\overline{LDAC}$ line is driven port line P3.2.

The 87C51 provides the LSB of its SBUF register as the first bit in the serial data stream. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that the don't care bits are the first to be transmitted to the AD7249 and the last bit to be sent is the LSB of the word to be loaded to the AD7249. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 87C51 transmits its serial data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. To load data to the AD7249, P3.3 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD7249 with DB12 used to select the appropriate DAC register. When the second serial transfer is complete, the P3.3 line is taken high and then taken low again to start the loading sequence to the second DAC (see timing diagram Figure 8).

Figure 15 shows the $\overline{LDAC}$ input of the AD7249 driven from the bit programmable port line P3.2. As a result, both DAC outputs can be updated simultaneously by taking the $\overline{LDAC}$ line low following the completion of the write cycle to the second DAC. Alternatively $\overline{LDAC}$ could be hardwired low and the analog output will be updated on the sixteenth falling edge of TXD after the $\overline{SYNC}$ signal for the DAC has gone low.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 15. AD7249–87C51 Interface

APPLICATIONS

OPTO-ISOLATED INTERFACE

In many process control type applications it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3 kΩ. The serial loading structure of the AD7249 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum.

Figure 16 shows a 2-channel isolated interface using the AD7249.

The sequence of events to program the output channels is as follows.

1. Take the $\overline{SYNC}$ line low.
2. Transmit the 16-bit word for DAC A (DB 12 of the 16-bit data word selects the DAC, DB12 = 0 to select DAC A) and bring the $\overline{SYNC}$ line high after the 16 bits have been transmitted.
3. Bring $\overline{SYNC}$ line low again and transmit 16 bits for DAC B, bring $\overline{SYNC}$ back high at end of transmission.
4. Pulse the $\overline{LDAC}$ line low. This updates both output channels simultaneously on the falling edge of $\overline{LDAC}$.

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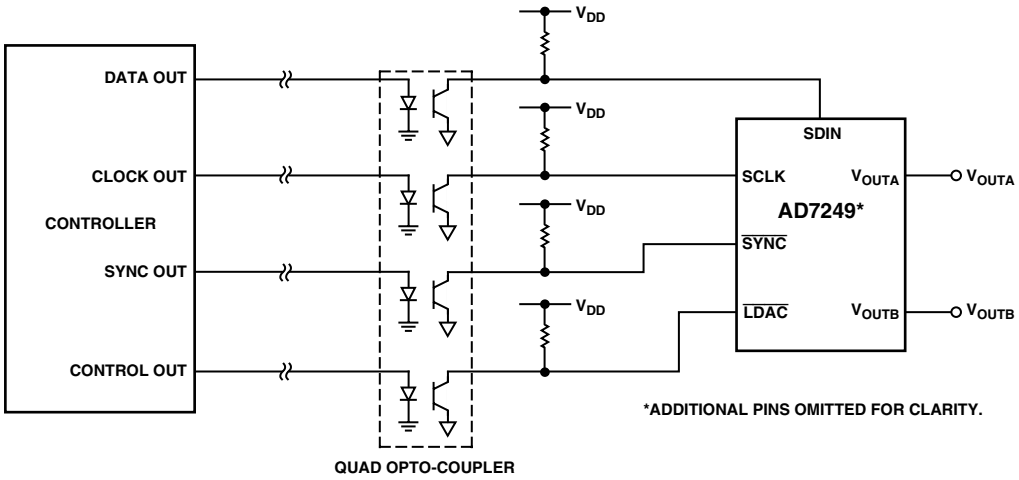

Figure 16. Opto-Isolated Interface

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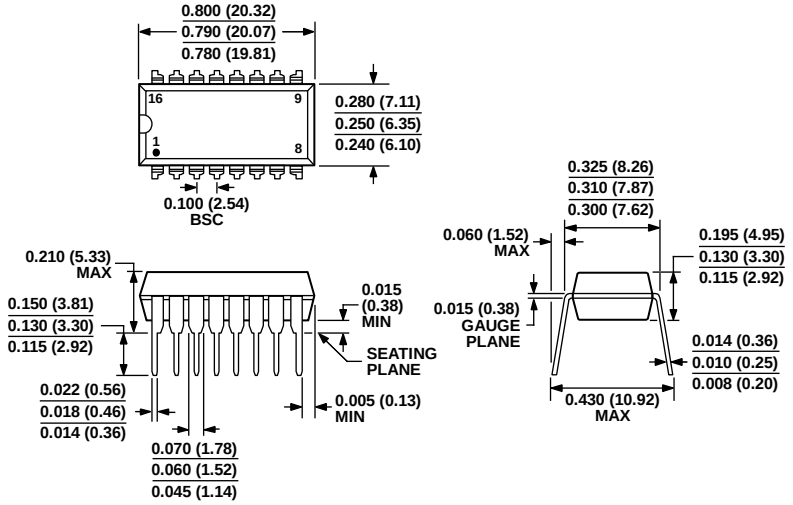
OUTLINE DIMENSIONS



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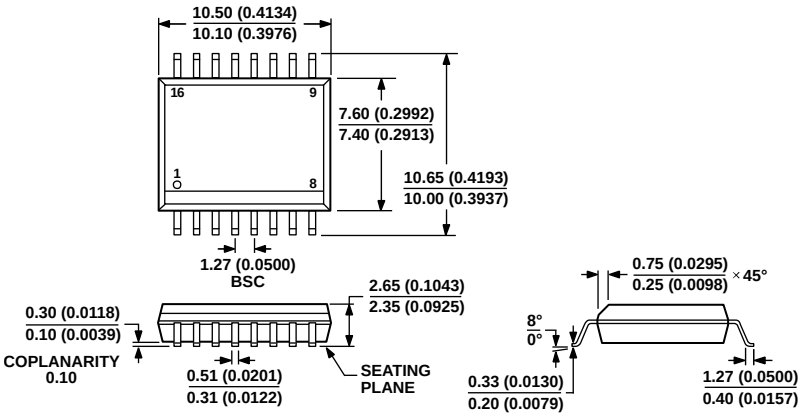
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 17. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)



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03-27-2007-B

Figure 18. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

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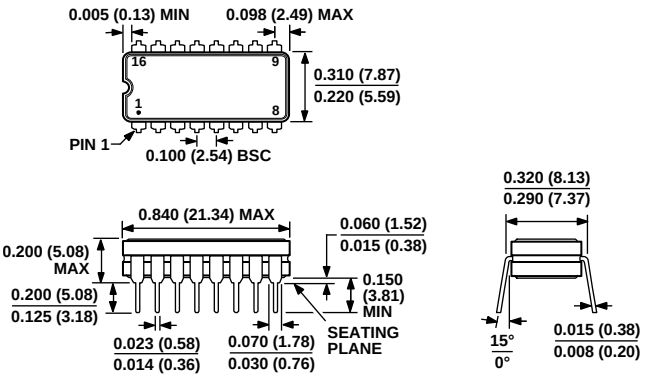

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Figure 19. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Description	Package Option
AD7249AN	–40°C to +85°C	±1 LSB	16-Lead PDIP	N-16
AD7249ANZ	–40°C to +85°C	±1 LSB	16-Lead PDIP	N-16
AD7249BNZ	–40°C to +85°C	±1/2 LSB	16-Lead PDIP	N-16
AD7249AR	–40°C to +85°C	±1 LSB	16-Lead SOIC_W	RW-16
AD7249AR-REEL	–40°C to +85°C	±1 LSB	16-Lead SOIC_W	RW-16
AD7249ARZ	–40°C to +85°C	±1 LSB	16-Lead SOIC_W	RW-16
AD7249ARZ-REEL	–40°C to +85°C	±1 LSB	16-Lead SOIC_W	RW-16
AD7249BR	–40°C to +85°C	±1/2 LSB	16-Lead SOIC_W	RW-16
AD7249BR-REEL	–40°C to +85°C	±1/2 LSB	16-Lead SOIC_W	RW-16
AD7249BRZ	–40°C to +85°C	±1/2 LSB	16-Lead SOIC_W	RW-16
AD7249BRZ-REEL	–40°C to +85°C	±1/2 LSB	16-Lead SOIC_W	RW-16
AD7249SQ	–55°C to +125°C	±1 LSB	16-Lead CERDIP	Q-16

[1] Z = RoHS Compliant Part.

REVISION HISTORY

10/13—Rev. C to Rev. D

Updated Outline Dimensions 13
Changes to Ordering Guide 14

6/00—Rev. B to Rev. C

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