AD582—SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6µs	•
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25µs	•
Aperture Delay, 20V p-p Input, Hold 0V	200ns	•
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	•
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5µs	•
Droop Current, Steady State, ±10V_{OUT}	100pA max	•
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	•
Sample to Hold Offset	0.5mV	•
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	•
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	•
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	•
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	•
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	•
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/µs	•
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	•
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	•
Output Short Circuit Current	±25mA	•
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	•
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3µA max (1.5µA typ)	•
Offset Current	300nA max (75nA typ)	•
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	•
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	•
Absolute Max Diff Input Voltage	30V	•
Absolute Max Input Voltage, Either Input	±V_S	•
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	•
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	•
+Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5µA	•
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	•
-Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	24µA	•
Sample Mode, +Logic @ 0V, -Logic @ 0V	4µA	•
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	•
Absolute Max Input Voltage, Either Input	±V_S	•
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	•
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	•
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	•
Lead Temperature (Soldering, 15 sec)	+300°C	•
PACKAGE OPTION[1,2]		
TO-100 (H-10A)	AD582KH	AD582SH
TO-116 (D-14)	AD582KD	AD582SD

NOTES
•Specifications same as AD582K.
[1]D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.
[2]For AD582/883B specifications, refer to Analog Devices Military Products Databook.
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

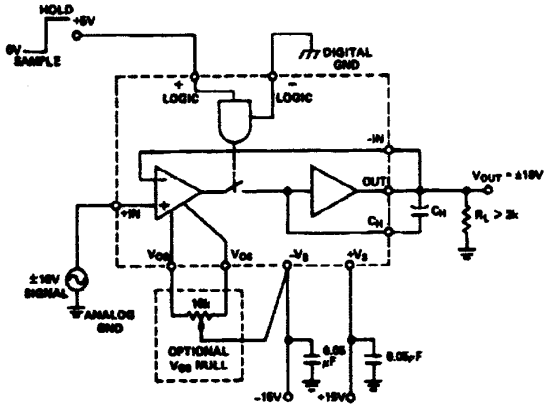


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

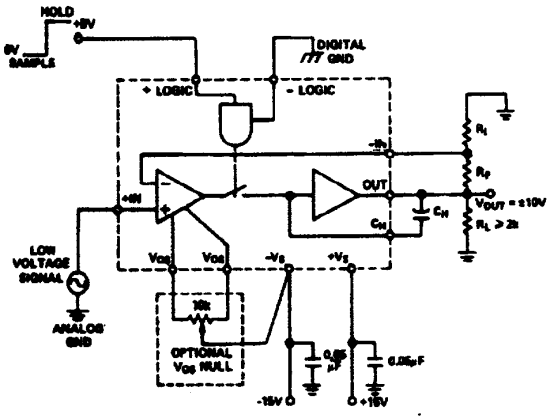


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

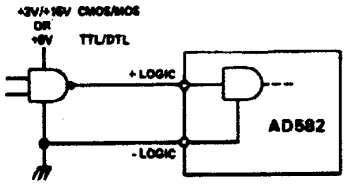


Figure 3A. Standard Logic Connection

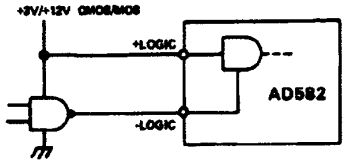


Figure 3B. Inverted Logic Sense Connection

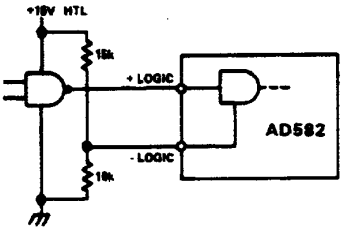


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

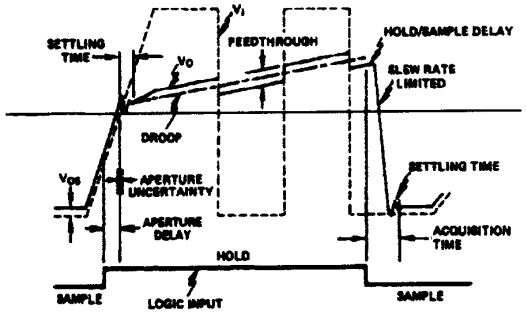


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Delay is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. The Aperture Time can be eliminated by advancing the sample-to-hold command 200ns with respect to the input signal. The Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(pA)}{C_H(pF)}$$

(See also Figure 6.)

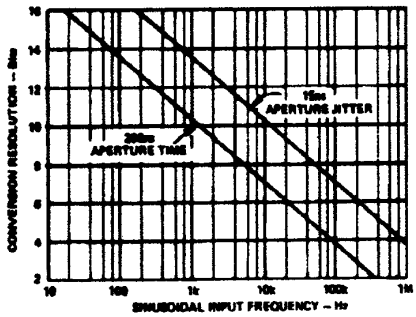


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

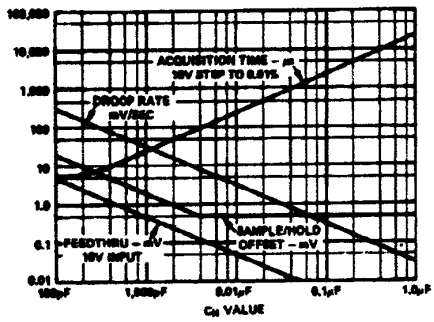


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Sample-to-Hold Offset is an output shift or step caused by charge injection into the hold capacitor as the device is switched from sample to hold. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H\ (pF)}$$

This offset also has a dc component as shown in Figure 6.

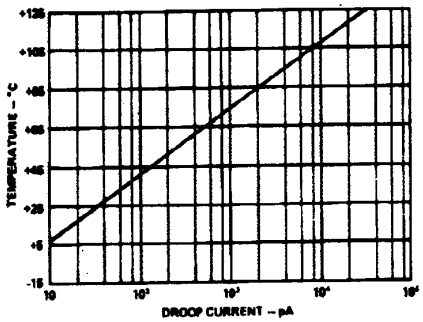
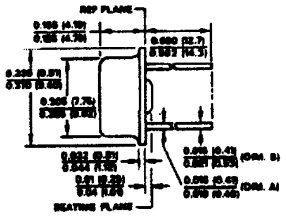


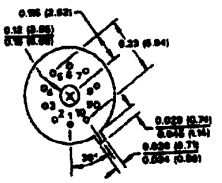
Figure 7. Droop Current vs. Temperature

OUTLINE DIMENSIONS

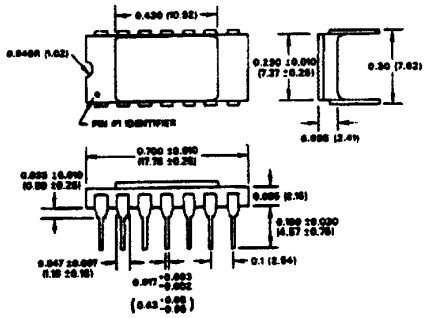
Dimensions shown in inches and (mm).

TO-100 "H"





TO-116 "D"



C538c–6–6/86

PRINTED IN U.S.A.