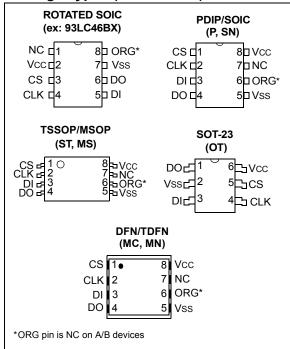
Package Types (not to scale)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Vcc	7.0V
All inputs and outputs w.r.t. Vss	0.6V to Vcc +1.0V
Storage temperature	65°C to +150°C
Ambient temperature with power applied	40°C to +125°C
ESD protection on all pins	≥ 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

		ly over the specified rwise noted.	Industrial Automotiv	. ,			°C, Vcc = +1.8V TO +5.5V 5°C, Vcc = +2.5V TO +5.5V
Param. No.	Symbol	Parameter	Min.	Тур	Max.	Units	Conditions
D1	VIH1 VIH2	High-level input voltage	2.0 0.7 Vcc		Vcc +1 Vcc +1	V	Vcc ≥ 2.7V Vcc < 2.7V
D2	VIL1 VIL2	Low-level input voltage	-0.3 -0.3	_	0.8 0.2 Vcc	V V	VCC ≥ 2.7V VCC < 2.7V
D3	Vol1 Vol2	Low-level output voltage	_	_	0.4 0.2	V	IOL = 2.1 mA, VCC = 4.5V IOL = 100 μ A, VCC = 2.5V
D4	VoH1 VoH2	High-level output voltage	2.4 VCC - 0.2	_	_	V V	IOH = -400 μ A, VCC = 4.5V IOH = -100 μ A, VCC = 2.5V
D5	ILI	Input leakage current	_	_	±1	μА	VIN = Vss or Vcc
D6	ILO	Output leakage current	_	_	±1	μА	Vout = Vss or Vcc
D7	CIN, COUT	Pin capacitance (all inputs/outputs)	_	_	7	pF	VIN/VOUT = 0V (Note 1) TA = 25°C, FCLK = 1 MHz
D8	Icc write	Write current	_	 500	2 —	mA μA	FCLK = 3 MHz, VCC = 5.5V FCLK = 2 MHz, VCC = 2.5V
D9	Icc read	Read current	_ _ _	_ _ 100	1 500 —	mA μA μA	FCLK = 3 MHz, VCC = 5.5V FCLK = 2 MHz, VCC = 3.0V FCLK = 2 MHz, VCC = 2.5V
D10	Iccs	Standby current		_	1 5	μA μA	I-Temp E-Temp CLK = CS = 0V ORG = DI = Vss or Vcc (Note 2) (Note 3)
D11	VPOR	Vcc voltage detect	_	1.5 3.8		V V	(Note 1) 93AA46A/B/C, 93LC46A/B/C 93C46A/B/C

Note 1: This parameter is periodically sampled and not 100% tested.

- 2: ORG pin not available on 'A' or 'B' versions.
- 3: Ready/Busy status must be cleared from DO; see Section 3.4 "Data Out (DO)".

TABLE 1-2: AC CHARACTERISTICS

		over the specified wise noted.	Industria Automo			0°C to +85°C, Vcc = +1.8V TO +5.5V 0°C to +125°C, Vcc = +2.5V TO +5.5V
Param. No.	Symbol	Parameter	Min.	Max.	Units	Conditions
A1	FCLK	Clock frequency	_	3 2 1	MHz MHz MHz	4.5V ≤ VCC < 5.5V, 93XX46C only 2.5V ≤ VCC < 5.5V 1.8V ≤ VCC < 2.5V
A2	Тскн	Clock high time	200 250 450	_	ns ns ns	4.5V ≤ VCC < 5.5V, 93XX46C only 2.5V ≤ VCC < 5.5V 1.8V ≤ VCC < 2.5V
A3	TCKL	Clock low time	100 200 450	_	ns ns ns	4.5V ≤ VCC < 5.5V, 93XX46C only 2.5V ≤ VCC < 5.5V 1.8V ≤ VCC < 2.5V
A4	Tcss	Chip Select setup time	50 100 250	_	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A5	Тсѕн	Chip Select hold time	0	_	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip Select low time	250	_	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data input setup time	50 100 250	_	ns	4.5V ≤ VCC < 5.5V, 93XX46C only 2.5V ≤ VCC < 5.5V 1.8V ≤ VCC < 2.5V
A8	TDIH	Data input hold time	50 100 250	_	ns	4.5V ≤ VCC < 5.5V, 93XX46C only 2.5V ≤ VCC < 5.5V 1.8V ≤ VCC < 2.5V
A9	TPD	Data output delay time		200 250 400	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	Tcz	Data output disable time	_	100 200	ns	4.5V ≤ VCC < 5.5V, (Note 1) 1.8V ≤ VCC < 4.5V, (Note 1)
A11	Tsv	Status valid time	_	200 300 500	ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A12	Twc	Program cycle time	_	6	ms	Erase/Write mode (AA and LC versions)
A13	Twc		_	2	ms	Erase/Write mode (93C versions)
A14	TEC			6	ms	ERAL mode, 4.5V ≤ Vcc ≤ 5.5V
A15	TWL		_	15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16	_	Endurance	1M	_	cycles	25°C, Vcc = 5.0V, (Note 2)

Note 1: This parameter is periodically sampled and not 100% tested.

^{2:} This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which may be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

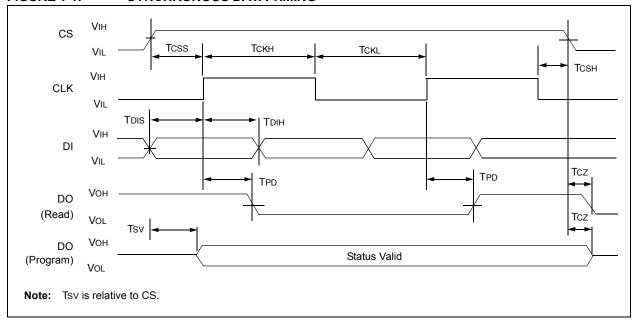


TABLE 1-3: INSTRUCTION SET FOR X16 ORGANIZATION (93XX46B OR 93XX46C WITH ORG = 1)

Instruction	SB	Opcode	Address			Data In	Data Out	Req. CLK Cycles			
ERASE	1	11	A5	A4	А3	A2	A1	A0	_	(RDY/BSY)	9
ERAL	1	00	1	0	X	X	X	X	_	(RDY/BSY)	9
EWDS	1	00	0	0	X	X	X	X	_	High-Z	9
EWEN	1	00	1	1	X	X	X	X	ı	High-Z	9
READ	1	10	A5	A4	A3	A2	A1	A0	_	D15 - D0	25
WRITE	1	01	A5	A4	А3	A2	A1	Α0	D15 - D0	(RDY/BSY)	25
WRAL	1	00	0	1	X	X	X	X	D15 - D0	(RDY/BSY)	25

TABLE 1-4: INSTRUCTION SET FOR X8 ORGANIZATION (93XX46A OR 93XX46C WITH ORG = 0)

Instruction	SB	Opcode		Address			Data In	Data Out	Req. CLK Cycles			
ERASE	1	11	A6	A5	A4	А3	A2	A1	A0	_	(RDY/BSY)	10
ERAL	1	00	1	0	X	X	X	X	X	_	(RDY/BSY)	10
EWDS	1	00	0	0	X	X	X	X	X	_	High-Z	10
EWEN	1	00	1	1	X	X	X	X	X	_	High-Z	10
READ	1	10	A6	A5	A4	А3	A2	A1	Α0		D7 - D0	18
WRITE	1	01	A6	A5	A4	A3	A2	A1	Α0	D7 - D0	(RDY/BSY)	18
WRAL	1	00	0	1	X	X	X	X	X	D7 - D0	(RDY/BSY)	18

2.0 FUNCTIONAL DESCRIPTION

When the ORG pin (93XX46C) is connected to Vcc, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High-Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High-Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note: When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active-high.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

All modes of operation are inhibited when Vcc is below a typical voltage of 1.5V for '93AA' and '93LC' devices or 3.8V for '93C' devices.

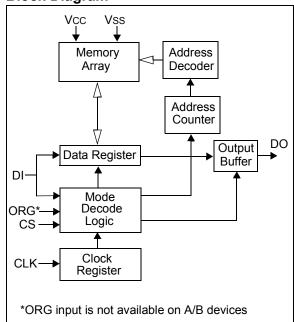
The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation and an external 10 k Ω pull-down protection resistor should be added

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

to the CS pin.

Block Diagram



2.4 Erase

The ERASE instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on '93C' devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TcsL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-1: ERASE TIMING FOR 93AA AND 93LC DEVICES

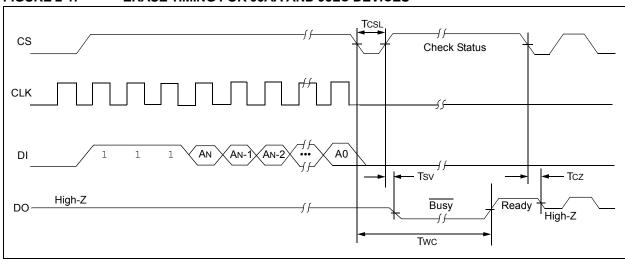
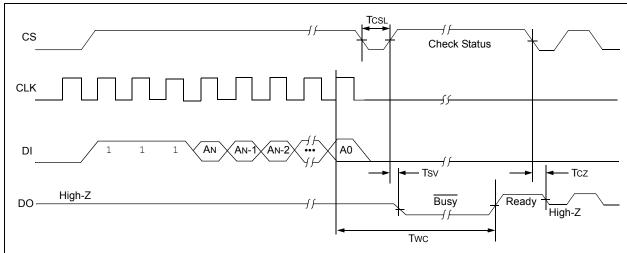


FIGURE 2-2: ERASE TIMING FOR 93C DEVICES



2.5 Erase All (ERAL)

The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on '93C' devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TcsL).

Note: After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

Vcc must be ≥4.5V for proper operation of ERAL.

FIGURE 2-3: ERAL TIMING FOR 93AA AND 93LC DEVICES

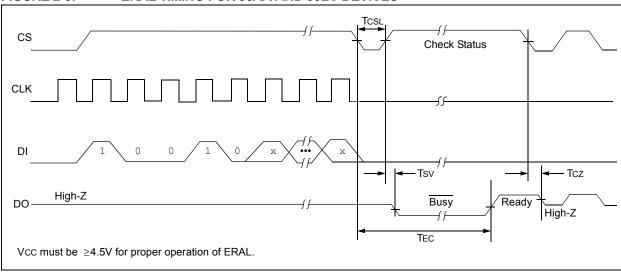
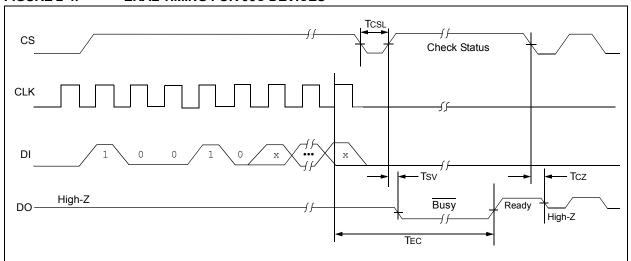


FIGURE 2-4: ERAL TIMING FOR 93C DEVICES



2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93XX46A/B/C powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains

enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.



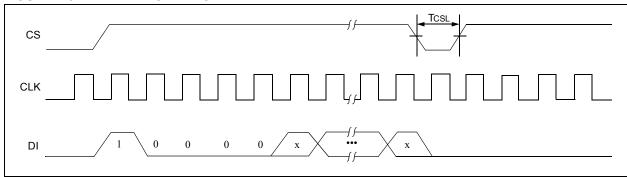
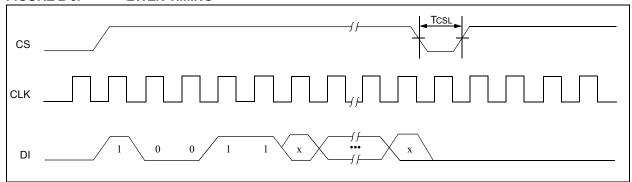


FIGURE 2-6: EWEN TIMING

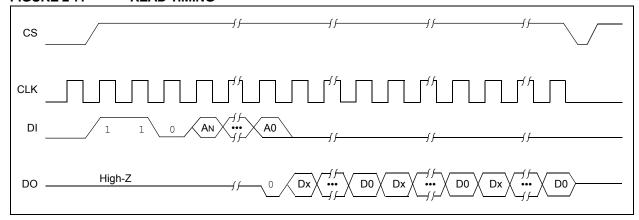


2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (if ORG pin is low or A-version devices) or 16-bit (if ORG pin is high or B-version devices) output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-7: READ TIMING



2.8 Write

The WRITE instruction is followed by 8 bits (if ORG is low or A-version devices) or 16 bits (if ORG pin is high or B-version devices) of data, which are written into the specified address. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the selftimed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TcsL). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: After the Write cycle is complete, issuing a

Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-8: WRITE TIMING FOR 93AA AND 93LC DEVICES

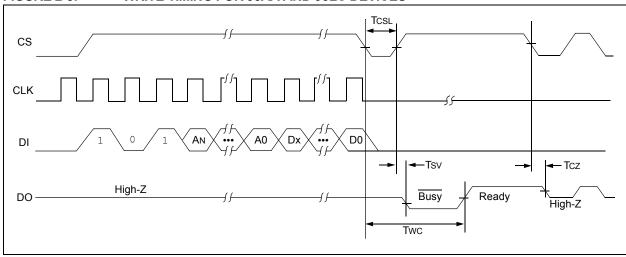
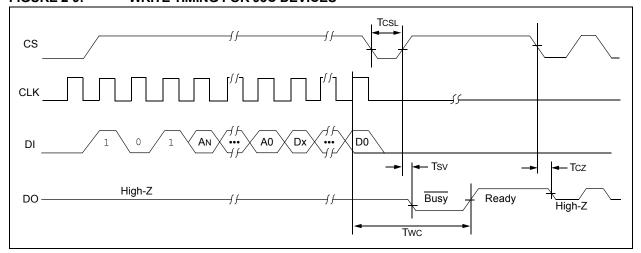


FIGURE 2-9: WRITE TIMING FOR 93C DEVICES



2.9 Write All (WRAL)

The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA46A/B/C and 93LC46A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C46A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (Tcsl.).

Note: After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

Vcc must be ≥4.5V for proper operation of WRAL.

FIGURE 2-10: WRAL TIMING FOR 93AA AND 93LC DEVICES

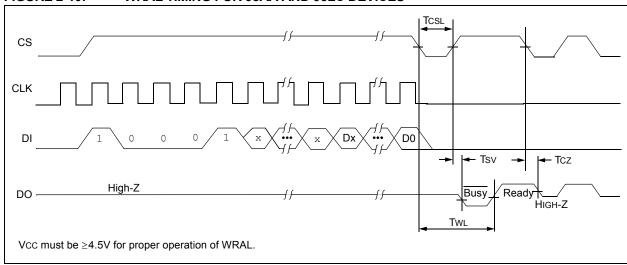
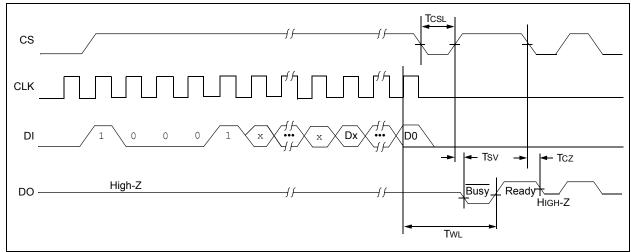


FIGURE 2-11: WRAL TIMING FOR 93C DEVICES



3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	PDIP	SOIC	TSSOP	MSOP	DFN ⁽¹⁾	TDFN ⁽¹⁾	SOT-23	Rotated SOIC	Function
CS	1	1	1	1	1	1	5	3	Chip Select
CLK	2	2	2	2	2	2	4	4	Serial Clock
DI	3	3	3	3	3	3	3	5	Data In
DO	4	4	4	4	4	4	1	6	Data Out
Vss	5	5	5	5	5	5	2	7	Ground
ORG/NC	6	6	6	6	6	6	_	8	Organization/93XX46C No Internal Connection/ 93XX46A/B
NC	7	7	7	7	7	7		1	No Internal Connection
Vcc	8	8	8	8	8	8	6	2	Power Supply

Note 1: The exposed pad on the DFN/TDFN packages can be connected to Vss or left floating.

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle that is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a "don't care" if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and

data bits before an instruction is executed. CLK and DI then become "don't care" inputs waiting for a new Start condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (TCSL) and an erase or write operation has been initiated.

The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High-Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

Note: After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

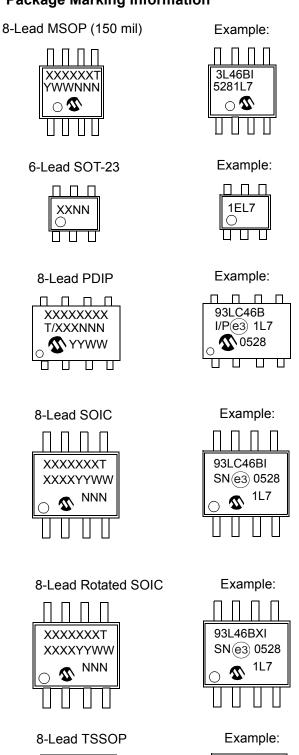
3.5 Organization (ORG)

When the ORG pin is connected to Vcc or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to Vss or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX46A devices are always (x8) organization and 93XX46B devices are always (x16) organization.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information



XXXX

TYWW NNN L46B I528

∭ 1L7

8-Lead 2x3 DFN



Example:



8-Lead 2x3 TDFN



Example:



	1st Line Marking Codes											
Part Number	TSSOP	MSOP	SOT	Г-23	DI	=N	TDFN					
	1330P		I Temp.	E Temp.	I Temp.	E Temp.	l Temp.	E Temp.				
93AA46A	A46A	3A46AT	1BNN	_	301	_	E01	_				
93AA46B	A46B	3A46BT	1LNN	_	311	_	E11					
93AA46C	A46C	3A46CT	_	_	321	_	E21	_				
93LC46A	L46A	3L46AT	1ENN	1FNN	304	_	E04	E05				
93LC46B	L46B	3L46BT	1PNN	1RNN	314	_	E14	E15				
93LC46C	L46C	3L46CT	_	_	324	_	E24	E25				
93C46A	C46A	3C46AT	1HNN	1JNN	307	_	E07	E08				
93C46B	C46B	3C46BT	1TNN	1UNN	317	_	E17	E18				
93C46C	C46C	3C46CT	_	_	327	_	E27	E28				

Note: T = Temperature grade (I, E) NN = Alphanumeric traceability code

Legend: XX...X Part number or part number code

T Temperature (I, E)

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code (2 characters for small packages)

(e3) Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator

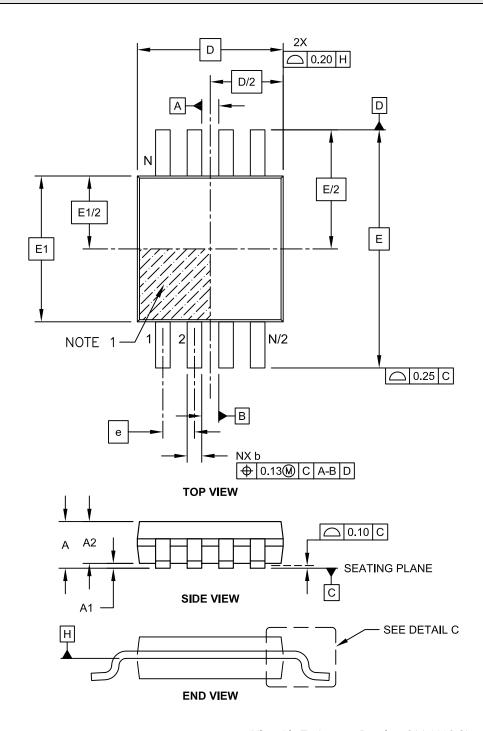
(e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available

characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

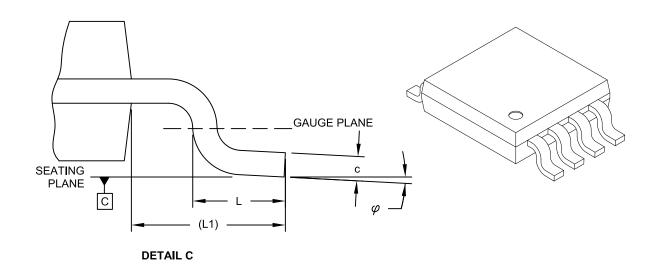
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units						
Dimensior	Limits	MIN	NOM	MAX			
Number of Pins	N		8				
Pitch	е		0.65 BSC				
Overall Height	Α	=	-	1.10			
Molded Package Thickness	A2	0.75	0.85	0.95			
Standoff	A1	0.00	-	0.15			
Overall Width	E	4.90 BSC					
Molded Package Width	E1		3.00 BSC				
Overall Length	D		3.00 BSC				
Foot Length	L	0.40	0.60	0.80			
Footprint	L1		0.95 REF				
Foot Angle	φ	0°	-	8°			
Lead Thickness	С	0.08	-	0.23			
Lead Width	b	0.22	-	0.40			

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

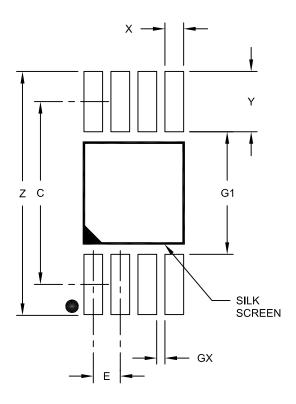
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Contact Pad Spacing	С		4.40		
Overall Width	Z			5.85	
Contact Pad Width (X8)	X1			0.45	
Contact Pad Length (X8)	Y1			1.45	
Distance Between Pads	G1	2.95			
Distance Between Pads	GX	0.20			

Notes:

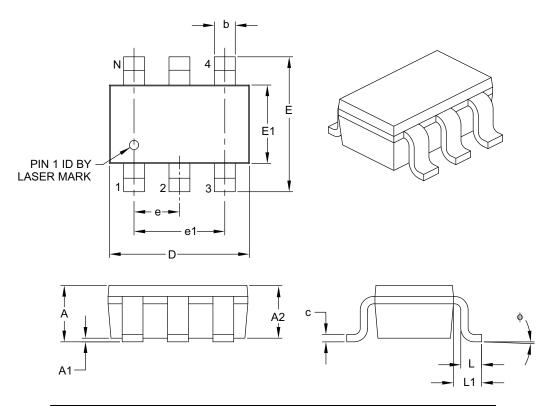
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		6		
Pitch	е		0.95 BSC		
Outside Lead Pitch	e1		1.90 BSC		
Overall Height	A	0.90	_	1.45	
Molded Package Thickness	A2	0.89	-	1.30	
Standoff	A1	0.00	_	0.15	
Overall Width	E	2.20	_	3.20	
Molded Package Width	E1	1.30	-	1.80	
Overall Length	D	2.70	-	3.10	
Foot Length	L	0.10	-	0.60	
Footprint	L1	0.35	_	0.80	
Foot Angle	ф	0°	_	30°	
Lead Thickness	С	0.08	_	0.26	
Lead Width	b	0.20	_	0.51	

Notes:

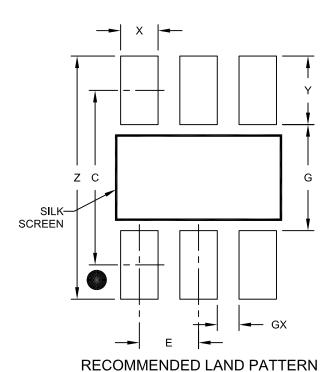
- 1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- 2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units **MILLIMETERS Dimension Limits** MIN NOM MAX Contact Pitch 0.95 BSC Ε Contact Pad Spacing С 2.80 Contact Pad Width (X6) Χ 0.60 Contact Pad Length (X6) Υ 1.10 Distance Between Pads G 1.70 Distance Between Pads GΧ 0.35 Z Overall Width 3.90

Notes:

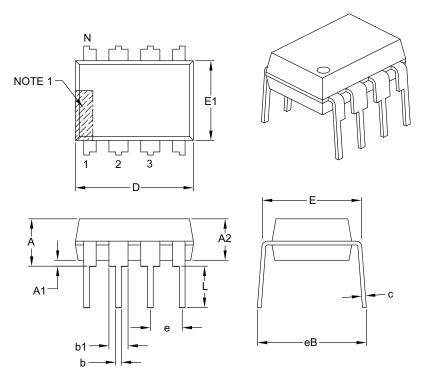
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е		.100 BSC		
Top to Seating Plane	А	_	_	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	_	-	
Shoulder to Shoulder Width	E	.290	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.348	.365	.400	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	_	_	.430	

Notes:

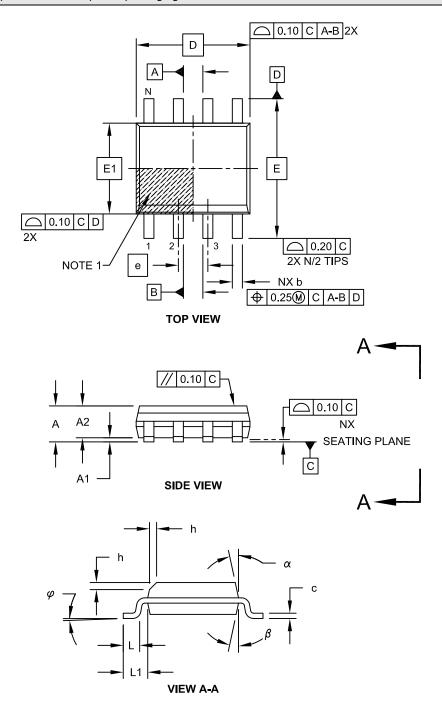
- 1. Pin 1 visual index feature may vary, but must be located with the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

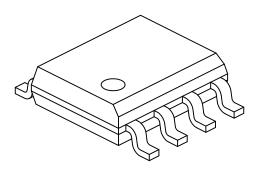
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	Limits	MIN	MOM	MAX		
Number of Pins	N		8			
Pitch	е		1.27 BSC			
Overall Height	Α	-	į	1.75		
Molded Package Thickness	A2	1.25	ı	ı		
Standoff §	A1	0.10	į	0.25		
Overall Width	Е	6.00 BSC				
Molded Package Width	E1	3.90 BSC				
Overall Length	D	4.90 BSC				
Chamfer (Optional)	h	0.25	İ	0.50		
Foot Length	L	0.40	į	1.27		
Footprint	L1		1.04 REF			
Foot Angle	φ	0°	ı	8°		
Lead Thickness	С	0.17	į	0.25		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M

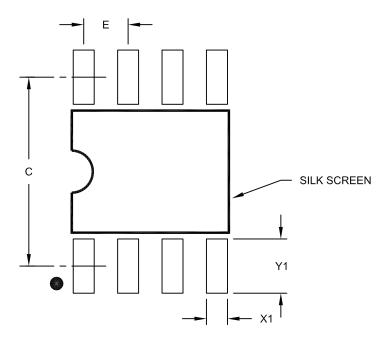
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		N	IILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

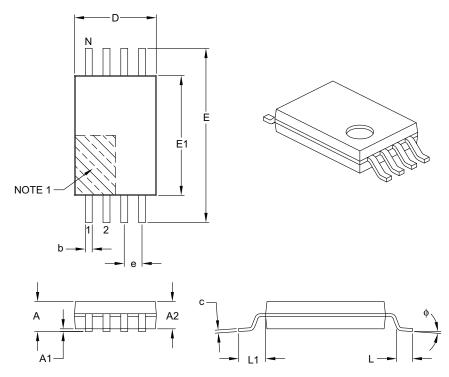
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		0.65 BSC	
Overall Height	A	_	_	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	_	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ф	0°	_	8°
Lead Thickness	С	0.09	_	0.20
Lead Width	b	0.19	_	0.30

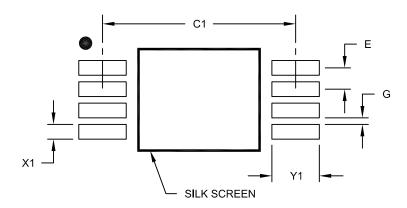
Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		N	II LLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Е		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

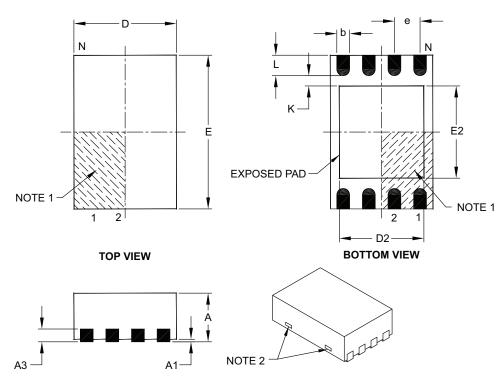
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	3
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	_	1.55
Exposed Pad Width	E2	1.50	-	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

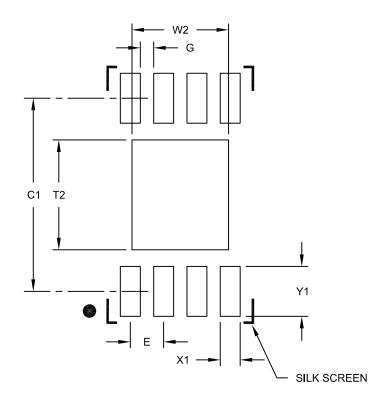
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		N	IILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	Contact Pitch E		0.50 BSC	
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

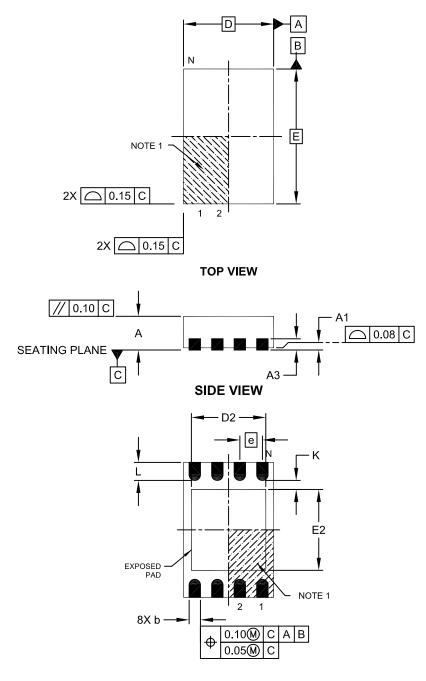
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

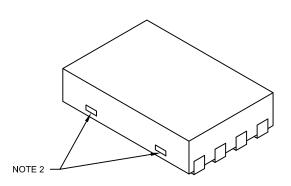


BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	N	IILLIMETER:	S
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		0.50 BSC	
Overall Height	Α	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D	2.00 BSC		
Overall Width	Е		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated
- 4. Dimensioning and tolerancing per ASME Y14.5M

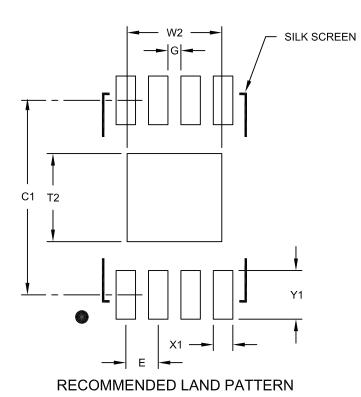
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		N	/ILLIMETER	S
Dimension Limits		MIN	NOM	MAX
Contact Pitch	ntact Pitch E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision D (12/2003)

Corrections to Section 1.0, Electrical Characteristics. Section 4.1, 6-Lead SOT-23 package to OT.

Revision E (3/2005)

Added DFN package.

Revision F (4/2005)

Added notes throughout.

Revision G (5/2008)

Revised Figures 2-1 through 2-4 and Figures 2-8 through 2-11; Revised Package Marking Information; Replaced Package Drawings; Revised Product ID section.

Revision H (08/2010)

Added 8-Lead Rotated SOIC marking information; Revised Package Drawings; Revised Product ID System.

Revision J (12/2011)

Added TDFN Package.

Revision K (06/2013)

Added E Temp to 93LC46C and 93C46C.

NOTES:

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. X Device Pinout	X 	X /XX X T T T T T T T T T T T T T T T T T	Exa	mp 9:
Device Pinout	гаре & Ке	el Temperature Package Lead Finish Range	b)	9: M
Device:		1K 1.8V Microwire Serial EEPROM 1K 1.8V Microwire Serial EEPROM	c)	9: S
	93AA46C		d)	9:
		1K 2.5V Microwire Serial EEPROM		Е
		1K 2.5V Microwire Serial EEPROM 1K 2.5V Microwire Serial EEPROM w/ORG	a)	93
	93C46A:	1K 5.0V Microwire Serial EEPROM	b)	9:
	93C46B: 93C46C:	1K 5.0V Microwire Serial EEPROM 1K 5.0V Microwire Serial EEPROM w/ORG	c)	S 9:
			()	T
Pinout:	Blank = X =	Standard pinout Rotated pinout (SOIC only)	d)	93
	× =	Rotated piriout (SOIC only)		Ε
Tape & Reel:	Blank =	Standard packaging	a)	93
	T =	Tape & Reel	b)	M 93
-		1000 1	5)	E
Temperature Range:	I = E =	-40°C to +85°C -40°C to +125°C	c)	93 S
			d)	93
Package:	MS =	Plastic MSOP (Micro Small outline), 8-lead		R
	OT =	Plastic SOT-23, 6-lead (Tape & Reel only)		
	P = SN =	Plastic DIP (300 mil body), 8-lead Plastic SOIC (3.9 mm body), 8-lead		
	SIN =	Plastic TSSOP (4.4 mm body), 8-lead		
	MC =	Plastic DFN (2x3x0.90 mm body), 8-lead		
	MNY ⁽¹⁾ =	Plastic TDFN (2x3x0.75 mm body), 8-lead (Tape & Reel only)		
Note 1: "Y" indica	atas a Nicks	Palladium Gold (NiPdAu) finish.		
HOLE I. I IIIUICA	ales a INICKE	i i aliadidiri Gold (NIFUAU) IIIIISII.		

- SAA46C-I/P: 1K, 128x8 or 64x16 Serial EPROM, PDIP package, 1.8V
- BAA46B-I/MS: 1K, 64x16 Serial EEPROM, ISOP package, 1.8V
- BAA46AT-I/OT: 1K, 128x8 Serial EEPROM, OT-23 package, tape and reel, 1.8V
- 3AA46CT-I/SN: 1K, 128x8 or 16x16 Serial EPROM, SOIC package, tape and reel, 1.8V
- BLC46A-I/MS: 1K, 128x8 Serial EEPROM, ISOP package, 2.5V
- BLC46BT-I/OT: 1K, 64x16 Serial EEPROM, OT-23 package, tape and reel, 2.5V
- BLC46B-I/ST: 1K, 64x16 Serial EEPROM, SSOP package, 2.5V
- BLC46CT-I/MNY: 1K, 128x8 or 64x16 Serial EPROM, TDFN package, tape and reel, 2.5V
- 3C46B-I/MS: 1K, 64x16 Serial EEPROM, SOP package, 5.0V
- 3C46C-I/MS: 1K, 128x8 or 64x16 Serial EPROM, MSOP package, 5.0V
- 3C46AT-I/OT: 1K, 128x8 Serial EEPROM, OT-23 package, tape and reel, 5.0V
- BC46BX-I/SN: 1K, 64x16 Serial EEPROM, otated SOIC Package, 5.0V

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