

**ELECTRICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	TYP.	MAX.	UNITS
Forward voltage drop	$V_{FM}^{(1)(2)}$	5 A	0.630	-	V
		10 A	0.735	0.810	
		20 A	0.840	0.890	
		5 A	0.530	-	
		10 A	0.615	0.660	
		20 A	0.730	0.770	
Reverse leakage current	$I_{RM}^{(1)}$	$T_J = 25\text{ }^{\circ}\text{C}$	-	50	μA
		$T_J = 125\text{ }^{\circ}\text{C}$	-	4	mA
Junction capacitance	C_T	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz), $25\text{ }^{\circ}\text{C}$	400	-	pF
Series inductance	L_S	Measured lead to lead 5 mm from package body	8.0	-	nH
Maximum voltage rate of change	dV/dt	Rated V_R	-	10 000	V/ μs

Notes

- (1) Pulse width < 300 μs , duty cycle < 2 %
 (2) Only 1 anode pin connected

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		- 55 to 175	$^{\circ}\text{C}$
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	2	$^{\circ}\text{C/W}$
Typical thermal resistance, case to heatsink	R_{thCS}		0.3	
Approximate weight			0.3	g
			0.01	oz.
Marking device		Case style I-PAK	10UT10	
		Case style D-PAK	10WT10FN	

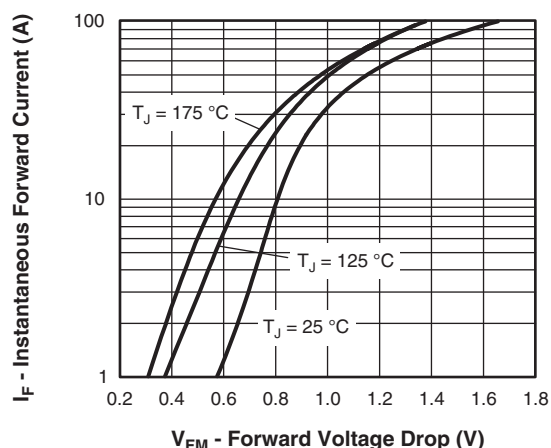


Fig. 1 - Maximum Forward Voltage Drop Characteristics

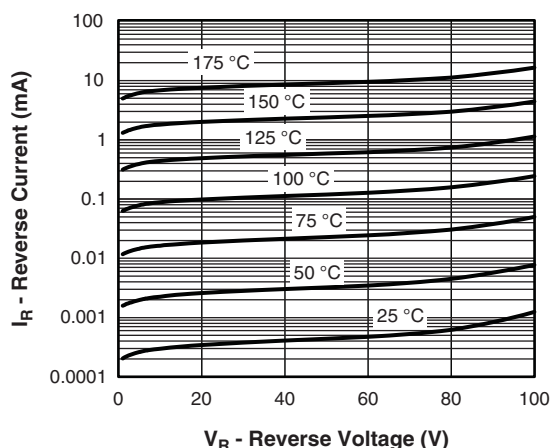


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

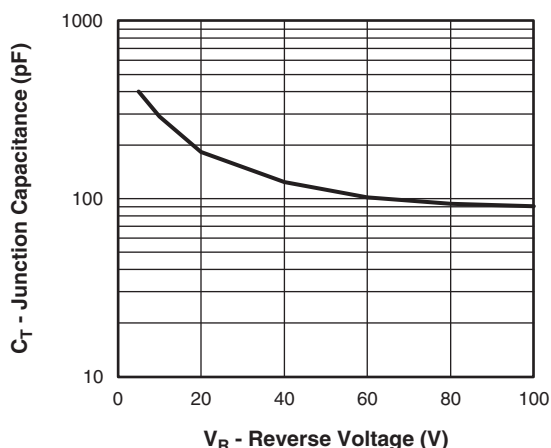


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

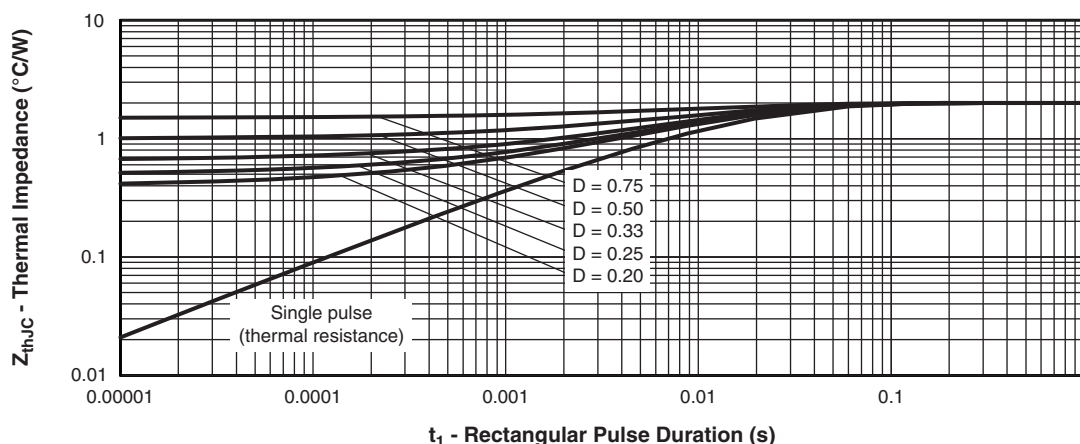
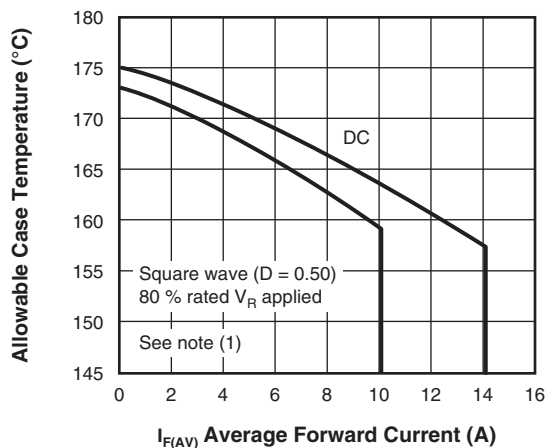

Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

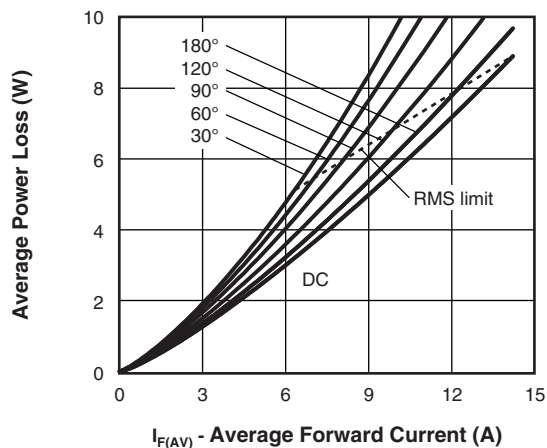


Fig. 6 - Forward Power Loss Characteristics

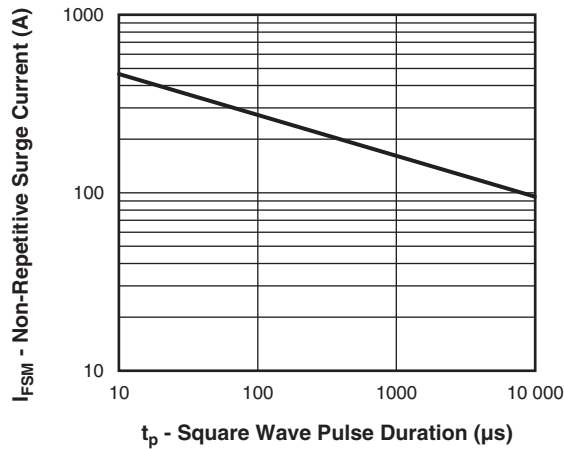


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R

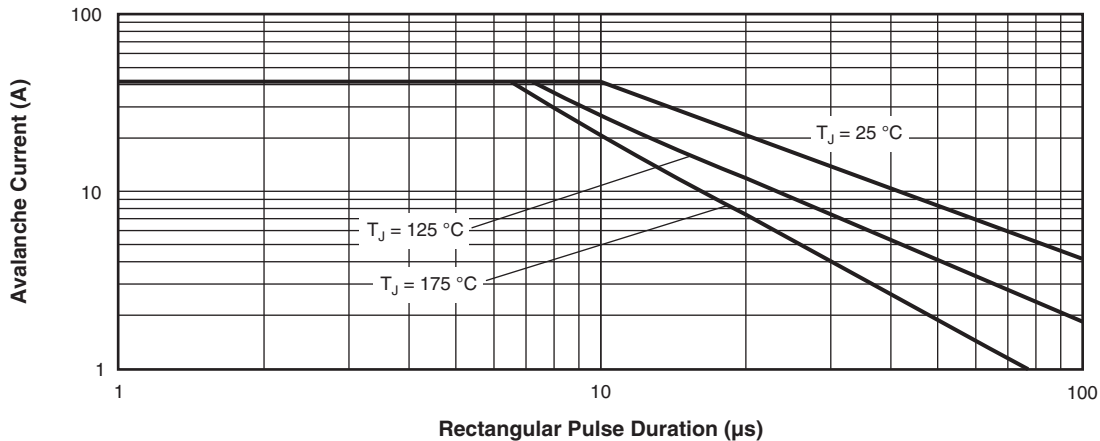


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

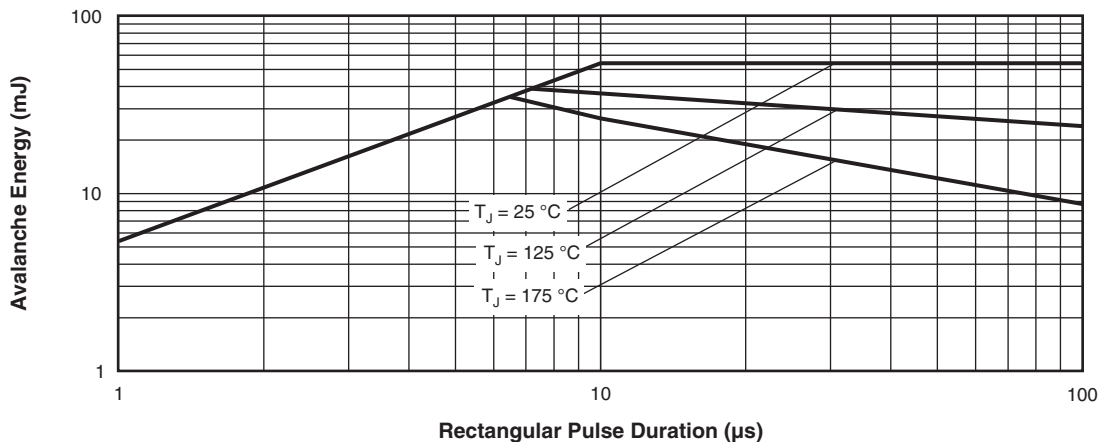


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)



ORDERING INFORMATION TABLE

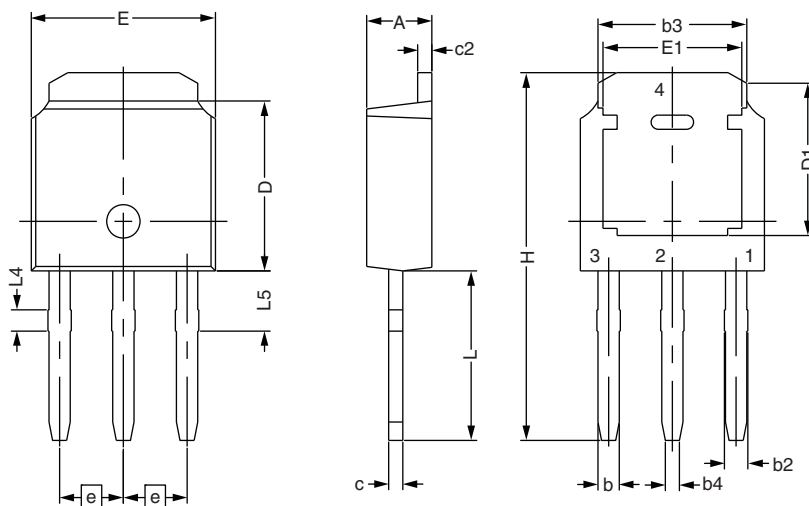
Device code	VS-	10	U	T	10	FN	TRL
	1	2	3	4	5	6	7

- 1** - Vishay Semiconductors product
- 2** - Current rating (10 A)
- 3** - Package:
 - U = I-PAK
 - W = D-PAK
- 4** - T = Trench
- 5** - Voltage code (100 V)
- 6** - TO-252AA (D-PAK)
- 7** - D-PAK, I-PAK:
 - None = Tube (75 pieces)
 - D-PAK only:
 - TR = Tape and reel
 - TRL = Tape and reel (left oriented)
 - TRR = Tape and reel (right oriented)

LINKS TO RELATED DOCUMENTS		
Dimensions	I-PAK (TO-251AA)	www.vishay.com/doc?95024
	D-PAK (TO-252AA)	www.vishay.com/doc?95448
Part marking information	I-PAK (TO-251AA)	www.vishay.com/doc?95025
	D-PAK (TO-252AA)	www.vishay.com/doc?95059
Packaging information		www.vishay.com/doc?95033
SPIICE model		www.vishay.com/doc?95026

I-PAK - S

DIMENSIONS FOR I-PAK - S in millimeters



SYMBOL	DIMENSIONAL REQUIREMENTS		
	MIN.	NOM.	MAX.
E	6.40	6.60	6.70
L	3.98	4.13	4.28
L4	0.66	0.76	0.86
L5	1.96	2.16	2.36
D	6.00	6.10	6.20
H	11.05	11.25	11.45
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
b4	0.41	0.51	0.61
e	2.286 BSC		
A	2.20	2.30	2.38
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D1	5.30	-	-
E1	4.40	-	-



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