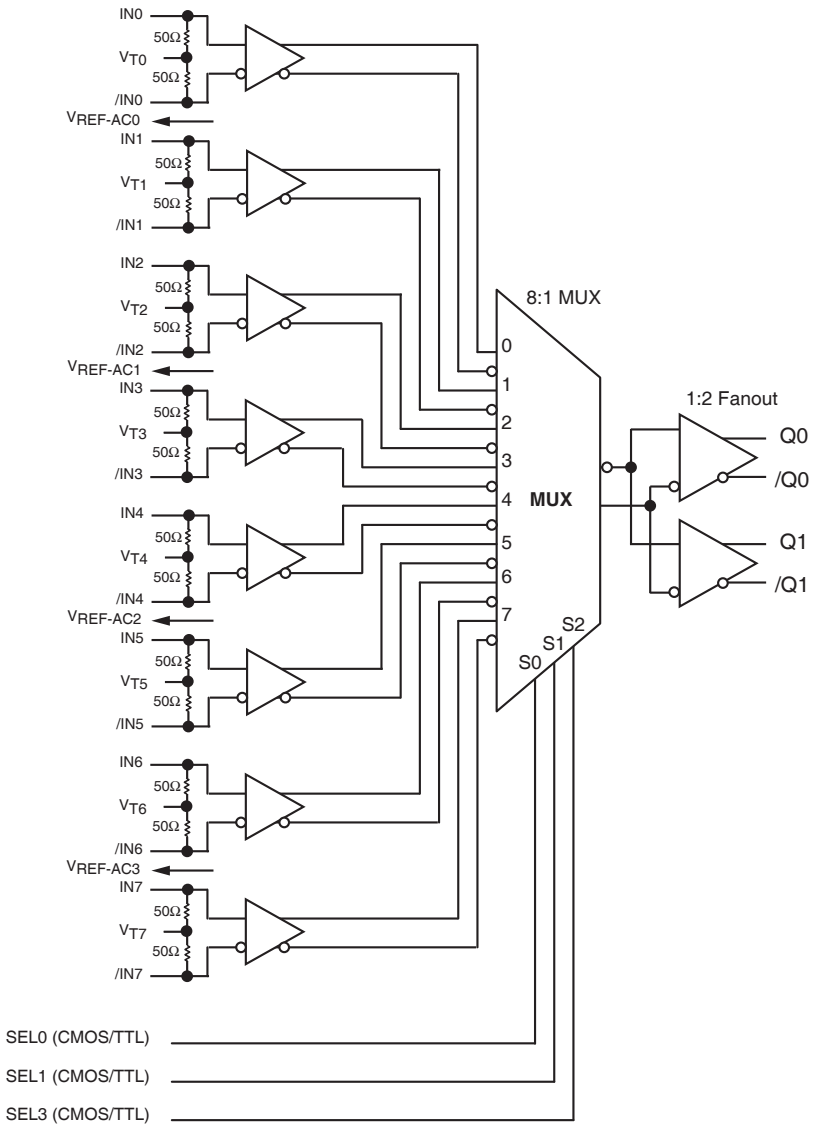
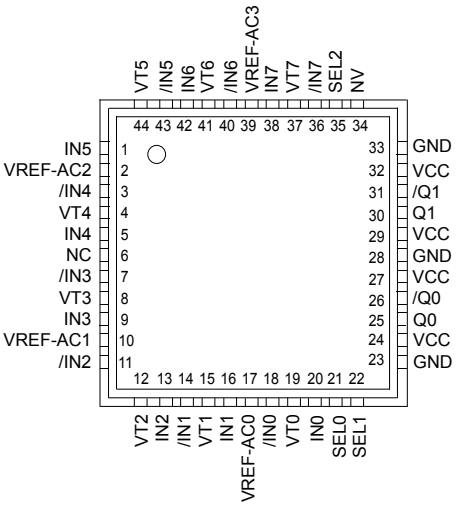
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

SEL2	SEL1	SEL0	Q	/Q
L	L	L	IN0	/IN0
L	L	H	IN1	/IN1
L	H	L	IN2	/IN2
L	H	H	IN3	/IN3
H	L	L	IN4	/IN4
H	L	H	IN5	/IN5
H	H	L	IN6	/IN6
H	H	H	IN7	/IN7

PACKAGE/ORDERING INFORMATION



44-Pin QFN

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58037UMY	QFN-44	Industrial	SY58037U with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY58037UMYTR[2]	QFN-44	Industrial	SY58037U with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
20, 18, 16, 14, 13, 11, 9, 7, 5, 3, 1, 43, 42, 40, 38, 36	IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3, IN4, /IN4, IN5,/IN5, IN6, /IN6, IN7, /IN7	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
19,15, 12, 8, 4, 44, 41, 37	VT0, VT1 VT2, VT3, VT4, VT5, VT6, VT7	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
17, 10, 2 39	VREF-AC0, VREF-AC1, VREF-AC2, VREF-AC3	Reference Voltage: This output biases to V_{CC}–1.2V. It is used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF_AC to the VT pin and bypass with a 0.01µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section for more details.
21, 22, 35	SEL0, SEL1, SEL2	The TTL/CMOS-compatible inputs select the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
24, 27, 29, 32	VCC	Positive Power Supply. Bypass with 0.1µF||0.01µF low ESR capacitors as close to each VCC pin.
25, 26, 30, 31	Q0,/Q0, Q1,/Q1	Differential Outputs: These CML output pairs are the outputs of the device. Please refer to the truth table below for details. Unused output pairs may be left open. Each output is designed to drive 400mV into 100Ω across each output pair.
23, 28, 33	GND, Exposed Pad	Ground. GND and exposed pad must both be connected to the most negative potential of chip ground.

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[3]
  Source or sink current on VT pin ..... ±100mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  QFN (θ_{JA})
    Still-Air ..... 24°C/W
  QFN (ψ_{JB})
    Junction-to-board ..... 12°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V.	2.375	2.5	2.625	V
		V_{CC} = 3.3V.	3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		145	200	mA
R_{IN}	Input Resistance (IN-to-V_T)		40	50	60	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)		V_{CC}–1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN-to-/IN)	See Figure 1b.	0.2			V
V_{T_IN}	IN to V_T (IN-to-/IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

CML OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 100Ω across each output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–0.040	V_{CC}–0.010	V_{CC}	V
V_{OUT}	Output Differential Swing Q, /Q	See Figure 1a.	325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	650	800		mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, R_L = 100Ω across each output pair or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ data Clock	5 4			Gbps GHz
t_{pd}	Differential Propagation Delay (IN-to-Q)	$V_{IN} \geq$ 100mV	240	35550	450	ps
	(SEL-to-Q)		100		550	ps
Δt_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			215		fs/°C
t_{SKEW}	Output-to-Output Skew	**Note 9**			15	ps
	Part-to-Part Skew	**Note 10**			150	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 11**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 12**			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	**Note 13** **Note 14**			1 10	ps_{RMS} ps_{PP}
	Crosstalk-induced Jitter	**Note 15**			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time	At full output swing, 20% to 80%.	20	40	70	ps

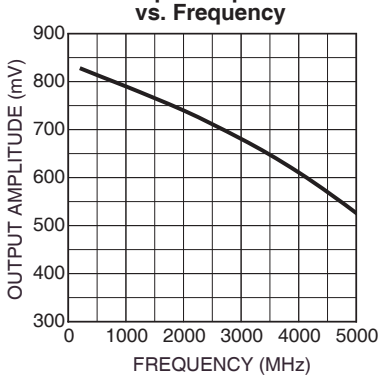
Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Output-to-output skew is measured between two different outputs under identical input transitions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs
11. Random jitter is measured with a K28.7 character pattern, measured at $\leq f_{MAX}$.
12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other adjacent inputs.

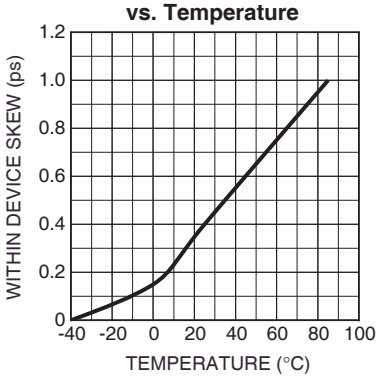
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

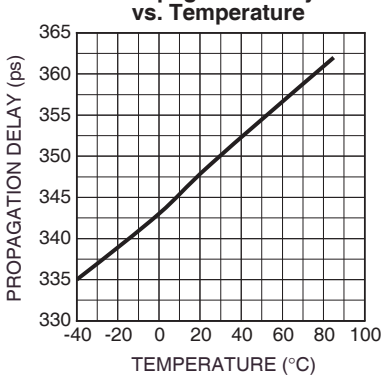
Output Amplitude vs. Frequency



Within Device Skew vs. Temperature



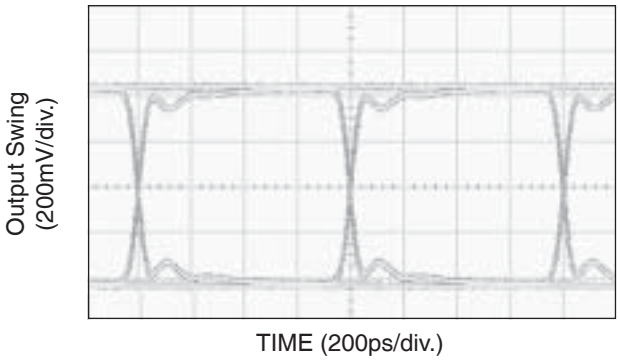
Propagation Delay vs. Temperature



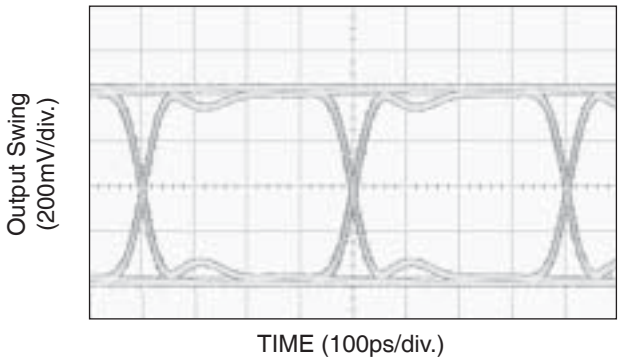
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

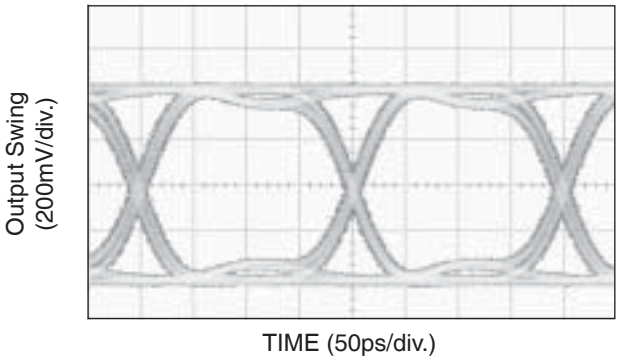
1.25Gbps Output (Q – /Q)



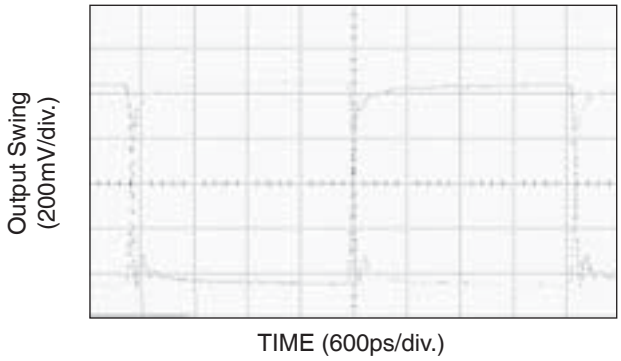
2.5Gbps Output (Q – /Q)



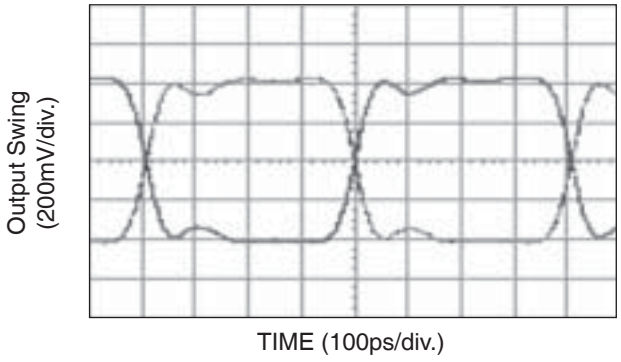
5Gbps Output (Q – /Q)



200MHz Output (Q – /Q)



622MHz Output (Q – /Q)



SINGLE-ENDED AND DIFFERENTIAL SWINGS

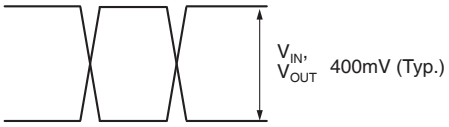


Figure 1a. Single-Ended Voltage Swing

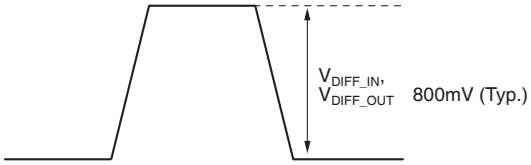


Figure 1b. Differential Voltage Swing

INPUT AND OUTPUT STAGES

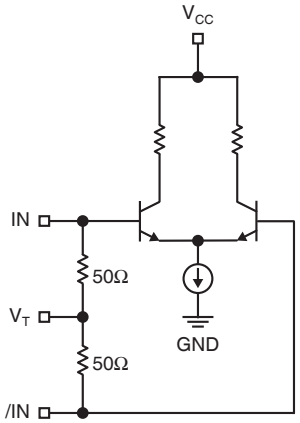


Figure 2a. Simplified Differential Input Stage

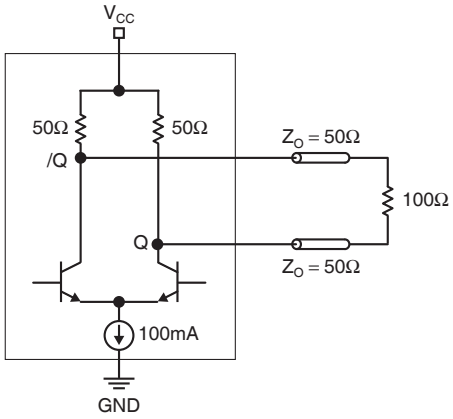


Figure 2b. CML DC-Coupled (100Ω Termination)

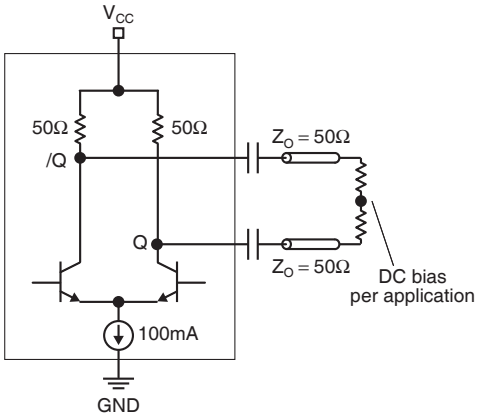
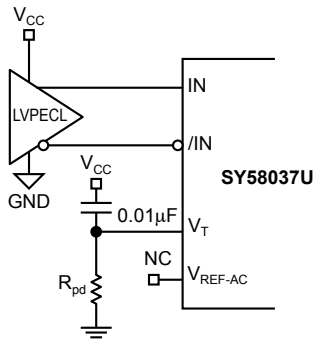


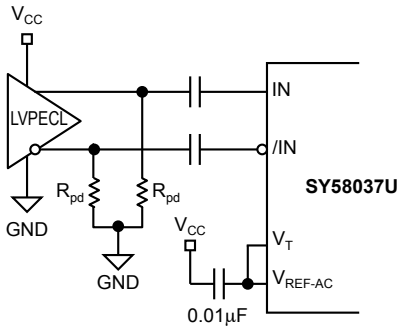
Figure 2c. CML AC-Coupled (50Ω Termination)

INPUT INTERFACE APPLICATIONS



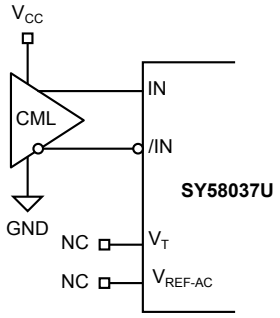
For V_{CC} = 3.3V, R_{pd} = 50Ω.
For V_{CC} = 2.5V, R_{pd} = 19Ω.

Figure 3a. LVPECL Interface (DC-Coupled)



For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

Figure 3b. LVPECL Interface (AC-Coupled)



Option: May connect V_T to V_{CC}.

Figure 3c. CML Interface (DC-Coupled)

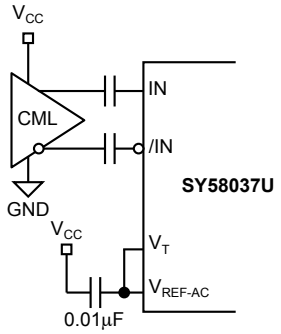


Figure 3d. CML Interface (AC-Coupled)

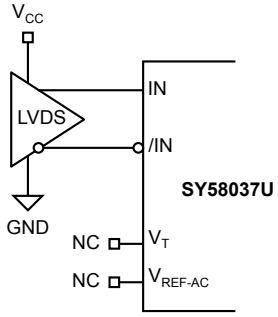
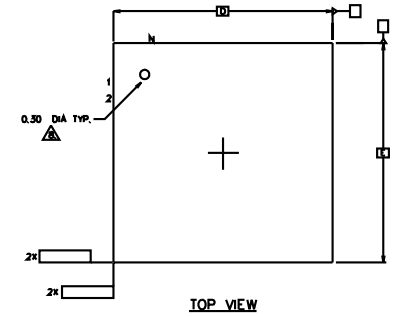


Figure 3e. LVDS Interface

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

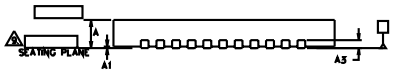
Part Number	Function	Data Sheet Link
SY58037U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 CML Fanout Buffer	http://www.micrel.com/product-info/products/sy58037u.shtml
SY58038U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 LVPECL Fanout Buffer	http://www.micrel.com/product-info/products/sy58038u.shtml
SY58039U	Ultra Precision 8:1 MUX with Internal Termination and 1:2 400mV LVPECL Fanout Buffer	http://www.micrel.com/product-info/products/sy58039u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

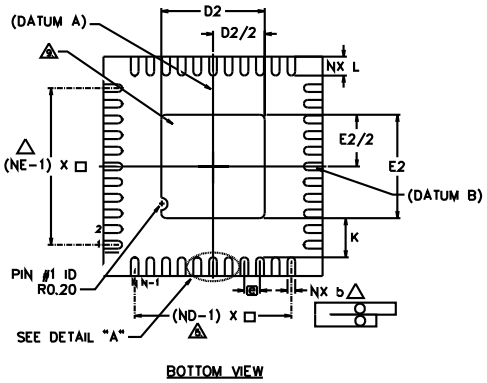
44-PIN QFN (QFN-44)

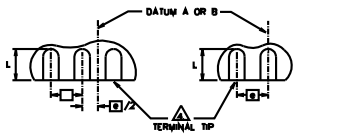


NOTES :

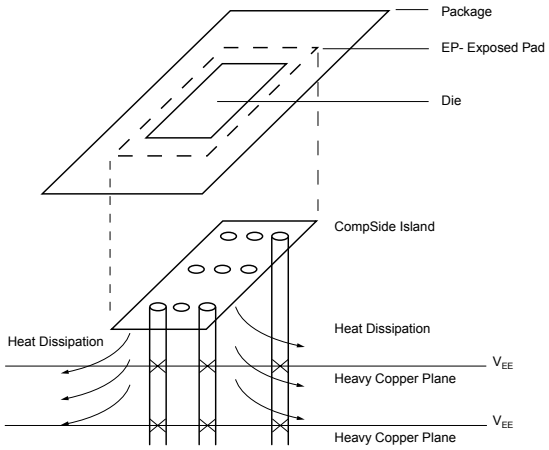
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220







SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		5
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	—	12	2



PCB Thermal Consideration for 44-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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