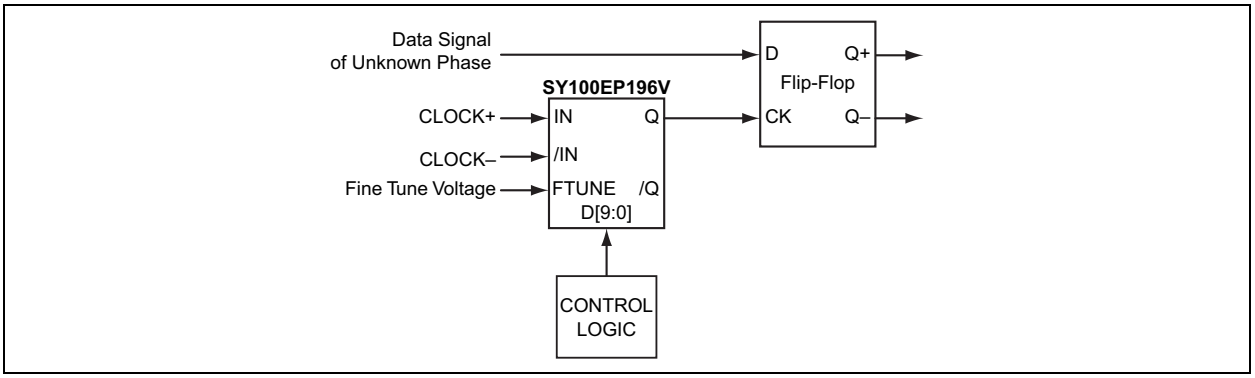
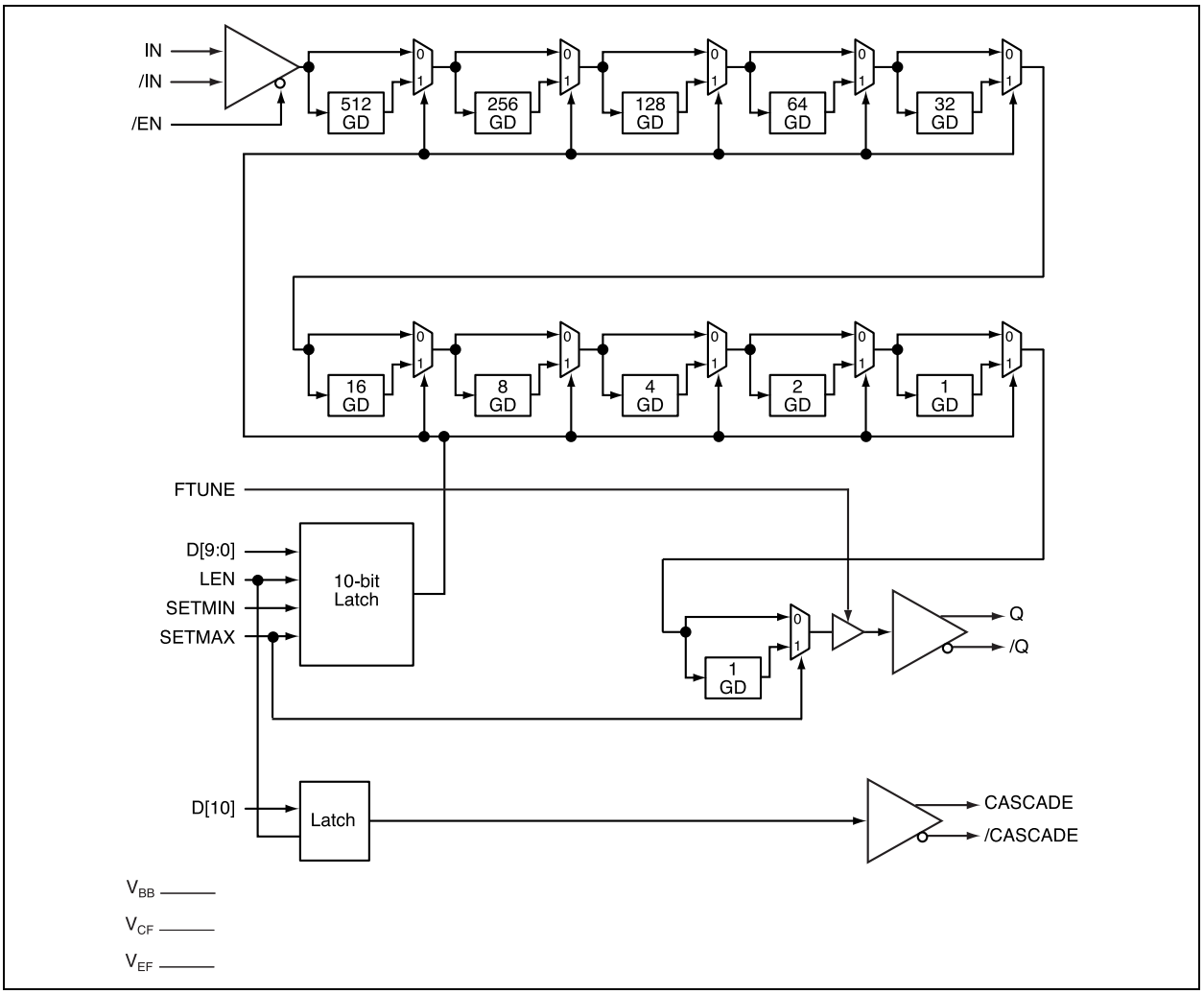
Typical Applications Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) PECL Mode (V_{EE} = 0V) ..... –0.5V to +6.0V
Supply Voltage (V_{EE}) NECL Mode (V_{CC} = 0V) ..... +0.5V to –6.0V
Any Input Voltage (V_{IN}) PECL Mode ..... –0.5V to V_{CC} + 0.5V
Any Input Voltage (V_{IN}) NECL Mode ..... +0.5V to V_{EE} – 0.5V
ECL Continuous Output Current (I_{OUT}) ..... 50 mA
ECL Surge Output Current (I_{OUT}) ..... 100 mA
I_{BB} Sink/Source Current ..... ±0.5 mA
ESD Rating (Note 1) ..... >1.5 kV

Operating Ratings ††

Supply Voltage (V_{CC}) PECL Mode (V_{EE} = 0V) ..... +3.0V to +5.5V
Supply Voltage (V_{EE}) NECL Mode (V_{CC} = 0V) ..... –3.0V to –5.5V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage (PECL)	V_{CC}	3.0	3.3	3.6	V	—
		4.5	5.0	5.5		
Power Supply Voltage (NECL)	V_{EE}	–3.6	–3.3	–3.0	V	—
		–5.5	–5.0	–4.5		
Power Supply Current (Note 1)	I_{EE}	—	150	175	mA	No load, over supply voltage

Note 1: Required 500 lfpm air flow when using +5V or –5V power supply.

(100kEP) LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V, V_{EE} = 0V; T_A = –40°C to +85°C (Note 1, Note 2)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	2155	2280	2405	mV	Figure 4-4, All loading with 50Ω to V_{CC} – 2V
Output LOW Voltage	V_{OL}	1355	1480	1605	mV	Figure 4-4, All loading with 50Ω to V_{CC} – 2V
Input HIGH Voltage, PECL	V_{IH}	2075	—	2420	mV	Figure 4-6 Figure 4-7
Input HIGH Voltage, CMOS		1815	—	—	mV	
Input HIGH Voltage, TTL		2000	—	—	mV	
Input LOW Voltage, PECL	V_{IL}	1355	—	1675	mV	Figure 4-6 Figure 4-7
Input LOW Voltage, CMOS		—	—	1485	mV	
Input LOW Voltage, TTL		—	—	800	mV	
Output Voltage Reference	V_{BB}	1775	1875	1975	mV	—
Input Select Voltage	V_{CF}	1610	1720	1825	mV	—

(100kEP) LVPECL DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 3.3V, V_{EE} = 0V; T_A = –40°C to +85°C (Note 1, Note 2)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Mode Connection	V_{EF}	1900	2000	2100	mV	—
Input HIGH Voltage Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	3.3	V	Figure 4-9
Input HIGH Current	I_{IH}	—	—	150	µA	—
Input LOW Current (IN)	I_{IL}	0.5	—	—	µA	—
Input LOW Current (/IN)		–150	—	—	µA	—

Note 1: Device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: Input and output parameters vary 1:1 with V_{CC}.

3: V_{IHCMR} maximum varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100kEP) PECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 5.0V, V_{EE} = 0V; T_A = –40°C to +85°C (Note 1, Note 2)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	3855	3980	4105	mV	Figure 4-4, All loading with 50Ω to V_{CC} – 2V
Output LOW Voltage	V_{OL}	3055	3180	3305	mV	Figure 4-4, All loading with 50Ω to V_{CC} – 2V
Input HIGH Voltage, PECL	V_{IH}	3775	—	4120	mV	Figure 4-6 Figure 4-7
Input HIGH Voltage, CMOS		2750	—	—	mV	
Input HIGH Voltage, TTL		2000	—	—	mV	
Input LOW Voltage, PECL	V_{IL}	3055	—	3375	mV	Figure 4-6 Figure 4-7
Input LOW Voltage, CMOS		—	—	2250	mV	
Input LOW Voltage, TTL		—	—	800	mV	
Output Voltage Reference	V_{BB}	3475	3575	3675	mV	—
Input HIGH Voltage Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	5.0	V	Figure 4-9
Input HIGH Current	I_{IH}	—	—	150	µA	—
Input LOW Current (IN)	I_{IL}	0.5	—	—	µA	—
Input LOW Current (/IN)		–150	—	—	µA	—

Note 1: Device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: Input and output parameters vary 1:1 with V_{CC}.

3: V_{IHCMR} maximum varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100kEP) NECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 0V, V_{EE} = –5.5V to –3.0V; T_A = –40°C to +85°C (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	–1145	–1020	–895	mV	Figure 4-5, All loading with 50Ω to V_{CC} – 2V
Output LOW Voltage	V_{OL}	–1945	–1820	–1695	mV	Figure 4-5, All loading with 50Ω to V_{CC} – 2V
Input HIGH Voltage, NECL	V_{IH}	–1225	—	–880	mV	Figure 4-8
Input LOW Voltage, NECL	V_{IL}	–1945	—	–1625	mV	Figure 4-8
Output Voltage Reference	V_{BB}	–1525	–1425	–1325	mV	—
Input HIGH Voltage Common Mode Range (Note 2)	V_{IHCMR}	V_{EE} + 2.0	—	0	V	Figure 4-10
Input HIGH Current	I_{IH}	—	—	150	µA	—
Input LOW Current (IN)	I_{IL}	0.5	—	—	µA	—
Input LOW Current (/IN)		–150	—	—	µA	—

Note 1: Device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥500 lfpm is maintained.

2: V_{IHCMR} maximum varies 1:1 with V_{EE}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0 to 5.5V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = –3.0 to –5.5V; T_A = –40°C to +85°C (Note 1, Note 2)

Parameter	Symbol	T_A = –40°C			T_A = +25°C			T_A = +85°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Maximum Frequency (Note 3)	f_{MAX}	—	2.5	—	—	2.5	—	—	2.5	—	GHz
Propagation Delay, IN to Q; D[0-10]=0	t_{PD}	1650	2000	2450	1800	2050	2600	1950	2250	2750	ps
Propagation Delay, IN to Q; D[0-10]=1023		9500	11500	13500	9800	12200	14000	10600	13300	15800	ps
Propagation Delay, /EN to Q: D[0-10]=0		1600	2150	2600	1800	2300	2800	2000	2500	3000	ps
Propagation Delay, D10 to CASCADE		300	420	500	325	450	550	325	525	625	ps
Programmable Range $t_{PD(MAX)}$ to $t_{PD(MIN)}$	t_{RANGE}	7850	9450	—	8200	10000	—	8850	10950	—	ps
Step Delay, D0 High (Note 4)	Δt	—	9	—	—	10	—	—	10	—	ps
Step Delay, D1 High		—	25	—	—	26	—	—	27	—	ps
Step Delay, D2 High		—	42	—	—	42	—	—	43	—	ps
Step Delay, D3 High		—	75	—	—	80	—	—	81	—	ps
Step Delay, D4 High		—	142	—	—	143	—	—	150	—	ps
Step Delay, D5 High		—	296	—	—	300	—	—	310	—	ps
Step Delay, D6 High		—	532	—	—	540	—	—	565	—	ps
Step Delay, D7 High		—	1080	—	—	1095	—	—	1140	—	ps
Step Delay, D8 High		—	2100	—	—	2150	—	—	2250	—	ps
Step Delay, D9 High		—	4250	—	—	4300	—	—	4500	—	ps
Linearity (Note 5)	Lin	—	±10	—	—	±10	—	—	±10	—	%LSB
Duty Cycle Skew t_{PHL} to t_{PLH} (Note 6)	t_{SKEW}	—	—	—	—	25	—	—	—	—	ps

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{CC} = 3.0 to 5.5V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = –3.0 to –5.5V; T_A = –40°C to +85°C (Note 1, Note 2)

Parameter	Symbol	T_A = –40°C			T_A = +25°C			T_A = +85°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Setup Time, D to LEN	t_S	200	0	—	200	0	—	200	0	—	ps
Setup Time, D to IN (Note 7)		300	140	—	300	160	—	300	180	—	ps
Setup Time, /EN to IN (Note 8)		300	150	—	300	170	—	300	180	—	ps
Hold Time, LEN to D	t_H	200	60	—	200	100	—	200	80	—	ps
Hold Time IN to /EN (Note 9)		400	250	—	400	280	—	400	300	—	ps
Release Time, /EN to IN (Note 10)	t_R	—	—	—	—	500	—	—	—	—	ps
Release Time, SETMAX to LEN		400	200	—	400	250	—	400	300	—	ps
Release Time, SETMIN to LEN		350	275	—	350	200	—	350	335	—	ps
Cycle-to-Cycle Jitter (Note 11)	t_{JIT}	—	0.2	<1	—	0.2	<1	—	0.2	<1	ps_{RMS}
Differential Input Voltage Swing	V_{PP}	150	800	1200	150	800	1200	150	800	1200	mV
Output Rise/Fall Time, 20% to 80% (Q)	t_r	—	180	250	—	210	300	—	230	325	ps
20% to 80% (CASCADE)	t_f	—	180	250	—	210	300	—	230	325	ps

Note 1: AC characteristics are guaranteed by design and characterization.

2: Measured using 750 mV source, 50% duty cycle clock source.

3: Refer to the Typical Operating Characteristics for output swing performance.

4: The delays of the individual bits are cumulative.

5: Linearity is the deviation from the ideal delay.

6: Duty cycle skew guaranteed only for differential operation measured from the crosspoint of the input edge to the crosspoint of the corresponding output edge.

7: Setup time defines the amount of time prior to an edge on IN, /IN that the D[0:9] bits must be set to guarantee the new delay will occur for that edge.

8: Setup time is the minimum that /EN must be asserted prior to the next transition of IN, /IN to prevent an output response greater than ±75 mV to that IN, /IN transition.

9: Hold time is the minimum time that /EN must remain asserted after a negative going IN or a positive going /IN to prevent an output response greater than ±75 mV to that IN, /IN transition.

10: Release time is the minimum time that /EN must be deasserted prior to the next IN, /IN transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.

11: This is the amount of generated jitter added to an otherwise jitter free clock signal, going from IN, /IN to Q, /Q, where the clock may be any frequency between 0.0 GHz and 2.5 GHz.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	T_J	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_A	–65	—	+150	°C	
Package Thermal Resistance						
Thermal Resistance, TQFP-32Ld	θ_{JA}	—	50	—	°C/W	Still-Air
	θ_{JA}	—	42	—	°C/W	500lfpm
	θ_{JC}	—	20	—	°C/W	—

2.0 TYPICAL OPERATING CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

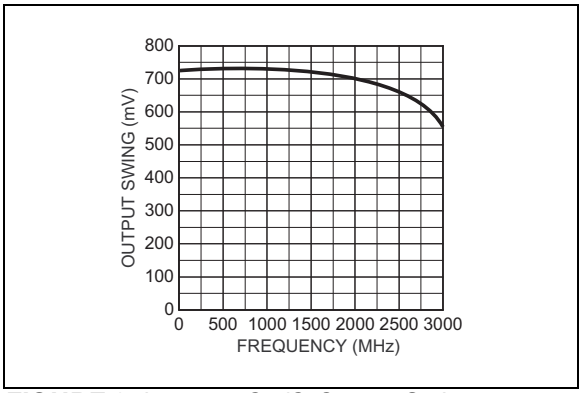


FIGURE 2-1: *Q, /Q Output Swing vs. Frequency.*

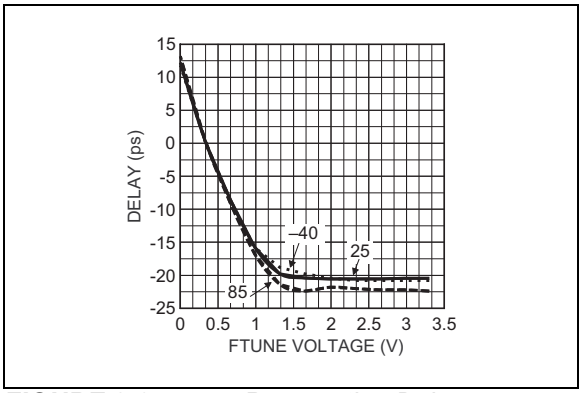


FIGURE 2-3: *Propagation Delay vs. FTUNE Voltage.*

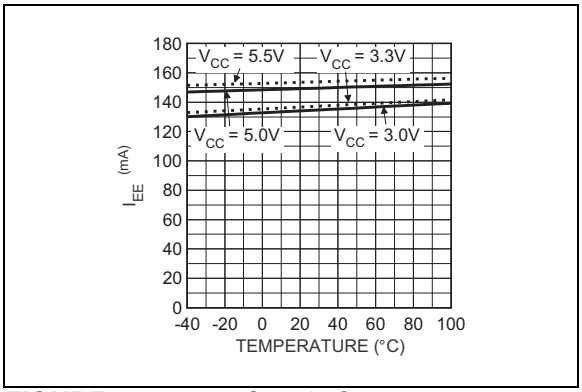


FIGURE 2-2: *Supply Current vs. Temperature.*

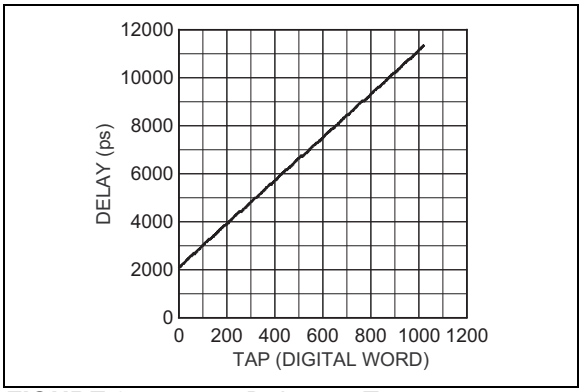


FIGURE 2-4: *Delay vs. Tap.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Function
23, 25, 26, 27, 29, 30, 31, 32, 1, 2	D[0:9]	CMOS, ECL, or TTL Select Inputs: These digital control signals adjust the amount of delay from IN to Q. Please refer to the AC Electrical Characteristics and Table 8-1 for delay values. Figure 6-4 through Figure 6-8 show how to interface these inputs to various logic family standards. These inputs default to logic low when left unconnected. Bit 0 is the least significant bit, and bit 9 is the most significant bit.
3	D[10]	CMOS, ECL, or TTL Select Input: This input latches just like D[0:9] does. It drives the CASCADE, /CASCADE differential pair. Use only when cascading two or more SY100EP196V to extend the range of delays required.
4, 5	IN, /IN	ECL Input: This is the signal to be delayed. If this input pair is left unconnected, this is equivalent to a logic low input.
6	VBB	Voltage Output Reference: When using a single-ended logic source for IN and /IN, connect the unused input of the differential pair to this pin. This pin can also re-bias AC-coupled inputs to IN and /IN. When used, de-couple this pin to VCC through an 0.01 µF capacitor. Limit current sinking or sourcing to 0.5 mA or less.
7	VEF	Voltage Output: Connect this pin to VCF when the D inputs are ECL. Refer to the Digital Control Logic Standard section to interface the D inputs to CMOS or TTL.
8	VCF	Voltage Input: The voltage at this pin sets the logic transition threshold for the D inputs.
9, 24, 28	VEE	Most Negative Supply. Supply ground for PECL systems.
10	LEN	ECL Control Input: When logic low, the D inputs flow through. Any changes to the D inputs reflect in the delay between IN, /IN and Q, /Q. When logic high, the logic values at D are latched, and these latched bits determine the delay.
11	SETMIN	ECL Control Input: When logic high, the contents of the D register are reset. This sets the delay to the minimum possible, equivalent to D[0:9] being set to 0000000000. When logic low, the value of the D register, or the logic value of SETMAX determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected.
12	SETMAX	ECL Control Input: When logic high and SETMIN is logic low, the contents of the D register are set high, and the delay is set to one step greater than the maximum possible with D[0:9] set to 1111111111. When logic low, the value of the D register, or the logic value of SETMIN determines the delay from IN, /IN to Q, /Q. This input defaults to logic low when left unconnected.
13, 18, 19, 22	VCC	Most Positive Supply: Supply ground for NECL systems. Bypass to VEE with 0.1 µF and 0.01 µF low ESR capacitors.
14, 15	CASCADE, /CASCADE	100k ECL Outputs: These outputs are used when cascading two or more SY100EP196V to /CASCADE extend the delay range required. Refer to Table 8-1 for delay values.
16	/EN	ECL Control Input: When set active low, Q, /Q are a delayed version of IN, /IN. When set inactive high, IN, /IN are gated such that Q, /Q become a differential logic low. This input defaults to logic low when left unconnected.
17	FTUNE	Voltage Control Input: By varying the voltage at this pin from VCC through VEE, the delay may be fine tuned by approximately ±15 ps.
20, 21	Q, /Q	100k ECL Outputs: This signal pair is the delayed version of IN, /IN.

4.0 DIAGRAMS

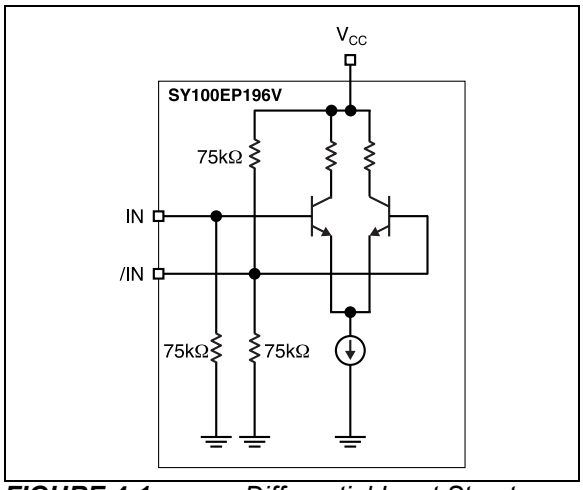


FIGURE 4-1: *Differential Input Structure.*

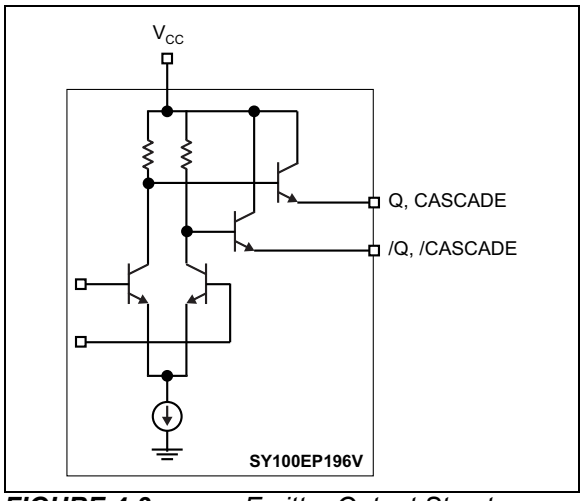


FIGURE 4-3: *Emitter Output Structure.*

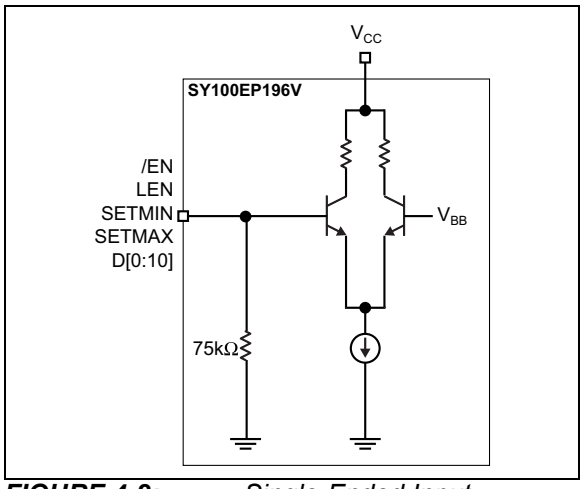


FIGURE 4-2: *Single-Ended Input Structure.*

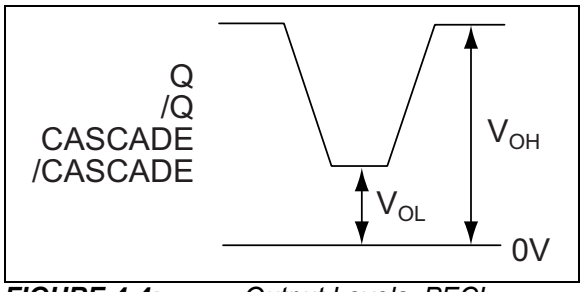


FIGURE 4-4: *Output Levels, PECL, LVPECL.*

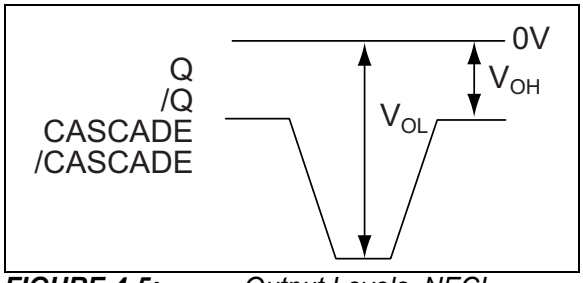


FIGURE 4-5: *Output Levels, NECL.*

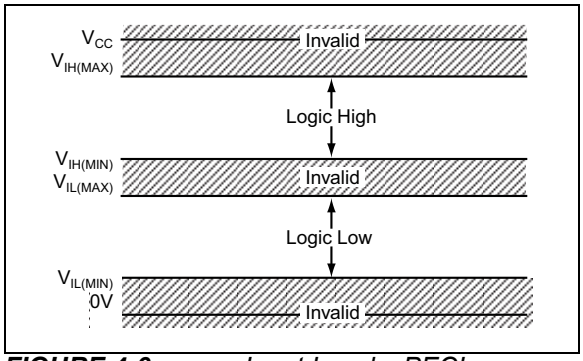


FIGURE 4-6: *Input Levels, PECL.*

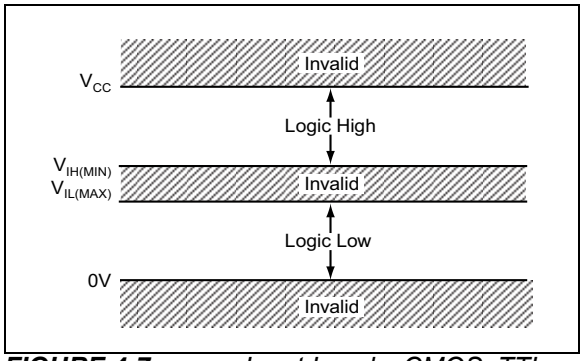


FIGURE 4-7: *Input Levels, CMOS, TTL.*

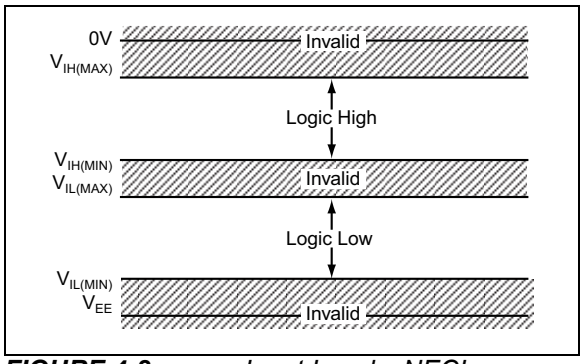


FIGURE 4-8: *Input Levels, NECL.*

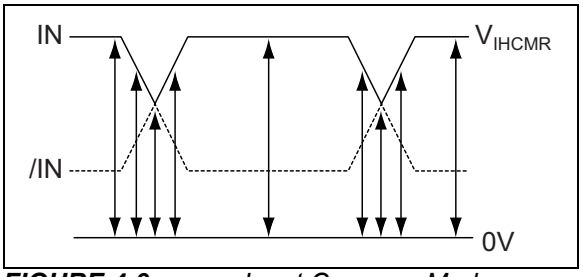


FIGURE 4-9: *Input Common Mode, PECL, LVPECL.*

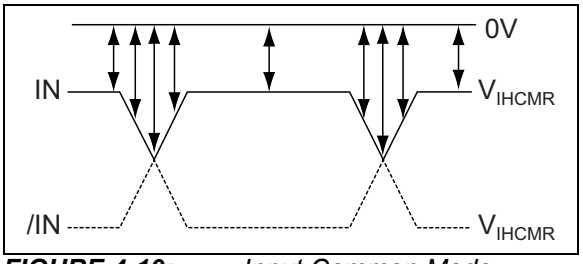


FIGURE 4-10: *Input Common Mode, NECL.*

5.0 TERMINATING PECL

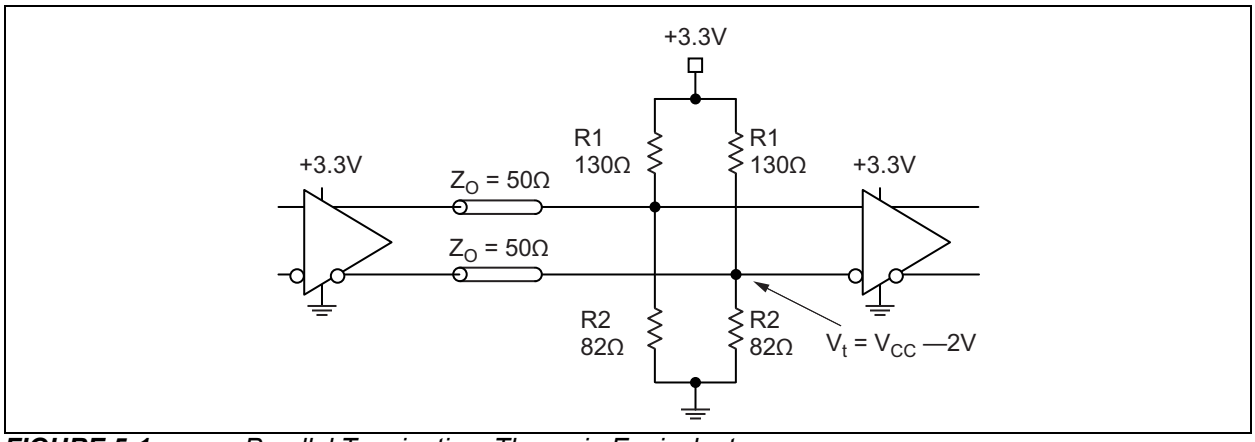


FIGURE 5-1: *Parallel Termination, Thevenin Equivalent.*

Note: For 5V systems: R1 = 82Ω, R2 = 130Ω.

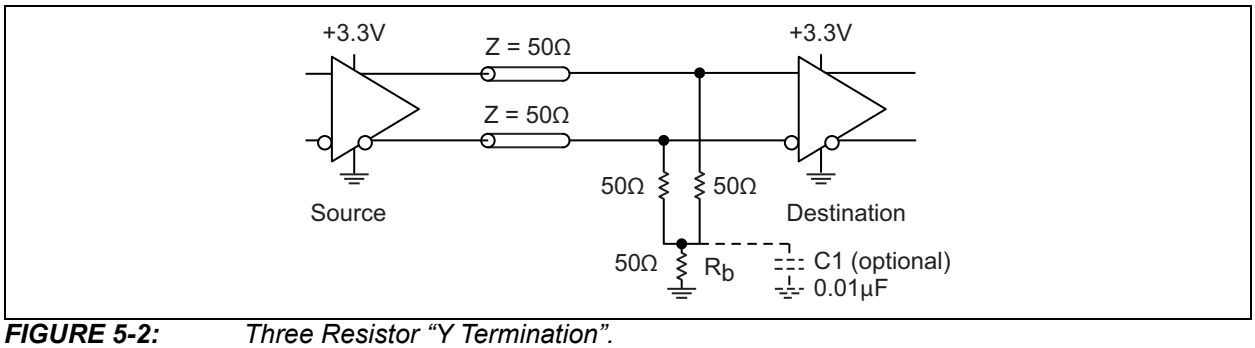


FIGURE 5-2: *Three Resistor "Y Termination".*

Note 1: Power saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

3: R_b resistor set the DC bias voltage, equal to V_t. For +3.3V systems, R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.

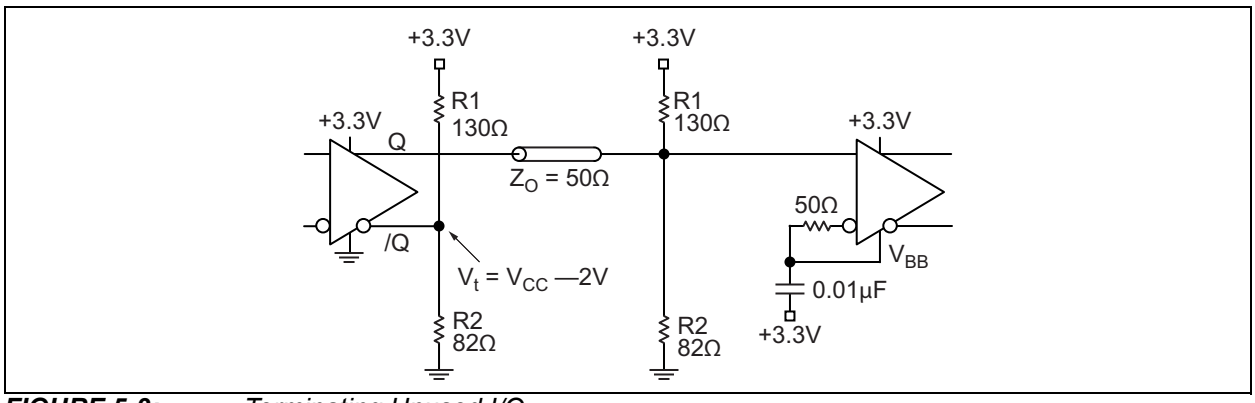


FIGURE 5-3: *Terminating Unused I/O.*

Note 1: Unused output (/Q) must be terminated to balance the output.

2: Microchip's differential I/O logic devices include a V_{BB} reference pin.

3: Connect unused input through 50Ω to V_{BB}. Bypass with a 0.01 µF capacitor to V_{CC}, not GND, as PECL is referenced to V_{CC}.

6.0 INTERFACING DIAGRAMS

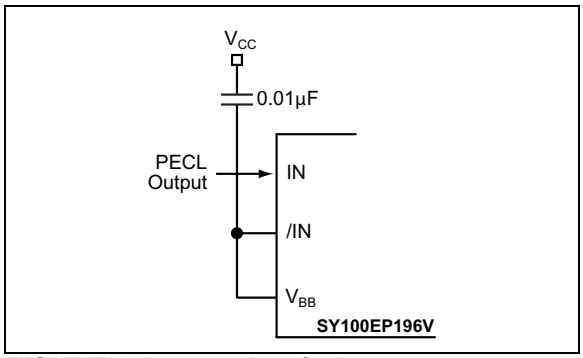


FIGURE 6-1: *Interfacing to a Single-Ended PECL Signal.*

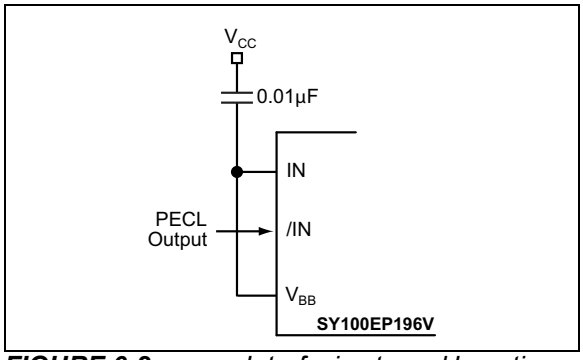


FIGURE 6-2: *Interfacing to and Inverting a Single-Ended PECL Signal.*

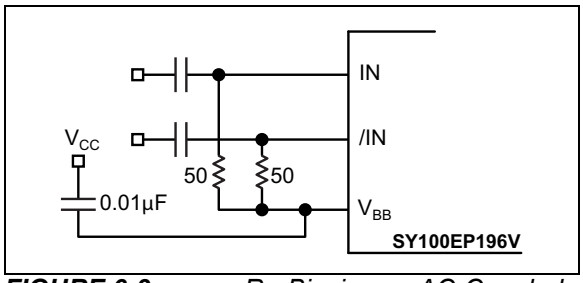


FIGURE 6-3: *Re-Biasing an AC-Coupled Signal.*

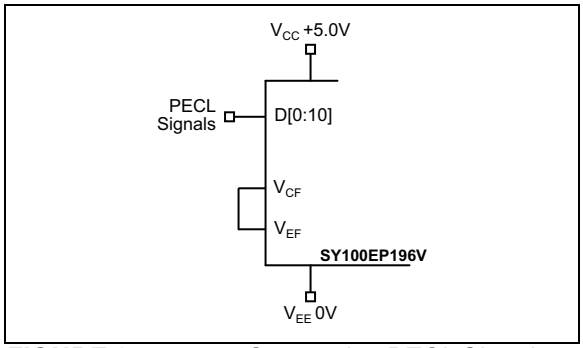


FIGURE 6-4: *Connecting PECL Signals to the D Inputs.*

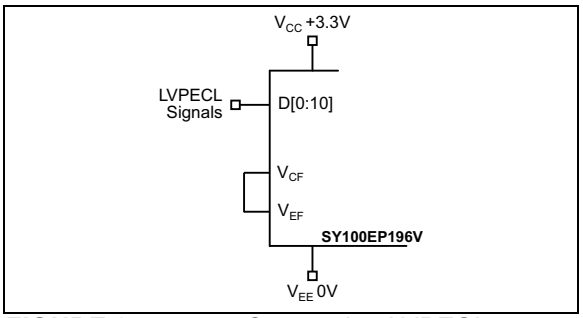


FIGURE 6-5: *Connecting LVPECL Signals to the D Inputs.*

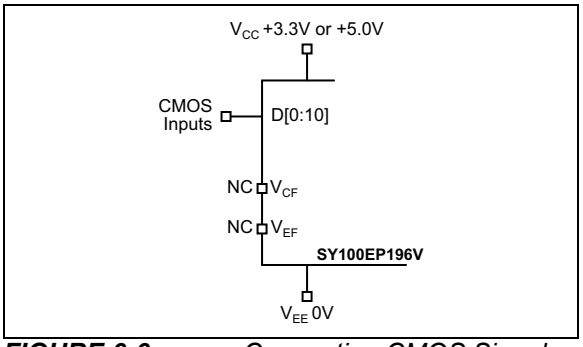


FIGURE 6-6: *Connecting CMOS Signals to the D Inputs (Note: V_{CF} and V_{EF} are not connected).*

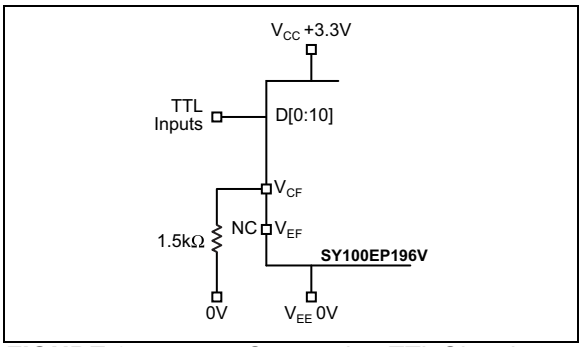


FIGURE 6-7: *Connecting TTL Signals to the D Inputs with V_{CC} = 3.3V.*

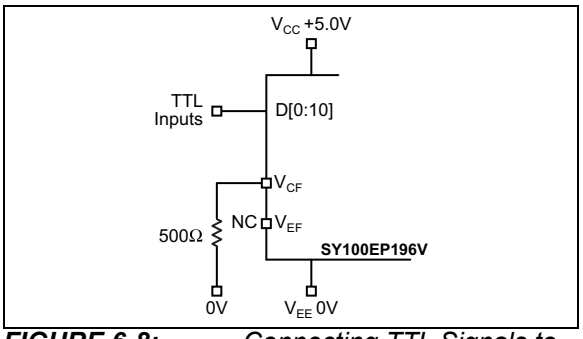


FIGURE 6-8: *Connecting TTL Signals to the D Inputs with V_{CC} = 5.0V.*

7.0 FUNCTIONAL DESCRIPTION

SY100EP196V is a programmable delay line, varying the delay of a PECL or NECL input signal by any amount between about 2.2 ns and 12.2 ns. A 10-bit digital control register affords delay steps of approximately 10 ps.

SY100EP196V implements the delay using a multiplexer chain and a set of fixed delay elements. Under digital control, various subsets of the delay elements are included in the signal chain. To simplify interfacing, the 10-bit digital delay control word interfaces to PECL, CMOS, or TTL interface standards.

Since multiplexers must appear in the delay path, SY100EP196V has a minimum delay of about 2.2 ns. Delays below this value are not possible. In addition, when cascading multiple SY100EP196V to extend the delay range, the minimum delay is about 2.2 ns times the number of SY100EP196V in cascade. An eleventh control bit, D[10], along with the CASCADE and /CASCADE outputs and the SETMIN and SETMAX inputs, simplifies the task of cascading.

7.1 Signal Path Logic Standard

The signal path, from IN, /IN to Q, /Q, interfaces to PECL, LVPECL, or NECL signals, as shown in Table 7-6. The choice of signal path logic standard may limit possible choices for the delay control inputs, D.

7.2 Input Enable

The /EN input gates the signal at IN, /IN. When disabled, the input is effectively gated out, just as if a logic low was being provided to SY100EP196V.

TABLE 7-1: /EN TRUTH TABLE

/EN	Value at Q, /Q
L	IN, /IN Delayed
H	Logic Low Delayed

7.3 Digital Control Latch

SY100EP196V can capture the digital delay control word into its internal 11-bit latch, 10 bits for D[0:9], and an extra bit for the D[10] cascade control. The LEN input controls the action of this latch, as per Table 7-2.

Note that the LEN input is always PECL, LVPECL, or NECL, the same as the IN, /IN signal pair. The 11-bit delay control word, however, may also be CMOS or TTL.

TABLE 7-2: LEN TRUTH TABLE

LEN	Latch Action
L	Pass Through D[0:10]
H	Latch D[0:10]

The nominal delay value is based on the binary value in D[0:9], where D[0] is the least significant bit, and D[9] is the most significant bit. This delay (in picoseconds) from IN, /IN to Q, /Q is about:

EQUATION 7-1:

$$\Delta t = 2200 + 10 \times value(D[9:0]) + delay(FTUNE)$$

7.4 Digital Control Logic Standard

When used in systems where V_{EE} connects to ground, SY100EP196V may interface either to PECL, CMOS, or TTL on its D[0:10] inputs. To this end, the VCF pin sets the threshold at which the D inputs switch between logic low and logic high.

As shown in Table 7-3, connecting VCF to VEF sets the threshold to PECL (if V_{CC} is 5V) or LVPECL (if V_{CC} is 3.3V). Leaving VCF and VEF open yields a threshold suitable for detecting CMOS output logic levels. Leaving VEF open and connecting VCF to a 1.5V source allows the D inputs to accept TTL signals.

TABLE 7-3: DIGITAL CONTROL STANDARD TRUTH TABLE

Logic Standard	VCF Connects to
ECL, PECL	VEF
CMOS	No Connect
TTL	1.5V Source

If a 1.5V source is not available, connecting VCF to VEE through an appropriate resistor will bias VCF at about 1.5V. The value of this resistor depends on the V_{CC} supply, as indicated in Table 7-4.

TABLE 7-4: RESISTOR VALUES FOR TTL INPUT

V_{CC}	Resistor Value
3.3V	1.5 kΩ
5.0V	500Ω

7.5 Cascade Logic

SY100EP196V is designed to ease cascading multiple devices in order to achieve a greater delay range. The SETMIN and SETMAX pins accomplish this, as set out in the applications section below. SETMIN and SETMAX override the delay by changing the value in the D latch register. Table 7-5 lists the action of these pins.

TABLE 7-5: SETMIN AND SETMAX ACTION

SETMIN	SETMAX	Nominal Delay (ps)
L	L	As per D Latch
L	H	2200 + 10 x 1024
H	L	2200
H	H	Not Allowed

7.6 Fine Tune Control

In addition to the digital delay control, the FTUNE input permits a continuous variation in delay. Though it may be set to any voltage between V_{CC} and V_{EE}, most of the delay variation occurs between V_{EE} and V_{EE} + 1.5V. Refer to the Typical Operating Characteristics. For convenience, a V_{CC} of 3.3V is assumed. Typically, the FTUNE input will be fed by a DAC whose purpose is to provide extremely fine delay under digital control.

TABLE 7-6: SIGNAL PATH LOGIC STANDARD

Logic	V_{CC}	V_{EE}	Delay Control Input Choices
PECL	+4.5V to +5.5V	0V	PECL, CMOS, TTL
LVPECL	+3.0V to +3.6V	0V	LVPECL, CMOS, TTL
NECL	0V	–3.0V to –5.5V	NECL

8.0 APPLICATION INFORMATION

For best performance, use good high frequency layout techniques, filter VCC supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the SY100EP196V data inputs and outputs.

8.1 VBB Supply

The VBB pin is an internally generated supply, and is available for use only by the SY100EP196V. When unused, this pin should be left unconnected. The two common uses for VBB are to handle a single-ended PECL input, and to re-bias inputs for AC-coupling applications.

If IN, /IN is driven by a single-ended output, VBB is used to bias the unused input. Please refer to Figure 6-1 and Figure 6-2. The PECL signal driving SY100EP196V may optionally be inverted in this case.

When the signal is AC-coupled, VBB is used, as shown in Figure 6-3, to re-bias IN, /IN. This ensures that SY100EP196V inputs are within its acceptable common mode range.

In all cases, VBB current sinking or sourcing must be limited to 0.5 mA or less.

8.2 Setting D Input Logic Thresholds

As explained earlier, in all designs where the SY100EP196V VEE supply is at zero volts, the D inputs may accommodate CMOS and TTL level signals, as well as PECL or LVPECL. Figure 6-4 through Figure 6-8 show how to connect VCF and VEF for all possible cases.

8.3 Cascading

Two or more SY100EP196V may be cascaded, in order to extend the range of delays permitted. Each additional SY100EP196V adds about 2200ps to the minimum delay, and adds another 10240 ps to the delay range.

Internal cascade circuitry has been included in the SY100EP196V. Using this internal circuitry, SY100EP196V may be cascaded without any external gating.

Examples of cascading two, three, or four SY100EP196V appear in Figure 8-1 through Figure 8-3. Table 8-1 lists the nominal delay for all the cases that appear in those figures.

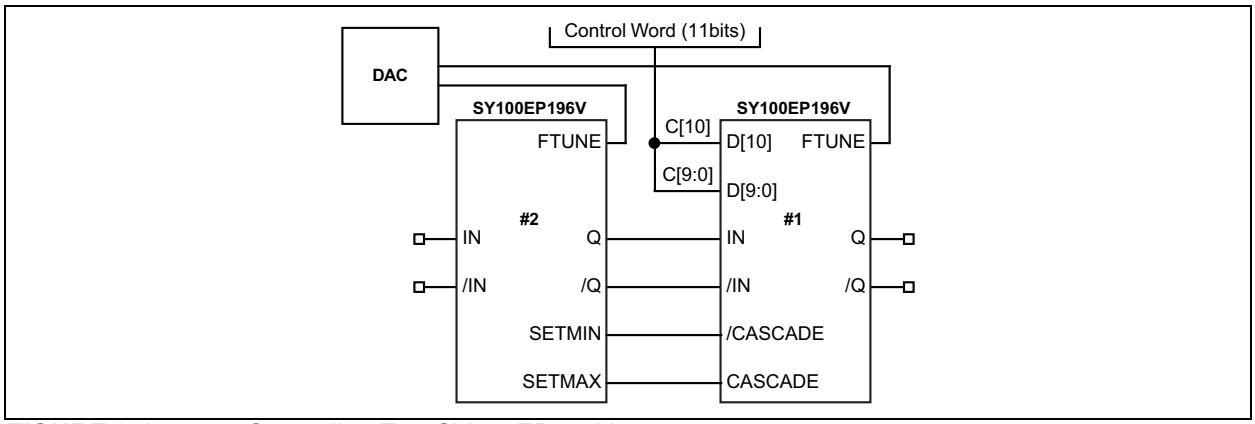


FIGURE 8-1: *Cascading Two SY100EP196V.*

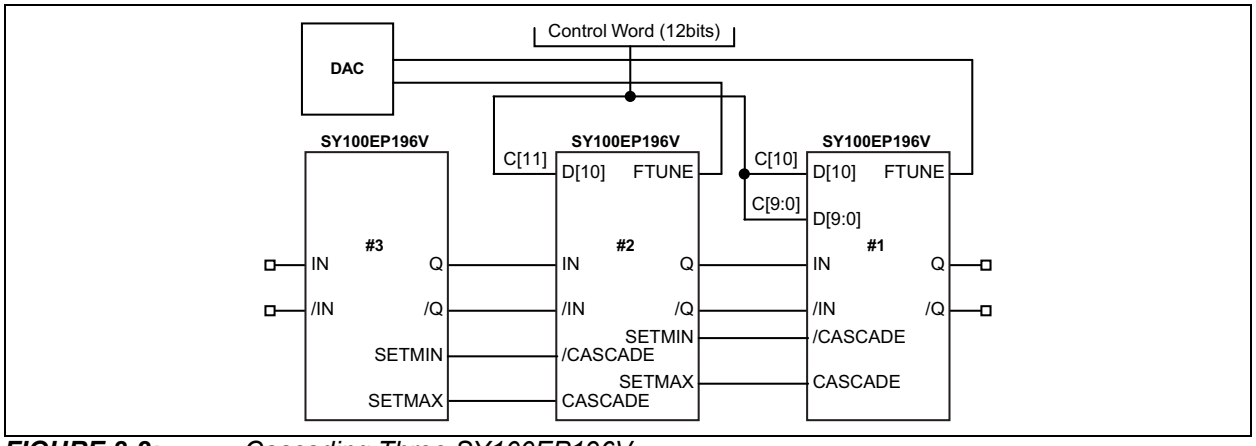


FIGURE 8-2: *Cascading Three SY100EP196V.*

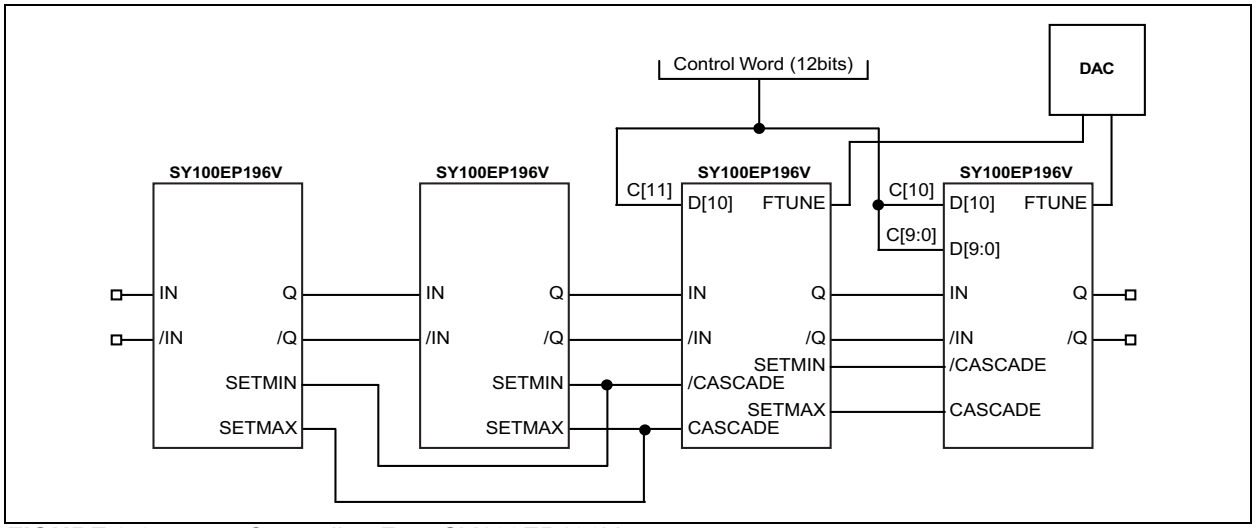


FIGURE 8-3: *Cascading Four SY100EP196V.*

TABLE 8-1: LIST OF NOMINAL DELAY VALUES FOR CASCADED SY100EP196V

Control Inputs			Nominal Delay (ps)			
D[11]	D[10]	D[9:0]	One Chip	Two Chips	Three Chips	Four Chips
0	0	0000000000	2200	4400	6600	8800
0	0	0000000001	2210	4410	6610	8810
0	0	0000000010	2220	4420	6620	8820
0	0	0000000100	2240	4440	6640	8840
0	0	0000001000	2280	4480	6680	8880
0	0	0000010000	2360	4560	6760	8960
0	0	0000100000	2520	4720	6920	9120
0	0	0001000000	2840	5040	7240	9440
0	0	0010000000	3480	5680	7880	10080
0	0	0100000000	4760	6960	9160	11360
0	0	1000000000	7320	9520	11720	13920
0	0	1111111111	12430	14630	16830	19030
0	1	0000000000	—	14640	16840	19040
0	1	0000000001	—	14650	16850	19050

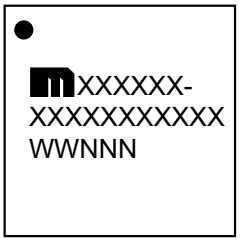
TABLE 8-1: LIST OF NOMINAL DELAY VALUES FOR CASCADED SY100EP196V (CONTINUED)

Control Inputs			Nominal Delay (ps)			
D[11]	D[10]	D[9:0]	One Chip	Two Chips	Three Chips	Four Chips
0	1	0000000010	—	14660	16860	19060
0	1	0000000100	—	14680	16880	19080
0	1	0000001000	—	14720	16920	19120
0	1	0000010000	—	14800	17000	19200
0	1	0000100000	—	14960	17160	19360
0	1	0001000000	—	15280	17480	19680
0	1	0010000000	—	15920	18120	20320
0	1	0100000000	—	17200	19400	21600
0	1	1000000000	—	19760	21960	24160
0	1	1111111111	—	24870	27070	29270
1	0	0000000000	—	—	27080	29280
1	0	0000000001	—	—	27090	29290
1	0	0000000010	—	—	27100	29300
1	0	0000000100	—	—	27120	29320
1	0	0000001000	—	—	27160	29360
1	0	0000010000	—	—	27240	29440
1	0	0000100000	—	—	27400	29600
1	0	0001000000	—	—	27720	29920
1	0	0010000000	—	—	28360	30560
1	0	0100000000	—	—	29640	31840
1	0	1000000000	—	—	32200	34400
1	0	1111111111	—	—	37310	39510
1	1	0000000000	—	—	27080	39520
1	1	0000000001	—	—	27090	39530
1	1	0000000010	—	—	27100	39540
1	1	0000000100	—	—	27120	39560
1	1	0000001000	—	—	27160	39600
1	1	0000010000	—	—	27240	39680
1	1	0000100000	—	—	27400	39840
1	1	0001000000	—	—	27720	40160
1	1	0010000000	—	—	28360	40800
1	1	0100000000	—	—	29640	42080
1	1	1000000000	—	—	32200	44640
1	1	1111111111	—	—	37310	49750

9.0 PACKAGING INFORMATION

9.1 Package Marking Information

32-Lead TQFP*



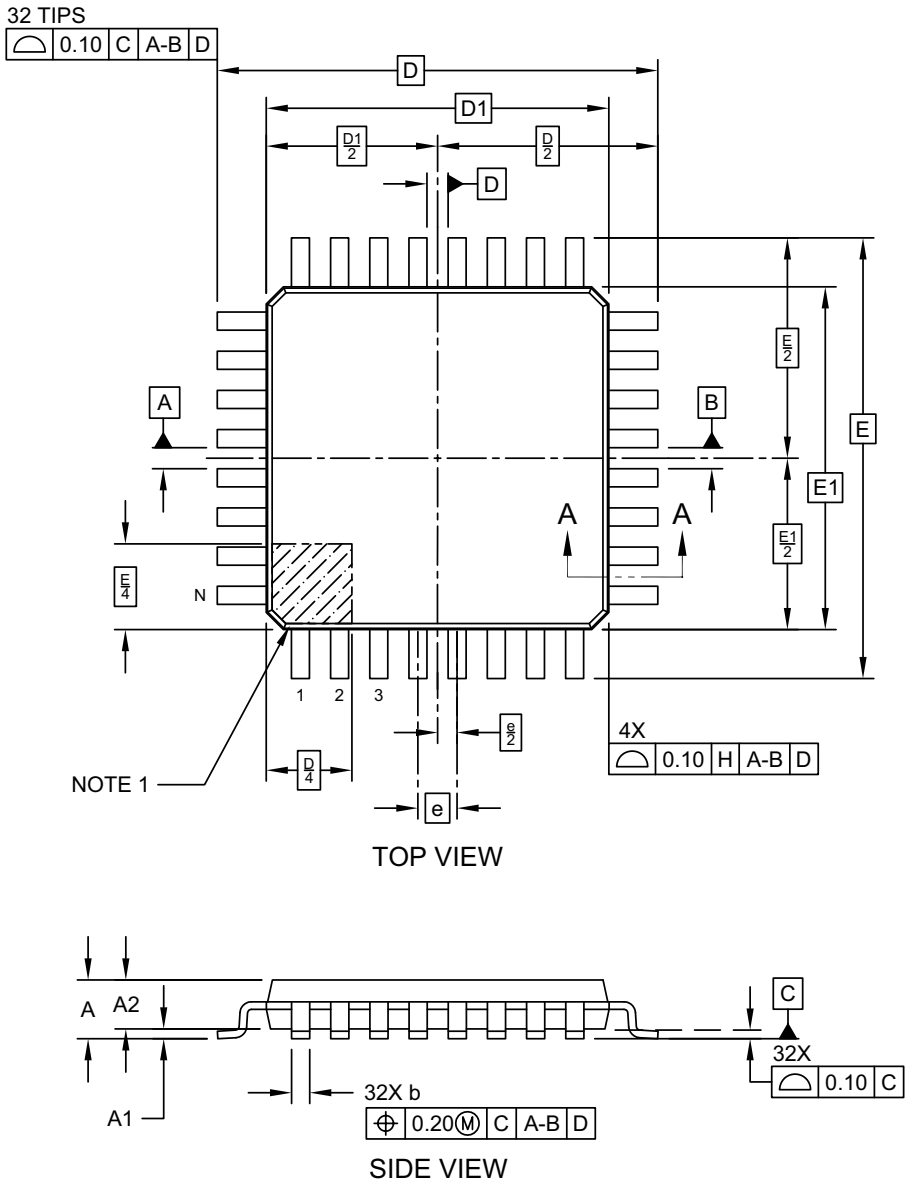
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

32-Lead 7 mm x 7 mm TQFP Package Outline and Recommended Land Pattern

32-Lead Thin Plastic Quad Flatpack (CMA) - 7x7 mm Body [TQFP]
Micrel Legacy Package TQFP7x7-32L

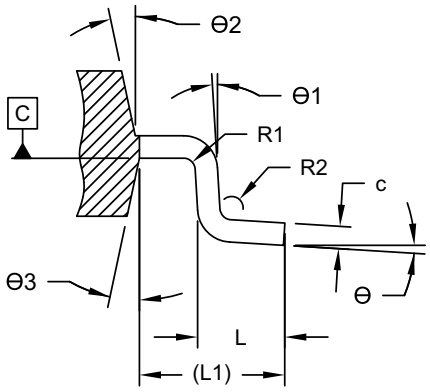
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



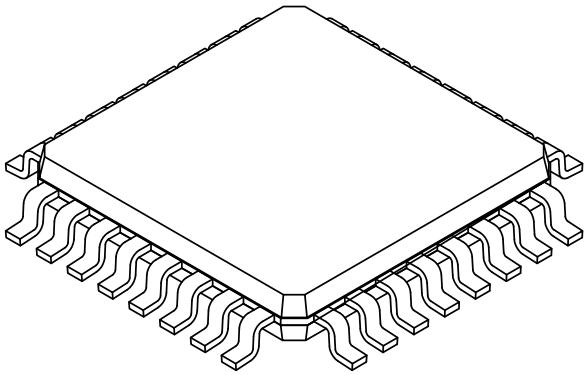
Microchip Technology Drawing C04-1174 Rev A Sheet 1 of 2

32-Lead Thin Plastic Quad Flatpack (CMA) - 7x7 mm Body [TQFP]
Micrel Legacy Package TQFP7x7-32L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		32	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Angle	Θ1	0°	-	-
Foot Angle	Θ	0°	3.5°	7°
Mold Draft Angle Top	Θ2	11°	12°	13°
Mold Draft Angle Bottom	Θ3	11°	12°	13°
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20

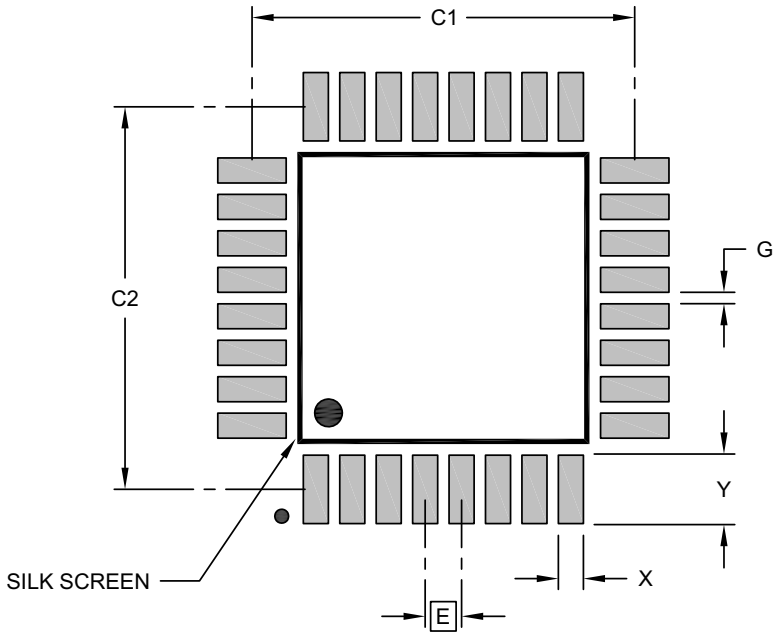
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1174 Rev A Sheet 2 of 2

32-Lead Thin Plastic Quad Flatpack (CMA) - 7x7 mm Body [TQFP]
Micrel Legacy Package TQFP7x7-32L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (Xnn)	X			0.55
Contact Pad Length (Xnn)	Y			1.55
Contact Pad to Contact Pad (Xnn)	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3174 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2021)

- Converted Micrel document SY100EP196V to Microchip data sheet template DS20006520A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Voltage Option	Package	Temperature Range	Special Processing

Device:	SY100EP169V:	3.3V/5V 2.5 GHz Programmable Delay Chip with Fine Tune Control	
Voltage Option:	V	=	3.3V/5V
Package:	T	=	32-Lead 7 mm x 7 mm TQFP
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	250/Tray
	TR	=	1,000/Reel

Examples:

a) SY100EP196VTG: SY100EP196V, 3.3V/5V, 32-Lead TQFP, –40°C to 85°C Temp. Range, 250/Tray

b) SY100EP196VTG-TR: SY100EP196V, 3.3V/5V, 32-Lead TQFP, –40°C to 85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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China - Shenzhen
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China - Wuhan
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China - Xian
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China - Xiamen
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China - Zhuhai
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India - New Delhi
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India - Pune
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Japan - Osaka
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Japan - Tokyo
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Korea - Daegu
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Malaysia - Kuala Lumpur
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Malaysia - Penang
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Philippines - Manila
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Taiwan - Hsin Chu
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Taiwan - Kaohsiung
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Thailand - Bangkok
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Vietnam - Ho Chi Minh
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Finland - Espoo
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Israel - Ra'anana
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Italy - Milan
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Netherlands - Drunen
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