Contents

List of tables

List of figures

1 Functional overview

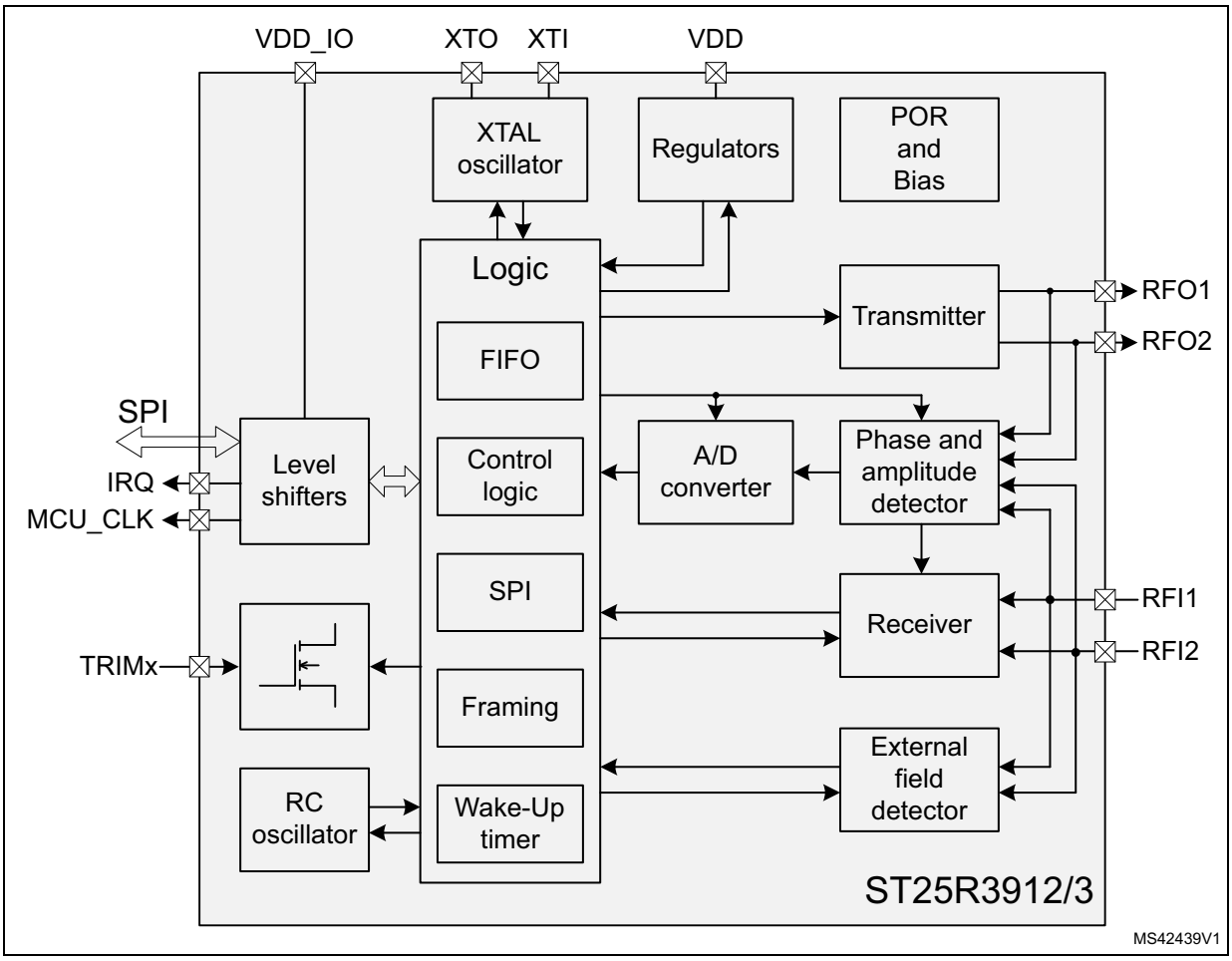
The ST25R3912/3 are suitable for a wide range of applications, among them

- Gaming
- Access control
- NFC infrastructure
- Ticketing

1.1 Block diagram

The block diagram is shown in *Figure 1*.

Figure 1. ST25R3912/3 block diagram



1.1.1 Transmitter

The transmitter incorporates drivers that drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally

contains a sub-block that modulates transmitted signal (OOK or configurable AM modulation).

The ST25R3912/3 transmitter is intended to directly drive antennas (without 50 Ω cable, usually antenna is on the same PCB). Operation with 50 Ω cable is also possible, but in that case some of the advanced features are not available.

By applying FFh to register 27h, the output drivers are in tristate.

1.1.2 Receiver

The receiver detects transponder modulation superimposed on the 13.56 MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance for each mode and bit rate (sub-carrier frequencies from 212 kHz to 6.8 MHz are supported). The receiver chain inputs are the RFI1 and RFI2 pins. The receiver chain incorporates several features that enable reliable operation in challenging phase and noise conditions.

1.1.3 Phase and amplitude detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2). The amplitude detector is observing the amplitude of the receiver input signals (RFI1 and RFI2) via self-mixing. The amplitude of the receiver input signals (RFI1 and RFI2) is directly proportional to the amplitude of the antenna LC tank signal.

The phase detector and the amplitude detector can be used for the following purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variation
- Average phase difference between RFOx pins and RFIx pins is used to check and optimize antenna tuning (only on ST25R3913)
- Amplitude of signal present on RFI1 and RFI2 pins is used to check and optimize antenna tuning

1.1.4 A/D converter

The ST25R3912/3 contain a built in Analog to Digital (A/D) converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of the A/D conversion is stored in the *A/D Converter Output Register* and can be read via SPI.

1.1.5 External field detector

The External field detector is a low power block used in NFC mode to detect the presence of an external RF field. It supports two different detection thresholds, Peer Detection Threshold and Collision Avoidance Threshold. The Peer Detection Threshold is used in the NFCIP-1 target mode to detect the presence of an initiator field, and is also used in active communication initiator mode to detect the activation of the target field. The Collision Avoidance Threshold is used to detect the presence of an RF field during the NFCIP-1 RF Collision Avoidance procedure.

1.1.6 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. The start-up time varies with crystal type, temperature and other parameters, hence the oscillator amplitude is observed and an interrupt is sent when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the *IO Configuration Register 1*.

1.1.7 Power supply regulators

Integrated power supply regulators ensure a high power supply rejection ratio for the complete reader system. If the reader system PSRR has to be improved, the command Adjust Regulators is sent. As a result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in the *Regulator and Timer Display Register*. It is also possible to define regulated voltage by writing to the *Regulator Voltage Control Register*. To decouple any noise sources from different parts of the IC there are three regulators integrated with separated external blocking capacitors (the regulated voltage of all of them is the same in 3.3 V supply mode). One regulator is for the analog blocks, one for the digital blocks, and one for the antenna drivers.

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

1.1.8 POR and Bias

This block provides the bias current and the reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply voltage levels.

1.1.9 RC oscillator and Wake-Up timer

The ST25R3912/3 includes several possibilities of low power detection of card presence (phase measurement, amplitude measurement). The RC oscillator and the register configurable Wake-Up timer are used to schedule the periodic card presence detection.

1.1.10 ISO-14443 and NFCIP-1 framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes the demodulated sub-carrier signal from the receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from the FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing the modulation signal to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal (the receiver output), is directly sent to the MISO pin, and the signal applied to the MOSI pin is directly used to modulate the transmitter.

1.1.11 FIFO

The ST25R3912/3 contain a 96-byte FIFO. Depending on the mode, it contains either data that has been received or data to be transmitted.

1.1.12 Control logic

The control logic contains I/O registers that define operation of device.

1.1.13 SPI

A 4-wire Serial Peripheral Interface (SPI) is used for communication between the external microcontroller and the ST25R3912/3.

1.2 Application information

The minimum configurations required to operate the ST25R3912/3 are shown in *Figure 2* and *Figure 3*.

Figure 2. Minimum configuration with single sided antenna driving (including EMC filter)

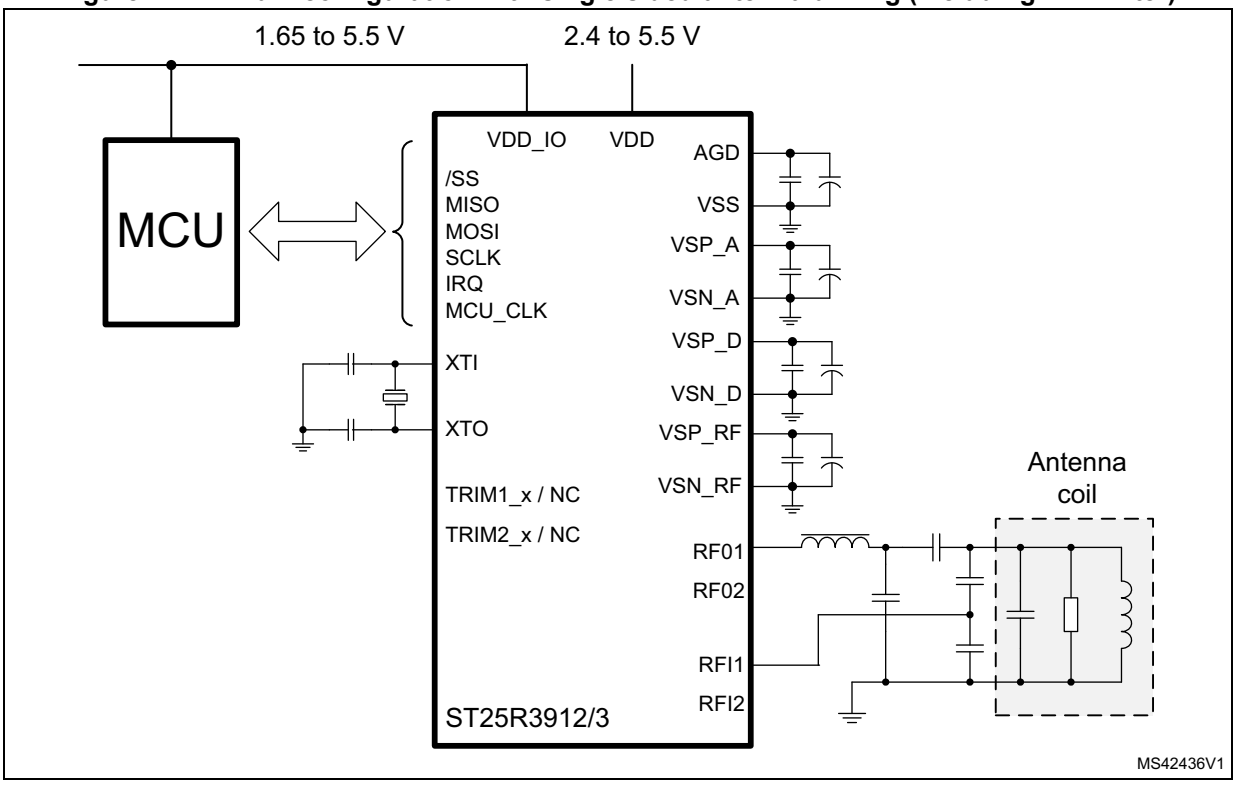
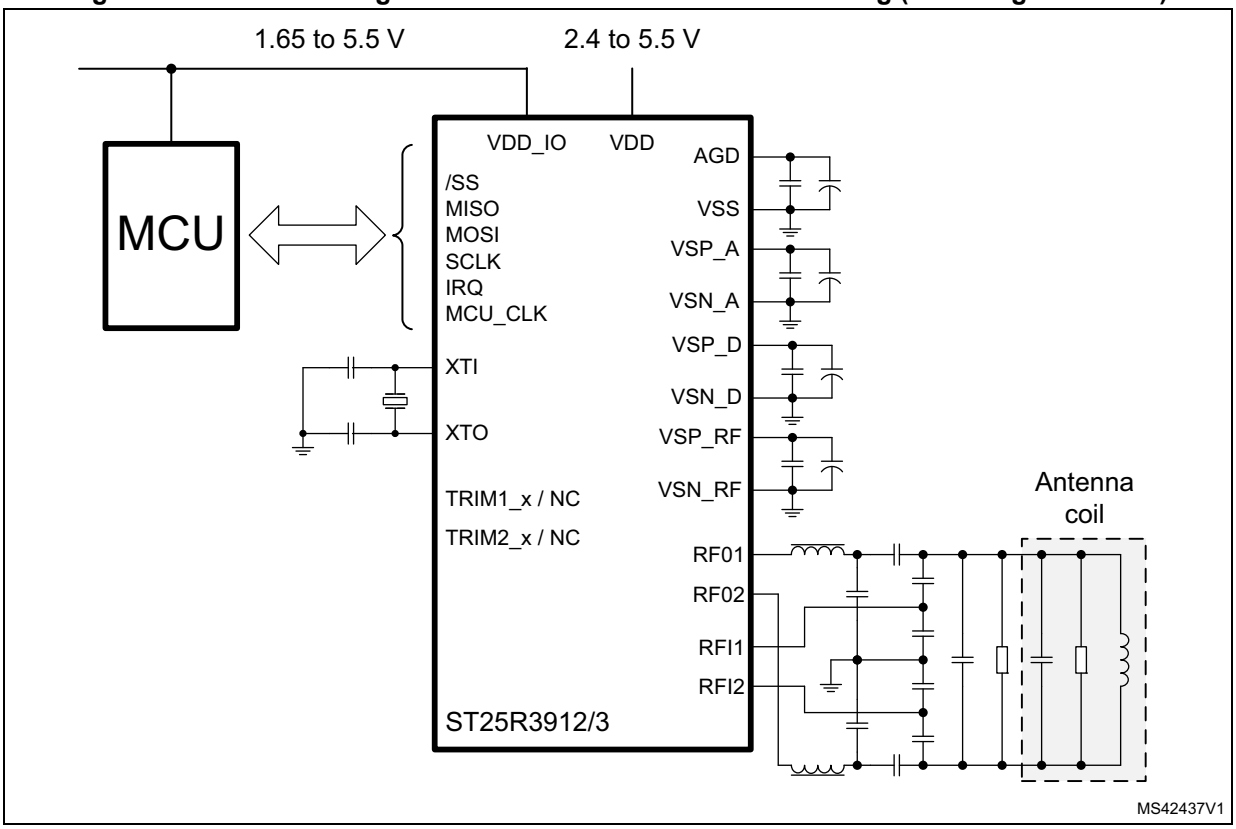


Figure 3. Minimum configuration with differential antenna driving (including EMC filter)



1.2.1 Operating modes

The ST25R3912/3 operating mode is defined by the contents of the *Operation Control Register*.

At power-up all bits of the *Operation Control Register* are set to 0, the ST25R3912/3 are in Power-down mode. In this mode AFE static power consumption is minimized, only the POR and part of the bias are active, while the regulators are transparent and are not operating. The SPI is still functional in this mode so all settings of ISO mode definition and configuration registers can be done.

Control bit en (bit 7 of the *Operation Control Register*) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in Ready mode. In this mode the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable.

Enable of receiver and transmitter are separated so it is possible to operate one without switching on the other (control bits rx_en and tx_en). In some cases this may be useful, if the reader field has to be maintained and there is no transponder response expected, the receiver can be switched-off to save current. Another example is the NFCIP-1 active communication receive mode in which the RF field is generated by the initiator and only the receiver operates.

Asserting the *Operation Control Register* bit wu while the other bits are set to 0 puts the ST25R3912/3 into the Wake-Up mode that is used to perform low power detection of card presence. In this mode the low power RC oscillator and register configurable Wake-Up timer

are used to schedule periodic measurement(s). When a difference of the measured value vs. the predefined reference is detected an interrupt is sent to wake-up the microcontroller.

1.2.2 Transmitter

The transmitter contains two identical push-pull driver blocks connected to the pins RFO1 and RFO2. These drivers are differentially driving the external antenna LC tank. It is also possible to operate only one of the two drivers by setting the *IO Configuration Register 1* bit single to 1. Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 2 Ω, when all segments are turned on; the output resistance is typically 1 Ω. All segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain segments when driving the non-modulated level to reduce the amplitude of the signal on the antenna and/or to reduce the antenna Q factor without making any hardware changes. The *RFO Normal Level Definition Register* defines which segments are turned on to define the normal transmission (non-modulated) level. Default setting is that all segments are turned on.

Using the single driver mode the number of the antenna LC tank components (and therefore the cost) is halved, but also the output power is reduced. In single mode it is possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the *IO Configuration Register 1* bit rfo2.

In order to transmit the data the transmitter output level needs to be modulated. Both AM and OOK modulation are supported. The type of modulation is defined by setting the bit tr_am in the *Auxiliary Definition Register*.

During the OOK modulation (for example ISO14443A) the transmitter drivers stop driving the carrier frequency. As consequence the amplitude of the antenna LC tank oscillation decays, the time constant of the decay is defined with the LC tank Q factor. The decay time in case of OOK modulation can be shortened by asserting the *Auxiliary Definition Register* bit ook_hr. When this bit is set to logic one the drivers are put in tristate during the OOK modulation.

AM modulation (for example ISO14443B) is done by increasing the output driver impedance during the modulation time. This is done by reducing the number of driver segments that are turned on. The AM modulated level can be automatically adjusted to the target modulation depth by defining the target modulation depth in the *AM Modulation Depth Control Register* and sending the Calibrate Modulation Depth direct command. Refer to *Section 1.2.19: AM modulation depth: definition and calibration* for further details.

Slow transmitter ramping

When the transmitter is enabled it starts to drive the antenna LC tank with full power, the ramping of the field emitted by antenna is defined by antenna LC tank Q factor.

However there are some reader systems where the reader field has to ramp up with a longer transition time when it is enabled. The STIF (Syndicat des transports d'Ile de France) specification requires a transition time from 10% to 90% of field longer than or equal to 10 µs.The ST25R3912/3 supports that feature. It is realized by collapsing VSP_RF regulated voltage when transmitter is disabled and ramping it when transmitter is enabled. Typical transition time is 15 µs at 3 V supply and 20 µs at 5 V supply.

Procedure to implement the slow transition:

1. When transmitter is disabled set *IO Configuration Register 2* bit slow_up to 1. Keep this state for at least 2 ms to allow discharge of VSP_RF.
2. Enable transmitter, its output will ramp slowly.
3. Before sending any command set the bit slow_up back to 0.

1.2.3 Receiver

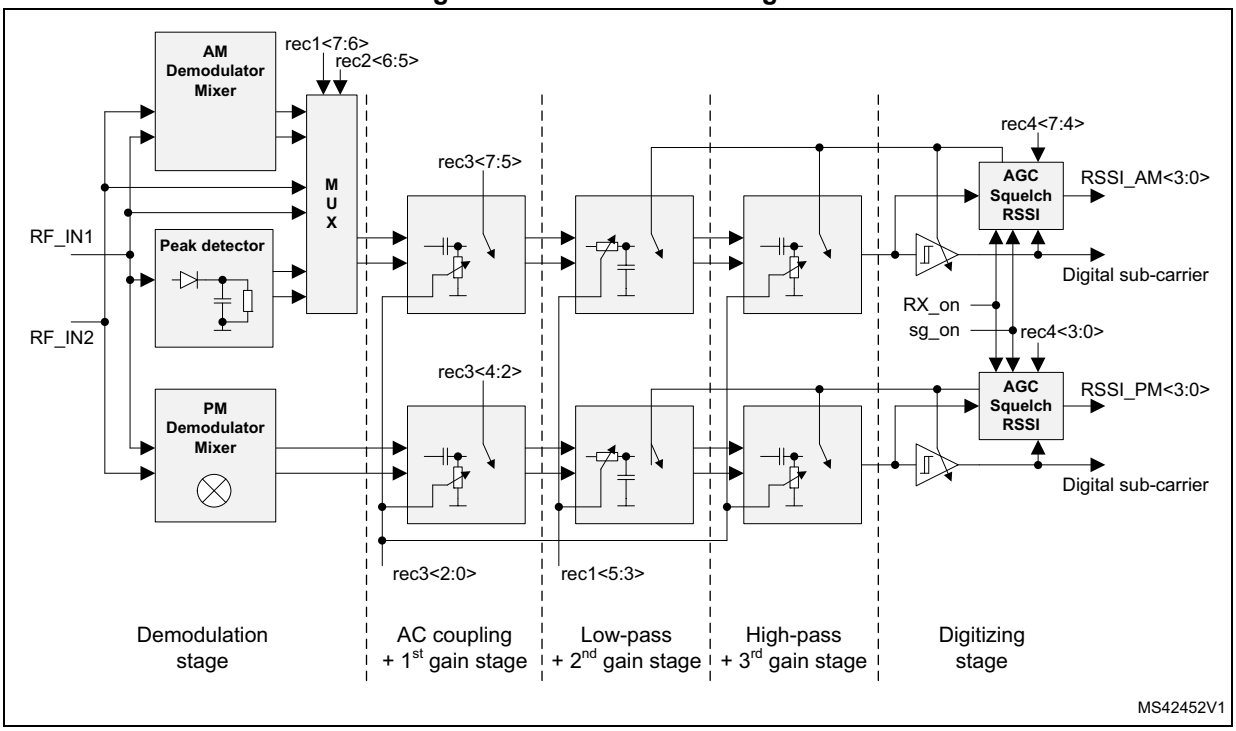
The receiver performs demodulation of the transponder sub-carrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM and/or PM demodulation, amplification, band-pass filtering and digitalization of sub-carrier signals. Additionally it performs RSSI measurement, automatic gain control (AGC) and Squelch.

In typical applications the receiver inputs RFI1 and RFI2 are outputs of capacitor dividers connected directly to the terminals of the antenna coil. This concept ensures that the two input signals are in phase with the voltage on the antenna coil. The design of the capacitive divider must ensure that the RFI1 and RFI2 input signal peak values do not exceed the V_{SP_A} supply voltage level.

The receiver comprises two complete receive channels, one for the AM demodulation and another one for the PM demodulation. In case both channels are active the selection of the channel used for reception framing is done automatically by the receive framing logic. The receiver is switched on when *Operation Control Register* bit rx_en is set to one. Additionally the *Operation Control Register* contains bits rx_chn and rx_man; rx_chn defines whether both, AM and PM, demodulation channels will be active or only one of them, while bit rx_man defines the channel selection mode in case both channels are active (automatic or manual). Operation of the receiver is controlled by four receiver configuration registers.

The operation of the receiver is additionally controlled by the signal rx_on that is set high when a modulated signal is expected on the receiver input. This signal is used to control RSSI and AGC and also enables processing of the receiver output by the framing logic. Signal rx_on is automatically set to high after the Mask Receive Timer expires. Signal rx_on can also be directly controlled by the controller by sending direct commands Mask Receive Data and Unmask Receive Data. *Figure 4* details the receiver block diagram.

Figure 4. Receiver block diagram



Demodulation stage

The first stage performs demodulation of the transponder sub-carrier signal, superimposed on the HF field carrier. Two different blocks are implemented for AM demodulation:

- Peak detector
- AM demodulator mixer.

The choice of the used demodulator is made by the *Receiver Configuration Register 1* bit amd_sel.

The peak detector performs AM demodulation using a peak follower. Both the positive and negative peaks are tracked to suppress any common mode signal. The peak detector is limited in speed; it can operate for sub-carrier frequencies up to fc/8 (1700 kHz). Its demodulation gain is G = 0.7. Its input is taken from one demodulator input only (usually RFI1).

The AM demodulator mixer uses synchronous rectification of both receiver inputs (RFI1 and RFI2). Its gain is G = 0.55.

By default the Peak detector is used, for data rates fc/8 and higher use of mixer is automatically preset by sending the direct command Analog Preset.

PM demodulation is also done by a mixer. The PM demodulator mixer has differential outputs with 60 mV differential signal for 1% phase change (16.67 mV / °). Its operation is optimized for sub-carrier frequencies up to fc/8 (1700 kHz).

In case the demodulation is done externally, it is possible to multiplex the LF signals applied to pins RFI1 and RFI2 directly to the gain and filtering stage by selecting the *Receiver Configuration Register 2* bit lf_en.

Filtering and gain stages

The receiver chain has band pass filtering characteristics. Filtering is optimized to pass sub-carrier frequencies while rejecting carrier frequency and low frequency noise and DC component. Filtering and gain is implemented in three stages, where the first and the last stage have first order high pass characteristics, and the second stage has second order low pass characteristic.

Gain and filtering characteristics can be optimized by writing the *Receiver Configuration Register 1* (filtering), the *Receiver Configuration Register 3* (gain in first stage) and the *Receiver Configuration Register 4* (gain in second and third stage).

The gain of the first stage is about 20 dB and can be reduced in six 2.5 dB steps. There is also a special boost mode available, which boosts the maximum gain by additional 5.5 dB. The first stage gain can only be modified by writing *Receiver Configuration Register 3*. The default setting of this register is the minimum gain. The default first stage zero is set at 60 kHz, it can also be lowered to 40 kHz or to 12 kHz by writing option bits in the *Receiver Configuration Register 1*. The control of the first and third stage zeros is done with common control bits (see *Table 1*).

Table 1. First and third stage zero setting

rec1<2> h200	rec1<1> h80	rec1<0> z12k	First stage zero	Third stage zero
0	0	0	60 kHz	400 kHz
1	0	0	60 kHz	200 kHz
0	1	0	40 kHz	80 kHz
0	0	1	12 kHz	200 kHz
0	1	1	12 kHz	80 kHz
1	0	1	12 kHz	200 kHz
Others			Not used	

The gain in the second and third stage is 23 dB and can be reduced in six 3 dB steps. The gain of these two stages is included in the AGC and Squelch loops. It can also be manually set in *Receiver Configuration Register 4*. Sending of direct command Reset Rx Gain is necessary to reset the AGC, Squelch and RSSI block. Sending this command clears the current Squelch setting and loads the gain reduction configuration from *Receiver Configuration Register 4* into the internal shadow registers of the AGC and Squelch block. The second stage has a second order low pass filtering characteristic, the pass band is adjusted according to the sub-carrier frequency using the bits lp2 to lp0 of the *Receiver Configuration Register 1*.

See *Table 2* for -1 dB cut-off frequency for different settings.

Table 2. Low pass control

rec1<5> lp2	rec1<4> lp1	rec1<3> lp0	-1 dB point
0	0	0	1200 kHz
0	0	1	600 kHz
0	1	0	300 kHz

Table 2. Low pass control (continued)

rec1<5> lp2	rec1<4> lp1	rec1<3> lp0	-1 dB point
1	0	0	2 MHz
1	0	1	7 MHz
Others			Not used

Table 3 provides information on the recommended filter settings. For all supported operation modes and receive bit rates there is an automatic preset defined, additionally some alternatives are listed. Automatic preset is done by sending direct command Analog Preset. There is no automatic preset for Stream and Transparent modes. Since the selection of the filter characteristics also modifies gain, the gain range for different filter settings is also listed.

Table 3. Receiver filter selection and gain range

rec1<5:3>lp<2:0>	rec1<2>h200	rec1<1>h80	rec1<0>z12k	Gain (dB)					Comments
				Max all	Min1 Max23	Max1 Min23	Min all	With boost	
000	0	0	0	43.4	28.0	26.4	11.0	49.8	Automatic preset for ISO14443A fc/128 and NFC Forum Type 1 Tag
000	1	0	0	44.0	29.0	27.5	12.0	49.7	Automatic preset for ISO14443B fc/128 ISO14443 fc/64
001	1	0	0	44.3	29	27.0	11.7	49.8	Recommended for 424/484 kHz sub-carrier
000	0	1	0	41.1	25.8	23.6	8.3	46.8	Alternative choice for ISO14443 fc/32 and fc/16
100	0	1	0	32.0	17.0	17.2	2.0	37.6	Automatic preset for ISO14443 fc/32 and fc/16 Alternative choice for fc/8 (1.7 kb/s)
100	0	0	0	32.0	17.0	17.2	2.0	37.6	Alternative choice for fc/8 (1.7 kb/s)
000	0	1	1	41.1	25.8	23.6	8.3	46.8	Automatic preset FeliCa™ (fc/64, fc/32) Alternative choice for ISO14443 fc/32 and fc/16
101	0	1	0	30.0	20.0	12.0	2.0	34.0	Alternative choice for fc/8 and fc/4
101	1	0	0	30.0	20.0	12.0	2.0	34.0	Automatic preset for fc/8 and fc/4
000	1	0	1	36.5	21.5	24.9	9.9	41.5	Automatic preset for NFCIP-1 (initiator and target)

Digitizing stage

The digitizing stage produces a digital representation of the sub-carrier signal coming from the receiver. This digital signal is then processed by the receiver framing logic. The digitizing stage consists of a window comparator with adjustable digitizing window (five possible settings, 3 dB steps, adjustment range from ±33 mV to ±120 mV). Adjustment of the digitizing window is included in the AGC and Squelch loops. In addition, the digitizing window can also be set manually in the *Receiver Configuration Register 4*.

AGC, Squelch and RSSI

As mentioned above, the second and third gain stage gain and the digitizing stage window are included in the AGC and Squelch loops. Eleven settings are available. The default state features minimum digitizer window and maximum gain. The first four steps increase the digitizer window in 3 dB steps, the next six steps additionally reduce the gain in the second and third gain stage, again in 3 dB steps. The initial setting with whom Squelch and AGC start is defined in *Receiver Configuration Register 4*. The *Gain Reduction State Register* displays the actual state of gain that results from Squelch, AGC and initial settings in *Receiver Configuration Register 4*. During bit anticollision like Type A, the AGC should be disabled.

Squelch

This feature is designed for operation of the receiver in noisy conditions. The noise can come from tags (caused by the processing of reader commands), or it can come from a noisy environment. This noise may be misinterpreted as start of transponder response, resulting in decoding errors.

During execution of the Squelch procedure the output of the digitizing comparator is observed. In case there are more than two transitions on this output in a 50 µs time period, the receiver gain is reduced by 3 dB, and the output is observed during the next 50 µs. This procedure is repeated until the number of transitions in 50 µs is lower or equal to two, or until the maximum gain reduction is reached. This gain reduction can be cleared sending the direct command Reset Rx Gain.

There are two possibilities of performing squelch: automatic mode and using the direct command Squelch.

1. Automatic mode is enabled in case bit sqm_dyn in the *Receiver Configuration Register 2* is set. It is activated automatically 18.88 µs after end of Tx and is terminated when the Mask Receive timer expires. This mode is primarily intended to suppress noise generated by tag processing during the time when a tag response is not expected (covered by Mask Receive timer).
2. Command Squelch is accepted in case it is sent when signal rx_on is low. It can be used when the time window in which noise is present is known by the controller.

AGC

AGC (Automatic Gain Control) is used to reduce gain to keep the receiver chain out of saturation. With gain properly adjusted the demodulation process is also less influenced by system noise.

AGC action starts when signal rx_on is asserted high and is reset when it is reset to low. At the high to low transitions of the rx_on signal the state of the receiver gain is stored in the *Gain Reduction State Register*. Reading this register at a later stage gives information on the gain setting used during last reception.

When AGC is switched on the receiver gain is reduced so that the input to the digitizer stage is not saturated. The AGC system comprises a comparator with a window 3.5 times larger than that of the digitizing window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on the output of its window comparator. This procedure ensures that the input to the digitizing window comparator is less than 3.5 times larger than its threshold.

AGC operation is controlled by the control bits agc_en, agc_m and agc_fast in the *Receiver Configuration Register 2*. Bit agc_en enables the AGC operation, bit agc_m defines the AGC mode, and bit agc_alg defines the AGC algorithm.

Two AGC modes are available. The AGC can operate during the complete Rx process (as long as signal rx_on is high), or it can be enabled only during the first eight sub-carrier pulses.

Two AGC algorithms are available. The AGC can either start by presetting code 4h (max digitizer window, max gain) or by resetting the code to 0h (min digitizer window, max gain).

The algorithm with preset code is faster, therefore it is recommended for protocols with short SOF (like ISO14443A fc/128).

Default AGC settings are:

- AGC is enabled
- AGC operates during complete Rx process
- algorithm with preset is used.

RSSI

The receiver also performs the RSSI (Received Signal Strength Indicator) measurement for both channels. The RSSI measurement is started after the rising edge of rx_on. It stays active as long as signal rx_on is high, it is frozen while rx_on is low. The RSSI is a peak hold system, and the value can only increase from the initial zero value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from zero. Result of RSSI measurements is a 4-bit value that can be observed by reading the *RSSI Display Register*. The LSB step is 2.8 dB, and the maximum code is Dh (13d).

Since the RSSI measurement is of peak hold type the RSSI measurement result does not follow any variations in the signal strength (the highest value will be kept). In order to follow RSSI variations it is possible to reset the RSSI bits and restart the measurement by sending the direct command Clear RSSI.

Receiver in NFCIP-1 active communication mode

There are several features built into the receiver to enable reliable reception of active NFCIP-1 communication. All these settings are automatically preset by sending the direct command Analog Preset after the NFCIP-1 mode has been configured. In addition to the filtering options, there are two NFCIP-1 active communication mode specific configuration bits stored in the *Receiver Configuration Register 3*.

Bit lim enables clipping circuits that are positioned after the first and second gain stages. The function of the clipping circuits is to limit the signal level for the following filtering stage (when the NFCIP-1 peer is close the input signal level can be quite high).

Bit rg_nfc forces gain reduction of second and third filtering stage to -6 dB while keeping the digitizer comparator window at maximum level.

1.2.4 Wake-Up mode

Asserting the *Operation Control Register* bit wu while the other bits are set to 0 puts the ST25R3912/3 in Wake-Up mode, used to perform low power detection of card presence. The ST25R3912/3 include several possibilities of low power detection of a card presence (phase measurement, amplitude measurement). An integrated low power 32 kHz RC

oscillator and a register configurable Wake-Up timer are used to schedule periodic detection.

Usually the presence of a card is detected by a so-called polling loop. In this process the reader field is periodically turned on and the controller checks whether a card is present using RF commands. This procedure consumes a lot of energy since the reader field has to be turned on for 5 ms before a command can be issued.

Low power detection of card presence is performed by detecting a change in the reader environment, produced by a card. When a change is detected, an interrupt is sent to the controller. As a result, the controller can perform a regular polling loop.

In the Wake-Up mode the ST25R3912/3 periodically perform the configured reader environment measurements and sends an IRQ to the controller when a difference to the configured reference value is detected.

Detection of card presence can be done by performing phaseand amplitude measurements.

Presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal phase and amplitude. The reader field activation time needed to perform the phase or the amplitude measurement is extremely short (~20 µs) compared to the activation time needed to send a protocol activation command.

Additionally the power level during the measurement can be lower than the power level during normal operation since the card does not have to be powered to produce a coupling effect. The emitted power can be reduced by changing the *RFO Normal Level Definition Register*.

The registers on locations from 31h to 3Dh are dedicated to Wake-Up timer configuration and display. The *Wake-Up Timer Control Register* is the main Wake-Up mode configuration register. The timeout period between the successive detections and the measurements are selected in this register. Timeouts in the range from 10 to 800 ms are available, 100 ms is the default value. Any combination of available measurements can be selected (one, two or all of them).

The next twelve registers (32h to 3Dh) are configuring the three possible detection measurements and storing the results, four registers are used for each measurement.

An IRQ is sent when the difference between a measured value and the reference value is larger than the configured threshold value. There are two possible definitions for the reference value:

1. The ST25R3912/3 can calculate the reference based on previous measurements (auto-averaging)
2. The controller determines the reference and stores it in a register

The first register in the series of four is the *Amplitude Measurement Configuration Register*. The difference to the reference value that triggers the IRQ, the method of reference value definition and the weight of the last measurement result in case of auto-averaging are defined in this register. The next register is storing the reference value in case the reference is defined by the controller. The following two registers are display registers. The first one stores the auto-averaging reference, and the second one stores the result of the last measurement.

The Wake-Up mode configuration registers have to be configured before the Wake-Up mode is entered. Any modification of the Wake-Up mode configuration while it is active may result in unpredictable behavior.

Auto-averaging

In case of auto-averaging the reference value is recalculated after every measurement as

NewAverage = OldAverage + (MeasuredValue - OldAverage) / Weight

The calculation is done on 13 bits to have sufficient precision.The auto-averaging process is initialized when the Wake-Up mode is entered for the first time after initialization (at power-up or after Set Default command). The initial value is taken from the measurement display registers (for example *Amplitude Measurement Display Register*) until the content of this register is not zero.

Every Measurement Configuration register contains a bit that defines whether the measurement that causes an interrupt is taken in account for the average value calculation (for example bit am_aam of the *Amplitude Measurement Configuration Register*).

1.2.5 Quartz crystal oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. The operation of quartz crystal oscillator is enabled when the *Operation Control Register* bit en is set to one. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable (see *Section 1.3.24: Main Interrupt Register*).

The status of oscillator can be observed by observing the *Auxiliary Display Register* bit osc_ok. This bit is set to ‘1’ when oscillator frequency is stable.

The oscillator is based on an inverter stage supplied by a controlled current source. A feedback loop is controlling the bias current in order to regulate amplitude on XTI pin to 1 V_{pp}.

To enable a fast reader start-up an interrupt is sent when the oscillator amplitude exceeds 750 mV_{pp}.

Division by two ensures that 13.56 MHz signal has a duty cycle of 50%, which is better for the transmitter performance (no PW distortion). Use of 27.12 MHz crystal is therefore recommended for better performance.

In case of 13.56 MHz crystal, the bias current of stage that is digitizing oscillator signal is increased to assure as low PW distortion as possible.

The oscillator output is also used to drive a clock signal output pin MCU_CLK) that can be used by the external microcontroller. The MCU_CLK pin is configured in the *IO Configuration Register 2*.

1.2.6 Timers

The ST25R3912/3 contains several timers that eliminate the need to run counters in the controller, thus reducing the effort of the controller code implementation and improve portability of code to different controllers.

Every timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers have to be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active may result in unpredictable behavior.

All timers except the Wake-Up timer are stopped by direct command Clear.

Note: In case bit nrt_emv in the General Purpose and No-Response Timer Control Register is set to one, the No-Response timer is not stopped

Mask Receive timer and No-Response timer

Mask Receive timer and No-Response timer are both automatically started at the end of transmission (at the end of EOF).

Mask Receive timer

The Mask Receive timer is blocking the receiver and reception process in framing logic by keeping the rx_on signal low after the end of Tx during the time the tag reply is not expected.

While the Mask Receive timer is running, the Squelch is automatically turned on (if enabled). Mask Receive timer does not produce an IRQ.

The Mask Receive timer timeout is configured in the *Mask Receive Timer Register*.

In the NFCIP-1 active communication mode the Mask Receive timer is started when the peer NFC device (a device with whom communication is going on) switches on its field.

The Mask Receive timer has a special use in the low power Initial NFC Target Mode. After the initiator field has been detected the controller turns on the oscillator, regulator and receiver. Mask Receive timer is started by sending direct command Start Mask Receive Timer. After the Mask Receive Timer expires the receiver output starts to be observed to detect start of the initiator message. In this mode the Mask Receive timer clock is additionally divided by eight it (one count is 512/fc) to cover range up to about 9.6 ms.

No-Response timer

As its name indicates, this timer is intended to observe whether a tag response is detected in a configured time started by end of transmission. The I_nre flag in the *Timer and NFC Interrupt Register* is signaling interrupt events resulting from this timer timeout.

The No-Response timer is configured by writing the two registers *No-Response Timer Register 1* and *No-Response Timer Register 2*. Operation options of the No-Response timer are defined by setting bits nrt_emv and nrt_step in the *General Purpose and No-Response Timer Control Register*.

Bit nrt_step configures the time step of the No-Response timer. Two steps are available, 64/fc (4.72 µs) to cover range up to 309 ms, and 4096/fc, covering the range up to 19.8 s.

Bit nrt_emv controls the timer operation mode:

- When this bit is set to 0 (default mode) the IRQ is produced in case the No-Response Timer expires before a start of a tag reply is detected and rx_on is forced to low to stop receiver process. In the opposite case, when start of a tag reply is detected before timeout, the timer is stopped, and no IRQ is produced.
- When this bit is set to 1 the timer unconditionally produces an IRQ when it expires, it is also not stopped by direct command Clear. This means that IRQ is independent of the fact whether or not a tag reply was detected. In case at the moment of timeout a tag reply is being processed no other action is taken, in the opposite case, when no tag response is being processed additionally the signal rx_on is forced to low to stop receive process.

The No-Response timer can also be started using direct command Start No-Response Timer. The intention of this command is to extend the No-Response timer timeout beyond the range defined in the No-Response timer control registers. In case this command is sent while the timer is running, it is reset and restarted. In NFCIP-1 active communication mode the No-Response timer cannot be started using the direct command.

In case this timer expires before the peer NFC device (a device with whom communication is going on) switches on its field an interrupt is sent.

In all modes, where timer is set to nonzero value, it is a must that M_txe is not set and interrupt I_txe is read via SPI for synchronization between transmitter and timer.

General Purpose timer

The triggering of the General Purpose timer is configured by setting the *General Purpose and No-Response Timer Control Register*. It can be used to survey the duration of the reception process (triggering by start of reception, after SOF) or to time out the PCD to PICC response time (triggered by end of reception, after EOF). In the NFCIP-1 active communication mode it is used to timeout the field switching off. In all cases an IRQ is sent when it expires.

The General Purpose timer can also be started by sending the direct command Start General Purpose Timer. In case this command is sent while the timer is running, it is reset and restarted.

Wake-Up timer

Wake timer is primarily used in the Wake-Up mode (see *Section 1.2.4: Wake-Up mode*). Additionally it can be used by sending a direct command Start Wake-Up Timer. This command is accepted in any operation mode except Wake-Up mode. When this command is sent the RC oscillator used as clock source for Wake-Up timer is started, timeout is defined by setting in the *Wake-Up Timer Control Register*. When the timer expires, an IRQ with the I_wt flag in the *Error and Wake-Up Interrupt Register* is sent.

Wake-Up timer is useful in the Low Power operation mode, in which other timers cannot be used (in the Low Power operation mode the crystal oscillator, which is clock source for the other timers, is not running).

Note: The tolerance of Wake-Up timer timeout is defined by tolerance of the RC oscillator.

1.2.7 A/D converter

The ST25R3912/3 contain an 8-bit successive approximation A/D converter. Inputs to the A/D converter can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of the last A/D conversion is stored in the *A/D Converter Output Register*.

The A/D converter has two operating modes, absolute and relative.

- In absolute mode the low reference is 0 V and the high reference is 2 V. This means that A/D converter input range is from 0 to 2 V, 00h code means input is 0 V or lower, FFh means that input is 2 V - 1 LSB or higher (LSB is 7.8125 mV).
- In relative mode low reference is 1/6 of V_{SP_A} and high reference is 5/6 of V_{SP_A}, so the input range is from 1/6 to 5/6 V_{SP_A}.

Relative mode is only used in phase measurement (phase detector output is proportional to power supply). In all other cases absolute mode is used.

1.2.8 Phase and amplitude detector

This block is used to provide input to A/D converter to perform measurements of amplitude and phase, expected by direct commands Measure Amplitude and Measure Phase. Several

phase and amplitude measurements are also performed by direct commands Calibrate Modulation Depth and Calibrate Antenna.

Phase detector

The phase detector is observing phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals RFI1 and RFI2, which are proportional to the signal on the antenna LC tank. These signals are first elaborated by digitizing comparators, then digitized signals are processed by a phase detector with a strong low pass filter to get average phase difference.

The phase detector output is inversely proportional to the phase difference between the two inputs. The 90° phase shift results in $V_{SP\_A}/2$ output voltage, in case both inputs are in phase output voltage is V_{SP_A}, in case they are in opposite phase output voltage is 0 V. During execution of direct command Measure Phase this output is multiplexed to A/D converter input (A/D converter is in relative mode during execution of command Measure Phase). Since the A/D converter range is from 1/6 to 5/6 V_{SP_A} the actual phase detector range is from 30º to 150º.

Figure 5 and *Figure 6* show the two inputs and the output of phase detector, respectively, in case of 90º and 135º shifts.

Figure 5. Phase detector inputs and output in case of 90º phase shift

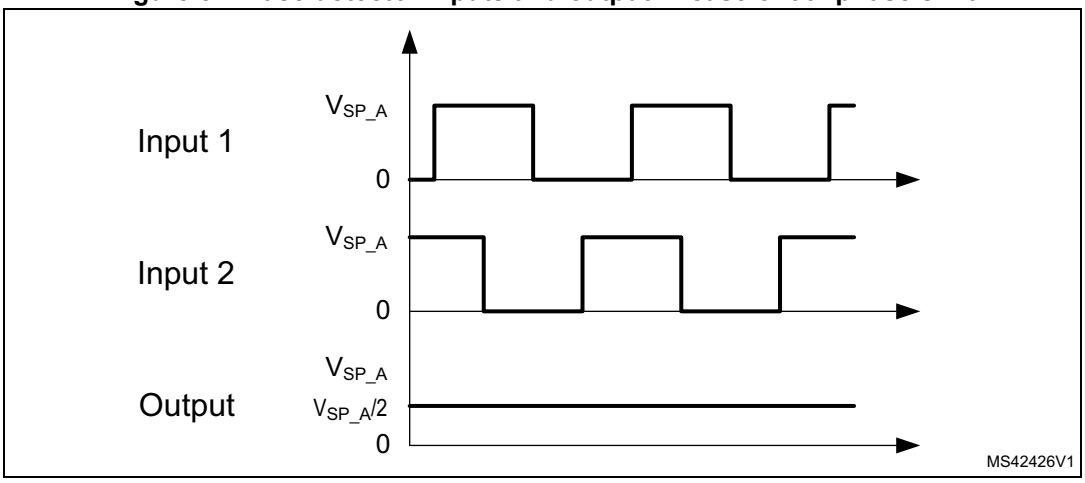
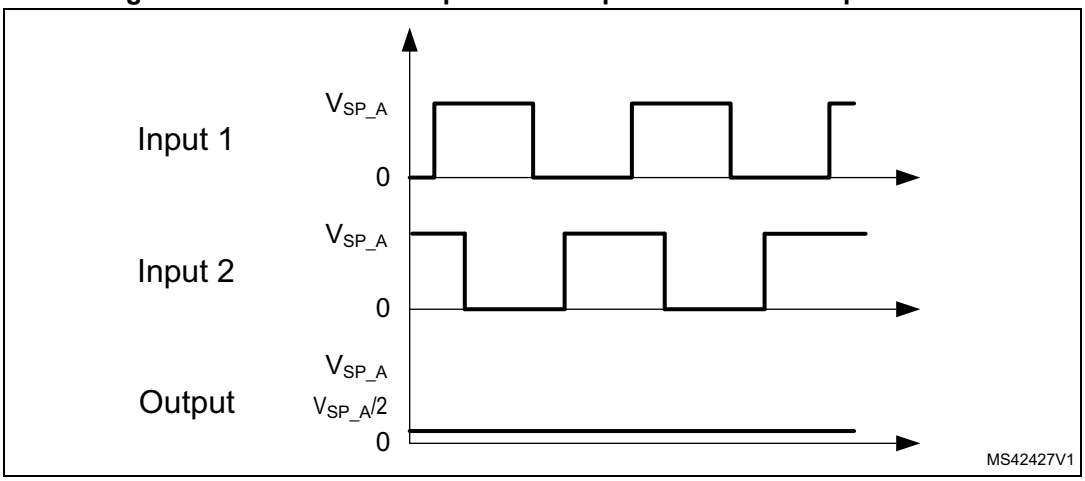


Figure 6. Phase detector inputs and output in case of 135º phase shift



Amplitude detector

Signals from pins RFI1 and RFI2 are used as inputs to the self-mixing stage. The output of this stage is a DC voltage proportional to amplitude of signal on pins RFI1 and RFI2. During execution of direct command Measure Amplitude this output is multiplexed to A/D converter input.

1.2.9 External field detector

The External Field Detector is used to detect the presence of an external device generating an RF field. It is automatically switched on in NFCIP-1 active communication modes; it can also be used in other modes. The External field detector supports two different detection thresholds, Peer Detection Threshold and Collision Avoidance Threshold. The two thresholds can be independently set by writing the *External Field Detector Threshold Register*. The actual state of the External field detector output can be checked by reading the *Auxiliary Display Register*. Input to this block is the signal from the RFI1 pin.

Peer detection threshold

This threshold is used to detect the field emitted by peer NFC device with whom NFC communication is going on (initiator field in case the ST25R3912/3 are targets and the opposite, target field in case the ST25R3912/3 areinitiators). It can be selected in the range from 75 to 800 mV_{pp}. When this threshold is enabled the External Field Detector is in low power mode. An interrupt is generated when an external field is detected and also when it is switched off. With such implementation it can also be used to detect the moment when the external field disappears. This is useful to detect the moment when the peer NFC device (it can be either an initiator or a target) has stopped emitting an RF field.

The External Field Detector is automatically enabled in the low power Peer Detection mode when NFCIP-1 mode (initiator or target) is selected in the *Bit Rate Definition Register*.

Additionally it can be enabled by setting bit en_fd in the *Auxiliary Definition Register*.

Collision Avoidance threshold

This threshold is used during the RF Collision Avoidance sequence that is executed by sending NFC Field ON commands (see *NFC Field ON commands*). It can be selected in the range from 25 to 800 mV_{pp}.

1.2.10 Power supply system

The ST25R3912/3 (*Figure 7*) features two positive supply pins, VDD and VDD_IO.

VDD is the main power supply pin. It supplies the ST25R3912/3 blocks through three regulators (VSP_A, VSP_D and VSP_RF).

V_{DD} range from 2.4 to 5.5 V is supported.

V_{DD_IO} is used to define supply level for digital communication pins (/SS, MISO, MOSI, SCLK, IRQ, MCU_CLK). Digital communication pins interface with ST25R3912/3 logic through level shifters, therefore the internal supply voltage can be either higher or lower than V_{DD_IO}. V_{DD_IO} range from 1.65 to 5.5 V is supported.

Figure 7. ST25R3912/3 power supply

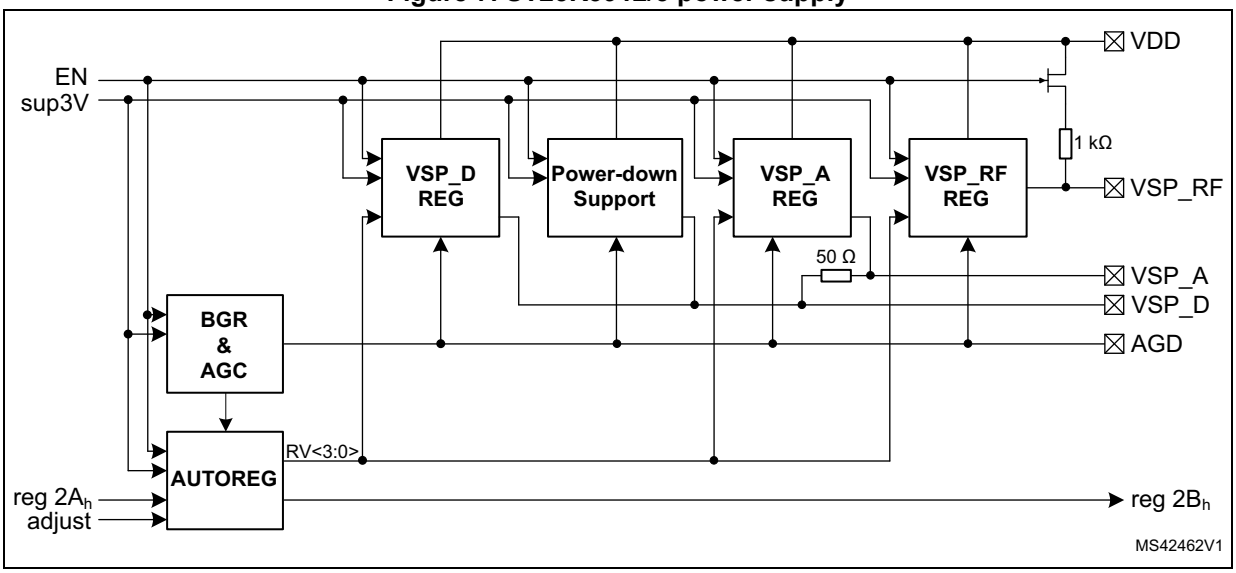


Figure 7 shows the building blocks of the ST25R3912/3 power supply system and the signals that control it.

The power supply system contains three regulators, a power-down support block, a block generating analog reference voltage (AGD) and a block performing automatic power supply adjustment procedure. The three regulators are providing supply to analog blocks (VSP_A), logic (VSP_D) and transmitter (VSP_RF). The use of VSP_A and VSP_D regulators is mandatory at 5 V power supply to provide regulated voltage to analog and logic blocks that only use 3.3 V devices. The use of VSP_A and VSP_D regulators at 3 V supply and VSP_RF regulator at any supply voltage is recommended to improve system PSRR.

Regulated voltage can be adjusted automatically to have maximum possible regulated voltage while still having good PSRR. All regulator pins also have corresponding negative supply pins that are externally connected to ground potential (VSS). The reason for separation is in decoupling of noise induced by voltage drops on the internal power supply lines.

Figure 2 and *Figure 3* show typical ST25R3912/3 application schematics with all regulators used. All regulator pins and AGD voltage are buffered with capacitors. Recommended blocking capacitor values are detailed in *Table 4*.

Table 4. Recommended blocking capacitor values

Pins	Recommended capacitors
AGD-VSS	1 µF, in parallel with 10 nF
VSP_A-VSN_A VSP_D-VSN_D	2.2 µF, in parallel with 10 nF 2.2 µF, in parallel with 10 nF
VSP_RF-VSN_RF	2.2 µF, in parallel with 10 nF

Regulators have two basic operation modes depending on supply voltage, 3.3 V supply mode (max 3.6 V) and 5 V supply mode (max 5.5 V). The supply mode is set by writing bit sup3 V in the *IO Configuration Register 2*. Default setting is 5 V, hence this bit has to be set to one after power-up in case of 3.3 V supply.

In 3.3 V mode all regulators are set to the same regulated voltage in range from 2.4 V to 3.4 V, while in 5 V only the VSP_RF can be set in range from 3.9 V to 5.1 V, while VSP_A and VSP_D are fixed to 3.4 V.

The regulators are operating when signal en is high (en is configuration bit in *Operation Control Register*. When signal en is low the ST25R3912/3 isare in low power Power-down mode. In this mode consumption of the power supply system is also minimized.

VSP_RF regulator

The intention of this regulator is to improve PSRR of the transmitter (the noise of the transmitter power supply is emitted and fed back to the receiver). The VSP_RF regulator operation is controlled and observed by writing and reading two regulator registers:

- *Regulator Voltage Control Register* controls the regulator mode and regulated voltage. Bit reg_s controls regulator mode. In case it is set to 0 (default state) the regulated voltage is set using direct command Adjust Regulators. When bit reg_s is asserted to 1 regulated voltage is defined by bits rege_3 to rege_1 of the same register. The regulated voltage adjustment range depends on the power supply mode. In case of 5 V supply mode the adjustment range is between 3.9 V and 5.1 V in steps of 120 mV, in case of 3.3 V supply mode the adjustment range is from 2.4 V to 3.4 V with steps of 100 mV. Default regulated voltage is the maximum one (5.1 V and 3.4 V in case of 5 V and 3.3 V supply mode respectively).
- *Regulator and Timer Display Register* is a read only register that displays actual regulated voltage when regulator is operating. It is especially useful in case of automatic mode, since the actual regulated voltage, which is the result of direct command Adjust Regulators, can be observed.

The VSP_RF regulator also includes a current limiter that limits the regulator typically to current of 200 mA_{rms} in normal operation (500 mA in case of short). In case the transmitter output current higher the 200 mA_{rms} is required, VSP_RF regulator cannot be used to supply the transmitter, VSP_RF has to be externally connected to VDD (connection of VSP_RF to supply voltage higher than V_{DD} is not allowed).

The voltage drop of the transmitter current is the main source of the ST25R3912/3 power dissipation. This voltage drop is composed of drop in the transmitter driver and in the drop on VSP_RF regulator. Due to this it is recommended to set regulated voltage using direct command Adjust Regulators. It results in good power supply rejection ration with relatively low dissipated power due to regulator voltage drop.

In Power-down mode the VSP_RF regulator is not operating.

VSP_RF pin is connected to VDD through 1 kΩ resistor.

Connection through resistors ensures smooth power-up of the system and a smooth transition from Power-down mode to other operating modes.

VSP_A and VSP_D regulators

VSP_A and VSP_D regulators are used to supply the ST25R3912/3 analog and digital blocks respectively. In 3.3 V mode, VSP_A and VSP_D regulator are set to the same regulated voltage as the VSP_RF regulator, in 5 V mode VSP_A and VSP_D regulated voltage is fixed to 3.4 V.

The use of VSP_A and VSP_D regulators is obligatory in 5 V mode since analog and digital blocks supplied with these two pins contain low voltage transistors that support maximum supply voltage of 3.6 V. In 3.3 V supply mode the use of regulators is strongly recommended in order to improve PSRR of analog processing.

For low cost applications it is possible to disable the VSP_D regulator and to supply digital blocks through external short between VSP_A and VSP_D (configuration bit vspd_off in the *IO Configuration Register 2*. In case VSP_D regulator is disabled VSP_D can alternatively be supplied from VDD (in 3.3 V mode only) in case VSP_A is not more than 300 mV lower than VDD.

Power-down support block

In the Power-down mode the regulators are disabled in order to save current. In this mode a low power Power-down support block that maintains the VSP_D and VSP_A in below 3.6 V is enabled. Typical regulated voltage in this mode is 3.1 V at 5 V supply and 2.2 V at 3 V supply. When 3.3 V supply mode is set the Power-down support block is disabled, its output is connected to VDD through 1 kΩ resistor.

Typical consumption of Power-down support block is 600 nA at 5 V supply.

Measurement of supply voltages

Using direct command Measure Power Supply it is possible to measure VDD and regulated voltages VSP_A, VSP_D, and VSP_RF.

1.2.11 Communication with an external microcontroller

The ST25R3912/3 are slave devices and the external microcontroller initiates all communication. Communication is performed by a 4-wire Serial Peripheral Interface (SPI). The ST25R3912/3 send an interrupt request (pin IRQ) to the microcontroller, which can use clock signal available on pin MCU_CLK when the oscillator is running.

Serial Peripheral Interface (SPI)

While signal /SS is high the SPI interface is in reset, while it is low the SPI is enabled. It is recommended to keep /SS high whenever the SPI is not in use. MOSI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). First two bits of first byte transmitted after high to low transition of /SS define SPI operation mode.

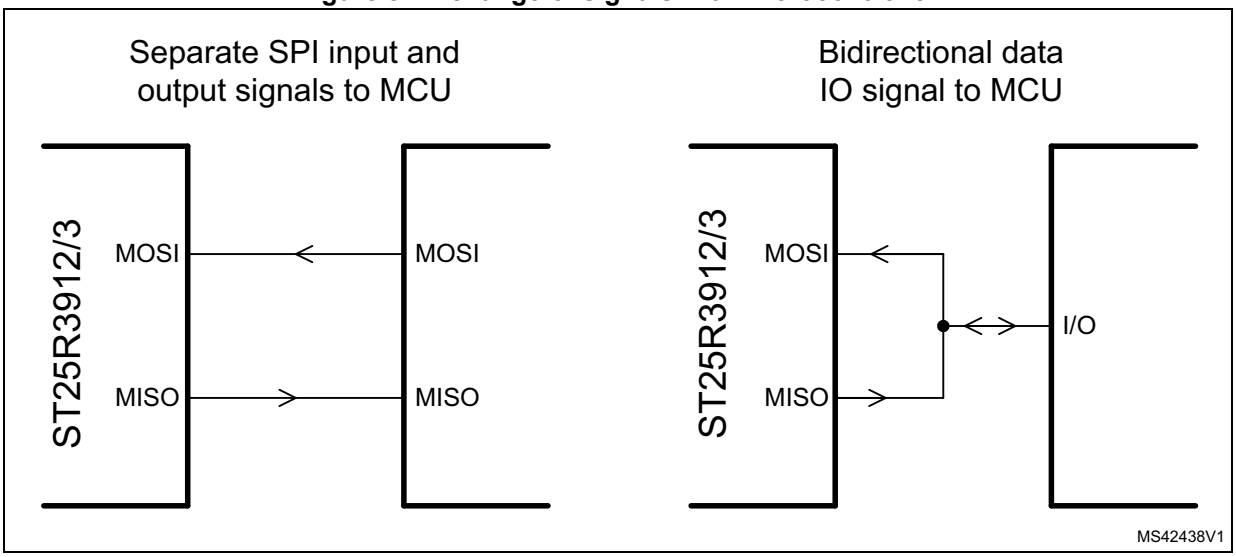
Table 5. Serial data interface (4-wire interface) signal lines

Name	Signal	Signal level	Description
/SS	Digital input	CMOS	SPI Enable (active low)
MOSI	Digital input		Serial data input
MISO	Digital output with tristate		Serial data output
SCLK	Digital input		Clock for serial communication

MSB bit is always transmitted first (valid for address and data).

Read and Write modes support address auto-incrementing. This means that if some additional data bytes are sent/read after the address and first data byte, they are written to/read from addresses incremented by '1'. *Figure 8* defines possible modes.

Figure 8. Exchange of signals with microcontroller



MISO output is usually in tristate, it is only driven when output data is available. Due to this the MOSI and the MISO can be externally shorted to create a bidirectional signal.

During the time the MISO output is in tristate, it is possible to switch on a 10 kΩ pull down by activating option bits miso_pd1 and miso_pd2 in the *IO Configuration Register 2*.

Table 6 provides information on the SPI operation modes. Reading and writing of registers is possible in any ST25R3912/3 operation mode. FIFO operations are possible in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Table 6. SPI operation modes

Mode	Pattern (communication bits)								Related data
	Mode		Trailer						
	M1	M0	C5	C4	C3	C2	C1	C0	
Register Write	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing)
Register Read	0	1	A5	A4	A3	A2	A1	A0	

Table 6. SPI operation modes (continued)

Mode	Pattern (communication bits)								Related data
	Mode		Trailer						
	M1	M0	C5	C4	C3	C2	C1	C0	
FIFO Load	1	0	0	0	0	0	0	0	One or more bytes of FIFO data
FIFO Read	1	0	1	1	1	1	1	1	
DirectCommand Mode	1	1	C5	C4	C3	C2	C1	C0	-

Writing data to addressable registers (Write mode)

Figure 9 and *Figure 10* show cases of writing a single byte and writing multiple bytes with auto-incrementing address. After the SPI operation mode bits, the address of register to be written is provided. Then one or more data bytes are transferred from the SPI, always from the MSB to the LSB. The data byte is written in register on falling edge of its last clock. In case the communication is terminated by putting /SS high before a packet of 8 bits (one byte) is sent, writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register no write is performed.

Figure 9. SPI communication: writing a single byte

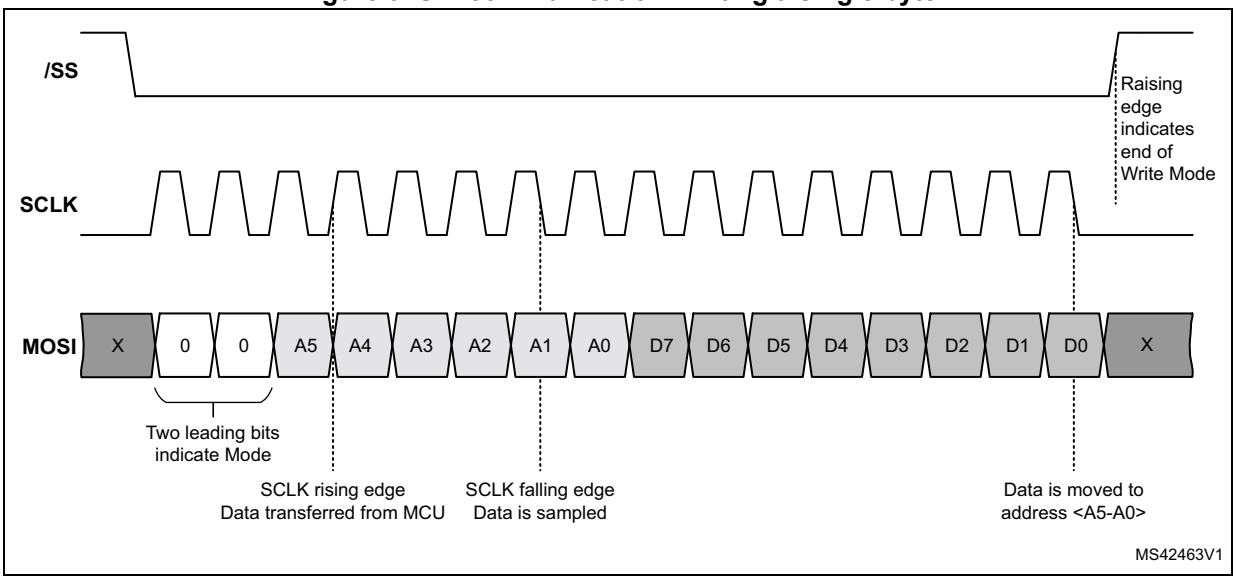
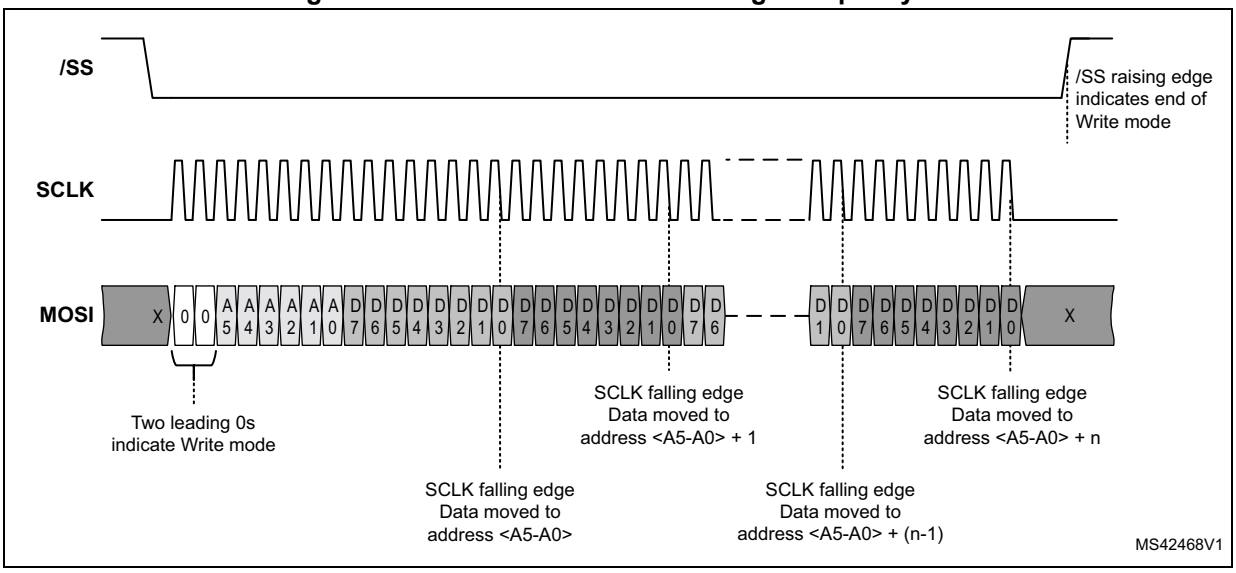


Figure 10. SPI communication: writing multiple bytes



Reading data from addressable registers (Read mode)

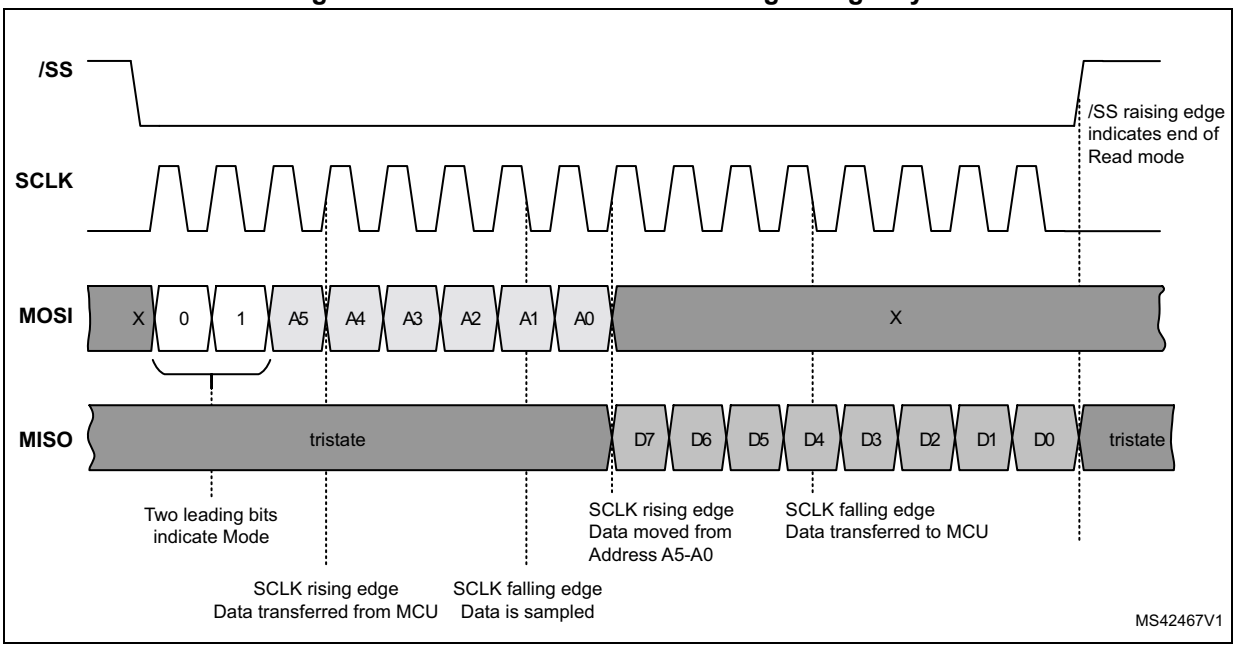
After the SPI operation mode bits the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes are transferred to MISO output, always from the MSB to the LSB. As in case of the write mode also the read mode supports auto-incrementing address.

MOSI is sampled at the falling edge of SCLK (like shown in the following diagrams), data to be read from the ST25R3912/3 internal register is driven to MISO pin on rising edge of SCLK and is sampled by the master at the falling edge of SCLK.

In case the register on defined address does not exist all 0 data is sent to MISO.

Figure 11 is an example for reading of single byte.

Figure 11. SPI communication: reading a single byte

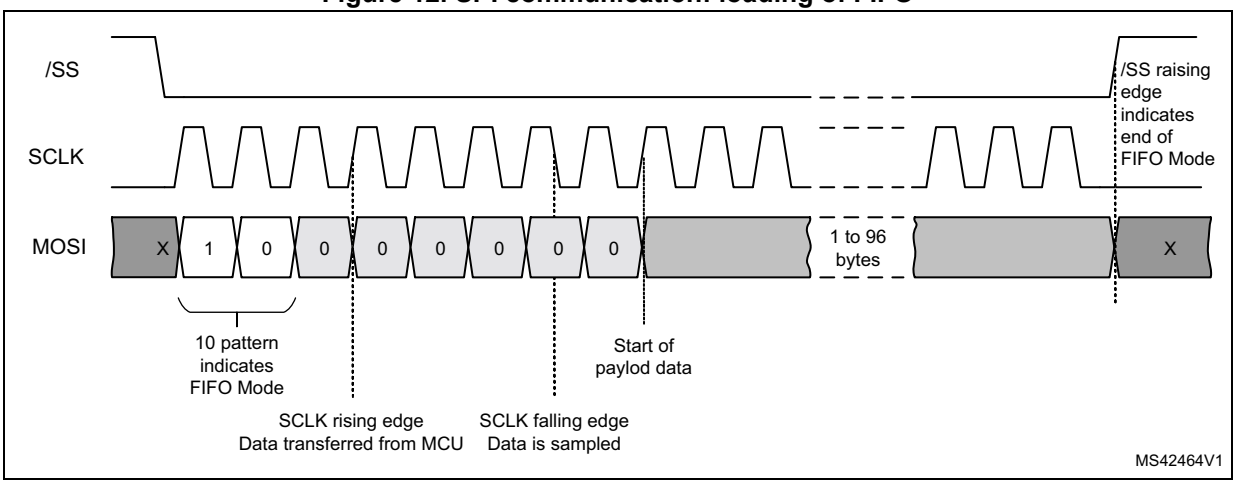


Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. Difference is that in case of loading more bytes all bytes go to the FIFO. SPI operation mode bits 10 indicate FIFO operations. In case of loading transmitting data into FIFO all bits <C5 – C0> are set to 0. Then a bit-stream, the data to be sent (1 to 96 bytes), can be transferred. In case the command is terminated by putting /SS high before a packet of 8 bits (one byte) is sent, writing of that particular byte in FIFO is not performed.

Figure 12 shows how to load the Transmitting Data into the FIFO.

Figure 12. SPI communication: loading of FIFO

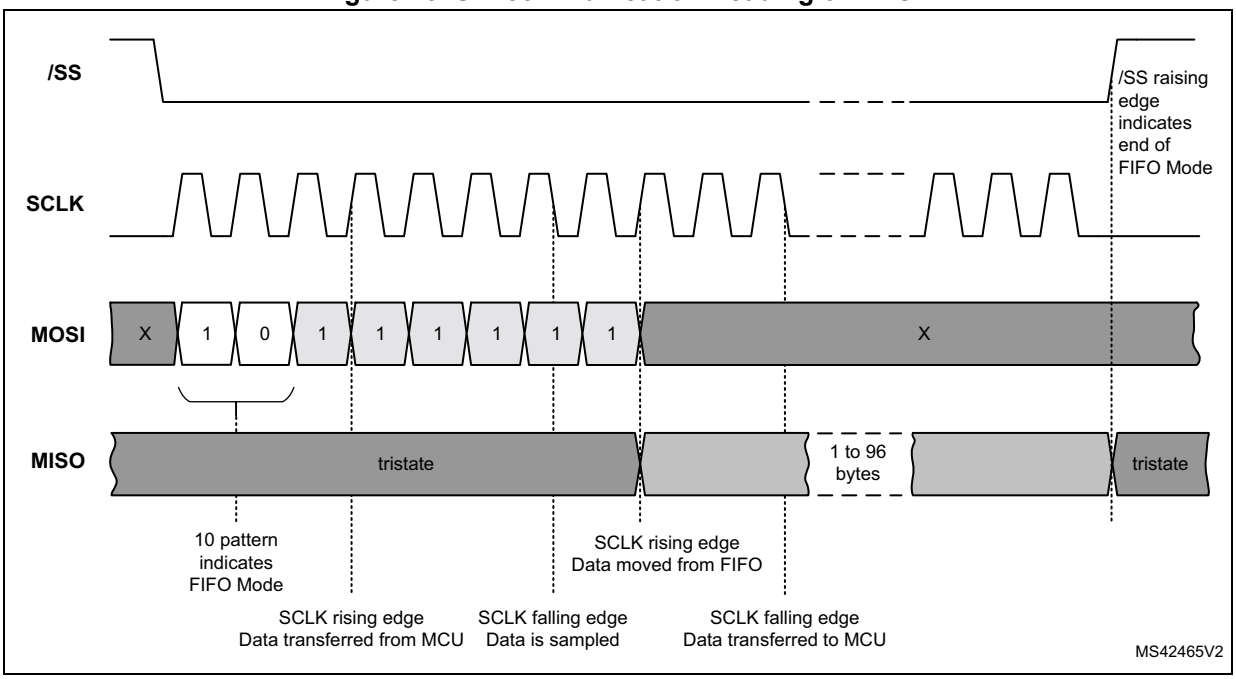


Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. Difference is that in case of reading more bytes they all come from the FIFO. SPI

operation mode bits 10 indicate FIFO operations. In case of reading the received data from the FIFO all bits <C5 – C0> are set to 1. On the following SCLK rising edges the data from FIFO appears as in case of read data from addressable registers. If the command is terminated by putting /SS high before a packet of 8 bits (one byte) is read, that particular byte is considered unread and will be the first one read in next FIFO read operation.

Figure 13. SPI communication: reading of FIFO

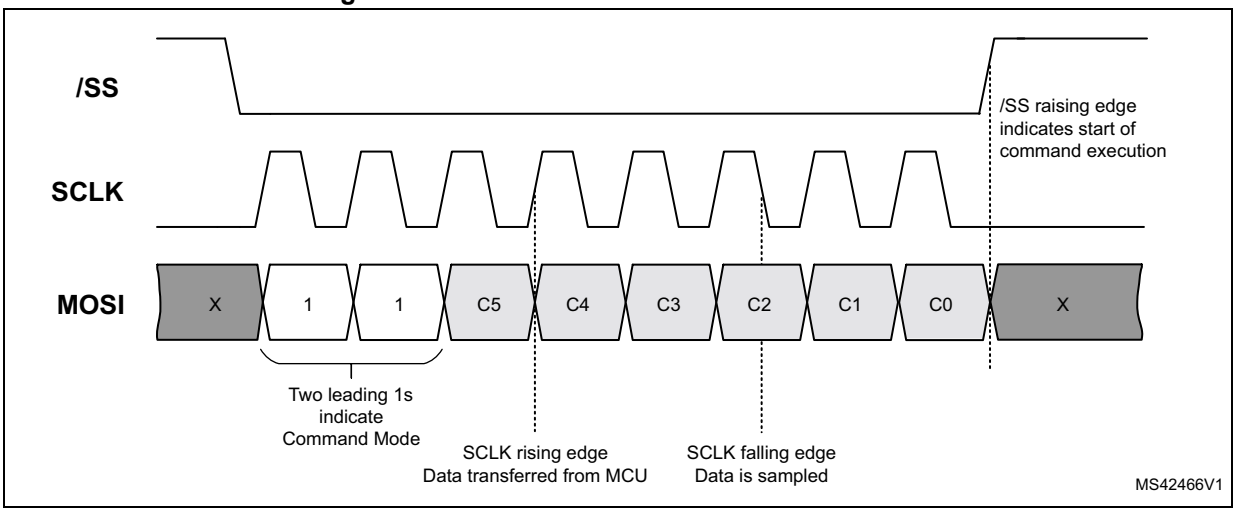


Direct Command Mode

Direct Command Mode has no arguments, so a single byte is sent. SPI operation mode bits 11 indicate Direct Command Mode. The following six bits define command code, sent MSB to LSB. The command is executed on falling edge of last clock (see *Figure 14*).

While execution of some Direct Commands is immediate, there are others that start a process of certain duration (calibration, measurement…). During execution of such commands it is not allowed to start another activity over the SPI interface. After execution of such a command is terminated an IRQ is sent.

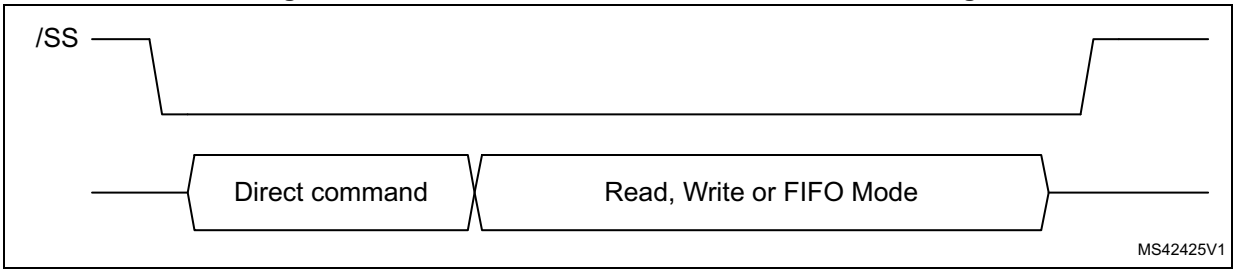
Figure 14. SPI communication: direct command



Direct command chaining

As shown in *Figure 15*, direct commands with immediate execution can be followed by another SPI mode (Read, Write or FIFO) without deactivating the /SS signal in between.

Figure 15. SPI communication: direct command chaining



SPI timing

Table 7. SPI timing

Symbol	Parameter	Min	Typ	Max	Unit	Comments
General timing (V_{DD} = V_{DD_IO} = V_{SP_D} = 3.3 V, 25 °C)						
T_{SCLK}	SCLK period	167	-	-	ns	T_{SCLK}=T_{SCLKL}+T_{SCLKH}, use of shorter SCLK period may lead to incorrect FIFO operation.
T_{SCLKL}	SCLK low	70	-	1		-
T_{SCLKH}	SCLK high	70	-	-		-
T_{SSH}	SPI reset (/SS high)	100	-	-		-
T_{NCSL}	/SS falling to SCLK rising	25	-	-		First SCLK pulse
T_{NCSH}	SCLK falling to /SS rising	300	-	-		Last SCLK pulse
T_{DIS}	Data in set-up time	10	-	-		-
T_{DIH}	Data in hold time	10	-	-		-

Table 7. SPI timing (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Read timing (V_{DD} = V_{DD_IO} = V_{SP_D} = 3.3 V, 25 °C, C_{LOAD} ≤ 50 pF)						
T_{DOD}	Data out delay	-	20	-	ns	-
T_{DOHZ}	Data out to high impedance delay	-	20	-		-

Figure 16. SPI general timing

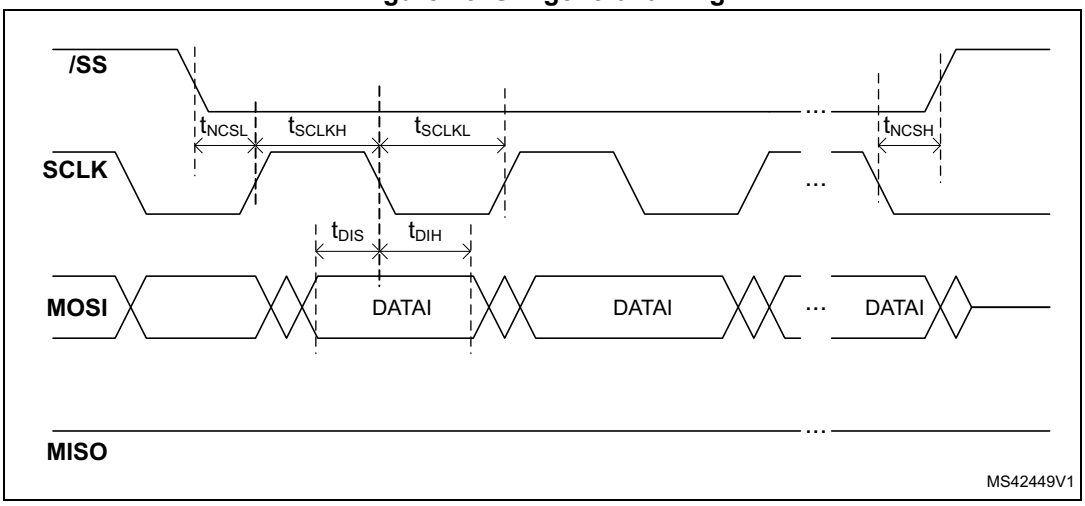
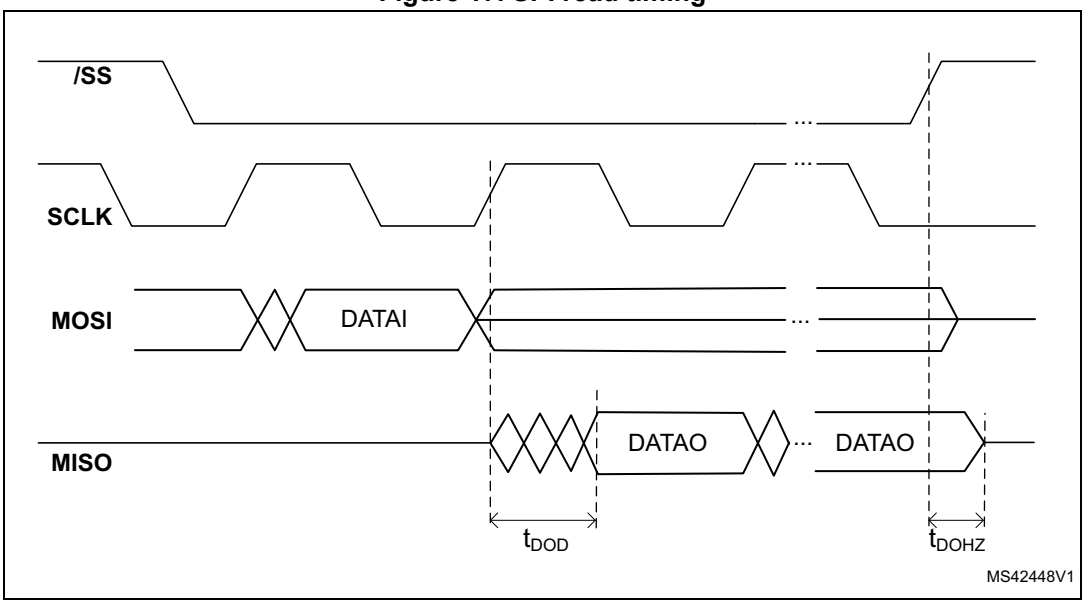


Figure 17. SPI read timing



Interrupt interface

There are three interrupt registers implemented in the ST25R3912/3: *Main Interrupt Register* contains information about six interrupt sources, while two bits reference to

interrupt sources detailed in *Timer and NFC Interrupt Register* and *Error and Wake-Up Interrupt Register*.

When an interrupt condition is met the source of interrupt bit is set in the *Main Interrupt Register* and the IRQ pin transitions to high.

Table 8. IRQ output

Name	Signal	Signal level	Description
IRQ	Digital output	CMOS	Interrupt output pin

The microcontroller then reads the *Main Interrupt Register* to distinguish between different interrupt sources. The interrupt registers 0x17, 0x18 and 0x19 are to be read in one attempt. After a particular Interrupt register is read, its content is reset to 0. Exceptions to this rule are the bits pointing to auxiliary registers. These bits are only cleared when corresponding auxiliary register is read. IRQ pin transitions to low after the interrupt bit(s) that caused its transition to high has (have) been read.

Note: There may be more than one interrupt bit set in case the microcontroller does not immediately read the interrupt registers after the IRQ signal has been set and another event causing interrupt has occurred. In that case the IRQ pin transitions to low after the last bit that caused interrupt is read.

If an interrupt from a certain source is not required, it can be disabled by setting corresponding bit in the Mask Interrupt registers. When masking a given interrupt source the interrupt is not produced, but the source of interrupt bit is still set in Interrupt registers.

FIFO water level and FIFO status registers

The ST25R3912/3 contain a 96 byte FIFO. In case of transmitting the Control logic shifts the data that was previously loaded by the external microcontroller to the Framing Block and further to the transmitter. During reception, the demodulated data is stored in the FIFO and the external microcontroller can download received data at a later moment.

Transmit and receive capabilities of the ST25R3912/3 are not limited by the FIFO size due to a FIFO water level interrupt system. During transmission an interrupt is sent (*IRQ* due to FIFO water level in the *Main Interrupt Register*) when the content of data in the FIFO passes from (water level + 1) to water level and the complete transmit frame has not been loaded in the FIFO yet. The external microcontroller can now add more data in the FIFO. The same stands for the reception: when the number of received bytes passes from (water level - 1) to water level an interrupt is sent to inform the external controller that data has to be downloaded from FIFO in order not to lose receive data due to FIFO overflow.

During transmission water level IRQ is additionally set in case all transmission bytes have not been written in FIFO yet and if number of bytes written into FIFO is lower than water level. In this case an IRQ is sent when number of bytes in FIFO drops below 4.

Note: FIFO IRQ is not produced while SPI is active in FIFO load or read mode. Due to this the FIFO loading/reading rate has to be higher than Tx/Rx bit rate, once FIFO loading/reading is finished the /SS pin has to be pulled to VDD (logic remains in FIFO load/read mode as long as /SS remains low).

The external controller has to serve the FIFO faster than data is transmitted or received. Using SCLK frequency that is at least double than the actual receive or transmit bit rate is recommended.

There are two settings of the FIFO water level available for receive and transmit in the *IO Configuration Register 1*.

At the beginning of a data reception the FIFO, *FIFO Status Register 1* and *FIFO Status Register 2* are cleared automatically.

After data reception is terminated the external microcontroller needs to know how much data is still stored in the FIFO: This information is available in the *FIFO Status Register 1* and *FIFO Status Register 2* that display number of bytes in the FIFO that were not read out. *FIFO Status Register 1* can also be read while reception and transmission processes are active to get info about current number of bytes in FIFO. In that case user has to take in account that Rx/Tx process is going on and that the number of data bytes in FIFO may have already changed by the time the reading of register is finished.

The *FIFO Status Register 2* contains the information on whether the last received byte was completed or not. An incomplete byte can occur on certain protocols that use frames shorter than one byte for status information or for example, if the receive data stream breaks in the middle due to an unexpected card removal. The status of the last received byte and the number of valid bits received is stored in the bits fifo_ncp, fifo_lb<2:0>, and np_lb. These bits are cleared when the *FIFO Status Register 2* is read and must be stored in the MCU if needed for further processing.

The *FIFO Status Register 2* additionally contains two bits that indicate that the FIFO was not correctly served during reception or transmission process (FIFO overflow and FIFO underflow).

FIFO overflow is set when too much data is written in FIFO. In case this bit is set during reception the external controller did not react on time on water level IRQ and more than 96 bytes were written in the FIFO. The received data is of course corrupted in such a case. During transmission this means that controller has written more data than FIFO size. The data to be transmitted was corrupted.

FIFO underflow is set when data was read from empty FIFO. In case this bit is set during reception the external controller read more data than was actually received. During transmission this means that controller has failed to provide the quantity of data defined in number of transmitted bytes registers on time.

Pin MCU_CLK

Pin MCU_CLK may be used as clock source for the external microcontroller. Depending on the operation mode either a low frequency clock (32 kHz) from the RC oscillator or the clock

signal derived from crystal oscillator is available on pin MCU_CLK. The MCU_CLK output pin is controlled by bits out_c1, out_cl0 and lf_clk_off in the *IO Configuration Register 1*. Bits out_cl enable the use of pin MCU_CLK as clock source and define the division for the case the crystal oscillator is running (13.56 MHz, 6.78 MHz and 3.39 MHz are available). Bit lf_clk_off controls the use of low frequency clock (32 kHz) in case the crystal oscillator is not running. By default configuration (defined at power-up) the 3.39 MHz clock is selected and the low frequency clock is enabled.

In Transparent mode (see *Section 1.2.21: Stream mode and Transparent mode*) the use of MCU_CLK is mandatory since clock that is synchronous to the field carrier frequency is needed to implement receive and transmit framing in the external controller. The use of MCU_CLK is recommended also for the case where the internal framing is used. Using MCU_CLK as the microcontroller clock source generates noise synchronous with the reader carrier frequency and is therefore filtered out by the receiver, while using some other incoherent clock source may produce noise that perturbs the reception.

Use of MCU_CLK is also better for EMC compliance.

1.2.12 Direct commands

Table 9. Direct commands

Command code (hex)	Command	Comments	Command chaining	Interrupt after Termination	Operation mode(1)
C1	Set Default	Puts the ST25R3912/3 in default state (same as after power-up)	No	No	All
C2, C3	Clear	Stops all activities and clears FIFO	Yes	No	en
C4	Transmit With CRC	Starts a transmit sequence using automatic CRC generation	Yes	No	en, tx_en
C5	Transmit Without CRC	Starts a transmit sequence without automatic CRC generation	Yes	No	en, tx_en
C6	Transmit REQA	Transmits REQA command (ISO14443A mode only)	Yes	No	en, tx_en
C7	Transmit WUPA	Transmits WUPA command (ISO14443A mode only)	Yes	No	en, tx_en
C8	NFC Initial Field ON	Performs Initial RF Collision Avoidance and switch on the field	Yes	Yes	en(2)
C9	NFC Response Field ON	Performs Response RF Collision Avoidance and switch on the field	Yes	Yes	en(2)
CA	NFC Response Field ON with n=0	Performs Response RF Collision Avoidance with n=0 and switch on the field	Yes	Yes	en(2)
CB	Go to Normal NFC Mode	Accepted in NFCIP-1 active communication bit rate detection mode	Yes	No	-
CC	Analog Preset	Presets Rx and Tx configuration based on state of *Mode Definition Register* and *Bit Rate Definition Register*	Yes	No	All
D0	Mask Receive Data	Receive after this command is ignored	Yes	No	en, rx_en
D1	Unmask Receive Data	Receive data following this command is normally processed (this command has priority over internal Mask Receive timer)	Yes	No	en, rx_en
D2	-	Not used	-	-	-
D3	Measure Amplitude	Amplitude of signal present on RFI inputs is measured, result is stored in *A/D Converter Output Register*	No	Yes	en

Table 9. Direct commands (continued)

Command code (hex)	Command	Comments	Command chaining	Interrupt after Termination	Operation mode(1)
D4	Squelch	Performs gain reduction based on the current noise level	No	No	en, rx_en
D5	Reset Rx Gain	Clears the current Squelch setting and loads the manual gain reduction from *Receiver Configuration Register 1*	No	No	en
D6	Adjust Regulators	Adjusts supply regulators according to the current supply voltage level	No	Yes	en(3)
D7	Calibrate Modulation Depth	Starts sequence that activates the Tx, measures the modulation depth and adapts it to comply with the specified modulation depth	No	Yes	en
D8	Calibrate Antenna	Starts the sequence to adjust parallel capacitances connected to TRIMx_y pins so that the antenna LC tank is in resonance	No	Yes	en(4)
D9	Measure Phase	Measurement of phase difference between the signal on RFO and RFI	No	Yes	en(4)
DA	Clear RSSI	Clears RSSI bits and restarts the measurement	Yes	No	en
DC	Transparent Mode	Amplitude of signal present on RFI inputs is measured, result is stored in *A/D Converter Output Register*	No	Yes	en
DF	Measure Power Supply	-	No	Yes	en
E0	Start General Purpose Timer	-	Yes	No	en
E1	Start Wake-Up Timer	-	Yes	No	All except wu
E2	Start Mask Receive Timer	-	Yes	No	See note (5)
E3	Start No-Response Timer	-	Yes	No	en, rx_en
FA	Clear Test Registers	Clears all test registers. Must be sent as chained sequence "FCFA"	Yes	No	All
FC	Test Access	Enable /W to test registers	Yes	No	All
Other Fx	-	Reserved for test	-	-	-
Other codes	-	Not used	-	-	-

1. Defines the bits of the *Operation Control Register* that have to be set in order to accept a particular command.
2. After termination of this command I_cat or I_cac IRQ is sent.

3. This command is not accepted in case the external definition of the regulated voltage is selected in the *Regulator Voltage Control Register* (bit reg_s is set to high).
4. ST25R3913 only.
5. Accepted only in the Initial NFC Active Target Communication Mode.

Set Default

This direct command puts the ST25R3912/3 in the same state as power-up initialization. All registers are initialized to the default state. The only exceptions are for *IO Configuration Register 1*, *IO Configuration Register 2* and *Operation Control Register* (not affected by Set Default command) that are set to default state only at power-up.

Note: Results of different calibration and adjust commands are also lost.

This direct command is accepted in all operating modes. In case this command is sent while en (bit 7 of the *Operation Control Register*) is not set FIFO and FIFO status registers are not cleared.

Direct command chaining is not allowed since this command clears all registers.

IRQ due to termination of direct command is not produced.

Clear

This direct command stops all current activities (transmission or reception), clears FIFO, clears FIFO status registers and stops all timers except Wake-Up timer. If bit nrt_emv in the *General Purpose and No-Response Timer Control Register* is set to 1, the No-Response timer is not stopped.If nfc_ar in the *Mode Definition Register* is set to 1, the internal timer for the Response RF Collision Avoidance is not stopped and the Response RF Collision Avoidance will take place once this timer epxires. Set nfc_ar to 0 prior to sending the direct command Clear to stop any Response RF Collision Avoidance activity too. It also clears collision and interrupt registers. This command has to be sent first in a sequence preparing a transmission before writing data to be transmitted in FIFO (except in case of direct commands Transmit REQA and Transmit WUPA).

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is possible.

IRQ due to termination of direct command is not produced.

Transmit commands

All Transmit commands (Transmit With CRC, Transmit Without CRC, Transmit REQA and Transmit WUPA) are accepted only in case the transmitter is enabled (bit tx_en is set).

Before sending commands Transmit With CRC and Transmit Without CRC direct command Clear has to be sent, followed by definition of number of transmitted bytes and writing data to be transmitted in FIFO.

Direct commands Transmit REQA and Transmit WUPA are used to transmit ISO14443A commands REQA and WUPA respectively. Sending command Clear before these two commands is not necessary.

The number of valid bits in the last byte must be set to zero (nbtx<2:0> in the *Number of Transmitted Bytes Register 2*) prior to executing Transmit REQA or Transmit WUPA.

Direct command chaining is possible.

IRQ due to termination of direct command is not produced.

NFC Field ON commands

These commands are used to perform the RF Collision Avoidance and switch the field on in case no collision was detected. The Collision Avoidance threshold defined in the *External Field Detector Threshold Register* is used to observe the RF_IN inputs and to determine whether there is some other device emitting the 13.56 MHz field, present close to the ST25R3912/3 antenna. In case collision is not detected the reader field is switched on automatically (bit tx_en in the *Operation Control Register* is set) and an IRQ with I_cat flag in *Timer and NFC Interrupt Register* is sent after minimum guard time defined by the NFCIP-1 standard to inform the controller that message transmission using a Transmit command can be initiated.

In case a presence of external field is detected an IRQ with I_cac flag is sent. In such case a transmission cannot be performed, NFC Field ON command has to be repeated as long as collision is not detected anymore. Command NFC Initial Field ON performs Initial Collision Avoidance according to NFCIP-1 standard; number n is defined by bits nfc_n1 and nfc_n0 in *Auxiliary Definition Register*.

Command NFC Response Field ON performs Response Collision Avoidance according to NFCIP-1 standard; number n is defined by bits nfc_n1 and nfc_n0 in *Auxiliary Definition Register*.

Command NFC Response Field ON with n=0 performs Response Collision Avoidance where n is 0.

Implemented active delay time is on lower NFCIP-1 specification limit, since the actual active delay time will also include detection of the field deactivation, controller processing delay and sending the NFC Field ON command.

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and both Xtal oscillator frequency and amplitude are stable.

Figure 18. Direct command NFC Initial Field ON

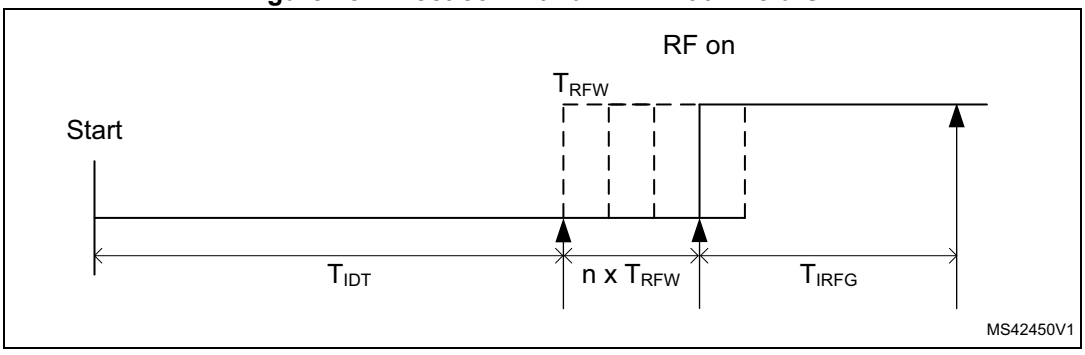


Figure 19. Direct command NFC Response Field ON

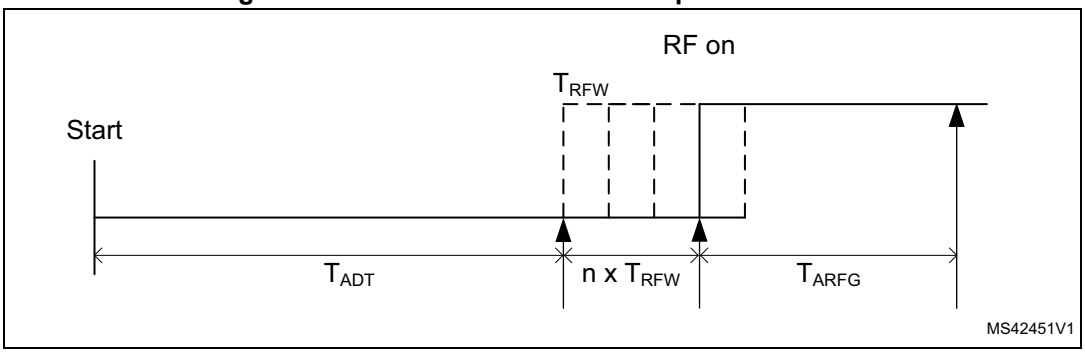


Table 10. Timing parameters of NFC Field ON commands

Symbol	Parameter	Value	Unit	Comments
T_{IDT}	Initial delay time	4096	/fc	NFC Initial Field ON
T_{RWF}	RF waiting time	512		-
T_{IRFG}	Initial guard time	>5	ms	NFC Initial Field ON
T_{ADT}	Active delay time	768	/fc	NFC Response Field ON
T_{ARFG}	Active guard time	1024		

Go to Normal NFC Mode

This command is used to transition from NFC target bit rate detection mode to normal mode. Additionally it copies the content of the *NFCIP Bit Rate Detection Display Register* to the *Bit Rate Definition Register* and correctly sets the bit tr_am in the *Auxiliary Definition Register*.

Analog Preset

This command is used to preset receiver and transmitter configuration based on state of *Mode Definition Register* and *Bit Rate Definition Register*. In case of Sub-carrier bit stream or BPSK bit stream mode, this command should not be used. The list of configuration bits that are preset is given in *Table 11*.

Table 11. Register preset bits

Bit	Bit name	Function
Address 02h: *Table 21: Operation Control Register*		
5	rx_chn	**1:** one channel enabled → NFCIP-1 active communication (both initiator and target)
3	tx_en	**0:** disable TX operation → NFCIP-1 active communication (both initiator and target)
Note: In case of any target mode or NFCIP-1 initiator mode bit **tx_en** is set to 0 to disable transmitter in case it was enabled. In NFCIP-1 mode the switching on of the transmitter field is controlled by dedicated commands.		
Address 05h: *Table 27: ISO14443A and NFC 106kb/s Settings Register*		
5	nfc_f0	**1:** Adds SB (F0) and LEN byte during Tx and skip SB (F0) byte during TX → NFCIP-1 active communication (both initiator and target)

Table 11. Register preset bits (continued)

Bit	Bit name	Function
Address 09h: *Table 35: Auxiliary Definition Register*		
5	tr_am	Tx Modulation type (depends on mode definition and Tx bit rate) **0:** OOK → ISO144443A, NFCIP-1 106 kb/s (both initiator and target), NFC Forum Type 1 Tag **1:** AM → ISO144443B, FeliCa™, NFCIP-1 212 kb/s and 424 kb/s
4	en_fd	Enables External Field Detector with Peer Detection threshold **0:** All modes except NFCIP-1 active communication **1:** NFCIP-1 active communication (both initiator and target)
Address 0Ah: *Table 36: Receiver Configuration Register 1*		
7	ch_sel	**0:** Enables AM channel → NFCIP-1 active communication (both initiator and target)
6	amd_sel	AM demodulator select (depend on Rx bit rate) **0:** Peak detector → All Rx bit rates equal or below fc/16 (848 kb/s) **1:** Mixer
5	lp2	Low pass control (depends on mode definition and Rx bit rate), see *Table 3: Receiver filter selection and gain range*
4	lp1	
3	lp0	
2	h200	First and third stage zero setting (depends on mode definition and Rx bit rate), see *Table 3: Receiver filter selection and gain range*
1	h80	
0	z12k	
Address 0Ch: *Table 38: Receiver Configuration Register 3*		
1	lim	Clips output of 1st and 2nd stage **0:** All modes except NFCIP-1 active communication **1:** NFCIP-1 active communication (both initiator and target)
0	rg_nfc	Forces gain reduction in 2nd and 3rd gain stage **0:** All modes except NFCIP-1 active communication **1:** NFCIP-1 active communication (both initiator and target)

Mask Receive Data and Unmask Receive Data

After the direct command Mask Receive Data the signal rx_on that enables the RSSI and AGC operation of the receiver (see *Section 1.1.2: Receiver*) is forced to low, processing of the receiver output by the receive data framing block is disabled. This command is useful to mask receiver and receive framing from processing the data when there is actually no input and only a noise would be processed (for example in case where a transponder processing time after receiving a command from the reader is long). Masking of receive is also possible using Mask Receive timer. Actual masking is a logical or of the two mask receive processes.

The direct command Unmask Receive Data is enabling normal processing of the received data (signal rx_on is set high to enable the RSSI and AGC operation), the receive data framing block is enabled. A common use of this command is to enable again the receiver operation after it was masked by the command Mask Receive Data. In case Mask Receive timer is running while command Unmask Receive Data is received, reception is enabled, Mask Receive timer is reset.

The commands Mask Receive Data and Unmask Receive Data are only accepted when the receiver is enabled (bit rx_en is set).

Direct command chaining is possible.

IRQ due to termination of direct command is not produced.

Measure Amplitude

This command measures the amplitude on the RFI inputs and stores the result in the *A/D Converter Output Register*.

When this command is executed the transmitter and Amplitude Detector are enabled, the output of the Amplitude Detector is multiplexed to the A/D converter input (the A/D converter is in absolute mode). The Amplitude Detector conversion gain is 0.6 V_{INPP}/ V_{OUT}. One LSB of the A/D converter output represents 13.02 mV_{pp} on the RFI inputs. A 3 V_{pp} signal (the maximum allowed level on each of the two RFI inputs), results in 1.8 V output DC voltage and will produce a value of 1110 0110b on the A/D converter output.

Duration time: 25 µs max.

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is not possible.

IRQ due to termination of direct command is produced after command execution is terminated.

Squelch

This direct command is intended to avoid demodulation problems of transponders that produce a lot of noise during data processing. It can also be used in a noisy environment. The operation of this command is explained in *Squelch*.

Duration time: 500 µs max.

This command is only accepted when the transmitter and the receiver are operating. Command is actually executed only in case signal rx_on is low.

Direct command chaining is not possible.

IRQ due to termination of direct command is not produced.

Reset Rx Gain

This command initializes the AGC, Squelch and RSSI block. Sending this command stops a squelch process in case it is going on, clears the current Squelch setting and loads the manual gain reduction from *Receiver Configuration Register 4*.

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is possible.

IRQ due to termination of direct command is not produced.

Adjust Regulators

When this command is sent the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to

ensure maximum possible stable regulated supply (see *Section 1.2.10: Power supply system*). The use of this command increases the system PSSR.

At the beginning of execution of the command, both the receiver and transmitter are switched on to have the maximum current consumption, and the regulators are set to their maximum regulated voltage (5.1 V in case of 5 V supply and 3.4 V in case of 3.3 V supply). After 300 µs V_{SP_RF} is compared to V_{DD}, if is not at least 250 mV lower the regulator setting is reduced by one step (120 mV in case of 5 V supply and 100 mV in case of 3.3 V supply) and measurement is done after another 300 µs. The procedure is repeated until V_{SP_RF} drops at least 250 mV below V_{DD}, or until the minimum regulated voltage (3.9 V in case of 5 V supply and 2.4 V in case of 3.3 V supply) is reached.

Duration time: 5 ms max.

This command is accepted if en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

This command is not accepted when the external definition of the regulated voltage is selected in the *Regulator Voltage Control Register*(bit reg_s is set to H).

Direct command chaining is not possible.

IRQ due to termination of direct command is produced after command execution is terminated.

Calibrate Modulation Depth

Starts a sequence that activates the transmission, measures the modulation depth and adapts it to comply with the modulation depth specified in the *AM Modulation Depth Control Register*. When calibration procedure is finished result is displayed in the same register. Refer to *Section 1.2.19: AM modulation depth: definition and calibration* for details about setting the AM modulation depth and running this command.

Duration time: 275 µs max.

This command is accepted when en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is not possible.

IRQ due to termination of direct command is produced after command execution is terminated.

Calibrate Antenna (ST25R3913 only)

Sending this command starts a sequence that adjusts the parallel capacitances connected to TRIMx_y pins so that the antenna LC tank is in resonance. See *Section 1.2.20: Antenna tuning (ST25R3913 only)* for details.

Duration time: 250 µs max.

This command is accepted when en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Measure Phase

This command measures the phase difference between the signals on the RFO outputs and the signals on the RFI inputs and stores the result in the *A/D Converter Output Register*.

During execution of the direct command Measure Phase the transmitter and Phase Detector are enabled, the Phase Detector output is multiplexed on the input of A/ D converter, which is set in relative mode. Since the A/D converter range is from 1/6 VSP_A to 5/6 VS_{P_A} the actual phase detector range is from 30º to 150º. Values below 30º result in FFh, while values above 150º result in 00h. One LSB of the A/D conversion output represents 0.13% of carrier frequency period (0.468°). The result of A/D conversion is in case of 90º phase shift in the middle of range (1000 0000b or 0111 1111b). A value higher than 1000 0000b means that phase detector output voltage is higher than $V_{SP\_A}/2$, which corresponds to case with phase shift lower than 90º. In the opposite case, when the phase shift is higher than 90º, the result of A/D conversion is lower than 0111 1111b. For example, the phase difference of 135º shown in *Figure 6* results in 0.75 V_{SP_A}, result stored in A/D converter is 31d (1Fh).

The phase measurement result can be calculating using the following formulas:

- 0º ≤ φ ≤ 30º: result = 255 (decimal)
- 30º < φ < 150º: angle (in º) = 30 + [(255 - u_angle) / 255) * 120]
- 150º ≤ φ ≤ 180º: result = 0 (decimal)

Duration time: 25 µs max.

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is not possible.

IRQ due to termination of direct command is produced after command execution is terminated.

Clear RSSI

The receiver automatically clears the RSSI bits in the *RSSI Display Register* and starts to measure the RSSI of the received signal when the signal rx_on is asserted. Since the RSSI bits store peak value (peak-hold type) the variations of the receiver input signal will not be followed (this may happen in case of long messages or test procedures). The direct command Clear RSSI clears the RSSI bits in the *RSSI Display Register*, and the RSSI measurement is restarted (in case, of course, rx_on is still high).

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is possible.

IRQ due to termination of direct command is not produced.

Transparent Mode

Enters in the Transparent mode. The Transparent mode is entered on the rising edge of signal /SS and is maintained as long as signal /SS is kept high.

This command is accepted when en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Measure Power Supply

This command performs the power supply measurement. Configuration bits mpsv1 and mpsv0 of the *Regulator Voltage Control Register* define which power supply is measured (VDD,VSP_A, VSP_D and VSP_RF can be measured). Result of measurement is stored in the *A/D Converter Output Register*.

During the measurement the selected supply input is connected to a 1/3 resistive divider, whose output is multiplexed to A/D converter in absolute mode. Due to division by 3, one LSB represents 23.438 mV.

Duration time: 25 µs max.

This command is accepted in case en (bit 7 of the *Operation Control Register*) is set and Xtal oscillator frequency is stable.

Direct command chaining is not possible.

IRQ due to termination of direct command is produced after command execution is terminated.

1.2.13 Start timers

See *Section 1.2.6: Timers on page 23*.

1.2.14 Test access

A direct command Test Access is used to enable RW access of test registers and entry in different test modes. Pins TO1 and TO2 are used as test pins.

Test mode entry and access to test registers

Test registers are not part of normal SPI register address space. After sending a direct command Test Access, test registers can be accessed using normal Read/Write register SPI command. Access to test registers is possible in a chained command sequence where first command Test Access is sent, followed by read/write access to test registers using auto increment feature. After SPI interface reset (SS toggle) the content of test registers is kept.

Test register are set to default state at power-up and by sending the command Clear Test Registers.

Table 12. Analog Test and Observation Register

Test Address 01h: Analog Test and Observation Register - Type: RW				
Bit	**Name**	**Default**	**Function**	**Comments**
7	tana_7	0	-	Reserved
6	tana_6	0	-	Reserved
5	tana_5	0	-	Reserved
4	-	0	Not used	-
3	tana_3	0	See *Table 13*	These test modes are also intended for observation in normal mode. Other modes of this register are also available when analog test mode is not set.
2	tana_2	0		
1	tana_1	0		
0	tana_0	0		

Table 13. Test Access Register - tana signal selection of TO1 and TO2 pins

Tana_				Pin TO1		Pin TO2		Comments
3	2	1	0	Type	Functionality	Type	Functionality	
0	0	0	1	AO	Analog output of AM channel (before digitizer)	DO	Digital output of AM channel (after digitizer)	Normal operation
0	0	1	0	AO	Analog output of PM channel (before digitizer)	DO	Digital output of PM channel (after digitizer)	Normal operation
0	0	1	1	AO	Analog output of AM channel (before digitizer)	AO	Analog output of PM channel (before digitizer)	Normal operation
0	1	0	0	DO	Digital output of AM channel (after digitizer)	DO	Digital output of PM channel (after digitizer)	Normal operation
0	1	0	1	AO	Analog signal after first stage	AO	Analog signal after second stage	Normal operation: – PM channel if enabled – AM if PM is not enabled
1	0	0	1	DO	Channel selection from logic	DO	Collision Avoidance detector output	Collision Avoidance detectors are enabled
1	0	1	0	DO	Digital TX modulation signal	DO	Select PM	Analog part of channel selection
0	0	0	1	AO	Analog output of AM channel (before digitizer)	DO	Digital output of AM channel (after digitizer)	Normal operation

1.2.15 Power-up sequence

At power-up, the ST25R3912/3 enter the Power-down mode. The content of all registers is set to the default state.

1. The microcontroller, after a power-up, must correctly configure the two IO configuration registers. The content of these two registers defines operation options related to hardware (power supply mode, Xtal type, use of MCU_CLK clock, antenna operation mode).
2. Configure the regulators. It is recommended to use direct command Adjust Regulators to improve the system PSRR.
3. When implementing the LC tank tuning (ST25R3913 only), send the direct command Calibrate Antenna.
4. When using the AM modulation (ISO-14443B for example), set the modulation depth in the *AM Modulation Depth Control Register* and send the command Calibrate Modulation Depth.
5. The ST25R3912/3 are now ready to operate.

1.2.16 Reader operation

To begin with, the operation mode and data rate have to be configured by writing the *Mode Definition Register* and *Bit Rate Definition Register*. Additionally, the receiver and transmitter operation options related to operation mode have to be defined. This is done automatically by sending the direct command Analog Preset. If more options are required apart from those defined by Analog Preset, then such options must be additionally set by writing the appropriate registers.

Next, the Ready mode has to be entered by setting the bit en of the *Operation Control Register*. In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable, an interrupt is sent.

Before sending any command to a transponder, the transmitter and receiver have to be enabled by setting the bits rx_en and tx_en. RFID protocols usually require that the reader field is turned on for a while before sending the first command (5 ms for ISO14443). General purpose timer can be used to measure this time interval.

If REQA or WUPA have to be sent, this is simply done by sending the appropriate direct command, otherwise the following sequence has to be followed:

1. Send the direct command Clear
2. Define the number of transmitted bytes in the *Number of Transmitted Bytes Register 1* and *Number of Transmitted Bytes Register 2*
3. Write the bytes to be transmitted in the FIFO
4. Send the direct command Transmit With CRC or Transmit Without CRC (whichever is appropriate)
5. When all the data is transmitted an interrupt is sent to inform the microcontroller that the transmission is finished (IRQ due to end of transmission)

After the transmission is executed, the ST25R3912/3 receiver automatically starts to observe the RFI inputs to detect a transponder response. The RSSI and AGC (when enabled) start. The framing block processes the sub-carrier signal from receiver and fills the FIFO with data. When the reception is finished and all the data is in the FIFO an interrupt is sent to the microcontroller (IRQ due to end of receive), additionally the *FIFO Status Register 1* and *FIFO Status Register 2* display the number of bytes in the FIFO so that the microcontroller can proceed with data download.

In case of an error or bit collision detected during reception, an interrupt with appropriate flag is sent.

Transmit and Receive when the data packet is longer than FIFO

In case a data packet is longer than FIFO the sequence explained above is modified.

Before transmit the FIFO is filled. During transmit an interrupt is sent when remaining number of bytes is lower than the water level (IRQ due to FIFO water level). The microcontroller in turn adds more data in the FIFO. When all the data is transmitted an interrupt is sent to inform the microcontroller that transmission is finished.

During reception situation is similar. In case the FIFO is loaded with more data than the receive water level, an interrupt is sent and the microcontroller in turn reads the data from the FIFO.

When reception is finished an interrupt is sent to the microcontroller (IRQ due to end of receive), additionally the *FIFO Status Register 1* and *FIFO Status Register 2* display the number of bytes in the FIFO that are still to be read out.

Anticollision – ISO 14443A

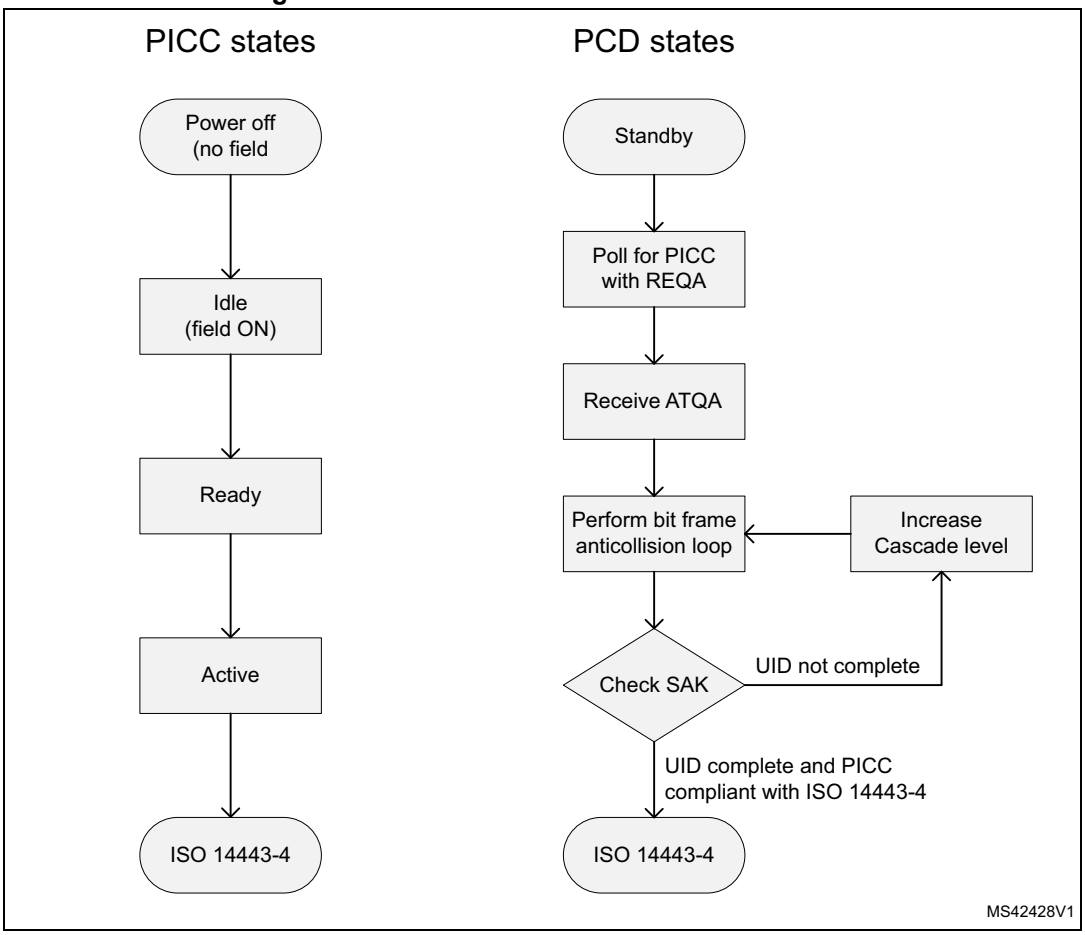
Note: For this section, it is assumed that there is more than one ISO/IEC 14443A PICC in the reader RF field, and all of them are compatible with ISO/IEC 14443 up to level 4.

This section describes the anticollision procedure of ST25R3912/3 for ISO14443A tags. After an ISO14443 type A tag enters in the reader field, the reader has to perform a selection process that brings it into the PROTOCOL state in which the actual application

implemented in the tag can be executed. This selection process is described in the ISO/IEC 14443-3. *Figure 20* shows the states that a tag and a reader have to pass through to enter the protocol state.

The selection procedure starts when a PICC enters the reader field and the PCD sends a REQA (or WUPA) command followed by an anticollision procedure (including SELECT, RATS and PPS).

Figure 20. ISO14443A states for PCD and PICC



Setting up the ST25R3912/3 for ISO 14443A anticollision

To set up the ST25R3912/3 for the ISO14443A anticollision follow the steps indicated below.

1. The Initiator operation mode of ST25R3912/3 must be set up for ISO 14443A in the *Mode Definition Register* (default is already for ISO14443A).
2. The Tx and Rx bit rates must be set to default (106 kbps) in the *Bit Rate Definition Register*.
3. Set the antcl bit in the *ISO14443A and NFC 106kb/s Settings Register*. This needs to be set before sending the REQA (or WUPA). As a result, the ST25R3912/3 will not trigger a framing error if in case the collision occurs in the ATQA or during anticollision procedure.

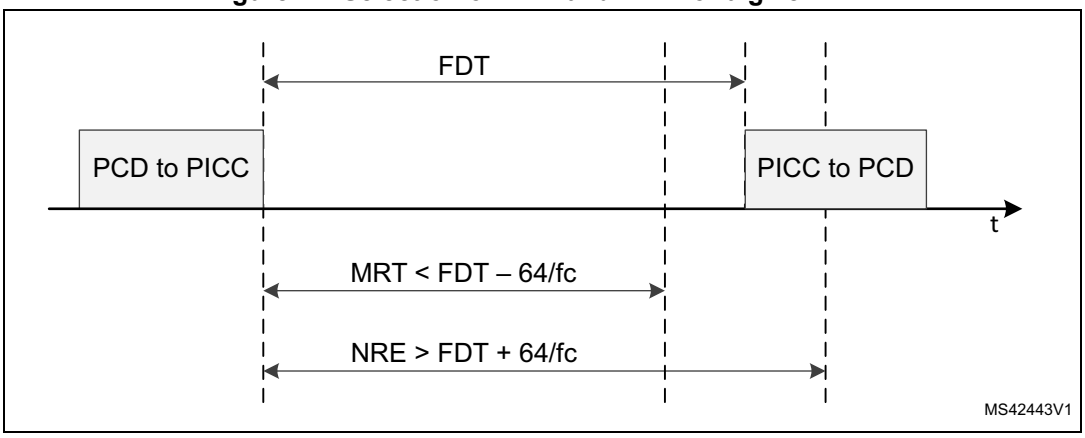
Note: This bit must be set to one for REQA, WUPA and ANTOCOLLISION commands, for other commands it has to be zero.

4. Review and set a value for *Mask Receive Timer Register* lower than the Frame delay time, as required by the ISO14443A., and set the *No-Response Timer Register 1* and *No-Response Timer Register 2* according to the requirements. This is typically larger than the FDT.

Note: ST25R3912/3 offer the resolution of n/2 (64/fc - half steps) compared to n (128/fc) as mentioned in ISO 14443A so that the receiver can be unmasked n/2 steps before the actual transmission from the PICC.

5. According to ISO 14443A the FDT must be 1236/fc if last transmitted bit is 1, or 1172/fc if last transmitted bit is 0. *Figure 21* shows an example of how MRT and NRT timers are set for a given FDT.

Figure 21. Selection of MRT and NRT for a given FDT



6. The receiver and transmitter operation options related to operation mode must be defined. This is done automatically by sending the direct command Analog Preset. If different options are required apart from those defined by Analog Preset, they must be additionally set by writing the appropriate registers.
7. Set rx_en and tx_en in the *Operation Control Register*. RFID protocols usually require that the reader field is turned on for a while before sending the first command (5 ms for ISO14443). General purpose timer can be used to count this time.
8. The reply from PICC for the REQA, WUPA, and replies within anticollision sequence before SAK do not contain CRC. In this case the no_CRC_rx bit in the *Auxiliary Definition Register* must be set to 1 (receive without CRC) before sending these commands.

REQA and WUPA

Sending these two commands is simple since they are implemented as direct commands (Transmit REQA and Transmit WUPA). The end of transmission of these commands is signaled to microcontroller by an interrupt - IRQ due to end of transmission). After the transmission is executed, the ST25R3912/3 receiver automatically starts to observe the RFI inputs to detect a transponder after the expiration of the Mask Receive timer.

As a response to REQA (or WUPA) all the PICC in the field respond simultaneously with an ATQA. A collision can occur in this state if there are PICC with different UID size or has the bit frame anticollision bits set differently. Hence it is important to set the antcl bit to 1. If there is any IRQ (except I_nre) that ST25R3912/3 signals, the microcontroller must consider as a valid presence of tag and must proceed with the anticollision procedure.

If more than one PICC is expected in the field, the following algorithm must be used to select multiple tags:

1. Send REQA, if there is any answer continue
2. Perform anticollision, and select one PICC
3. Send HLTA to move the selected PICC to the HALT state
4. Go to step 1, and repeat this procedure until all the PICCs are in HALT state and all the UIDs have been extracted.

Anticollision procedure

After receiving the ATQA from the tags in the field, the next step is to execute the anticollision procedure to resolve the IDs of the tags.

The procedure mainly uses the ANTICOLLISION and SELECT commands, which consist of:

- Select code SEL (1 byte)
- Number of valid bits NVB (1 byte)
- 0 to 40 data bits of UID CLn according to the value of NVB

The ANTICOLLISION command uses bit oriented anticollision frame (it does not use CRC). In this case the transmit needs to be done with direct command Transmit Without CRC and for the receive, the no_CRC_rx bit in the *Auxiliary Definition Register* must be set to 1. The final SELECT command and its response SAK contains a CRC, so the transmit needs to be done with command Transmit With CRC and before sending this command the configuration bit no_CRC_rx bit in the *Auxiliary Definition Register* must be set back to 0.

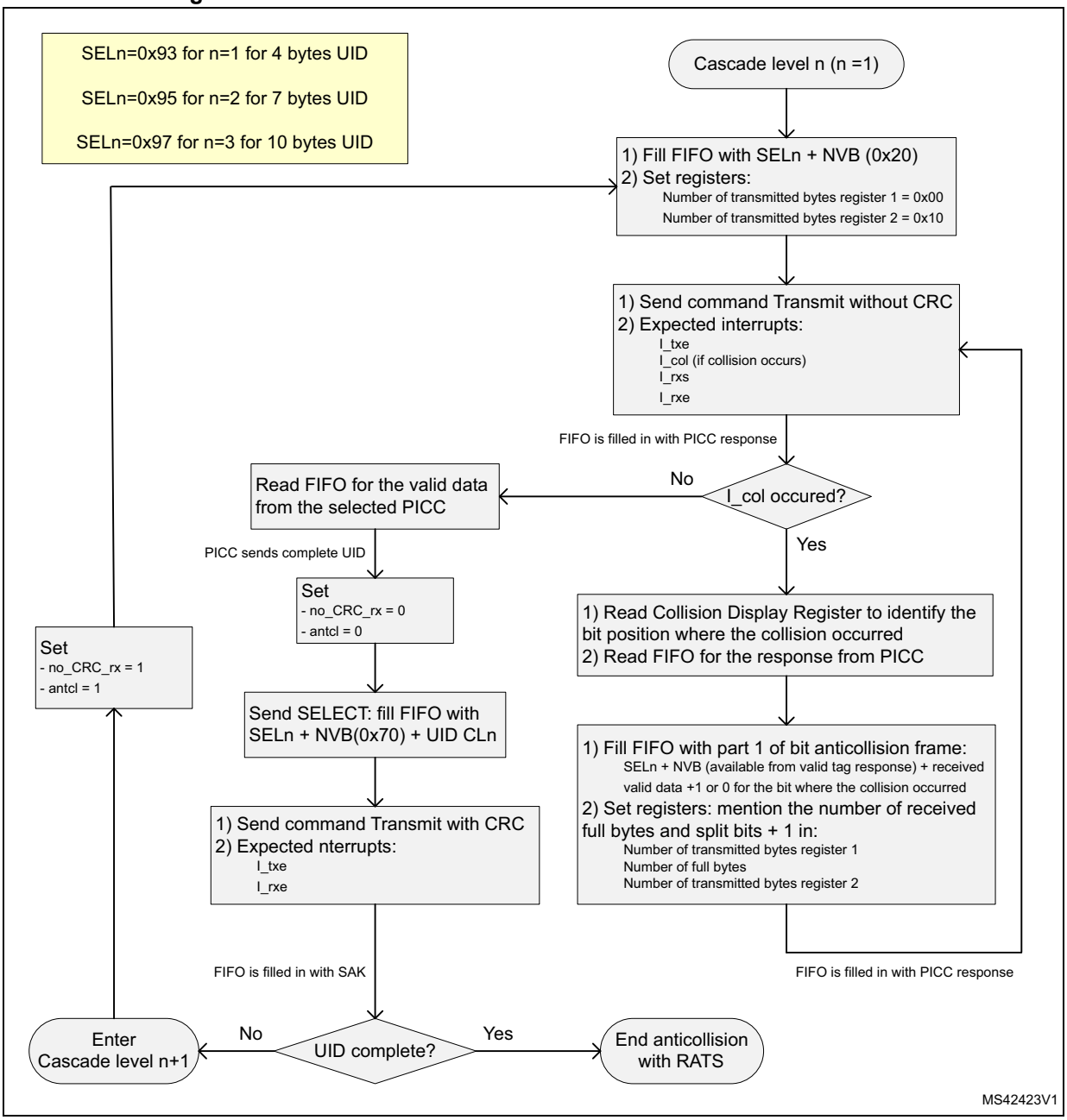
If there is more than one PICC in the field, the collision will occur when the tags reply to the ANTICOLLISION command during anticollision, when the PICCs reply back with their UID. This collision can occur after a complete byte (Full byte scenario) or it can occur within a byte (Split byte scenario). The antcl bit in *ISO14443A and NFC 106kb/s Settings Register* must be set during this procedure too. As a result, the ST25R3912/3 will not trigger a Framing Error. This bit is also responsible for correct timing of anticollision and correct parity extraction.

Note: It must only be set before sending an anticollision frame, REQA or WUPA. This bit must not be used in any other commands.

Figure 22 shows how to implement the anticollision with ST25R3912/3.

Since SPI is byte oriented, in case of Split byte scenario, the invalid MSB bits must be ignored when reading out the FIFO for the received data. Similarly, 0s must be concatenated as MSB bits to complete a byte for the Transmit (which will then be ignored based on register 0x1E).

Figure 22. Flowchart for ISO14443A anticollision with ST25R3912/3



1.2.17 FeliCa™ reader mode

The general recommendation from *Section 1.2.16: Reader operation* is valid for FeliCa™ reader mode as well. Both 212 and 424 kb/s bit rates are supported, they are same in both directions (reader to tag and tag to reader). Modulation reader to tag is AM.

In FeliCa™ mode the FeliCa™ frame format (see *Table 14*) is supported.

Table 14. FeliCa™ frame format

Preamble	Sync	Length	Payload	CRC
48 data bits, all logical 0	2 bytes (B2h, 4Dh)	Length byte (value= payload length + 1), the length range is from 2 to 255	Payload	2 bytes

FeliCa™ transmission

In order to transmit FeliCa™ frame only the Payload data is put in the FIFO. The number of Payload bytes is defined in the *Number of Transmitted Bytes Register 1* and *Number of Transmitted Bytes Register 2*. Preamble length is defined by bits f_p1 and f_p0 in the *ISO14443B and FeliCa Settings Register*, default value is 48 bits, but other options are possible.

Transmission is triggered by sending direct command Transmit With CRC. First preamble is sent, followed by SYNC and Length bytes. Then Payload stored in FIFO is sent, transmission is terminated by two CRC bytes that are calculated by the ST25R3912/3. Length byte is calculated from 'number of transmitted bytes'. The following equation is used:

length = payload length + 1 = number of transmitted bytes +1

FeliCa™ reception

After transmission is done the ST25R3912/3 logic starts to parse the receiver output to detect the Preamble of FeliCa™ tag reply.

Once the Preamble (followed by the two SYNC bytes) is detected the Length byte and Payload data are put in the FIFO. CRC bytes are internally checked.

1.2.18 NFCIP-1 operation

The ST25R3912/3 support all NFCIP-1 initiator modes and active communication target modes. All NFCIP-1 bit rates (106, 212 and 424 kbit/s) are supported.

NFCIP-1 passive communication Initiator

NFCIP-1 passive communication is equivalent to reader (PCD) to tag (PICC) communication where initiator acts as a reader and target acts as tag. The only difference is that in case of the NFCIP-1 passive communication the initiator performs Initial RF Collision Avoidance procedure at the beginning of communication.

In order to act as NFCIP-1 passive communication initiator the ST25R3912/3 have to be configured according to *Table 15*.

Table 15. Operation mode/bit rate setting for NFCIP-1 passive communication

NFCIP-1 bit rate (kb/s)	Operation mode setting	Bit rate for Tx (kb/s)	Bit rate for Rx (kb/s)	Comments
106	ISO14443A	fc/128 (~106)	fc/128 (~106)	-
212	FeliCa™	fc/64 (~212)	-	In FeliCa Mode data rate is the same in both directions
424		fc/32 (~424)	-	

Initial set-up of the *Operation Control Register* before the start of communication is the same as in case of reader to tag communication, with the exception that the transmitter is

not enabled by setting the tx_en bit. The direct command NFC Initial Field ON is sent instead.

This command first performs the Initial RF Collision Avoidance with Collision Avoidance Threshold defined in the *External Field Detector Threshold Register*. The timing of Collision Avoidance is according to NFCIP-1 standard (for timing details see *Table 10: Timing parameters of NFC Field ON commands*). In case collision is not detected the tx_en bit is automatically set to switch the transmitter on. After minimum guard time T_{IRFG} the I_cat IRQ is sent to inform controller that the first initiator command can be sent.

From this point on communication is the same as for ISO14443A (for 106 kb/s) or for FeliCa™ (for 242 and 424 kb/s) reader communication.

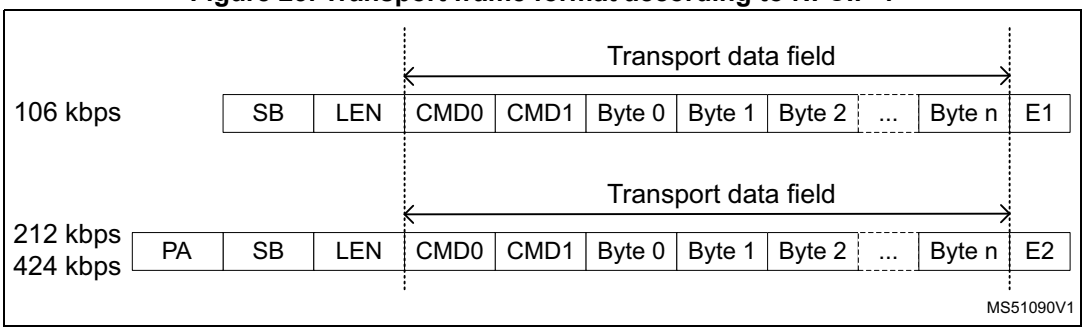
In case a presence of external field is detected an I_cac IRQ is sent. In such case a transmission should not be performed, command NFC Initial Field ON has to be repeated until collision is not detected anymore.

Initial Collision Avoidance is not limited to modes supported by NFCIP-1. The initial Collision Avoidance according to procedure described above can be performed before any reader mode is started to avoid collision with an HF reader or an NFC device operating in proximity.

Support of NFCIP-1 transport frame format

Figure 23 shows the transport frame according to NFCIP-1.

Figure 23. Transport frame format according to NFCIP-1



Transport Frame for bit rate 212 and 424 kb/s has the same format as communication frame used during Initialization and SDD. This format is also used in FeliCa™ protocol (see also *Section 1.2.17: FeliCa™ reader mode*). In case of 106 kb/s the SB (Start byte at F0h) and LEN (length byte) are only used in Transport Frame.

Support of Transport Frame for 106 kb/s NFCIP-1 communication is enabled by setting bit nfc_f0 in the *ISO14443A and NFC 106kb/s Settings Register*.

Once this bit is set and ISO 14443A mode with bit rate 106 kb/s is configured, the ST25R3912/3 behave as indicated in the next subsections.

Transmission

In order to transmit a Transport Frame only the Transport Data has to be put in FIFO. The number of Transport Data bytes is defined in the *Number of Transmitted Bytes Register 1* and *Number of Transmitted Bytes Register 2*. Transmission is triggered by sending direct command Transmit With CRC. First Start byte with value F0h followed by Length byte are sent. Then Transport Data stored in FIFO is sent, transmission is terminated by two CRC bytes (E1 in *Figure 23*) that are calculated by the ST25R3912/3. Length byte is calculated from ‘number of transmitted bytes’. The following equation is used:

length = Transport Data length + 1 = number of transmitted bytes +1

Reception

After transmission is done the ST25R3912/3 logic starts to parse the receiver output to detect the start of tag reply.

Once the start of communication sequence is detected the first byte (Start Byte with value F0h) is checked the Length byte and Transport Data bytes are put in the FIFO. CRC bytes are internally checked. In case the Start byte is not equal to F0h the following data bytes are still put in FIFO, additionally a soft framing error IRQ is set to indicate the Start Byte error.

NFCIP-1 Active Communication Initiator

During NFCIP-1 active communication both, initiator and target switch on its field when transmitting and switch off its field when receiving. In order to operate as NFCIP-1 active communication initiator the ST25R3912/3 have to be configured according to *Table 16* (bit targ in *Mode Definition Register* has to be 0):

Table 16. Operation mode/bit rate setting for NFCIP-1 active communication initiator

NFCIP-1 bit rate (kb/s)	Initiator operation mode setting	Bit rate for Tx (kb/s)	Bit rate for Rx (kb/s)	Comments
106	NFCIP-1 active communication	fc/128 (~106)	-	Data rate is the same in both directions for all NFCIP-1 communication.
212		fc/64 (~212)	-	
424		fc/32 (~424)	-	

After selecting the NFCIP-1 active communication mode the receiver and transmitter have to be configured properly. This configuration can be done automatically by sending direct command Analog Preset (see *Analog Preset*).

During NFCIP-1 active communication the RF Collision Avoidance and switching on the field is performed using NFC Field ON commands (see *NFC Field ON commands*), while the sending of message is performed using Transmit commands as in the case of reader communication. Alternatively the Response RF Collision Avoidance sequence is started automatically when the switching off of target field is detected in case the bit nfc_ar in the *Mode Definition Register* is set.

When NFCIP-1 mode is activated the External Field Detector is automatically enabled by setting bit en_fd in the *Auxiliary Display Register*. The Peer Detection Threshold is used to detect target field. During execution of ‘NFC Field ON’ commands, the Collision Avoidance Threshold is used.

Initial set-up of the *Operation Control Register* before the start of communication is the same as in case of reader to tag communication with the exception that the transmitter is not enabled by setting the tx_en bit. The tx_en bit and therefore switching on of the transmitter is controlled by NFC Field ON commands. Switching off the field is performed automatically after a message has been sent. The *General Purpose and No-Response Timer Control Register* is used to define the time during which the field stays switched on after a message has been transmitted.

In order to receive the NFCIP-1 active reply only the AM demodulation channel is used. Due to this the receiver AM channel has to be enabled. The preset done by Analog Preset

command enables only the AM demodulation channel, while PM channel is disabled to save current.

In NFCIP-1 active communication the NFCIP-1Transport Frame format (see *Figure 23*) is always used. Due to this the *ISO14443A and NFC 106kb/s Settings Register* bit nfc_f0 is set by Analog Preset command (see *Support of NFCIP-1 transport frame format*).

NFCIP-1 active communication sequence when bit nfc_ar in the *Mode Definition Register* is set (automatic Response RF Collision Avoidance sequence). During this sequence bits nfc_n1 and nfc_n0 of the *Auxiliary Definition Register* have to be 0 to produce Response Collision Avoidance sequence with n=0:

1. The direct command NFC Initial Field ON is sent. In case no collision was detected during RF Collision Avoidance the field is switched on and an IRQ with I_cat flag set is sent to controller after T_{IRFG}.
2. The message, prepared as in case of reader to tag communication, is transmitted using Transmit command.
3. After the message is sent the field is switched off. The time between the end of the message and switching off the field is defined by the General Purpose timer (the General Purpose timer IRQ may be masked since controller does not need this information).
4. After switching off its field the ST25R3912/3 starts the No-Response timer and observes the External Field Detector output to detect the switching on of the target field. In case the target field is not detected before No-Response timer timeout, an IRQ due No-Response timer expire is sent.
5. When Target field is detected an IRQ with I_eon flag set is sent to controller and Mask Receive timer is started. After the Mask Receive Timer expires the receiver output starts to be observed to detect start of the target response. The reception process goes on as in case of reader to tag communication.
6. When the External Field Detector detects that the target has switched off its field, it sends an IRQ with I_eof flag set to the controller, and in case bit nfc_ar is set automatically activates the sequence of direct command NFC Response Field ON. In case no collision is detected during RF Collision Avoidance the field is switched on and an IRQ with I_cat flag set is sent to controller after T_{ARFG}.
7. Sequence loops through point 2. In case the last initiator command is sent in next sequence (DLS_REQ in case of NFCIP-1 protocol) the bit nfc_ar in the *Mode Definition Register* has to be put to 0 to avoid switching on the initiator field after the target has switched of its field.

NFCIP-1 active communication target

The ST25R3912/3 target mode is activated by setting bit targ in the *Mode Definition Register* to 1. When target mode is activated the External Field Detector is automatically enabled by setting bit en_fd in the *Auxiliary Definition Register*.

When bit targ is set and all bits of the *Operation Control Register* are set to 0, the ST25R3912/3 are in low power Initial NFC Target Mode.

In this mode the External Field Detector with Peer Detection Threshold is enabled.

There are two different NFC target modes implemented (defined by mode bits of the *Mode Definition Register*): the bit rate detection mode and normal mode. In the bit rate detection mode the framing logic performs automatic detection of the initiator data rate and writes it in

the *NFCIP Bit Rate Detection Display Register*. In the normal mode it is supposed that the data rate defined in the *Bit Rate Definition Register* is used.

After selecting the NFCIP-1 active target mode the receiver and transmitter have to be configured properly. Configuration is the same as in case of NFCIP-1 active initiator mode. This configuration can be done automatically by sending direct command Analog Preset (see Analog Preset).

NFCIP-1 active communication sequence when bit nfc_ar in the *Mode Definition Register* is set (automatic Response RF Collision Avoidance sequence). During this sequence bits nfc_n1 and nfc_n0 of the *Auxiliary Definition Register* have to be 0 to produce Response Collision Avoidance with n=0.

The following sequence assumes that the ST25R3912/3 are in the low power Initial NFC Target Mode with the bit rate detection mode selected. Bit nfc_ar in the *Mode Definition Register* is set (automatic Response RF Collision Avoidance sequence). When the initiator field is detected the following sequence is executed:

1. An IRQ with I_eon flag set is sent to the controller.
2. The controller turns on the oscillator, regulator and receiver. Mask Receive timer is started by sending direct command Start Mask Receive timer Timer. After the Mask Receive Timer expires the receiver output starts to be observed to detect start of the initiator message.
3. Once the start of initiator message is detected, an IRQ due to start of receive is sent, the framing logic switches on a module that automatically recognizes the bit rate of signal sent by the initiator. Once the bit rate is recognized an IRQ with I_nfct flag set is sent and the bit rate is automatically loaded in the *NFCIP Bit Rate Detection Display Register*. Detection of bit rate is also a condition that automatic Response RF Collision Avoidance sequence is enabled). The received message is decoded and put into the FIFO, IRQ is sent as after any received message.
4. The controller sends direct command Go to Normal NFC Mode, to copy the content of the *NFCIP Bit Rate Detection Display Register* to the *Bit Rate Definition Register* and to change the NFCIP-1 target mode to normal (the command Go To Normal Mode and reading of received data can be chained). Since the Tx modulation type depends on bit rate, the Tx modulation type also has to be correctly set at this point.
5. When the External Field Detector detects that the target has switched off its field, it sends an IRQ with I_eof flag set to the controller, and in case bit nfc_ar is set automatically activates the sequence of direct command NFC Response Field ON. Bits nfc_n1 and nfc_n0 of the *Auxiliary Definition Register* are used to define number n of Response RF Collision Avoidance sequence. In case no collision is detected during RF Collision Avoidance the field is switched on and an IRQ with I_cat flag set is sent to controller after T_{ARFG}.
6. The reply, prepared as in case of reader to tag communication is transmitted using Transmit command.
7. After the message is sent the field is switched off. The time between the end of the message and switching off the field is defined in the General Purpose timer (the General Purpose timer IRQ may be masked since controller does not need this information).

From this point on the communication with initiator loops through the following sequence (during this sequence bits nfc_n1 and nfc_n0 of the *Auxiliary Definition Register* have to be 0 to produce Response RF Collision Avoidance with n=0):

1. After switching off its field the ST25R3912/3 start the No-Response timer and observes the External Field Detector output to detect the switching on of the initiator field. In case the initiator field is not detected before No-Response timer timeout, an IRQ due No-Response timer expire is sent.
2. When initiator field is detected an IRQ with I_eon flag set is sent to controller and Mask Receive timer is started. After the Mask Receive Timer expires the receiver output starts to be observed to detect start of the initiator response. The reception process goes on as in case of reader to tag communication.
3. When the External Field Detector detects that the target has switched off its field, it sends an IRQ with I_eof flag set to the controller, and in case bit nfc_ar is set automatically activates the sequence of direct command NFC Response Field ON. In case no collision is detected during RF Collision Avoidance the field is switched on and an IRQ with I_cat flag set is sent to controller after T_{ARFG}.
4. The reply that was prepared as in case of reader to tag communication is transmitted using Transmit command
5. After the message is sent the field is switched off. The time between the end of the message and switching off the field is defined in General Purpose timer. In case a new command from initiator is expected the General Purpose timer IRQ may be masked since controller does not need this information.
6. In case a new command from Initiator is expected the sequence loops through point 1. In case the target reply was the last in a sequence (DLS_RES in case of NFCIP-1 protocol) a new command from initiator is not expected.
   At the moment the field is switched off, a General Purpose timer IRQ is received and the ST25R3912/3 are put back in the low power NFC Target Mode by deactivating the *Operation Control Register*. NFC mode is changed back to rate detection mode by writing the *Mode Definition Register*.

1.2.19 AM modulation depth: definition and calibration

The ST25R3912/3 transmitter supports OOK and AM modulation.

The choice between OOK and AM modulation is done by writing bit tr_am in the *Auxiliary Definition Register*. AM modulation is preset by direct command Analog Preset in case the following protocols are configured:

- ISO14443B
- FeliCa™
- NFCIP-1 212 and 424 kb/s

The AM modulation depth can be automatically adjusted by setting the *AM Modulation Depth Control Register* and sending the direct command Calibrate Modulation Depth. There is also an alternative possibility where the command Calibrate Modulation Depth is not used and the modulated level is defined by writing the Antenna driver *RFO AM Modulated Level Definition Register*.

AM modulation depth definition using the direct command Calibrate Modulation Depth

Before sending the direct command Calibrate Modulation Depth the *AM Modulation Depth Control Register* has to be configured in the following way:

- Bit 7 (am_s) has to be set to 0 to choose definition by the command Calibrate Modulation Depth
- Bits 6 to 1 (mod5 to mod0) define target AM modulation depth

Definition of modulation depth using bits mod5 to mod0

The RFID standard documents usually define the AM modulation level in form of the modulation index. The modulation index is defined as (a - b) / (a + b), where a and b are, respectively, the amplitude of the non-modulated carrier and of the modulated carrier.

The modulation index specification is different for different standards. The ISO-14443B modulation index is typically 10% with allowed range from 8 to 14%, while range from 10 to 30% is defined in the ISO-15693, and 8 to 30% in the FeliCa™ and NFCIP-1 212 kb/s and 424 kb/s.

The bits mod5 to mod0 are used to calculate the amplitude of the modulated level. The non-modulated level that was before measured by the A/D converter and stored in an 8 bit register is divided by a binary number in the range from 1 to 1.98. Bits mod5 to mod0 define binary decimals of this number.

Example

In case of the modulation index 10% the ratio between the non-modulated level (a) and the modulated level (b) is 1.2222, which, converted to binary and truncated to six decimals is 1.001110. So, in order to define the modulation index 10% the bits mod5 to mod0 have to be set to 001110.

Table 17 shows the setting of the mod bits and the associated modulation indexes.

Table 17. Setting mod bits

Modulation Index (%)	mod5 … mod0	Modulation Index (%)	mod5 … mod0
0.0	000000	20.0	100000
0.8	000001	20.5	100001
1.5	000010	21.0	100010
2.3	000011	21.5	100011
3.0	000100	22.0	100100
3.8	000101	22.4	100101
4.5	000110	22.9	100110
5.2	000111	23.4	100111
5.9	001000	23.8	101000
6.6	001001	24.3	101001
7.2	001010	24.7	101010
7.9	001011	25.1	101011

Table 17. Setting mod bits (continued)

Modulation Index (%)	mod5 … mod0	Modulation Index (%)	mod5 … mod0
8.6	001100	25.6	101100
9.2	001101	26.0	101101
9.9	001110	26.4	101110
10.5	001111	26.9	101111
11.1	010000	27.3	110000
11.7	010001	27.7	110001
12.3	010010	28.1	110010
12.9	010011	28.5	110011
13.5	010100	28.9	110100
14.1	010101	29.3	110101
14.7	010110	29.7	110110
15.2	010111	30.1	110111
15.8	011000	30.4	111000
16.3	011001	30.8	111001
16.9	011010	31.2	111010
17.4	011011	31.6	111011
17.9	011100	31.9	111100
18.5	011101	32.3	111101
19.0	011110	32.6	111110
19.5	011111	33.0	111111

Execution of direct command Calibrate Modulation Depth

The modulation level is adjusted by increasing the RFO1 and RFO2 driver output resistance. The RFO drivers are composed of 8 binary weighted segments. Usually all these segments are turned on to define the normal, non-modulated level, there is also a possibility to increase the output resistance of the non-modulated state by writing the *RFO Normal Level Definition Register*.

Before sending the direct command Calibrate Modulation Depth the oscillator and regulators have to be turned on. When the direct command Calibrate Modulation Depth is sent the following procedure is executed:

1. The transmitter is turned on, non-modulated level is established.
2. The amplitude of the non-modulated carrier level established on the inputs RFI1 and RFI2 is measured by the A/D converter and stored in the *A/D Converter Output Register*.
3. Based on the measurement of the non-modulated level and the target modulated level defined by the bits mod5 to mod0 the target modulated level is calculated.
4. The output driver strength is adjusted using a successive approximation algorithm until the field strength is as close as possible to the calculated target modulated level.
5. The result of the output driver strength adjustment is copied in the *AM Modulation Depth Display Register*. Content of this register is used to define the AM modulated level.

Note: After the calibration procedure is finished, the content of the RFO Normal Level Definition Register should not be changed. Modifications of the content of this register will change the non-modulated amplitude and therefore the ratio between the modulated and non-modulated level.

Note: In case the calibration of antenna resonant frequency in used, the command Calibrate Antenna has to be run before AM modulation depth adjustment.

AM modulation depth definition using the RFO AM Modulated Level Definition Register

When bit 7 (am_s) of the *AM Modulation Depth Control Register* is set to 1 the AM modulated level is controlled by writing the *RFO Normal Level Definition Register*. If the setting of the modulated level is already known it is not necessary to run the calibration procedure, the modulated level can be defined just by writing this register.

It is also possible to implement calibration procedure through an external controller using the *RFO Normal Level Definition Register* and the direct command Measure Amplitude. This procedure has to be used when the target modulation depth is deeper than 33%.

The procedure is the following:

1. Write the non-modulated level in the *RFO Normal Level Definition Register* (usually it is all 0 to have the lower possible output resistance).
2. Switch on the transmitter.
3. Send the direct command Measure Amplitude. Read result from the *A/D Converter Output Register*.
4. Calculate the target modulated level from the target modulation index and result of the previous point.
5. In the following iterations content of the *RFO Normal Level Definition Register* is modified, the command Measure Amplitude executed and the result compared with the target modulated level as long as the result is not equal (or as close as possible) to the target modulated level.
6. At the end the content of the *RFO Normal Level Definition Register* that results in the target modulated level is written in the *RFO AM Modulated Level Definition Register* while the *RFO Normal Level Definition Register* is restored with the non-modulated definition value.

1.2.20 Antenna tuning (ST25R3913 only)

The ST25R3913 integrate the blocks needed to check and to adjust the antenna LC tank resonance frequency. The Phase and Amplitude Detector block is used for resonance frequency checking and adjustment.

In order to implement the antenna LC tank calibration tuning capacitors have to be connected between the two coil terminals to the pins TRIM1_3 to TRIM1_0 and TRIM2_3 to TRIM2_0. In case single driver is used only the pins TRIM1_3 to TRIM1_0 are used, pins TRIM2_3 to TRIM2_0 are left open. *Figure 24* shows the connection of the trim capacitors for both single (left side) and differential (right side) driving for the simple case where the antenna LC tank is directly connected to RFO pins.

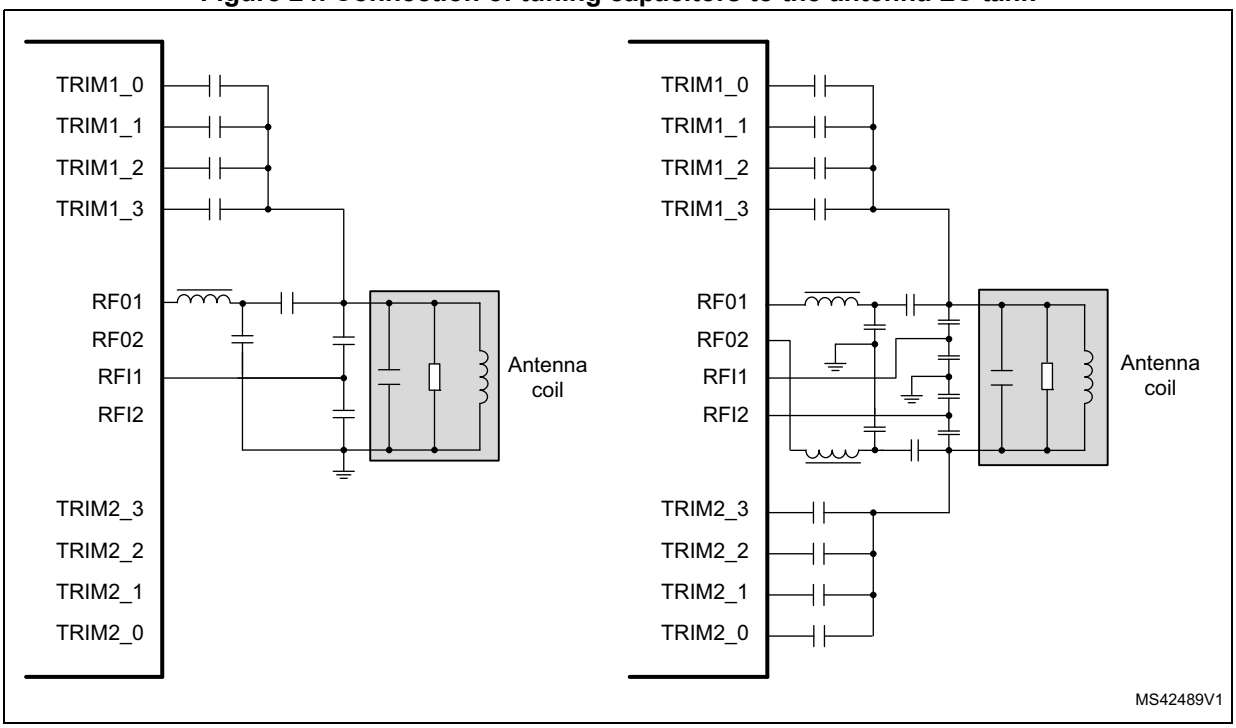
The TRIMx_y pins contain the HVNMOS switching transistors to VSS.

The on resistance of TRIM1_0 and TRIM2_0 switch transistors to be connected to LSB tuning capacitor is 50 Ω typ. at 3 V VSP_D, the on resistance of other pins is binary weighted (the on resistance of TRIM1_3 and TRIM2_3 is 6.25 Ω typ.) The breakdown voltage of the HVNMOS switch transistors is 25 V, putting a limit to the maximum peak to peak voltage on LC tank in case tuning is used.

During tuning procedure the resonance frequency is adjusted by connecting some of the tuning capacitors to VSS and leaving others floating. The switches of the same binary weight are driven from the same source and are both on or off (the switches TRIM1_2 and TRIM2_2 are for example both either on or off).

Antenna tuning can be automatically performed by sending direct command Calibrate Antenna or by an algorithm implemented in external controller by performing phase and amplitude measurements and controlling the TRIM switches using *Antenna Calibration Control Register*.

Figure 24. Connection of tuning capacitors to the antenna LC tank



Antenna tuning using Calibrate Antenna direct command (ST25R3913 only)

In order to perform the antenna LC tank using direct command Calibrate Antenna binary weighted tuning capacitors have to be connected between the two coil terminals to the pins TRIM1_3 to TRIM1_0 and TRIM2_3 to TRIM2_0.

During automatic procedure, started by sending the direct command Calibrate Antenna, the ST25R3913 finds the position of TRIM switches where the phase difference between the RFO output signal and RFI input signal is as close as possible to the target phase defined in the *Antenna Calibration Target Register*.

In case the antenna LC tank is directly connected to RFO pins (see *Figure 24*, where the cases of single and differential driving are reported, respectively on the left and on the right) there is 90° phase shift between signal on the RFO outputs and the voltage on the RFI inputs when antenna LC tank is in resonance. In case additional EMC filter is inserted between RFO outputs and antenna LC tank the phase shift in case of resonance depends on additional phase shift generated by EMC filter.

During execution of the direct command Calibrate Antenna the ST25R3913 runs several phase measurements and changes configuration of TRIMx_y pins in order to find the best possible setting. Due to this the format of the *Antenna Calibration Target Register* is the same as the format of direct command Measure Phase result.

The TRIMx_y pin configuration that is the result of the direct command Calibrate Antenna can be observed by reading the *Antenna Calibration Display Register*. This register also contains an error flag that is set in case the tuning to target phase was not possible.

After the execution of direct command Calibrate Antenna the actual phase can be checked by sending direct command Measure Phase.

Antenna tuning using Antenna Calibration Control Register (ST25R3913 only)

There is also a possibility to control the position of the TRIM switches by writing the *Antenna Calibration Control Register*.

When the bit trim_s of this register is set to 1 position of the trim switches is controlled by bits tre_3 to tre_0.

Using this register and performing phase and amplitude measurements (using direct commands Measure Phase and Measure Amplitude) different tuning algorithms can be implemented in the external controller.

1.2.21 Stream mode and Transparent mode

Standard and custom 13.56 MHz RFID reader protocols not supported by the ST25R3912/3 framing can be implemented using the ST25R3912/3 AFE and framing implemented in the external microcontroller.

Transparent mode

After sending the direct command Transparent Mode the external microcontroller directly controls the transmission modulator and gets the receiver output (control logic becomes “transparent”).

The Transparent mode is entered on rising edge of signal /SS after sending the command Transparent Mode and is maintained as long as the signal /SS is kept high. Before sending the direct command Transparent Mode the transmitter and receiver have to be turned on, the AFE has to be configured properly.

While the ST25R3912/3 are in the Transparent mode, the AFE is controlled directly through the SPI:

- Transmitter modulation is controlled by pin MOSI (high is modulator on)
- Signal rx_on is controlled by pin SCLK (high enables RSSI and AGC)
- Output of receiver AM demodulation chain (digitized sub-carrier signal) is sent to pin MISO
- Output of receiver PM demodulation chain (digitized sub-carrier signal) is sent to pin IRQ

By controlling the rx_on advanced receiver features like the RSSI and AGC can be used. The receiver channel selection bits are valid also in Transparent mode, therefore it is possible to use only one of the two channel outputs. In case single channel is selected it is always multiplexed to MISO, while IRQ is kept low.

Configuration bits related to the ISO mode, framing and FIFO are meaningless in Transparent mode, while all other configuration bits are respected.

Use of Transparent mode to implement active Peer to Peer (NFC) communication

The framing implemented in the ST25R3912/3 supports all active modes according to the NFCIP-1 specification (ISO/IEC 18092:2004). In case any amendments to this specification or some custom active NFC communication need to be implemented Transparent mode can be used.

There is no special NFC active communication transparent mode, controlling of the Tx modulation and the Rx is done as described above. The difference comparing to the reader transparent mode is that the emission of the carrier field has to be enabled only during Tx. This is done by writing the *Operation Control Register* before and after Tx. Since with every SPI command the Transparent mode is lost it has to be re-entered.

In order to receive the reply in active NFC communication mode only the AM demodulation channel is used. Due to this the receiver AM channel has to be enabled, while PM can be disabled.

Implementing active communication requires detection of external field. Setting the bit en_fd in the *Auxiliary Definition Register* enables the External Field Detector with Peer Detection Threshold. When bit en_fd is selected and the ST25R3912/3 are in Transparent mode, the External Field Detector output is multiplexed to pin IRQ. This enables detection of external target/initiator field and performing RF Collision Avoidance.

In case timing of the NFC Field ON command is correct for the NFC active protocol being implemented, these commands can be used in combination with the Transparent mode. These commands are used to perform the RF Collision Avoidance, switching on the field and timing out the minimum time from switching on the field to start of transmitting the message. After getting the interrupt, the controller generates the message in the Transparent mode.

When bit en_fd is set and all bits of the *Operation Control Register* are set to 0 the ST25R3912/3 are in the low power NFC Target Mode (same as in case of setting of targ bit, (see NFCIP-1 Active Communication Target). In this mode initiator field is detected.

After getting an IRQ with I_eon flag set, the controller turns on the oscillator, regulator and receiver and performs reception in the Transparent mode.

MIFARE™ Classic compatibility

For communication with MIFARE™ Classic compliant devices the bit6 and bit7 from the register 05h can be used to enable Type A custom frames. Alternatively, the stream mode of ST25R3912/3 can be used to send and receive MIFARE™ Classic compliant or custom frames.

Stream mode

Stream mode can be used to implement protocols, where the low level framing needed for ISO14443 receive coding can be used and decoded information can be put in FIFO. The main advantage of this mode over the Transparent mode is that timing is generated in the ST25R3912/3 therefore the external controller does not have to operate in real time. The stream mode is selected in the *Mode Definition Register*, the operating options are defined in the *Stream Mode Definition Register*.

Two different modes are supported for tag to reader communication (Sub-carrier and BPSK Stream Modes). General rule for Stream mode is that the first bit sent/received is put on the LSB position of the FIFO byte.

After selecting the stream mode the receiver and transmitter have to be configured properly (Analog Preset direct command doesn't apply for stream mode).

Sub-Carrier Stream Mode

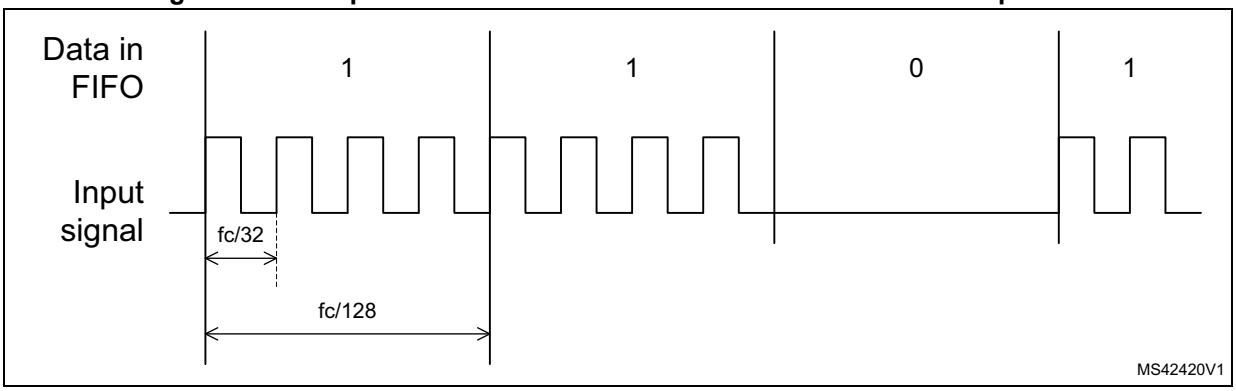
This mode supports protocols where during the tag to reader communication the time periods with sub-carrier signal are interchanged with time periods without modulation (like in the ISO14443A 106 kbit/s mode). In this mode the sub-carrier frequency and number of sub-carrier frequency periods in one reporting period is defined. Sub-carrier frequency in the range from fc/64 (212 kHz) to fc/8 (1695 kHz) are supported.

Supported number of sub-carrier frequency periods in one reporting period range from two to eight.

Start of receive interrupt is sent and the first data bit is put in FIFO after the first reporting time period with sub-carrier is detected. One bit of FIFO data gives information about status of input signal during one reporting period. Logic 1 means that the sub-carrier was detected during reporting period, while 0 means that no modulation was detected during reporting period. End of receive is reported when no sub-carrier signal in more than eight reporting periods have been detected.

Figure 25 shows an example for setting scf = 01b and scp = 10b. With this setting the sub-carrier frequency is set to fc/32 (424 kHz) and the reporting period to four sub-carrier periods (128/fc ~106 µs).

Figure 25. Example of sub-carrier stream mode for scf = 01b and scp = 10b



BPSK Stream Mode

This mode supports protocols where during the tag to reader communication BPSK code is used (like in the ISO14443B mode).

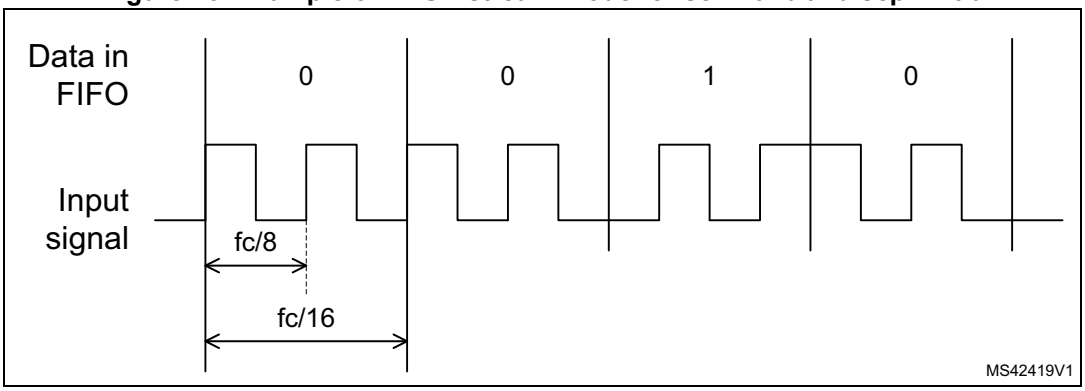
In this mode the sub-carrier frequency and number of sub-carrier frequency periods in one reporting period is defined. Sub-carrier frequency in the range from fc/16 (848 kHz) to fc/4 (3390 kHz) are supported. Supported number of sub-carrier frequency periods in one reporting period range from one to eight.

Start of receive interrupt is sent and the first data bit is put in FIFO after the first reporting time period with sub-carrier is detected. Logic 0 is used for the initially detected phase, while logic 1 indicates inverted phase comparing to the initial phase.

End of receive is reported when the first reporting period without sub-carrier is detected.

Figure 26 shows an example for setting scf = 01b and scp = 01b. With this setting the sub-carrier frequency is set to fc/8 (1695 kHz) and the reporting period to two sub-carrier periods (16/fc ~1.18 µs).

Figure 26. Example of BPSK stream mode for scf = 01b and scp = 10b



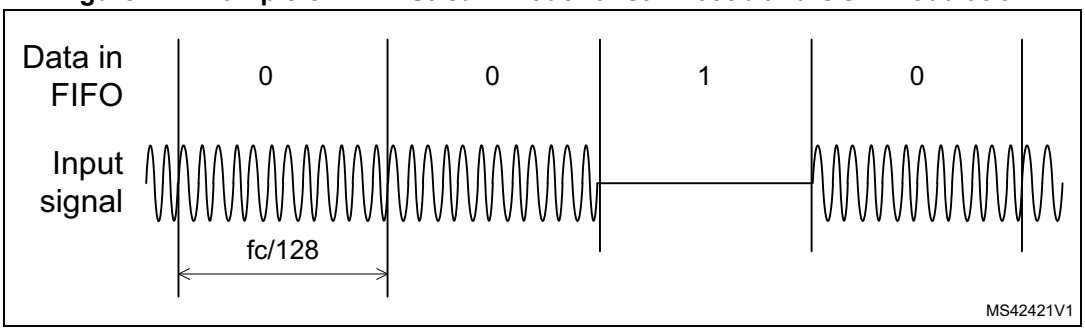
Reader to Tag Communication in Stream Mode

Reader to tag communication control is the same for both stream modes. Reader to tag coding is defined by data put in FIFO. The stx bits of *Stream Mode Definition Register* define the Tx time period during which one bit of FIFO data define the status of transmitter. In case the data bit is set to logic 0 there is no modulation, in case it is logic 1 the transmitted carrier signal is modulated according to current modulation type setting (AM or OOK).

Transmission in stream mode is started by sending direct commands Transmit Without CRC or Transmit With CRC.

Figure 27 shows an example for setting stx = 000b. With this setting the Tx time period is defined to 128/fc (~9,44 µs).

Figure 27. Example of Tx in Stream Mode for stx = 000b and OOK modulation



1.3 Registers

The 6-bit register addresses below are defined in hexadecimal notation. The possible addresses range from 00h to 3Fh.

There are two types of registers implemented in the ST25R3912/3:

- configuration registers
- display registers

The configuration registers are used to configure the ST25R3912/3. They can be read and written (RW) through the SPI. The display registers are read only (R); they contain information about the ST25R3912/3 internal state.

Registers are set to their default state at power-up and after sending direct command Set Default. The exceptions are *IO Configuration Register 1*, *IO Configuration Register 2* and *Operation Control Register*.. These registers are related to the hardware configuration and are reset to their default state only at power-up.

Table 18. Registers map

Address (hex)	Main function	Content	Comment	Type
00	IO configuration	*IO Configuration Register 1*	Set to default state only at power-up	RW
01		*IO Configuration Register 2*		RW
02	Operation control and Mode definition	*Operation Control Register*	Set to default state only at power-up	RW
03		*Mode Definition Register*	-	RW
04		*Bit Rate Definition Register*	-	RW
05	Configuration	*ISO14443A and NFC 106kb/s Settings Register*	-	RW
06		*ISO14443B Settings Register 1*	-	RW
07		*ISO14443B and FeliCa Settings Register*	-	RW
08		*Stream Mode Definition Register*	-	RW
09		*Auxiliary Definition Register*	-	RW
0A		*Receiver Configuration Register 1*	-	RW
0B		*Receiver Configuration Register 2*	-	RW
0C		*Receiver Configuration Register 3*	-	RW
0D		*Receiver Configuration Register 4*	-	RW
0E	Timer definition	*Mask Receive Timer Register*	-	RW
0F		*No-Response Timer Register 1*	-	RW
10		*No-Response Timer Register 2*	-	RW
11		*General Purpose and No-Response Timer Control Register*	-	RW
12		*General Purpose Timer Register 1*	-	RW
13		*General Purpose Timer Register 2*	-	RW

Table 18. Registers map (continued)

Address (hex)	Main function	Content	Comment	Type
14	Interrupt and associated reporting	*Main Interrupt Register*	-	RW
15		*Mask Timer and NFC Interrupt Register*	-	RW
16		*Mask Error and Wake-Up Interrupt Register*	-	RW
17		*Main Interrupt Register*	-	R
18		*Mask Timer and NFC Interrupt Register*	-	R
19		*Error and Wake-Up Interrupt Register*	-	R
1A		*FIFO Status Register 1*	-	R
1B		*FIFO Status Register 2*	-	R
1C		*Collision Display Register*	-	R
1D	Definition of transmitted bytes	*Number of Transmitted Bytes Register 1*	-	RW
1E		*Number of Transmitted Bytes Register 2*	-	RW
1F	NFCIP bit rate detection display	*NFCIP Bit Rate Detection Display Register*	-	R
20	A/D converter output	*A/D Converter Output Register*	-	R
21	Antenna calibration	*Antenna Calibration Control Register*	-	RW
22		*Antenna Calibration Target Register*	-	RW
23		*Antenna Calibration Display Register*	-	R
24	AM modulation depth and Antenna driver	*AM Modulation Depth Control Register*	-	RW
25		*AM Modulation Depth Display Register*	-	R
26		*RFO AM Modulated Level Definition Register*	-	RW
27		*RFO Normal Level Definition Register*	-	RW
29	External field detector threshold	*External Field Detector Threshold Register*	-	RW
2A	Regulator	*Regulator Voltage Control Register*	-	RW
2B		*Regulator and Timer Display Register*	-	R
2C	Receiver State display	*RSSI Display Register*	-	R
2D		*Gain Reduction State Register*	-	R
2E	Reserved	-	-	R
2F		-	-	R
30	Auxiliary display	*Auxiliary Display Register*	-	R

Table 18. Registers map (continued)

Address (hex)	Main function	Content	Comment	Type
31	Wake-Up	*Wake-Up Timer Control Register*	-	RW
32		*Amplitude Measurement Configuration Register*	-	RW
33		*Amplitude Measurement Reference Register*	-	RW
34		*Amplitude Measurement Auto-Averaging Display Register*	-	R
35		*Amplitude Measurement Display Register*	-	R
36		*Phase Measurement Configuration Register*	-	RW
37		*Phase Measurement Reference Register*	-	RW
38		*Phase Measurement Auto-Averaging Display Register*	-	R
39		*Phase Measurement Display Register*	-	R
3A	Reserved	-	-	R
3B	Reserved	-	-	R
3C	Reserved	-	-	R
3D	Reserved	-	-	R
3F	IC Identity	*IC Identity Register*	-	R

1.3.1 IO Configuration Register 1

Address: 00h

Type: RW

Table 19. IO Configuration Register 1(1)

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="4">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>single</td><td>0</td><td colspan="4">1: Only one RFO driver will be used</td><td>Choose between single and differential antenna driving</td></tr>
<tr><td>6</td><td>rfo2</td><td>0</td><td colspan="4">0: RFO1, RFI1
1: RFO2, RFI2</td><td>Choose which output driver and which input will be used in case of single driving</td></tr>
<tr><td>5</td><td>fifo_lr</td><td>0</td><td colspan="4">0: 64
1: 80</td><td>FIFO water level for receive</td></tr>
<tr><td>4</td><td>fifo_lt</td><td>0</td><td colspan="4">0: 32
1: 16</td><td>FIFO water level for transmit</td></tr>
<tr><td>3</td><td>osc</td><td>1</td><td colspan="4">0: 13.56 MHz Xtal
1: 27.12 MHz Xtal</td><td>Selector for crystal oscillator</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">out_cl1</td><td rowspan="4">0</td><td>out_cl1</td><td>out_cl0</td><td>MCU_CLK</td><td rowspan="5">Selection of clock frequency on MCU_CLK output in case Xtal oscillator is running. In case of “11” MCU_CLK output is permanently low.</td></tr>
<tr><td>0</td><td>0</td><td>3.39 MHz</td></tr>
<tr><td>0</td><td>1</td><td>6.78 MHz</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">out_cl0</td><td rowspan="2">0</td><td>1</td><td>0</td><td>13.56 MHz</td></tr>
<tr><td>1</td><td>1</td><td>disabled</td></tr>
<tr><td>0</td><td>lf_clk_off</td><td>0</td><td colspan="4">1: No LF clock on MCU_CLK</td><td>By default the 32 kHz LF clock is present on MCU_CLK output when Xtal oscillator is not running and the MCU_CLK output is not disabled.</td></tr>
</table>

1. Default setting takes place at power-up only.

1.3.2 IO Configuration Register 2

Address: 01h

Type: RW

Table 20. IO Configuration Register 2(1)

Bit	Name	Default	Function	Comments
7	sup3 V	0	0: 5 V supply 1: 3.3 V supply	5 V supply, range: 4.1 V to 5.5 V 3.3 V supply, range: 2.4 V to 3.6 V
6	vspd_off	0	1: Disable VSP_D regulator	Used for low cost applications. When this bit is set: – At 3 V or 5 V supply VSP_D and VSP_A shall be shorted externally – For 3.3 V applications VSP_D can alternatively be supplied from V_{DD} in case V_{SP_A} is not more than 300 mV lower then V_{DD}
5	-	-	Not used	-
4	miso_pd2	0	1: Pull-down on MISO, when /SS is low and MISO is not driven by the ST25R3912/3	-
3	miso_pd1	0	1: Pull-down on MISO when /SS is high	-
2	io_18	0	1: Increase MISO driving level in case of 1.8 V V_{DD_IO}	-
1	-	-	Not used	-
0	slow_up	0	1: Slow ramp at Tx on	≥ 10 µs, 10% to 90%, for B

1. Default setting takes place at power-up only.

1.3.3 Operation Control Register

Address: 02h

Type: RW

Table 21. Operation Control Register(1)

Bit	Name	Default	Function	Comments
7	en	0	1: Enables oscillator and regulator (Ready mode)	-
6	rx_en	0	1: Enables Rx operation	-
5	rx_chn	0	0: Both, AM and PM, channels enabled 1: One channel enabled	In case only one Rx channel is enabled, selection is done by the *Receiver Configuration Register 1* bit ch_sel
4	rx_man	0	0: Automatic channel selection 1: Manual channel selection	In case both Rx channels are enabled, it chooses the method of channel selection, manual selection is done by the *Receiver Configuration Register 1* bit ch_sel
3	tx_en	0	1: Enables Tx operation	This bit is automatically set by NFC Field ON commands and reset in NFC active communication modes after transmission is finished
2	wu	0	1: Enables Wake-up mode	According to settings in *Wake-Up Timer Control Register*
1	-	-	Not used	-
0	-	-		-

1. Default setting takes place at power-up only.

1.3.4 Mode Definition Register

Address: 03h

Type: RW

Table 22. Mode Definition Register(1)

Bit	Name	Default	Function	Comments
7	targ	0	0: Initiator 1: Target	-
6	om3	0	Refer to *Table 23* and *Table 24*	Selection of operation mode Different for initiator and target modes
5	om2	0		
4	om1	0		
3	om0	1		
2	-	0	Not used	-
1	-	0		-
0	nfc_ar	0	1: Automatic start Response RF Collision Avoidance sequence	Automatically starts the Response RF Collision Avoidance if an external field off is detected

1. Default setting takes place at power-up and after Set Default command.

Table 23. Initiator Operation Modes(1)

om3	om2	om1	om0	Comments
0	0	0	0	NFCIP-1 active communication
0	0	0	1	ISO14443A
0	0	1	0	ISO14443B
0	0	1	1	FeliCa™
0	1	0	0	NFC Forum Type 1 Tag (Topaz)
1	1	1	0	Sub-carrier stream mode
1	1	1	1	BPSK stream mode
Other combinations				Not used

1. If a non supported operation mode is selected the Tx/Rx operation is disabled.

Table 24. Target Operation Modes(1)

om3	om2	om1	om0	Comments
0	0	0	0	NFCIP-1 active communication, bit rate detection mode
0	0	0	1	NFCIP-1 active communication, normal mode
Other combinations				Not used

1. If a non supported operation mode is selected the Tx/Rx operation is disabled.

1.3.5 Bit Rate Definition Register

Address: 04h

Type: RW

Table 25. Bit Rate Definition Register(1)(2)

Bit	Name	Default	Function	Comments
7	tx_rate3	0	Refer to *Table 26*	Selects bit rate for Tx
6	tx_rate2	0		
5	tx_rate1	0		
4	tx_rate0	0		
3	rx_rate3	0		Selects bit rate for Rx in case selected protocol allows different bit rates for Rx and Tx
2	rx_rate2	0		
1	rx_rate1	0		
0	rx_rate0	0		

1. Default setting takes place at power-up and after Set Default command.
2. Automatically loaded by direct command Go to Normal NFC Mode.

Table 26. Bit rate coding(1)

rate3	rate2	rate1	rate0	Bit rate (kbit/s)	Comments
0	0	0	0	fc/128 (~106)	-
0	0	0	1	fc/64 (~212)	-
0	0	1	0	fc/32 (~424)	-
0	0	1	1	fc/16 (~848)	-
Other combinations				-	Not used

1. If a non supported bit rate is selected the Tx/Rx operation is disabled.

1.3.6 ISO14443A and NFC 106kb/s Settings Register

Address: 05h

Type: RW

Table 27. ISO14443A and NFC 106kb/s Settings Register(1)

Bit	Name	Default	Function	Comments
7	no_tx_par(2)	0	1: No parity bit is generated during Tx	Data stream is taken from FIFO, transmit has to be done using command Transmit Without CRC.
6	no_rx_par(2)	0	1: Receive without parity and CRC	When set to 1 received bit stream is put in the FIFO, no parity and CRC detection is done, must be set to 0 when not in ISO14443A mode.
5	nfc_f0	0	1: Support of NFCIP-1 Transport Frame format	Add SB (F0) and LEN bytes during Tx and skip SB (F0) byte during Rx.
4	p_len3	0	Refer to *Table 28*	Modulation pulse width, defined in number of 13.56 MHz clock periods.
3	p_len2	0		
2	p_len1	0		
1	p_len0	0		
0	antcl	0	1: ISO14443 anticollision frame	Must be set to 1 when ISO14443A bit oriented anticollision frame is sent.

1. Default setting takes place at power-up and after Set Default command.
2. no_tx_par and no_rx_par are used to send and receive custom frames like Mifare™ Classic frames.

Table 28. ISO14443A modulation pulse width

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1/fc for different bit rates			
				fc/128	fc/64	fc/32	fc/16
0	1	1	1	42	-	-	-
0	1	1	0	41	20	-	-
0	1	0	1	40	21	-	-
0	1	0	0	39	22	13	-
0	0	1	1	38	21	12	8
0	0	1	0	37	20	11	7
0	0	0	1	36	19	10	6
0	0	0	0	35	18	9	5
1	1	1	1	34	17	8	4
1	1	1	0	33	16	7	3
1	1	0	1	32	15	6	2
1	1	0	0	31	14	5	-
1	0	1	1	30	13	-	-
1	0	1	0	29	12	-	-

Table 28. ISO14443A modulation pulse width (continued)

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1/fc for different bit rates			
				fc/128	fc/64	fc/32	fc/16
1	0	0	1	28	-	-	-
1	0	0	0	27	-	-	-

1.3.7 ISO14443B Settings Register 1

Address: 06h

Type: RW

Table 29. ISO14443B Settings Register 1(1)

Bit	Name	Default	Function				Comments
7	egt2	0	egt2	egt1	egt0	Number of etu	EGT defined in number of etu
			0	0	0	0	
6	egt1	0	0	0	1	1	
			⋮	⋮	⋮	⋮	
5	egt0	0	1	1	0	6	
			1	1	1	6	
4	sof_0	0	0: 10 etu 1: 11 etu				SOF, number of etu with logic 0 (10 or 11)
3	sof_1	0	0: 2 etu 1: 3 etu				SOF, number of etu with logic 1 (2 or 3)
2	eof	0	0: 10 etu 1: 11 etu				EOF, number of etu with logic 0 (10 or 11)
1	half	0	0: SOF, and EOF defined by sof_0, sof_1, and eof bit 1: SOF 10.5, 2.5, EOF: 10.5				Sets SOF and EOF settings in middle of specification
0	rx_st_om	0	0: Start/stop bit must be present for Rx 1: Start/stop bit omission for Rx				SOF= fixed to 10 low - 2 high, EOF not defined, put in FIFO last full byte(2)

1. Default setting takes place at power-up and after Set Default command.
2. Start/stop bit omission for Tx can be implemented by using Stream mode.

1.3.8 ISO14443B and FeliCa Settings Register

Address: 07h

Type: RW

Table 30. ISO14443B and FeliCa Settings Register(1)

Bit	Name	Default	Function	Comments
7	tr1_1	0	Refer to *Table 31*	-
6	tr1_0	0		
5	no_sof	0	1: No SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3 Support of B'
4	no_eof	0	1: No EOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3
3	eof_12	0	0: PICC EOF 10 to 11 etu 1: PICC EOF 10 to 12 etu	Support of B(2)
2	phc_th	0	1: Increased tolerance of phase change detection	-
1	f_p1	0	00: 48 01: 64 10: 80 11: 96	FeliCa preamble length (valid also for NFCIP-1 active communication bit rates 242 and 484 kb/s)
0	f_p0	0		

1. Default setting takes place at power-up and after Set Default command.
2. Detection of EOF requires larger tolerance range for bit rates with only one sub-carrier frequency period per bit (fc/16 and higher). Due to this it is not possible to distinguish between EOF with 11 and 12 etu and setting this bit has no impact on EOF detection.

Table 31. Minimum TR1 codings

tr1_1	tr1_0	Minimum TR1 for a PICC to PCD Bit Rate	
		fc/128	>fc/128
0	0	80/fs	80/fs
0	1	64/fs	32/fs
1	0	Not used	Not used
1	1	Not used	Not used

1.3.9 Stream Mode Definition Register

Address: 08h

Type: RW

Table 32. Stream Mode Definition Register(1)

Bit	Name	Default	Function			Comments
7		0	-			-
6	scf1	0	Refer to *Table 33*			Sub-carrier frequency definition for Sub-carrier and BPSK stream mode
5	scf0	0				
4	scp1	0	**scp1**	**scp0**	**Number of pulses**	Number of sub-carrier pulses in report period for Sub-carrier and BPSK stream mode
			0	0	1 (BPSK only)	
			0	1	2	
3	scp0	0	1	0	4	
			1	1	8	
2	stx2	0	Refer to *Table 34*			Definition of time period for Tx modulator control (for Sub-carrier and BPSK stream mode)
1	stx1	0				
0	stx0					

1. Default setting takes place at power-up and after Set Default command.

Table 33. Sub-carrier frequency definition for Sub-Carrier and BPSK Stream Mode

scf1	scf0	Sub-Carrier Mode	BPSK Mode
0	0	fc/64 (212 kHz)	fc/16 (848 kHz)
0	1	fc/32 (424 kHz)	fc/8 (1695 kHz)
1	0	fc/16 (848 kHz)	fc/4 (3390 kHz)
1	1	fc/8 (1695 kHz)	Not used

Table 34. Definition of time period for Stream Mode Tx Modulator Control

stx2	stx1	stx0	Time period
0	0	0	fc/128 (106 kHz)
0	0	1	fc/64 (212 kHz)
0	1	0	fc/32 (424 kHz)
0	1	1	fc/16 (848 kHz)
1	0	0	fc/8 (1695 kHz)
1	0	1	fc/4 (3390 kHz)
1	1	0	fc/2 (6780 kHz)
1	1	1	Not used

1.3.10 Auxiliary Definition Register

Address: 09h

Type: RW

Table 35. Auxiliary Definition Register(1)

Bit	Name	Default	Function	Comments
7	no_crc_rx	0	1: Receive without CRC	Valid for all protocols, for ISO14443A REQA, WUPA and anticollision receive without CRC is done automatically(2)
6	crc_2_fifo	0	1: Make CRC check, but put CRC bytes in FIFO and add them to number of receive bytes	Needed for EMV compliance
5	tr_am	0	0: OOK 1: AM	Set automatically by command Analog Preset, can be modified by register write, has to be defined for transparent and bit stream mode Tx
4	en_fd	0	1: Enable External Field Detector	External Field Detector with Peer Detection threshold is activated. Preset for NFCIP-1 active communication mode
3	ook_hr	0	1: Put RFO driver in tristate during OOK modulation	Valid for all protocols using OOK modulation (also in transparent mode)
2	rx_tol	1	1: BPSK fc/32: more tolerant BPSK decoder for bit rate fc/32, ISO14443A fc/128, NFCIP-1 fc/128: more tolerant processing of first byte	-
1	nfc_n1	0	-	Value of n for direct commands NFC Initial Field ON and NFC Response Field ON (0 ... 3)
0	nfc_n0	0		

1. Default setting takes place at power-up and after Set Default command.
2. Receive without CRC is done automatically when REQA and WUPA commands are sent using direct commands Transmit REQA and Transmit WUPA, respectively, and in case anticollision is performed setting bit antcl.

1.3.11 Receiver Configuration Register 1

Address: 0Ah

Type: RW

Table 36. Receiver Configuration Register 1(1)

Bit	Name	Default	Function	Comments
7	ch_sel	0	0: Enable AM channel 1: Enable PM channel	If only one Rx channel is enabled in the *Operation Control Register* it defines which channel is enabled. If both channels are enabled and manual channel selection is active, it defines which channel is used for receive framing.
6	amd_sel	0	0: Peak detector 1: Mixer	AM demodulator type select
5	lp2	0	Low pass control (see *Table 2*)	For automatic and other recommended filter settings, refer to *Table 3*.
4	lp1	0		
3	lp0	0		
2	h200	0	First and third stage zero setting (see *Table 1*)	
1	h80	0		
0	z12k	0		

1. Default setting takes place at power-up and after Set Default command.

1.3.12 Receiver Configuration Register 2

Address: 0Bh

Type: RW

Table 37. Receiver Configuration Register 2(1)

Bit	Name	Default	Function	Comments
7	rx_lp	0	1: Low power receiver operation	-
6	lf_op	0	0: Differential LF operation 1: LF input split (RFI1 to AM channel, RFI2 to PM channel)	-
5	lf_en	0	1: LF signal on receiver input	-
4	agc_en	1	1: AGC is enabled	-
3	agc_m	1	0: AGC operates on first eight sub-carrier pulses 1: AGC operates during complete receive period	-
2	agc_alg	0	0: Algorithm with preset is used 1: Algorithm with reset is used	Algorithm with preset is recommended for protocols with short SOF (like ISO14443A fc/128)
1	sqm_dyn	1	1: Automatic squelch activation after end of Tx	Squelch is started 18.88 µs after end of Tx, and stopped when Mask Receive Timer expires
0	pmix_cl	0	0: RFO 1: Internal signal	PM demodulator mixer clock source, in single mode internal signal is always used

1. Default setting takes place at power-up and after Set Default command.

1.3.13 Receiver Configuration Register 3

Address: 0Ch (1st stage gain settings)

Type: RW

Table 38. Receiver Configuration Register 3(1)

Bit	Name	Default	Function	Comments
7	rg1_am2	1	Gain reduction/boost in first gain stage of AM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost +5.5 dB
6	rg1_am1	1		
5	rg1_am0	0		
4	rg1_pm2	1	Gain reduction/boost in first gain stage of PM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost +5.5 dB
3	rg1_pm1	1		
2	rg1_pm0	0		
1	lim	0	1: Clip output of 1st and 2nd stage	Signal clipped to 0.6 V, preset for NFCIP-1 active communication mode
0	rg_nfc	0	1: Forces gain reduction in 2nd and 3rd gain stage to -6 dB and maximum comparator window	Preset for NFCIP-1 active communication mode. After clearing this bit, receiver must be restarted.

1. Default setting takes place at power-up and after Set Default command.

1.3.14 Receiver Configuration Register 4

Address: 0Dh (2nd and 3rd stage gain settings)

Type: RW

Table 39. Receiver Configuration Register 4(1)(2)

Bit	Name	Default	Function	Comments
7	rg2_am3	0	AM channel: Gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3dB steps – values from 5h to Ah additionally reduce the gain in 2nd and 3rd gain stage, always in 3 dB steps.
6	rg2_am2	0		
5	rg2_am1	0		
4	rg2_am0	0		
3	rg2_pm3	0	PM channel: Gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3dB steps – values from 5h to Ah additionally reduce the gain in 2nd and 3rd gain stage, always in 3 dB steps.
2	rg2_pm2	0		
1	rg2_pm1	0		
0	rg2_pm0	0		

1. Default setting takes place at power-up and after Set Default command.
2. Sending of direct command Reset Rx Gain is necessary to load the value of this register into AGC, Squelch, and RSSI block.

1.3.15 Mask Receive Timer Register

Address: 0Eh

Type: RW

Table 40. Mask Receive Timer Register(1)(2)

Bit	Name	Default	Function	Comments
7	mrt7	0	Defined in steps of 64/fc (4.72 µs). Range from 256/fc (~18.88 µs) to 16320/fc (~1.2 ms) Timeout = mrt<7:0> * 64/fc Timeout (0 ≤ mrt<7:0> ≤ 4) = 4 * 64/fc (18.88 µs) In NFCIP-1 bit rate detection mode one step is 512/fc (37.78 µs)	Defines time after end of Tx during which receiver output is masked (ignored). For the case of ISO14443A 106 kbit/s the Mask Receive timer is defined according to PCD to PICC frame delay time definition, where bits mrt<7:0> define the number of n/2 steps. Minimum mask receive time of 18.88 µs covers the transients in receiver after end of transmission.
6	mrt6	0		
5	mrt5	0		
4	mrt4	0		
3	mrt3	1		
2	mrt2	0		
1	mrt1	0		
0	mrt0	0		

1. Default setting takes place at power-up and after Set Default command.
2. In NFCIP-1 bit rate detection mode, the clock of the Mask Receive timer is additionally divided by eight (one count is 512/fc) to cover range up to ~9.6 ms.

1.3.16 No-Response Timer Register 1

Address: 0Fh

Type: RW

Table 41. No-Response Timer Register 1(1)

Bit	Name	Default	Function	Comments
7	nrt15	0	No-Response timer definition MSB bits Defined in steps of 64/fc (4.72 µs). Range from 0 to 309 ms If bit nrt_step in *General Purpose and No-Response Timer Control Register* is set the step is changed to 4096/fc	Defines timeout after end of Tx. In case this timeout expires without detecting a response a No-Response interrupt is sent. In NFC mode the No-Response timer is started only when external field is detected. In the NFCIP-1 active communication mode the No-Response timer is automatically started when the transmitter is turned off after the message has been sent All 0: No-Response timer is not started. No-Response timer is reset and restarted with Start No-Response Timer direct command.
6	nrt14	0		
5	nrt13	0		
4	nrt12	0		
3	nrt11	0		
2	nrt10	0		
1	nrt9	0		
0	nrt8	0		

1. Default setting takes place at power-up and after Set Default command.

1.3.17 No-Response Timer Register 2

Address: 10h

Type: RW

Table 42. No-Response Timer Register 2(1)

Bit	Name	Default	Function	Comments
7	nrt7	0	No-Response timer definition LSB bits	-
6	nrt6	0		
5	nrt5	0		
4	nrt4	0		
3	nrt3	0		
2	nrt2	0		
1	nrt1	0		
0	nrt0	0		

1. Default setting takes place at power-up and after Set Default command.

1.3.18 General Purpose and No-Response Timer Control Register

Address: 11h

Type: RW

Table 43. General Purpose and No-Response Timer Control Register(1)

Bit	Name	Default	Function	Comments
7	gptc2	0	Defines the timer trigger source. Refer to *Table 44*.	-
6	gptc1	0		-
5	gptc0	0		-
4	-	0	-	-
3	-	0	-	-
2	-	0	-	-
1	nrt_emv	0	1: EMV mode of No-Response timer	-
0	nrt_step	0	0: 64/fc 1: 4096/fc	Selects the No-Response timer step.

1. Default setting takes place at power-up and after Set Default command.

Table 44. Timer Trigger Source

gptc2	gptc1	gptc0	Trigger source
0	0	0	No trigger source, start only with direct command Start General Purpose Timer.
0	0	1	End of Rx (after EOF)
0	1	0	Start of Rx
0	1	1	End of Tx in NFC mode, when General Purpose Timer expires the field is switched off
1	0	0	Not used
1	0	1	
1	1	0	
1	1	1	

1.3.19 General Purpose Timer Register 1

Address: 12h

Type: RW

Table 45. General Purpose Timer Register 1(1)

Bit	Name	Default	Function	Comments
7	gpt15	-	General purpose timeout definition MSB bits Defined in steps of 8/fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt14	-		
5	gpt13	-		
4	gpt12	-		
3	gpt11	-		
2	gpt10	-		
1	gpt9	-		
0	gpt8	-		

1. Default setting takes place at power-up and after Set Default command.

1.3.20 General Purpose Timer Register 2

Address: 13h

Type: RW

Table 46. General Purpose Timer Register 2(1)

Bit	Name	Default	Function	Comments
7	gpt7	-	General purpose timeout definition LSB bits Defined in steps of 8/fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt6	-		
5	gpt5	-		
4	gpt4	-		
3	gpt3	-		
2	gpt2	-		
1	gpt1	-		
0	gpt0	-		

1. Default setting takes place at power-up and after Set Default command.

1.3.21 Mask Main Interrupt Register

Address: 14h

Type: RW

Table 47. Mask Main Interrupt Register(1)

Bit	Name	Default	Function	Comments
7	M_osc	0	1: Mask IRQ when oscillator frequency is stable	-
6	M_wl	0	1: Mask IRQ due to FIFO water level	-
5	M_rxs	0	1: Mask IRQ due to start of receive	-
4	M_rxe	0	1: Mask IRQ due to end of receive	-
3	M_txe	0	1: Mask IRQ due to end of transmission	-
2	M_col	0	1: Mask IRQ due to bit collision	-
1	-	0	Not used	-
0	-	0		-

1. Default setting takes place at power-up and after Set Default command.

1.3.22 Mask Timer and NFC Interrupt Register

Address: 15h

Type: RW

Table 48. Mask Timer and NFC Interrupt Register(1)

Bit	Name	Default	Function	Comments
7	M_dct	0	1: Mask IRQ due to termination of direct command	-
6	M_nre	0	1: Mask IRQ due to No-Response Timer expire	-
5	M_gpe	0	1: Mask IRQ due to general purpose timer expire	-
4	M_eon	0	1: Mask IRQ due to detection of external field higher than Target activation level	-
3	M_eof	0	1: Mask IRQ due to detection of external field drop below Target activation level	-
2	M_cac	0	1: Mask IRQ due to detection of collision during RF Collision Avoidance	-
1	M_cat	0	1: Mask IRQ after minimum guard time expire	-
0	M_nfct	0	1: Mask IRQ when in target mode the initiator bit rate was recognized	-

1. Default setting takes place at power-up and after Set Default command.

1.3.23 Mask Error and Wake-Up Interrupt Register

Address: 16h

Type: RW

Table 49. Mask Error and Wake-Up Interrupt Register(1)

Bit	Name	Default	Function	Comments
7	M_crc	0	1: Mask IRQ due to CRC error	-
6	M_par	0	1: Mask IRQ due to parity error	-
5	M_err2	0	1: Mask IRQ due to soft framing error	-
4	M_err1	0	1: Mask IRQ due to hard framing error	-
3	M_wt	0	1: Mask IRQ due to wake-up timer interrupt	-
2	M_wam	0	1: Mask Wake-up IRQ due to amplitude measurement	-
1	M_wph	0	1: Mask Wake-up IRQ due to phase measurement.	-
0	M_wcap	0	1: Mask Wake-up IRQ due to capacitance measurement	-

1. Default setting takes place at power-up and after Set Default command.

1.3.24 Main Interrupt Register

Address: 17h

Type: R

Table 50. Main Interrupt Register(1)(2)

Bit	Name	Default	Function	Comments
7	I_osc	-	IRQ when oscillator frequency is stable	Set after oscillator is started by setting *Operation Control Register* bit en.
6	I_wl	-	IRQ due to FIFO water level	Set during receive, informing that FIFO is almost full and has to be read out. Set during transmit, informing that FIFO is almost empty and that additional data has to be sent.
5	I_rxs	-	IRQ due to start of receive	-
4	I_rxe	-	IRQ due to end of receive	-
3	I_txe	-	IRQ due to end of transmission	-
2	I_col	-	IRQ due to bit collision	-
1	I_tim	-	IRQ due to timer or NFC event	Details in *Timer and NFC Interrupt Register*
0	I_err	-	IRQ due to error and wake-up timer	Details in *Error and Wake-Up Interrupt Register*

1. At power-up and after Set Default command content of this register is set to 0.
2. After Main Interrupt Register has been read, its content is set to 0, except for bits 1 and 0, which are set to 0 after corresponding interrupt register is read.

1.3.25 Timer and NFC Interrupt Register

Address: 18h

Type: R

Table 51. Timer and NFC Interrupt Register(1)(2)

Bit	Name	Default	Function	Comments
7	I_dct	-	IRQ due to termination of direct command	-
6	I_nre	-	IRQ due to No-Response Timer expire	-
5	I_gpe	-	IRQ due to general purpose timer expire	-
4	I_eon	-	IRQ due to detection of external field higher than Target activation level	-
3	I_eof	-	IRQ due to detection of external field drop below Target activation level	-
2	I_cac	-	IRQ due to detection of collision during RF Collision Avoidance	An external field was detected during RF Collision Avoidance
1	I_cat	-	IRQ after minimum guard time expire	An external field was not detected during RF Collision Avoidance, field was switched on, IRQ is sent after minimum guard time according to NFCIP-1
0	I_nfct	-	IRQ when in target mode the initiator bit rate was recognized	-

1. At power-up and after Set Default command content of this register is set to 0.
2. After Main Interrupt Register has been read, its content is set to 0.

1.3.26 Error and Wake-Up Interrupt Register

Address: 19h

Type: R

Table 52. Error and Wake-Up Interrupt Register(1)(2)

Bit	Name	Default	Function	Comments
7	I_crc	-	CRC error	-
6	I_par	-	Parity error	-
5	I_err2	-	Soft framing error	Framing error which does not result in corrupted Rx data
4	I_err1	-	Hard framing error	Framing error which results in corrupted Rx data
3	I_wt	-	Wake-up timer interrupt	Timeout after execution of Start Wake-Up Timer command In case option with IRQ at every timeout is selected
2	I_wam	-	Wake-up interrupt due to amplitude measurement	Result of amplitude measurement was Δam larger than reference
1	I_wph	-	Wake-up interrupt due to phase measurement.	Result of phase measurement was Δpm larger than reference
0	I_wcap	-	Wake-up interrupt due to capacitance measurement	Result of capacitance measurement was Δcm larger than reference

1. At power-up and after Set Default command content of this register is set to 0.
2. After Main Interrupt Register has been read, its content is set to 0.

1.3.27 FIFO Status Register 1

Address: 1Ah

Type: R

Table 53. FIFO Status Register 1(1)

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	fifo_b6	-	Number of bytes (binary coded) in the FIFO which were not read out	Valid range is from 0 (000 0000b) to 96 (110 0000b)
5	fifo_b5	-		
4	fifo_b4	-		
3	fifo_b3	-		
2	fifo_b2	-		
1	fifo_b1	-		
0	fifo_b0	-		

1. At power-up and after Set Default command content of this register is set to 0.

1.3.28 FIFO Status Register 2

Address: 1Bh

Type: R

Table 54. FIFO Status Register 2(1)(2)(3)

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	fifo_unf	-	1: FIFO underflow	Set when more bytes then actual content of FIFO were read
5	fifo_ovr	-	1: FIFO overflow	-
4	fifo_ncp	-	1: Last FIFO byte is not complete	fifo_lb<2:0> and np_lb indicate the number of valid bits received in the incomplete byte
3	fifo_lb2	-	Number of bits in the last FIFO byte if it was not complete (fifo_ncp=1)	The received bits are stored in the LSB part of the last byte in the FIFO
2	fifo_lb1	-		
1	fifo_lb0	-		
0	np_lb	-	1: Parity bit is missing in last byte	This is a framing error

1. At power-up and after Set Default command content of this register is set to 0.
2. If FIFO is empty, the value of *FIFO Status Register 1* (0x1Ah) is 0x00, register bits fifo_ncp, fifo_lb2, fifo_lb1 and fifo_lb0 in register block 0x1Bh are cleared.
3. Correct procedure for FIFO read is to read both *FIFO Status Register 1* and *FIFO Status Register 2*, and then read FIFO. Second register values need to be saved in MCU because bits fifo_ncp, fifo_lb<2:0>, and np_lb are cleared automatically at readout.

1.3.29 Collision Display Register

Address: 1Ch

Type: R

Table 55. Collision Display Register(1)

Bit	Name	Default	Function	Comments
7	c_byte3	-	Number of full bytes before the bit collision happened.	The *Collision Display Register* range covers ISO14443A anticollision command. In case collision (or framing error that is interpreted as collision) happens in a longer message, the *Collision Display Register* is not set.
6	c_byte2	-		
5	c_byte1	-		
4	c_byte0	-		
3	c_bit2	-	Number of bits before the collision in the byte where the collision happened	
2	c_bit1	-		
1	c_bit0	-		
0	c_pb	-	1: Collision in parity bit	This is an error, reported in case it is the first collision detected

1. At power-up and after Set Default command content of this register is set to 0.

1.3.30 Number of Transmitted Bytes Register 1

Address: 1Dh

Type: RW

Table 56. Number of Transmitted Bytes Register 1(1)

Bit	Name	Default	Function	Comments
7	ntx12	0	Number of full bytes to be transmitted in one command, MSB bits	Maximum supported number of bytes is 8191
6	ntx11	0		
5	ntx10	0		
4	ntx9	0		
3	ntx8	0		
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

1. Default setting takes place at power-up and after Set Default command.

1.3.31 Number of Transmitted Bytes Register 2

Address: 1Eh

Type: RW

Table 57. Number of Transmitted Bytes Register 2(1)(2)

Bit	Name	Default	Function	Comments
7	ntx4	0	Number of full bytes to be transmitted in one command, MSB bits	Maximum supported number of bytes is 8191
6	ntx3	0		
5	ntx2	0		
4	ntx1	0		
3	ntx0	0		
2	nbtx2	0	Number of bits in the split byte 000 means that there is no split byte (all bytes all complete)	Applicable for ISO14443A: Bit oriented anticollision frame in case last byte is split byte Tx is done without parity bit generation
1	nbtx1	0		
0	nbtx0	0		

1. Default setting takes place at power-up and after Set Default command.
2. If anctl bit is set while card is in idle state and nbtx is not 000, then i_par will be triggered during WUPA direct command is issued.

1.3.32 NFCIP Bit Rate Detection Display Register

Address: 1Fh

Type: R

Table 58. NFCIP Bit Rate Detection Display Register(1)

Bit	Name	Default	Function	Comments
7	nfc_rate3	-	Refer to *Table 26*	This register stores result of automatic bit rate detection in the NFCIP-1 active communication bit rate detection mode
6	nfc_rate2	-		
5	nfc_rate1	-		
4	nfc_rate0	-		
3	-	-	Not used	-
2	-	-		
1	-	-		
0	-	-		

1. At power-up and after Set Default command content of this register is set to 0.

1.3.33 A/D Converter Output Register

Address: 20h

Type: R

Table 59. A/D Converter Output Register(1)

Bit	Name	Default	Function	Comments
7	ad7	-	Displays result of last A/D conversion.	-
6	ad6	-		
5	ad5	-		
4	ad4	-		
3	ad3	-		
2	ad2	-		
1	ad1	-		
0	ad0	-		

1. At power-up and after Set Default command, see *Table 9*, content of this register is set to 0.

1.3.34 Antenna Calibration Control Register

Address: 21h

Type: RW

Table 60. Antenna Calibration Control Register(1)

Bit	Name	Default	Function	Comments
7	trim_s	0	0: LC trim switches are defined by result of Calibrate Antenna command, see *Table 9* 1: LC trim switches are defined by bits tre_x written in this register	Defines source of driving switches on TRIMx pins
6	tre_3	0	MSB	LC trim switches are defined by data written in this register in case trim_s=1. A bit set to 1 switch on transistor on TRIM1_x and TRIM2_x pin.
5	tre_2	0	-	
4	tre_1	0	-	
3	tre_0	0	LSB	
2	-	0	-	-
1	-	0		
0	-	0		

1. Default setting takes place at power-up and after Set Default command.

1.3.35 Antenna Calibration Target Register

Address: 22h

Type: RW

Table 61. Antenna Calibration Target Register(1)

Bit	Name	Default	Function	Comments
7	act7	1	Define target phase for Calibrate Antenna direct command, see *Table 9*	-
6	act6	0		-
5	act5	0		-
4	act4	0		-
3	act3	0		-
2	act2	0		-
1	act1	0		-
0	act0	0		-

1. Default setting takes place at power-up and after Set Default command.

1.3.36 Antenna Calibration Display Register

Address: 23h

Type: R

Table 62. Antenna Calibration Display Register(1)

Bit	Name	Default	Function	Comments
7	tri_3	-	MSB	This register stores result of Calibrate Antenna command. LC trim switches are defined by data written in this register in case trim_s = 0. A bit set to 1 indicates that corresponding transistor on TRIM1_x and TRIM2_x pin is switched on.
6	tri_2	-	-	
5	tri_1	-	-	
4	tri_0	-	LSB	
3	tri_err	-	1: Antenna calibration error	Set when Calibrate Antenna sequence has not been able to adjust resonance
2	-	-	Not used	-
1	-	-		
0	-	-		

1. At power-up and after Set Default command content of this register is set to 0.

1.3.37 AM Modulation Depth Control Register

Address: 24h

Type: RW

Table 63. AM Modulation Depth Control Register(1)

Bit	Name	Default	Function	Comments
7	am_s	0	0: AM modulated level is defined by bits mod5 to mod0. Level is adjusted automatically by Calibrate Modulation Depth command, see *Table 9* 1: AM modulated level is defined by bits dram7 to dram0.	-
6	mod5	0	MSB	See *Section 1.2.19: AM modulation depth: definition and calibration* for details about AM modulation level definition.
5	mod4	0	-	
4	mod3	0	-	
3	mod2	0	-	
2	mod1	0	-	
1	mod0	0	LSB	
0	-	0	-	-

1. Default setting takes place at power-up and after Set Default command.

1.3.38 AM Modulation Depth Display Register

Address: 25h

Type: R

Table 64. AM Modulation Depth Display Register(1)

Bit	Name	Default	Function	Comments
7	md_7	-	MSB	Displays result of Calibrate Modulation Depth command. Antenna drivers are composed of 8 binary weighted segments. Bit md_x set to one indicates that this particular segment will be disabled during AM modulated state. In case of error all 1 value is set.
6	md_6	-	-	
5	md_5	-	-	
4	md_4	-	-	
3	md_3	-	-	
2	md_2	-	-	
1	md_1	-	-	
0	md_0	-	LSB	

1. At power-up and after Set Default command content of this register is set to 0.

1.3.39 RFO AM Modulated Level Definition Register

Address: 26h

Type: RW

Table 65. RFO AM Modulated Level Definition Register(1)

Bit	Name	Default	Function	Comments
7	dram7	0	2 Ohm	Antenna drivers are composed of eight binary weighted segments. Setting a bit dram to 1 will disable corresponding segment during AM modulated state in case am_s bit is set to 1.
6	dram6	0	4 Ohm	
5	dram5	0	8 Ohm	
4	dram4	0	16 Ohm	
3	dram3	0	32 Ohm	
2	dram2	0	64 Ohm	
1	dram1	0	128 Ohm	
0	dram0	0	256 Ohm	

1. Default setting takes place at power-up and after Set Default command.

1.3.40 RFO Normal Level Definition Register

Address: 27h

Type: RW

Table 66. RFO Normal Level Definition Register(1)

Bit	Name	Default	Function	Comments
7	droff7	0	2 Ohm	Antenna drivers are composed of eight binary weighted segments. Setting a bit droff to 1 will disable corresponding segment during normal non-modulated operation. The TX drivers are made up of 8 segments, binary weighted from 2 to 256 Ohm (nominal). As an example, setting this register to 0xC0 disables the 2 Ohm and 4 Ohm segments.
6	droff6	0	4 Ohm	
5	droff5	0	8 Ohm	
4	droff4	0	16 Ohm	
3	droff3	0	32 Ohm	
2	droff2	0	64 Ohm	
1	droff1	0	128 Ohm	
0	droff0	0	256 Ohm	

1. Default setting takes place at power-up and after Set Default command.

Applying value FFh to the register 27h will put the drivers in tristate.

1.3.41 External Field Detector Threshold Register

Address: 29h

Type: RW

Table 67. External Field Detector Threshold Register(1)

Bit	Name	Default	Function	Comments
7	-	0	Not used	-
6	trg_l2	0	Peer Detection Threshold. Refer to *Table 68*.	-
5	trg_l1	1		
4	trg_l0	1		
3	rfe_t3	0	Collision Avoidance Threshold. Refer to *Table 69*.	-
2	rfe_t2	0		
1	rfe_t1	1		
0	rfe_t0	1		

1. Default setting takes place at power-up and after Set Default command.

Table 68. Peer detection threshold as seen on RFI1 input

trg_l2	trg_l1	trg_l0	Target peer detection threshold voltage (mV_{pp} on RFI1)
0	0	0	75
0	0	1	105
0	1	0	150
0	1	1	205
1	0	0	290
1	0	1	400
1	1	0	560
1	1	1	800

Table 69. Collision Avoidance threshold as seen on RFI1 input

rfe_3	rfe_2	rfe_1	rfe_0	Typical Collision Avoidance threshold voltage (mV_{pp} on RFI1)
0	0	0	0	75
0	0	0	1	105
0	0	1	0	150
0	0	1	1	205
0	1	0	0	290
0	1	0	1	400
0	1	1	0	560

Table 69. Collision Avoidance threshold as seen on RFI1 input (continued)

rfe_3	rfe_2	rfe_1	rfe_0	Typical Collision Avoidance threshold voltage (mV_{pp} on RFI1)
0	1	1	1	800
1	0	0	0	25
1	0	0	1	33
1	0	1	0	47
1	0	1	1	64
1	1	0	0	90
1	1	0	1	125
1	1	1	0	175
1	1	1	1	250

1.3.42 Regulator Voltage Control Register

Address: 2Ah

Type: RW

Table 70. Regulator Voltage Control Register(1)

Bit	Name	Default	Function	Comments
7	reg_s	0	0: Regulated voltages are defined by result of Adjust Regulators command 1: Regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting.
6	rege_3	0	External definition of regulated voltage. Refer to *Table 72* for definition. In 5 V mode V_{SP_D} and V_{SP_A} regulators are set to 3.4 V	-
5	rege _2	0		
4	rege _1	0		
3	rege _0	0		
2	mpsv1	0	00: V_{DD} 01: V_{SP_A} 10: V_{SP_D} 11: V_{SP_RF}	Defines source of direct command Measure Power Supply.
1	mpsv0	0		
0	-	0	-	-

1. Default setting takes place at power-up and after Set Default command.

1.3.43 Regulator and Timer Display Register

Address: 2Bh

Type: R

Table 71. Regulator and Timer Display Register(1)

Bit	Name	Default	Function	Comments
7	reg_3	-	Actual regulated voltage setting. Refer to *Table 72* for definition.	-
6	reg_2	-		
5	reg_1	-		
4	reg_0	-		
3	-	-	-	-
2	gpt_on	-	1: General purpose timer is running	
1	nrt_on	-	1: No-Response timer is running	
0	mrt_on	-	1: Mask receive timer is running	

1. 1. At power-up and after Set Default command regulated voltage is set to maximum 3.4V.

Table 72. Regulated voltages

reg_3	reg_2	reg_1	reg_0	Typical regulated voltage (V)	
rege_3	rege_2	rege_1	rege_0	5 V mode	3.3 V mode
1	1	1	1	5.1	3.4
1	1	1	0	4.98	3.3
1	1	0	1	4.86	3.2
1	1	0	0	4.74	3.1
1	0	1	1	4.62	3.0
1	0	1	0	4.50	2.9
1	0	0	1	4.38	2.8
1	0	0	0	4.26	2.7
0	1	1	1	4.14	2.6
0	1	1	0	4.02	2.5
0	1	0	1	3.90	2.4
Other combinations				Not used	

1.3.44 RSSI Display Register

Address: 2Ch

Type: R

Table 73. RSSI Display Register(1)(2)

Bit	Name	Default	Function	Comments
7	rssi_am_3	-	AM channel RSSI peak value. Refer to *Table 74* for definition.	Stores peak value of AM channel RSSI measurement. Automatically cleared at beginning of transponder message and with Clear RSSI command.
6	rssi_am_2	-		
5	rssi_am_1	-		
4	rssi_am_0	-		
3	rssi_pm_3	-	PM channel RSSI peak value. Refer to *Table 74* for definition.	Stores peak value of PM channel RSSI measurement. Automatically cleared at beginning of transponder message and with Clear RSSI command.
2	rssi_pm_2	-		
1	rssi_pm_1	-		
0	rssi_pm_0	-		

1. At power-up and after Set Default command content of this register is set to 0.
2. Bit 0x30[7] indicates which RSSI value is use in the logic for internal use.

Table 74. RSSI

rssi_3	rssi_2	rssi_1	rssi_0	Typical signal on RFI1 (mV_{rms})
0	0	0	0	≤20
0	0	0	1	>20
0	0	1	0	>27
0	0	1	1	>37
0	1	0	0	>52
0	1	0	1	>72
0	1	1	0	>99
0	1	1	1	>136
1	0	0	0	>190
1	0	0	1	>262
1	0	1	0	>357
1	0	1	1	>500
1	1	0	0	>686
1	1	0	1	>950
1	1	1	0	>1150
1	1	1	1	

1.3.45 Gain Reduction State Register

Address: 2Dh

Type: R

Table 75. Gain Reduction State Register(1)

Bit	Name	Default	Function	Comments
7	gs_am_3	-	MSB	Actual gain reduction of second stage of AM channel (including register gain reduction, squelch and AGC)
6	gs_am_2	-	-	
5	gs_am_1	-	-	
4	gs_am_0	-	LSB	
3	gs_pm_3	-	MSB	Actual gain reduction of second stage of PM channel (including register gain reduction, squelch and AGC)
2	gs_pm_2	-	-	
1	gs_pm_1	-	-	
0	gs_pm_0	-	LSB	

1. At power-up and after Set Default command content of this register is set to 0.

1.3.46 Reserved Register

Address: 2Eh

Type: R

Table 76. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.47 Reserved Register

Address: 2Fh

Type: R

Table 77. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.48 Auxiliary Display Register

Address: 30h

Type: R

Table 78. Auxiliary Display Register(1)

Bit	Name	Default	Function	Comments
7	a_cha	-	0: AM 1: PM	Currently selected channel
6	efd_o	-	1: External field detected	External Field Detector output
5	tx_on	-	1: Transmission is active	-
4	osc_ok	-	1: Xtal oscillation is stable	Indication that Xtal oscillator is active and its output is stable
3	rx_on	-	1: Receive coder is enabled	-
2	rx_act	-	1: Receive coder is receiving a message	-
1	nfc_t	-	1: External Field Detector is active in peer detection mode	-
0	en_ac	-	1: External Field Detector is active in RF Collision Avoidance mode	-

1. At power-up and after Set Default command content of this register is set to 0.

1.3.49 Wake-Up Timer Control Register

Address: 31h

Type: RW

Table 79. Wake-Up Timer Control Register(1)

Bit	Name	Default	Function	Comments
7	wur	0	0: 100 ms 1: 10 ms	Wake-up timer range
6	wut2	0	Refer to *Table 80*	Wake-up timer timeout value
5	wut1	0		
4	wut0	0		
3	wto	0	1: IRQ at every timeout	-
2	wam	0	1: At timeout perform amplitude measurement	IRQ if difference larger than Δam
1	wph	0	1: At timeout perform phase measurement	IRQ if difference larger than Δpm
0	RFU	0	-	-

1. Default setting takes place at power-up and after Set Default command.

Table 80. Typical wake-up time

wut2	wut1	wut0	100 ms range (wur=0)	10 ms range (wur=1)
0	0	0	100 ms	10 ms
0	0	1	200 ms	20 ms
0	1	0	300 ms	30 ms
0	1	1	400 ms	40 ms
1	0	0	500 ms	50 ms
1	0	1	600 ms	60 ms
1	1	0	700 ms	70 ms
1	1	1	800 ms	80 ms

1.3.50 Amplitude Measurement Configuration Register

Address: 32h

Type: RW

Table 81. Amplitude Measurement Configuration Register(1)

Bit	Name	Default	Function	Comments
7	am_d3	0	Definition of Δam (difference to reference that triggers interrupt)	-
6	am_d2	0		
5	am_d1	0		
4	am_d0	0		
3	am_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Include/exclude the measurement that causes IRQ (having difference > Δam to reference) in auto-averaging
2	am_aew1	0	00: 4 01: 8 10: 16 11: 32	Define weight of last measurement result for auto-averaging
1	am_aew2	0		
0	am_ae	0	0: Use *Amplitude Measurement Reference Register* 1: Use amplitude measurement auto-averaging as reference	Select reference value for amplitude measurement Wake-Up mode

1. Default setting takes place at power-up and after Set Default command.

1.3.51 Amplitude Measurement Reference Register

Address: 33h

Type: RW

Table 82. Amplitude Measurement Reference Register(1)

Bit	Name	Default	Function	Comments
7	am_ref7	0	-	-
6	am_ref6	0	-	-
5	am_ref5	0	-	-
4	am_ref4	0	-	-
3	am_ref3	0	-	-
2	am_ref2	0	-	-
1	am_ref1	0	-	-
0	am_ref0	0	-	-

1. Default setting takes place at power-up and after Set Default command.

1.3.52 Amplitude Measurement Auto-Averaging Display Register

Address: 34h

Type: R

Table 83. Amplitude Measurement Auto-Averaging Display Register(1)

Bit	Name	Default	Function	Comments
7	amd_aad7	0	-	-
6	amd_aad6	0	-	-
5	amd_aad5	0	-	-
4	amd_aad4	0	-	-
3	amd_aad3	0	-	-
2	amd_aad2	0	-	-
1	amd_aad1	0	-	-
0	amd_aad0	0	-	-

1. At power-up and after Set Default command content of this register is set to 0.

1.3.53 Amplitude Measurement Display Register

Address: 35h

Type: R

Table 84. Amplitude Measurement Display Register(1)

Bit	Name	Default	Function	Comments
7	am_amd7	0	-	-
6	am_amd6	0	-	-
5	am_amd5	0	-	-
4	am_amd4	0	-	-
3	am_amd3	0	-	-
2	am_amd2	0	-	-
1	am_amd1	0	-	-
0	am_amd0	0	-	-

1. At power-up and after Set Default command content of this register is set to 0.

1.3.54 Phase Measurement Configuration Register

Address: 36h

Type: RW

Table 85. Phase Measurement Configuration Register(1)

Bit	Name	Default	Function	Comments
7	pm_d3	0	Definition of Δpm (difference to reference that triggers interrupt)	-
6	pm_d2	0		
5	pm_d1	0		
4	pm_d0	0		
3	pm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Include/exclude the measurement that causes IRQ (having difference > Δpm to reference) in auto-averaging
2	pm_aew1	0	00: 4 01: 8 10: 16 11: 32	Define weight of last measurement result for auto-averaging
1	pm_aew0	0		
0	pm_ae	0	0: Use *Phase Measurement Reference Register* 1: Use phase measurement auto-averaging as reference	Select reference value for phase measurement Wake-Up mode

1. Default setting takes place at power-up and after Set Default command.

1.3.55 Phase Measurement Reference Register

Address: 37h

Type: RW

Table 86. Phase Measurement Reference Register(1)

Bit	Name	Default	Function	Comments
7	pm_ref7	0	-	-
6	pm_ref6	0	-	-
5	pm_ref5	0	-	-
4	pm_ref4	0	-	-
3	pm_ref3	0	-	-
2	pm_ref2	0	-	-
1	pm_ref1	0	-	-
0	pm_ref0	0	-	-

1. Default setting takes place at power-up and after Set Default command.

1.3.56 Phase Measurement Auto-Averaging Display Register

Address: 38h

Type: R

Table 87. Phase Measurement Auto-Averaging Display Register(1)

Bit	Name	Default	Function	Comments
7	pm_aad7	0	-	-
6	pm_aad6	0	-	-
5	pm_aad5	0	-	-
4	pm_aad4	0	-	-
3	pm_aad3	0	-	-
2	pm_aad2	0	-	-
1	pm_aad1	0	-	-
0	pm_aad0	0	-	-

1. At power-up and after Set Default command content of this register is set to 0.

1.3.57 Phase Measurement Display Register

Address: 39h

Type: R

Table 88. Phase Measurement Display Register(1)

Bit	Name	Default	Function	Comments
7	pm_amd7	0	0	-
6	pm_amd6	0	0	-
5	pm_amd5	0	0	-
4	pm_amd4	0	0	-
3	pm_amd3	0	0	-
2	pm_amd2	0	0	-
1	pm_amd1	0	0	-
0	pm_amd0	0	0	-

1. At power-up and after Set Default command content of this register is set to 0.

1.3.58 Reserved Register

Address: 3Ah

Type: R

Table 89. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.59 Reserved Register

Address: 3Bh

Type: R

Table 90. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.60 Reserved Register

Address: 3Ch

Type: R

Table 91. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.61 Reserved Register

Address: 3Dh

Type: R

Table 92. Reserved Register

Bit	Name	Default	Function	Comments
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

1.3.62 IC Identity Register

Address: 3Fh

Type: R

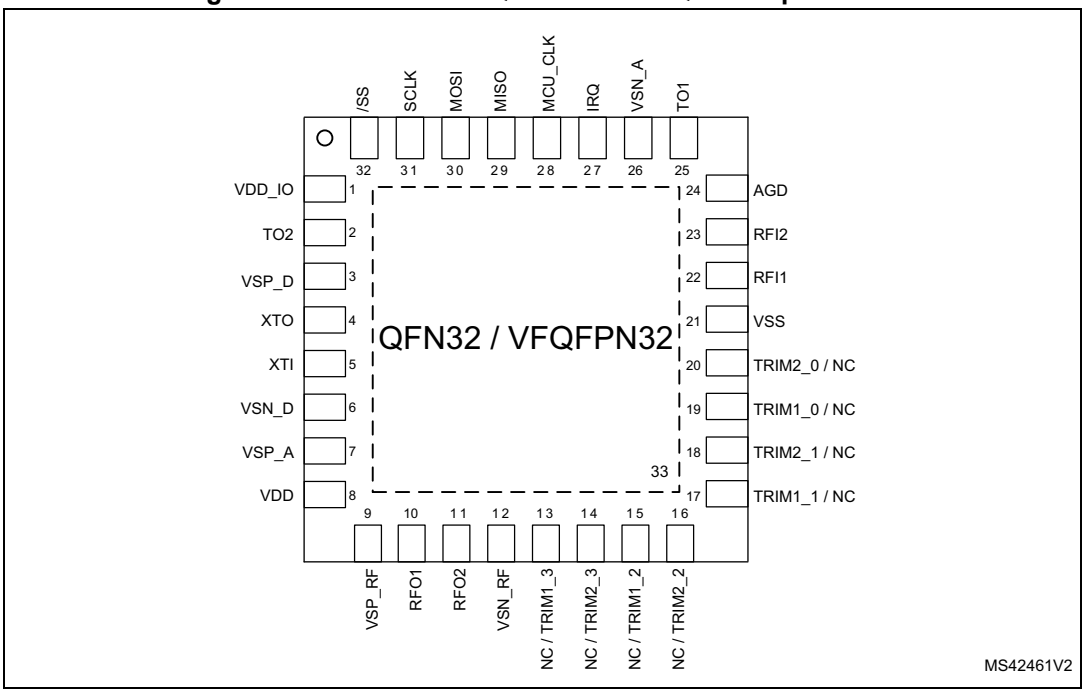
Table 93. IC Identity Register

Bit	Name	Default	Function	Comments
7	ic_type4	-	Code for ST25R3912/3: 00001	5-bit IC type code
6	ic_type3	-		
5	ic_type2	-		
4	ic_type1	-		
3	ic_type0	-		
2	ic_rev2	-	010: silicon r3.1 011: silicon r3.3 100: silicon r4.0 101: silicon r4.1	3-bit IC revision code
1	ic_rev1	-		
0	ic_rev0	-		

2 Pinouts and pin description

The ST25R3912/3 pin and pad assignments are described in *Figure 28* and *Figure 29*.

Figure 28. ST25R3912/3 QFN32 and VFQFPN32 pinouts(1)



1. The above figure shows the package top view.

Figure 29. ST25R3912 WLCSP top view

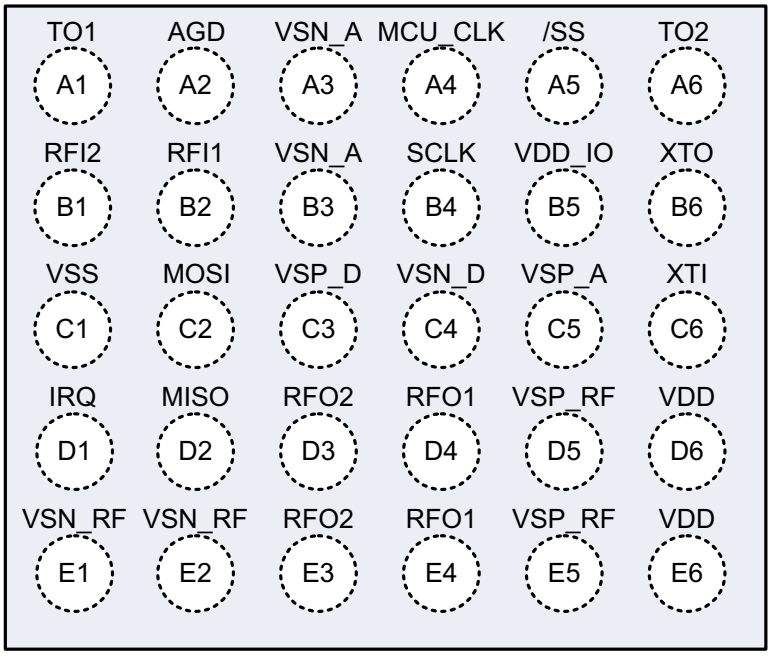


Table 94. ST25R3912/3 pin definitions - QFN32, VFQFPN32 and WLCSP packages

Pin number		Pin name		Pin type	Description
QFN32 VFQFPN32	WLCSP	ST25R3912	ST25R3913		
1	B5	VDD_IO		Supply pad	Positive supply for peripheral communication
2	A6	TO2		Analog output	Test output 2
3	C3	VSP_D			Digital supply regulator output
4	B6	XTO			Xtal oscillator output
5	C6	XTI		Analog input / Digital input	Xtal oscillator input
6	C4	VSN_D		Supply pad	Digital ground
7	C5	VSP_A		Analog output	Analog supply regulator output
8	D6, E6	VDD		Supply pad	External positive supply
9	D5, E5	VSP_RF		Analog output	Supply regulator output for antenna drivers
10	D4, E4	RFO1			Antenna driver output
11	D3, E3	RFO2			
12	E1, E2	VSN_RF		Supply pad	Ground of antenna drivers
13	NA	NC	TRIM1_3	Analog I/O	Input to trim antenna resonant circuit (pads not connected in ST25R3912)
14	NA	NC	TRIM2_3		
15	NA	NC	TRIM1_2		
16	NA	NC	TRIM2_2		
17	NA	NC	TRIM1_1		
18	NA	NC	TRIM2_1		
19	NA	NC	TRIM1_0		
20	NA	NC	TRIM2_0		
21	C1	VSS		Supply pad	Ground, die substrate potential
22	B2	RFI1		Analog input	Receiver input
23	B1	RFI2			
24	A2	AGD		Analog I/O	Analog reference voltage
25	A1	TO1		Analog input	Test output 1
26	A3, B3	VSN_A		Supply pad	Analog ground
27	D1	IRQ		Digital output	Interrupt request output
28	A4	MCU_CLK			Microcontroller clock output
29	D2	MISO		Digital output / tristate	Serial Peripheral Interface data output

Table 94. ST25R3912/3 pin definitions - QFN32, VFQFPN32 and WLCSP packages (continued)

Pin number		Pin name		Pin type	Description
QFN32 VFQFPN32	WLCSP	ST25R3912	ST25R3913		
30	C2	MOSI		Digital input	Serial Peripheral Interface data input
31	B4	SCLK			Serial Peripheral Interface clock
32	A5	/SS			Serial Peripheral Interface enable (active low)
33	NA	VSS		Exposed pad	Ground, die substrate potential, connected to V_{SS} on PCB

3 Electrical characteristics

3.1 Absolute maximum ratings

Stresses beyond those listed in *Table 95*, *Table 96* and *Table 97* may cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in *Section 3.2* is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 95. Electrical parameters

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	DC supply voltage	-0.5	6.0	V	-
V_{DD_IO}	DC_IO supply voltage	-0.5	6.0	V	-
V_{INTRIM}	Input pin voltage TRIM pins	-0.5	25.0	V	-
V_{IN}	Input pin voltage for peripheral communication pins	-0.5	6.5	V	-
V_{INA}	Input pin voltage for analog pins	-0.5	6.0	V	-
I_{scr}	Input current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78
I_{outmax}	Drive capability of output driver	0	250	mA	-

Table 96. Electrostatic discharge

Symbol	Parameter	Min	Max	Unit	Comments
ESD	Electrostatic discharge	±2		kV	Standard JS-001-2014 (Human Body Model)
		±500		V	Standard JS-001-2014 (Human Body Model) Valid for TRIMx_x pins (pins 13 - 20, ST25R3913 only)

Table 97. Temperature ranges and storage conditions

Symbol	Parameter	Min	Max	Unit	Comments
T_{strg}	Storage temperature	-55	125	°C	-
T_{body}	Package body temperature	-	260	°C	The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative Humidity non-condensing	5	85	%	-

Table 97. Temperature ranges and storage conditions (continued)

Symbol	Parameter	Min	Max	Unit	Comments
MSL	Moisture Sensitivity Level	3		-	QFN32 only.
		1		-	WLCSP only.

3.2 Operating conditions

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

All defined tolerances for external components in this specification need to be assured over the whole operating conditions range and over lifetime.

Table 98. Operating conditions

Symbol	Parameter	Min	Max	Unit	Comments
V_{DD}	Positive supply voltage	2.4	5.5	V	In case power supply is lower than 2.6 V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4 V).
V_{DD_IO}	Peripheral communication supply voltage	1.65	5.5	V	
V_{SS}	Negative supply voltage	0	0	V	-
V_{INTRIM}(1)	Input pin voltage TRIM pins	-	20	V	-
T_{JUN}	Junction temperature	-40	125	°C	-
V_{RFI_A}	RFI input amplitude	0.150	3	V_{pp}	Minimum RFI input signal definition is meant for NFC receive mode. In HF reader mode and NFC transmit mode the recommended signal level is 2.5 V_{pp}.
RFO	Driver current	0	250	mA	-

1. ST25R3913 only.

3.3 DC/AC characteristics for digital inputs and outputs

3.3.1 CMOS inputs

Valid for input pins \SS, MOSI, and SCLK.

Table 99. CMOS inputs

Symbol	Parameter	Min	Max	Unit
V_{IH}	High level input voltage	0.7 * V_{DD_IO}	V_{DD_IO}	V
V_{IL}	Low level input voltage	V_{SS}	0.3 * V_{DD_IO}	V
I_{LEAK}	Input leakage current	-1	1	µA

3.3.2 CMOS outputs

Valid for output pins MISO, IRQ and MCU_CLK, io_18=0 (*IO Configuration Register 2*).

Table 100. CMOS outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	$I_{SOURCE/SINK}$ = 1mA, measured at V_{DDIO} = 2.4 V	0.9 * V_{DD_IO}	-	V_{DD_IO}	V
V_{OL}	Low level output voltage	$I_{SOURCE/SINK}$ = 0.5 mA, measured at V_{DDIO} = 1.65 V	0	-	0.1 * V_{DD_IO}	V
C_L	Capacitive load	-	0	-	50	pF
R_O	Output resistance	-	0	250	550	Ω
R_{PD}	Pull-down resistance pin MISO	Pull-down can be enabled while MISO output is in tristate. The activation is controlled by register setting.	5	10	15	kΩ

3.4 Electrical specifications

V_{DD}= 3.3 V, temperature 25 °C unless noted otherwise.

3.3 V supply mode, regulated voltages set to 3.4 V, 27.12 MHz Xtal connected to XTO and XTI.

Table 101. Electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{PD}	Supply current in Power-down mode	-	0.7	2	µA	Register 00h set to 0Fh (no clock on MCU_CLK), register 01h set to 80h (3 V supply mode), register 02hset to 00h register 03h set to 08h, other registers in default state.
I_{NFCT}	Supply current in initial NFC Target mode	-	3.5	7	µA	Register 00h set to 0Fh (no clock on MCU_CLK), register 01h set to 80h (3 V supply mode), register 02hset to 00h register 03h set to 80h (enable NFC Target mode), other registers in default state.
I_{WU}	Supply current in Wake-up mode	-	3.6	8	µA	Register 00h set to 0Fh (no clock on MCU_CLK), register 01h set to 80h (3 V supply mode), register 02h set to 04h (enable Wake-up mode), register 03hset to 08h, register 31h set to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
I_{RD}	Supply current in Ready mode	-	5.4	7.5	mA	Register 00h set to 0Fh (no clock on MCU_CLK), register 01h set to C0h (3 V supply mode, disable VSP_D), register 02h set to 80h, register 03h set to 08h, other registers in default state, short VSP_A and VSP_D.

Table 101. Electrical specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
I_{AL}	Supply current, all active	-	8.7	12.5	mA	Register 00h set to 0Fh, register 01h set to C0h (3 V supply mode, disable VSP_D), register 02h set to E8h (one channel Rx, enable Tx), register 03h set to 08h, register 0Bh set to 00h, register 27h set to FFh (all RFO segments disabled), other registers in default state, short VSP_A and VSP_D.
I_{LP}	Supply current, all active, low power receiver mode	-	6.8	10	mA	Register 00h set to 0Fh, register 01h set to C0h (3 V supply mode, disable VSP_D), register 02h set to E8h (one channel Rx, enable Tx), register 03h set to 08, register 0Bh set to 80 (low power mode), register 27h set to FFh (all RFO segments disabled), other registers in default state, short VSP_A and VSP_D.
R_{RFO}	RFO1 and RFO2 driver output resistance	0.25	0.6	1.8	Ω	I_{RFO} = 10 mA The following measurement procedure, which cancels resistance of measurement setup, is used: – all driver segments are switched on, resistance is measured – all driver segments except the MSB segment are switched on, resistance is measured – difference between the two measurements is the resistance of MSB segment – resistance of MSB segment multiplied by two is the value of R_{RFO}.
Z_{load}	Load impedance across RFO1 and RFO2	8	10	50	Ω	Using a load impedance lower than the minimum value can result in permanent damage to the device.
V_{RFI}	RFI input sensitivity	-	0.5	-	mV_{rms}	f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.
R_{RFI}	RFI input resistance	5	10	15	kΩ	-
V_{POR}	Power on Reset voltage	1.31	1.5	1.75	V	-
V_{AGD}	AGD voltage	1.4	1.5	1.6	V	Register 00h set to 0Fh (no clock on MCU_CLK), register 01h set to C0h (3 V supply mode, disable VSP_D), register 02h set to 80h, register 03h set to 08h, other registers in default state, short VSP_A and VSP_D.
V_{REG}	Regulated voltage	2.80	3.0	3.32	V	Manual regulator mode, regulated voltage set to 3.0 V, measured on pin VSP_RF: register 00h set to 0Fh, register 01h set to 80h (3 V supply mode), register 02h set to E8h (one channel Rx, enable Tx), register $2A_h$ set to $D8_h$.
T_{OSC}	Oscillator start-up time	0.65	0.7	10	ms	13.56 MHz or 27.12 MHz crystal ESR_{MAX}= 150 Ω max, load capacitance according to crystal specification, IRQ is issued once the oscillator frequency is stable. This parameter changes with ESRMAX parameter.

3.5 Typical operating characteristics

3.5.1 Thermal resistance and maximum power dissipation

Figure 30. T_{CASE} vs. power dissipation for different copper areas at T_{amb} = 25 °C

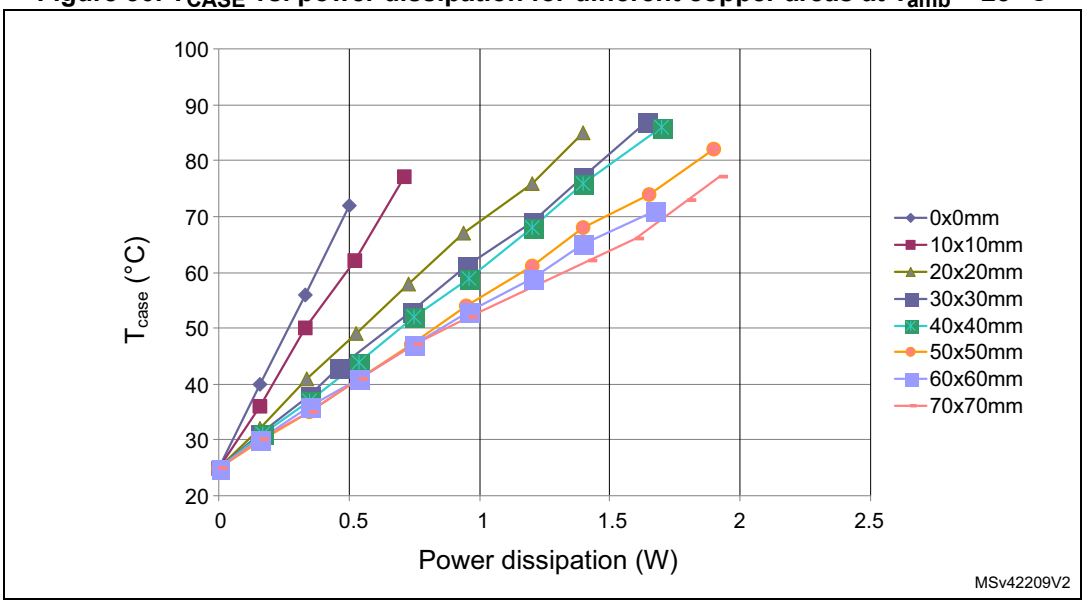
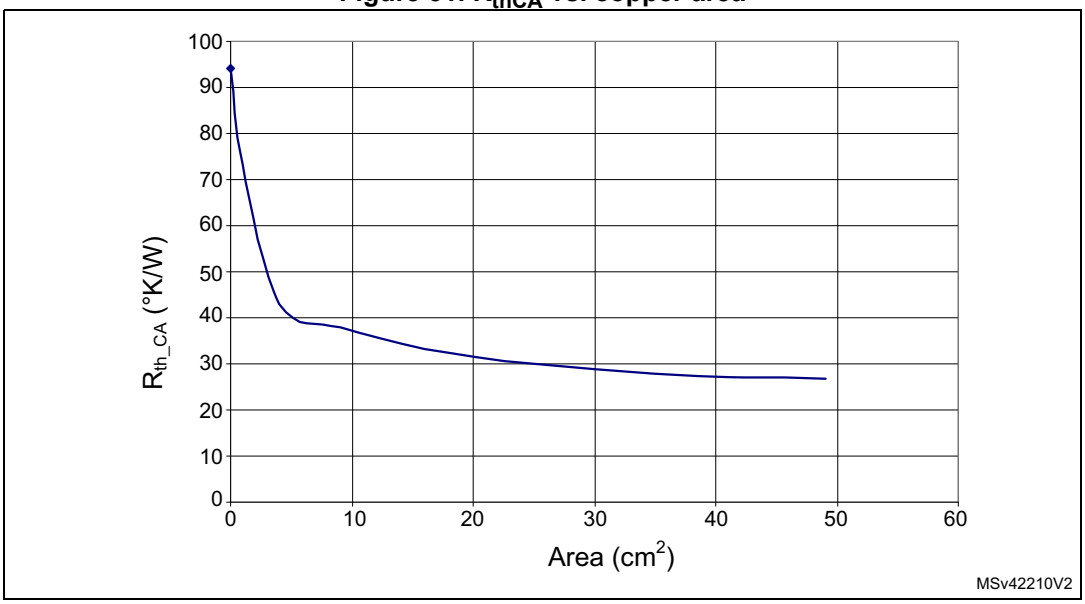


Figure 31. R_{thCA} vs. copper area



4 Package information

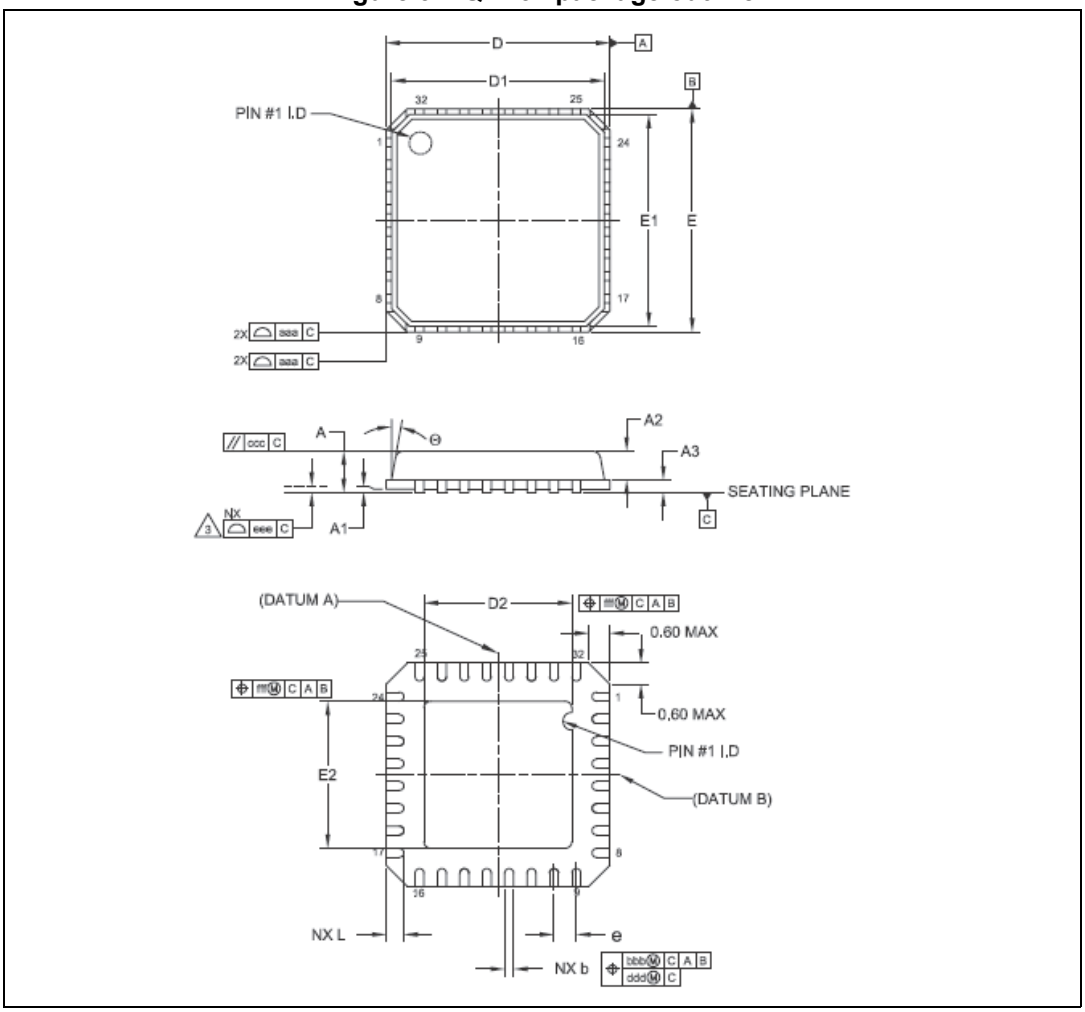
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK® is an ST trademark.

4.1 QFN32 package information

The ST25R3912/3 are available in a 32-pin QFN (5 mm x 5 mm) package (see *Figure 32*). Dimensions are detailed in *Table 102*.

Figure 32. QFN32 package outline



1. Dimensioning and tolerances conform to ASME Y14.5M-1994.
2. Co-planarity applies to the exposed heat slug as well as to the terminal.
3. Radius on terminal is optional.
4. N is the total number of terminals.
5. This drawing is subject to change without notice.

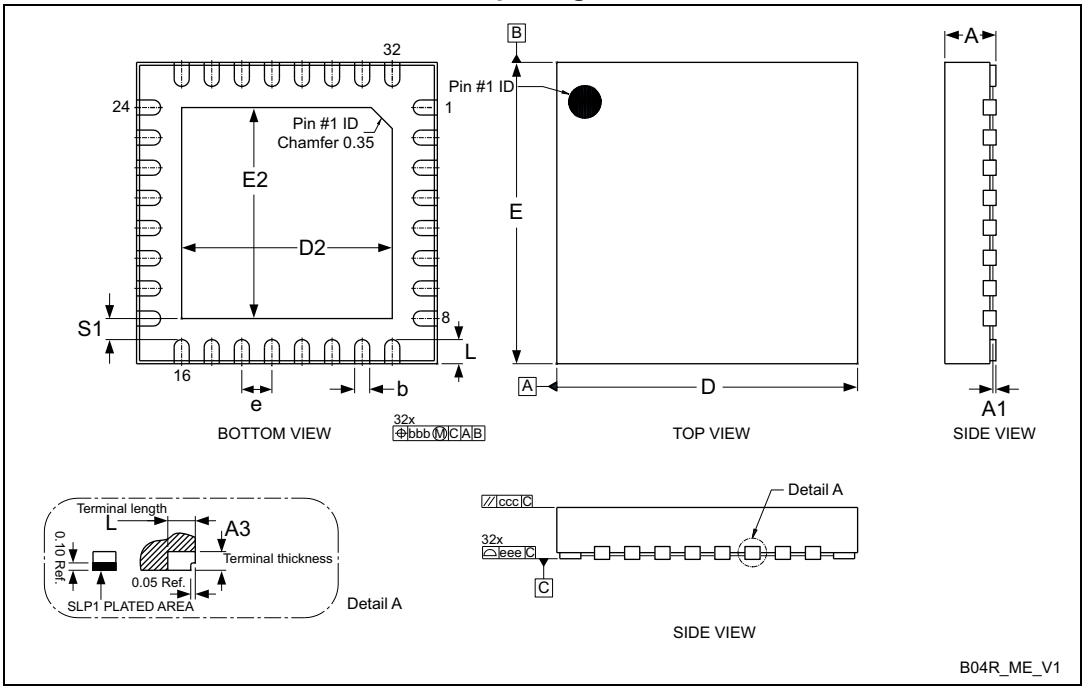
Table 102. QFN32 5 mm x 5 mm dimensions(1)

Symbol (as specified in *Figure 32*)	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20	-
L	0.35	0.40	0.45
q	0º	-	14º
b	0.18	0.25	0.30
D	-	5.00 (with BSC)	-
E	-	5.00 (with BSC)	-
e	-	0.50 (with BSC)	-
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
D1	-	4.75 (with BSC)	-
E1	-	4.75 (with BSC)	-
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N(2)	32		

1. All dimensions are in mm. All angles are in degrees.
2. Total number of terminals.

4.2 VFQFPN32 package information

Figure 33. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead package outline



1. Drawing is not to scale.
2. Coplanarity applies to the exposed pad as well as the terminal.

Table 103. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead mechanical data

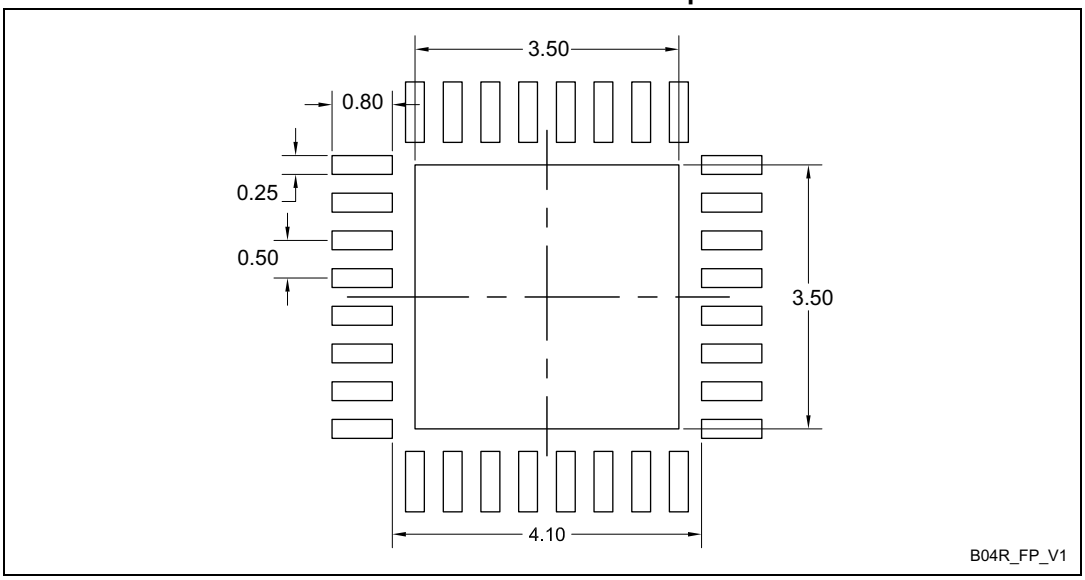
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0	-	0.050	0	-	0.0020
A3		0.200			0.0079	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D		5.000			0.1969	
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E		5.000			0.1969	
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e		0.500			0.0197	
S1		0.350			0.0138	
bbb	-	0.100	-	-	0.0039	-

Table 103. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ccc	-	0.100	-	-	0.0039	-
eee	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. VFQFPN - 32 pins, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead recommended footprint



1. Dimensions are expressed in millimeters.

4.3 WLCSP30 package information

Figure 35. WLCSP30 30-ball, 3.065 x 2.865 mm, 0.5 mm pitch wafer level chip scale package outline

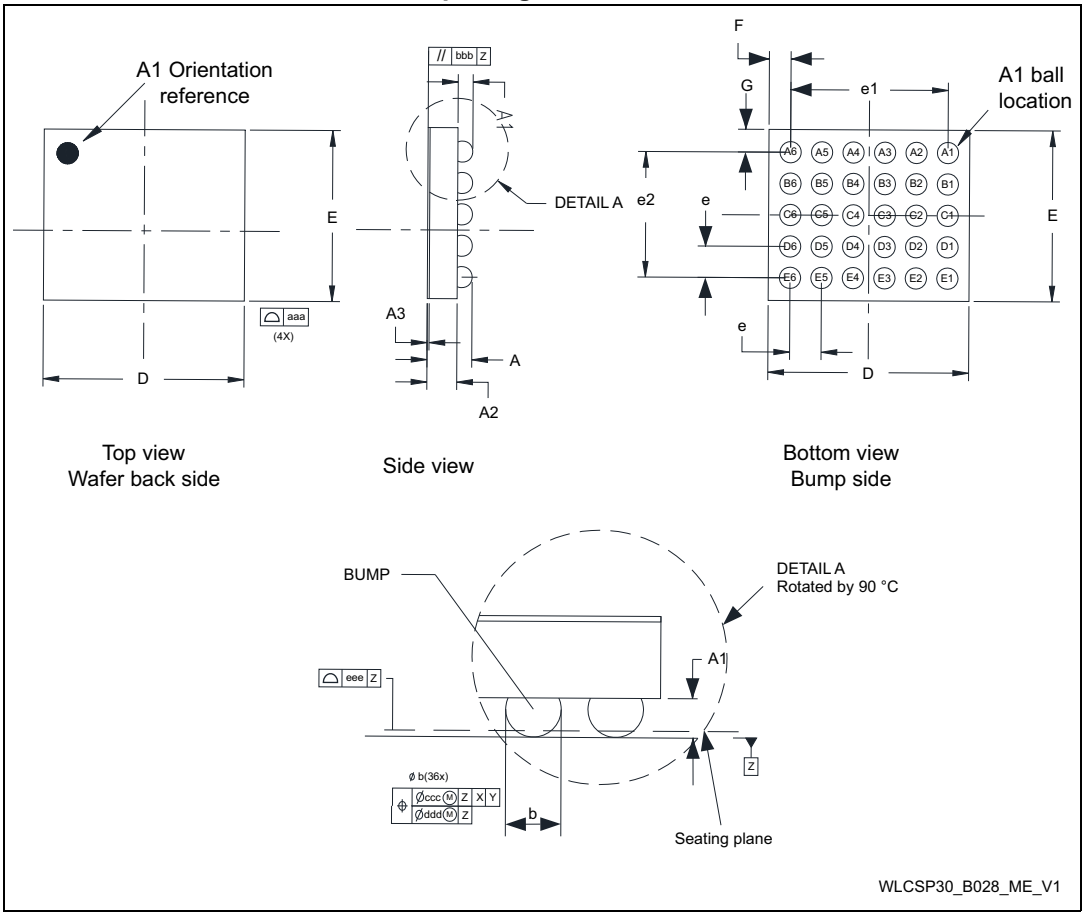


Table 104. WLCSP30 30-ball, 3.065 x 2.865 mm, 0.5 mm pitch wafer level chip scale mechanical data

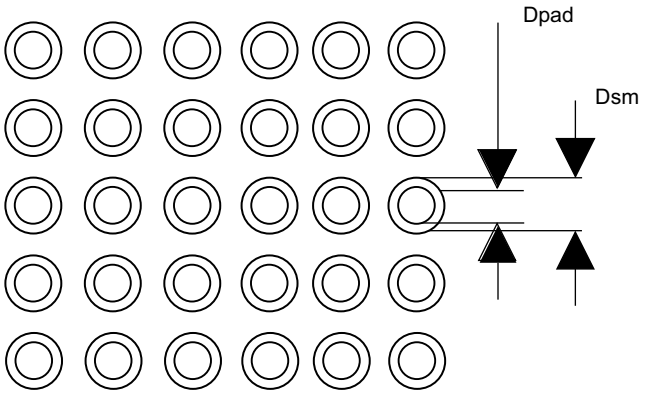
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.620	0.650	0.680	0.0244	0.0256	0.0268
A1	-	0.232	-	-	0.0091	-
A2	-	0.393	-	-	0.0155	-
A3	-	0.025	-	-	0.0010	-
b	-	0.329	-	-	0.0130	-
D	3.015	3.065	3.115	0.1187	0.1207	0.1226
E	2.815	2.865	2.915	0.1108	0.1128	0.1148
e	-	0.5	-	-	0.0197	-

Table 104. WLCSP30 30-ball, 3.065 x 2.865 mm, 0.5 mm pitch wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e1	-	2.5	-	-	0.0984	-
e2	-	2	-	-	0.0787	-
F	-	0.2825	-	-	0.0111	-
G	-	0.4325	-	-	0.0170	-
N	-	30	-	-	1.1811	-
aaa	-	0.10	-	-	0.0039	-
bbb	-	0.10	-	-	0.0039	-
ccc	-	0.10	-	-	0.0039	-
ddd	-	0.05	-	-	0.0020	-
eee	-	0.05	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. WLCSP30 30-ball, 3.065 x 2.865 mm, 0.5 mm pitch wafer level chip scale recommended footprint



1. Dimensions are expressed in millimeters.

Table 105. WLCSP30 30-ball, 3.065 x 2.865 mm, 0.5 mm pitch wafer level chip scale recommended PCB

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.314 mm
Dsm	0.359 mm typ. (depends on the solder-mask registration tolerance)
Stencil opening	0.329 mm
Stencil thickness	0.100 mm

5 Ordering information

Table 106. Ordering information scheme

Example: ST25 R 39 12 - A QF T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = Reader

Frequency range

39 = HF products

Product feature

12 = High performance HF reader / NFC initiator for payment applications with 1W output power

13 = High performance HF reader / NFC initiator for payment applications with 1W output power supporting AAT

Temperature range

A = -40 °C to 125 °C

Package/Packaging

QF = 32-pin QFN (5 mm x 5 mm) (ST25R3913 only)

QW = 32-pin VFQFPN (5 mm x 5 mm) with wettable flanks (ST25R3912 only)

WL = WLCSP (ST25R3912 only)

Tape and Reel

T = 4000 pcs/reel

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6 Revision history

Table 107. Document revision history

Date	Revision	Changes
13-Oct-2016	1	Initial release.
05-Jan-2017	2	Updated document title, *Features* and *Description*. Updated *Section 1: Functional overview*, *Section 1.1.1: Transmitter*, *Section 1.1.2: Receiver*, *Section 1.1.3: Phase and amplitude detector*, *Section 1.1.5: External field detector*, *Section 1.1.6: Quartz crystal oscillator*, *Section 1.1.7: Power supply regulators*, *Section 1.1.8: POR and Bias*, *Section 1.1.9: RC oscillator and Wake-Up timer*, *Section 1.2.2: Transmitter*, *Demodulation stage*, *Filtering and gain stages*, *Digitizing stage*, *Squelch*, *Receiver in NFCIP-1 active communication mode*, *Section 1.2.4: Wake-Up mode*, *Auto-averaging*, *Section 1.2.7: A/D converter*, *Section 1.2.11: Communication with an external microcontroller* and *Section 4.1: QFN32 package information*. Added *Section 1.2.12: Direct commands*. Updated *Table 11: Register preset bits*, *Table 18: Registers map*. *Table 19: IO Configuration Register 1*, *Table 22: Mode Definition Register*, *Table 29: ISO14443B Settings Register 1*, *Table 35: Auxiliary Definition Register*, *Table 37: Receiver Configuration Register 2*, *Table 38: Receiver Configuration Register 3*, *Table 43: General Purpose and No-Response Timer Control Register*, *Table 47: Mask Main Interrupt Register*, *Table 48: Mask Timer and NFC Interrupt Register*, *Table 49: Mask Error and Wake-Up Interrupt Register*, *Table 52: Error and Wake-Up Interrupt Register*, *Table 54: FIFO Status Register 2*, *Table 55: Collision Display Register*, *Table 57: Number of Transmitted Bytes Register 2*, *Table 60: Antenna Calibration Control Register*, *Table 65: RFO AM Modulated Level Definition Register*, *Table 66: RFO Normal Level Definition Register*, *Table 67: External Field Detector Threshold Register*, *Table 70: Regulator Voltage Control Register*, *Table 71: Regulator and Timer Display Register*, *Table 73: RSSI Display Register*, *Table 78: Auxiliary Display Register*, *Table 81: Amplitude Measurement Configuration Register*, *Table 85: Phase Measurement Configuration Register*, *Table 93: IC Identity Register*, *Table 96: Electrostatic discharge*, *Table 101: Electrical specifications* and *Table 106: Ordering information scheme*. Removed footnote from *Table 31: Minimum TR1 codings*. Updated figures *9* to *14* in *Section 1.2.11: Communication with an external microcontroller*, *Figure 24: Connection of tuning capacitors to the antenna LC tank* and *Figure 28: ST25R3912/3 QFN32 and VFQFPN32 pinouts(1)*.
12-May-2017	3	Updated *Figure 34: WLCSP package outline*.

Table 107. Document revision history (continued)

Date	Revision	Changes
27-Jul-2017	4	Updated *Features* and *Description*. Updated *Clear*, *FIFO water level and FIFO status registers* and *Test mode entry and access to test registers*. Updated *Table 6: SPI operation modes*, *Table 17: Setting mod bits*, *Table 54: FIFO Status Register 2* and its footnotes, *Table 74: RSSI*, *Table 93: IC Identity Register*, *Table 97: Temperature ranges and storage conditions* and *Table 101: Electrical specifications*. Updated *Section 4.3: WLCSP30 package information*. Updated title of *Section 5: Ordering information* and *Note:*.
12-Mar-2018	5	Updated *Table 2: Low pass control*, *Table 6: SPI operation modes*, *Table 9: Direct commands* and *Table 27: ISO14443A and NFC 106kb/s Settings Register*. Updated *Example* and *Section 1.3.62: IC Identity Register*.
01-Aug-2018	6	Updated *Features* and image caption on cover page. Updated *Figure 23: Transport frame format according to NFCIP-1*, *Figure 28: ST25R3912/3 QFN32 and VFQFPN32 pinouts(1)*, *Figure 30: TCASE vs. power dissipation for different copper areas at Tamb = 25 °C* and *Figure 31: RthCA vs. copper area*. Replaced former *Figure 24: FeliCa™ frame format* with *Table 14: FeliCa™ frame format*. Updated *Table 94: ST25R3912/3 pin definitions - QFN32, VFQFPN32 and WLCSP packages* and *Table 106: Ordering information scheme*. Added *Section 4.2: VFQFPN32 package information*.