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REVISION HISTORY

5/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			125	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		60	250	μV
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			450	nA
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			600	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 1.0\text{ V to } 4.0\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		5	nA
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $1\text{ V} \leq V_{OUT} \leq 4\text{ V}$	86			V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$R_L = 2\text{ k}\Omega$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	50	240		dB
Bias Current Drift	$\Delta I_B/\Delta T$		25			V/mV
				0.2	2.00	V/mV
				150		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1.0\text{ mA}$	4.80			$\text{pA}/^\circ\text{C}$
Output Voltage Low	V_{OL}	$I_L = 1.0\text{ mA}$			125	V
Output Current	I_{OUT}		± 6.5			mV
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	$V_{OUT} = 2.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1.45	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	1.65	2.4		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.01%, 1.0 V step		2.5		μs
Gain Bandwidth Product	GBP			3.25		MHz
Phase Margin	Φ_M			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		0.3		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		3.9		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.4		$\text{pA}/\sqrt{\text{Hz}}$

$V_S = \pm 15.0 \text{ V}$, $V_{CM} = 0 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80	200	μV
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			450	nA
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			600	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -14.0 \text{ V to } +14.0 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-15	90	50	V
Large Signal Voltage Gain	A_{VO}	$R_L = 2 \text{ k}\Omega$, $-10 \text{ V} \leq V_{OUT} \leq 10 \text{ V}$	86	1000		dB
		$R_L = 2 \text{ k}\Omega$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	75			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2	2.00	$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/ $^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1.0 \text{ mA}$	14.8			V
Output Voltage Low	V_{OL}	$I_L = 1.0 \text{ mA}$			-14.875	V
Output Current	I_{OUT}		± 10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.0 \text{ V to } \pm 18 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	90			dB
Supply Current/Amplifier	I_{SY}	$V_{OUT} = 0 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.0	mA
		$V_S = \pm 18 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2 \text{ k}\Omega$	2.4	4.0		V/ μs
Full Power Bandwidth	BW_p	1% distortion, $R_L = 2 \text{ k}\Omega$, $V_{OUT} = 29 \text{ V p-p}$		35		kHz
Settling Time	t_s	To 0.01%, 10 V step		4		μs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Φ_M			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_n \text{ p-p}$	0.1 Hz to 10 Hz		0.3		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1 \text{ kHz}$		3.9		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.4		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Input Voltage	$\pm 18\text{ V}$
Differential Input Voltage ¹	$\pm 0.6\text{ V}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	300°C

¹ For input voltages greater than 0.6 V, the input current must be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device soldered in the circuit board for the SOIC package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	158	43	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

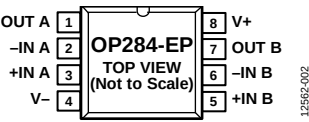


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	-IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	-IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

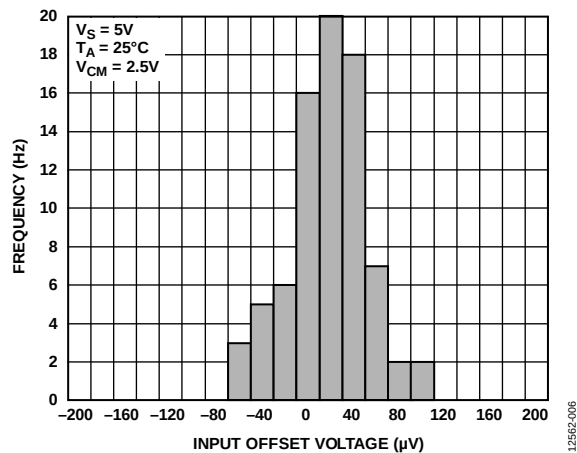
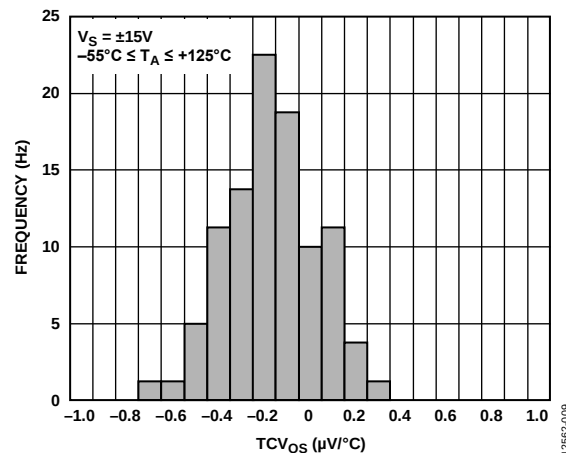
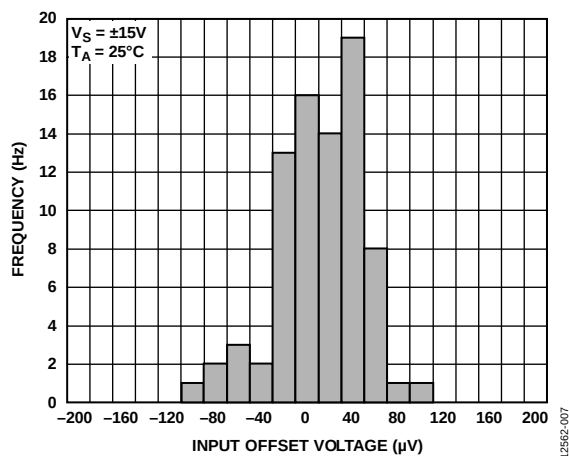
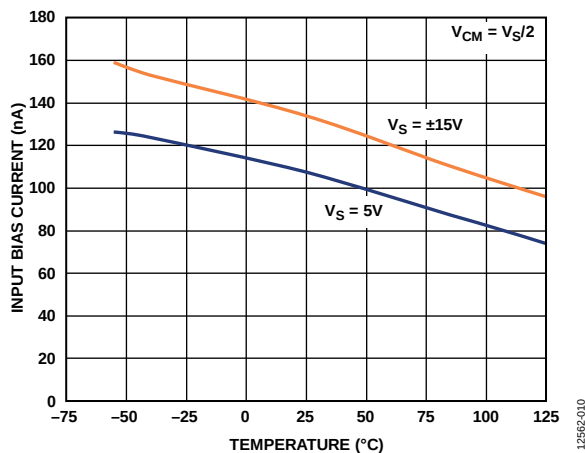
Figure 3. Input Offset Voltage Distribution, $V_S = 5V$ Figure 6. Input Offset Voltage Drift Distribution, $V_S = \pm 15V$ Figure 4. Input Offset Voltage Distribution, $V_S = \pm 15V$ 

Figure 7. Bias Current vs. Temperature

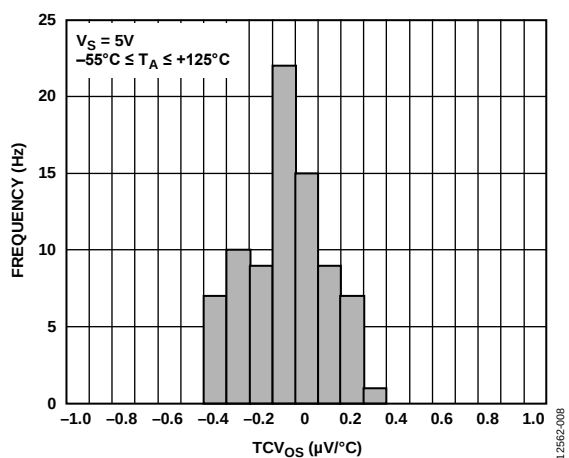
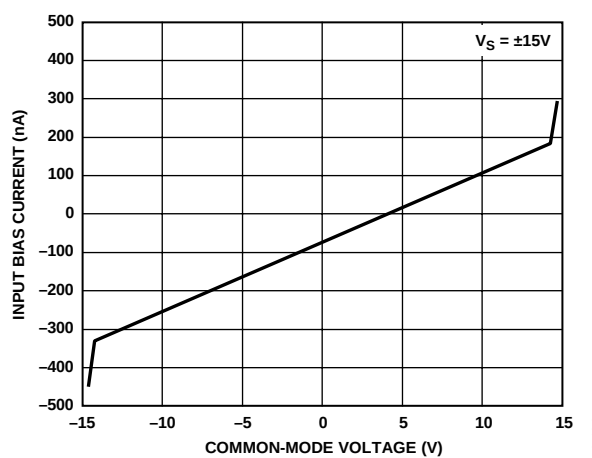
Figure 5. Input Offset Voltage Drift Distribution, $V_S = 5V$ 

Figure 8. Input Bias Current vs. Common-Mode Voltage

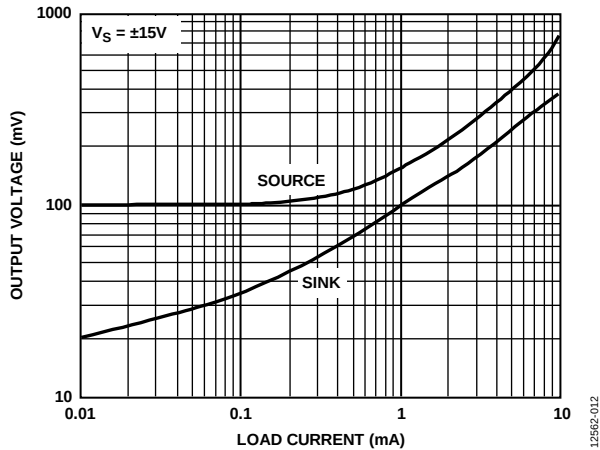


Figure 9. Output Voltage to Supply Rail vs. Load Current

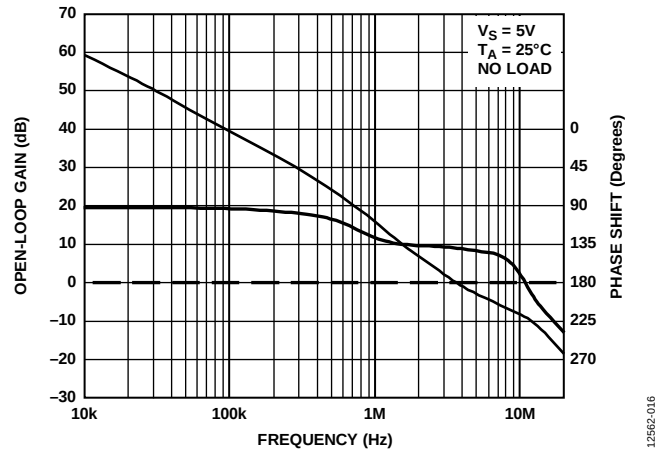


Figure 12. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = 5V$

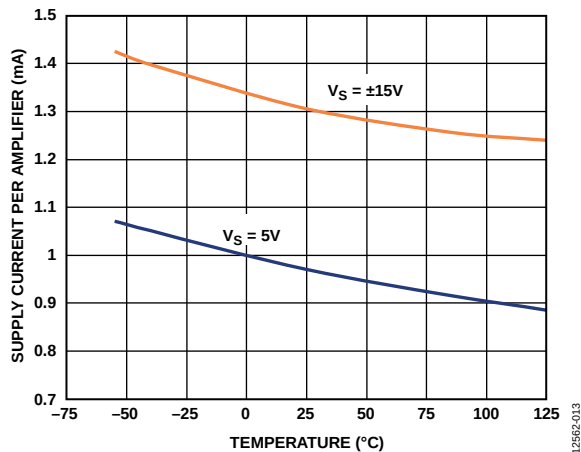


Figure 10. Supply Current vs. Temperature

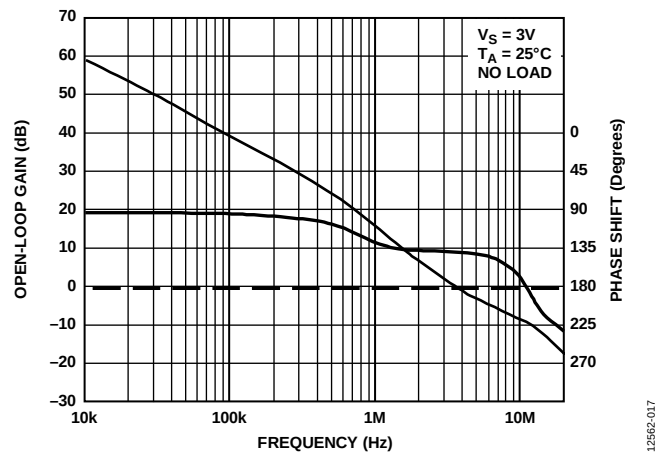


Figure 13. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = 3V$

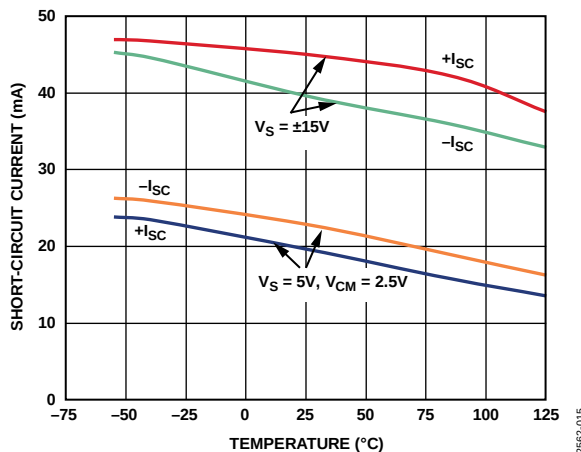


Figure 11. Short-Circuit Current vs. Temperature

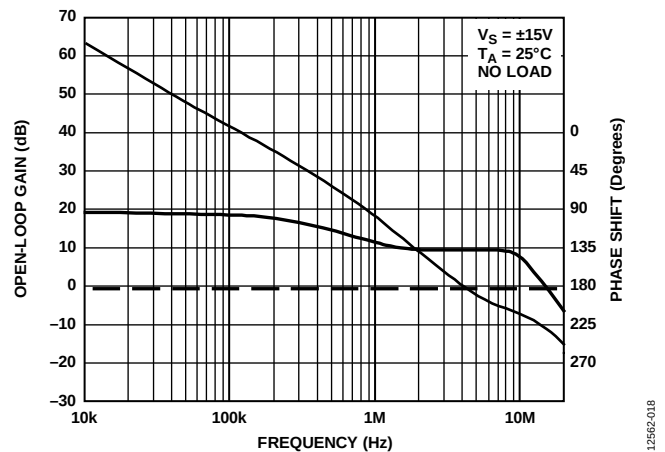


Figure 14. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = \pm 15V$

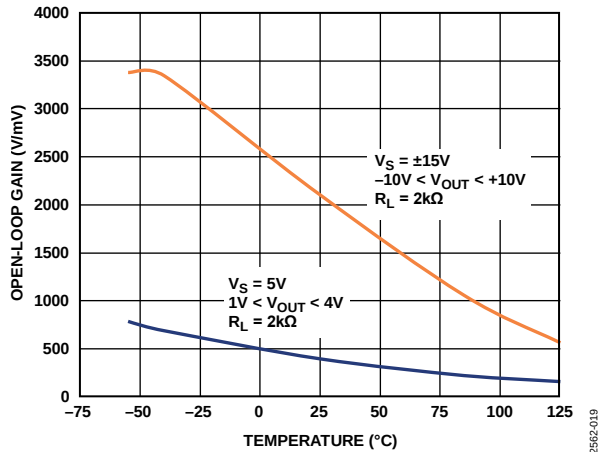


Figure 15. Open-Loop Gain vs. Temperature

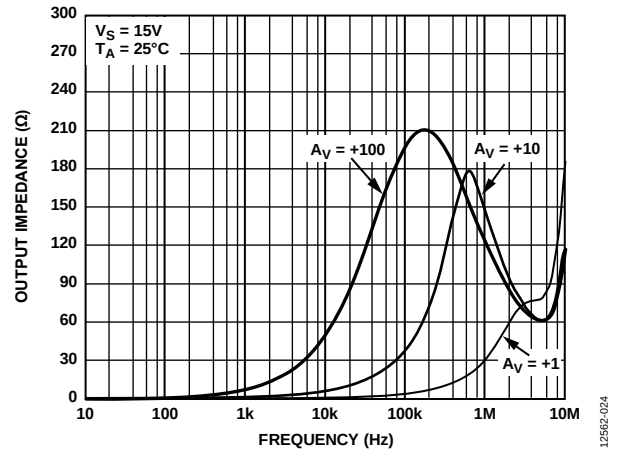


Figure 18. Output Impedance vs. Frequency

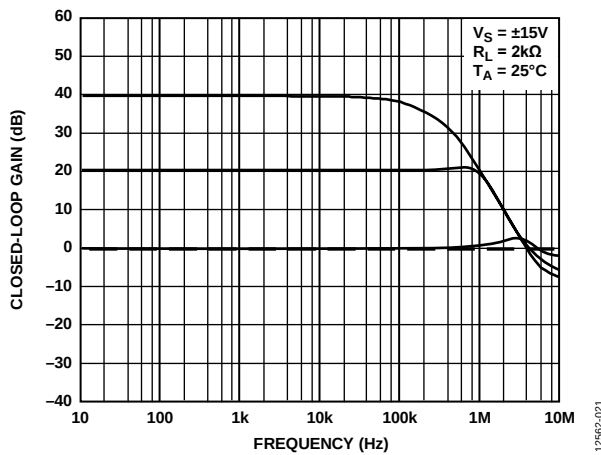


Figure 16. Closed-Loop Gain vs. Frequency (2 kΩ Load)

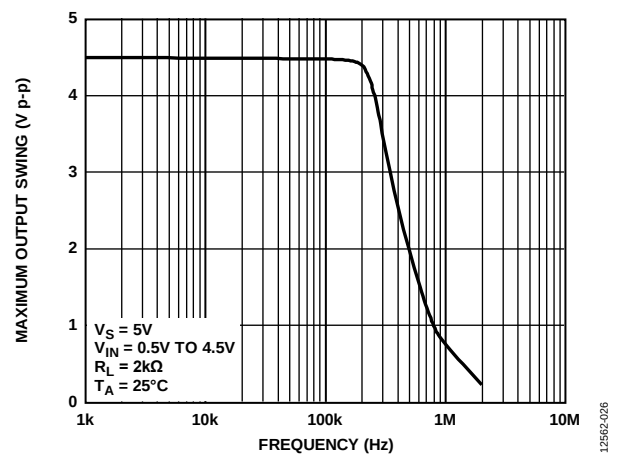


Figure 19. Maximum Output Swing vs. Frequency

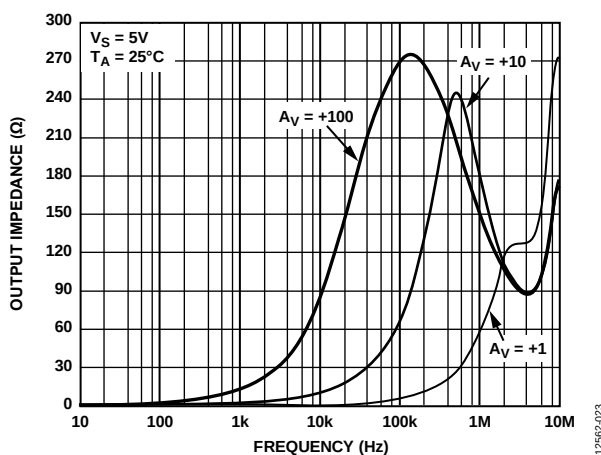


Figure 17. Output Impedance vs. Frequency

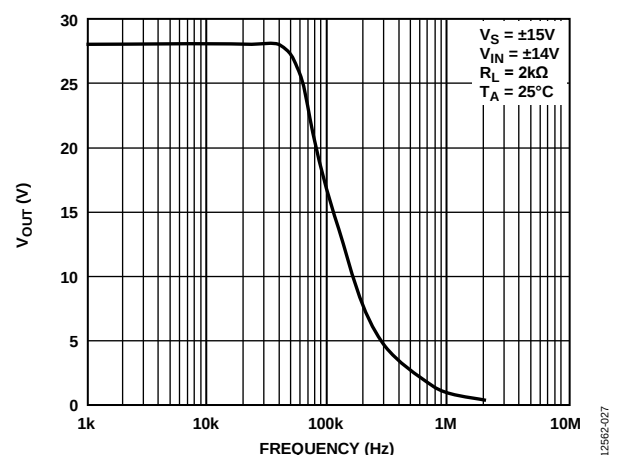


Figure 20. Maximum Output Swing vs. Frequency

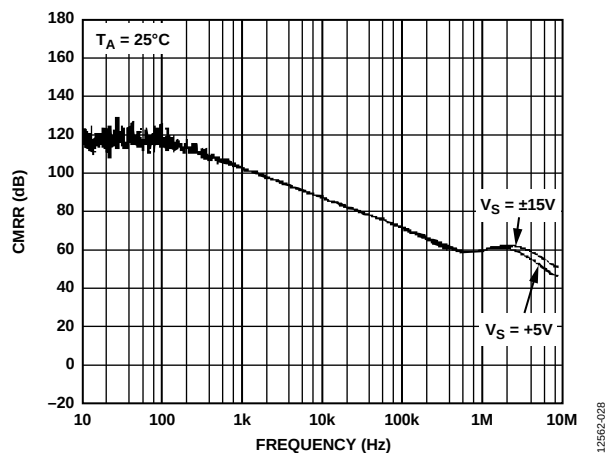


Figure 21. CMRR vs. Frequency

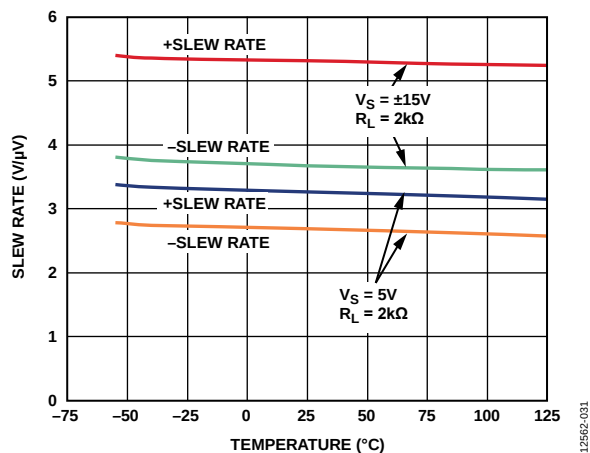


Figure 24. Slew Rate vs. Temperature

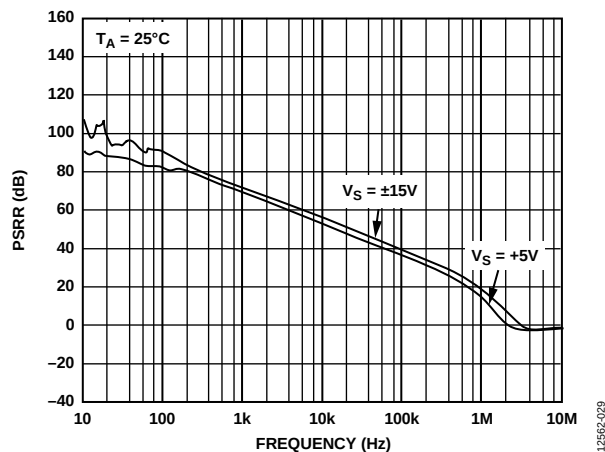


Figure 22. PSRR vs. Frequency

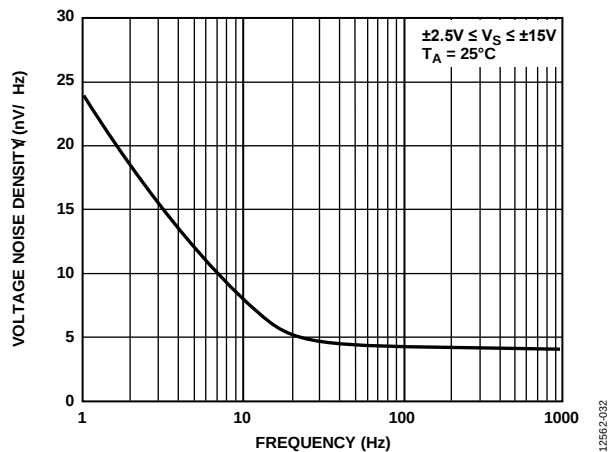


Figure 25. Voltage Noise Density vs. Frequency

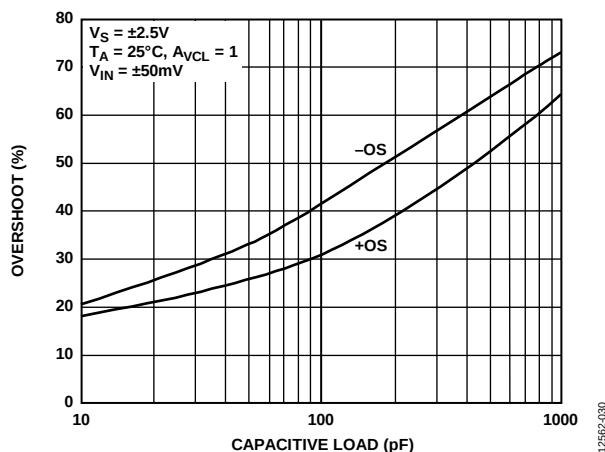


Figure 23. Small Signal Overshoot vs. Capacitive Load

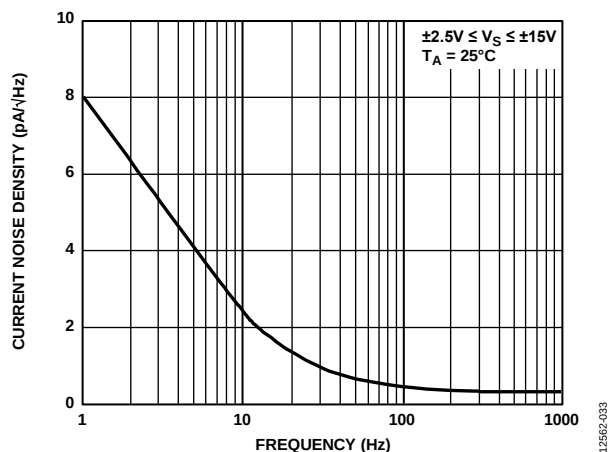
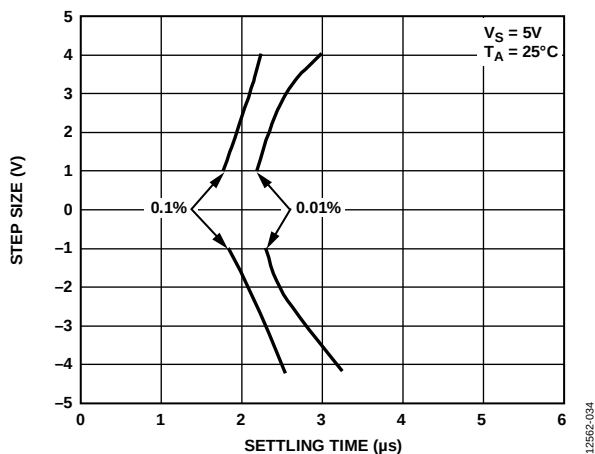
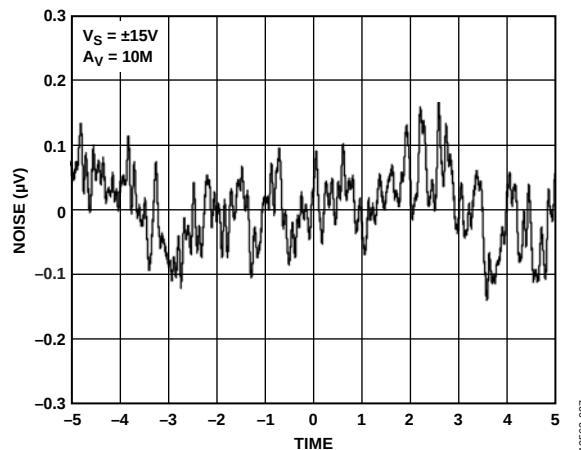


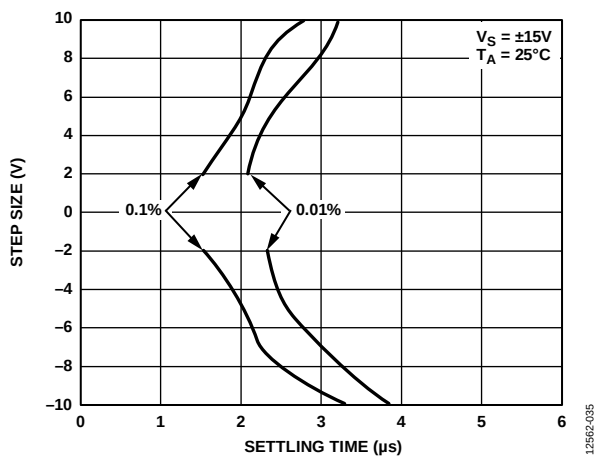
Figure 26. Current Noise Density vs. Frequency

Figure 27. Step Size vs. Settling Time, $V_S = 5\text{ V}$

12562-034

Figure 30. 0.1 Hz to 10 Hz Noise, $V_S = \pm 15\text{ V}$

12562-037

Figure 28. Step Size vs. Settling Time, $V_S = \pm 15\text{ V}$

12562-035

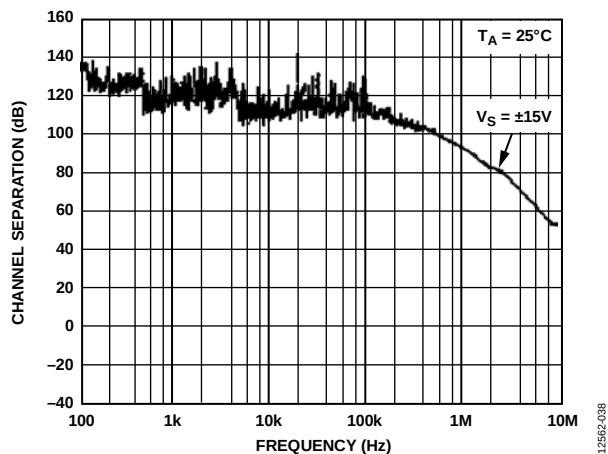
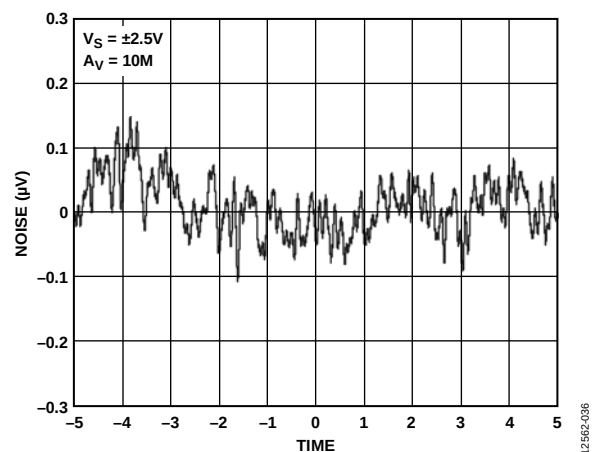


Figure 31. Channel Separation vs. Frequency

12562-038

Figure 29. 0.1 Hz to 10 Hz Noise, $V_S = \pm 2.5\text{ V}$

12562-036

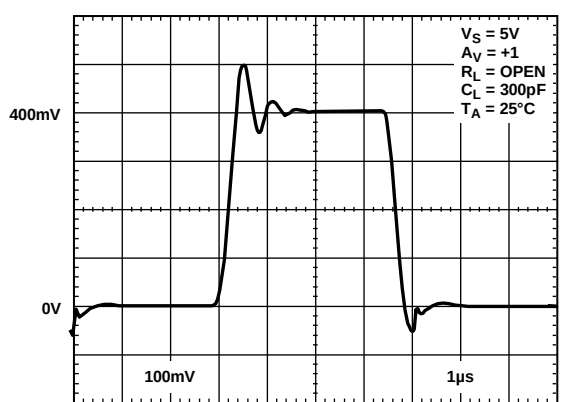


Figure 32. Small Signal Transient Response

12562-039

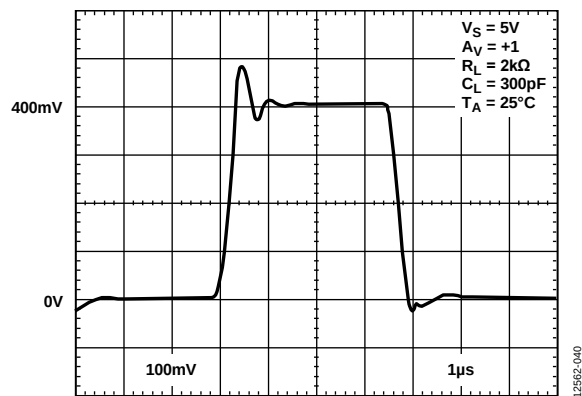


Figure 33. Small Signal Transient Response

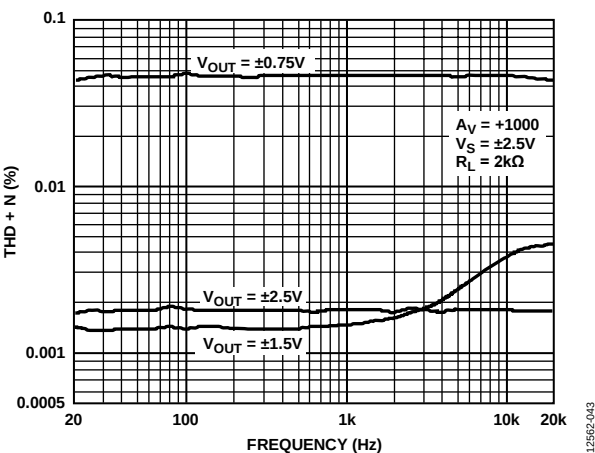
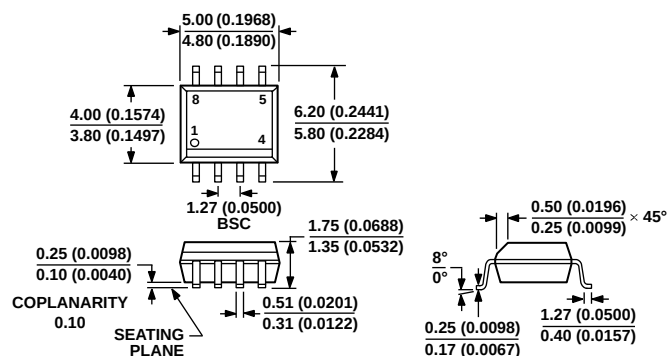


Figure 34. Total Harmonic Distortion + Noise vs. Frequency

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
OP284TRZ-EP-R7	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

¹ Z = RoHS Compliant Part.