

Absolute Maximum Ratings

DCIN, CSSP, CSSS, CSSN,
 VHP, VHN, DHI to GND -0.3V to +30V
 VHP, DHI to VHN -0.3V to +6V
 BATT, CSIP, CSIN, BLKP to GND -0.3V to +20V
 CSIP to CSIN, CSSP to CSSN,
 CSSP to CSSS, PGND to GND -0.3V to +0.3V
 CCI, CCS, CCV, REF, IINP to GND -0.3V to ($V_{LDO} + 0.3V$)
 DBST to GND -0.3V to ($V_{DLOV} + 0.3V$)
 DLOV, VCTL, ICTL, REFIN, CELLS,
 CLS, LDO, ASNS, SHDN to GND -0.3V to +6V

LDO Current 50mA
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 32-Pin Thin QFN 5mm x 5mm
 (derate 21mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 1.7W
 Operating Temperature Range
 MAX1870AETJ -40°C to $+85^\circ\text{C}$
 Storage Temperature Range -60°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32 TQFN

Package Code	T3255+4
Outline Number	21-0140
Land Pattern Number	90-0012

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
VCTL Range		0		3.6	V
Battery Regulation Voltage Accuracy	$V_{VCTL} = V_{LDO}$ (2 cells)	-0.5		+0.5	%
	$V_{VCTL} = V_{LDO}$ (3 cells)	-0.5		+0.5	
	$V_{VCTL} = V_{LDO}$ (4 cells)	-0.5		+0.5	
	$V_{VCTL} = V_{REFIN}$ (2 cells)	-0.8		+0.8	
	$V_{VCTL} = V_{REFIN}$ (3 cells)	-0.8		+0.8	
	$V_{VCTL} = V_{REFIN}$ (4 cells)	-0.8		+0.8	
	$V_{VCTL} = V_{REFIN} / 20$ (2 cells)	-1.2		+1.2	
	$V_{VCTL} = V_{REFIN} / 20$ (3 cells)	-1.2		+1.2	
	$V_{VCTL} = V_{REFIN} / 20$ (4 cells)	-1.2		+1.2	
VCTL Default Threshold	VCTL rising	4.0	4.1	4.2	V
VCTL Input Bias Current	$0 < V_{VCTL} < V_{REFIN}$	-1		+1	μA
	$DCIN = 0$, $V_{REFIN} = V_{VCTL} = 3.6V$	-1		+1	
	$V_{CTL} = DCIN = 0$, $V_{REFIN} = 3.6V$	-1		+1	

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-CURRENT REGULATION						
ICTL Range			0		3.6	V
Quick-Charge-Current Accuracy	$V_{ICTL} = V_{REFIN}$		67	73	79	mV
	$V_{ICTL} = V_{REFIN} \times 0.8$		54	59	64	
	$V_{ICTL} = V_{REFIN} \times 0.583$		39	43	47	
Trickle-Charge-Current Accuracy	$V_{ICTL} = V_{REFIN} \times 0.0625$		3.0	4.5	6.0	mV
BATT/CSIP/CSIN Input Voltage Range			0		19	V
CSIP Input Current	DCIN = 0		0.1		2	μ A
	ICTL = 0		0.1		2	
	ICTL = REFIN		350		600	
CSIN Input Current	DCIN = 0		0.1		2	μ A
	ICTL = 0		0.1		2	
	ICTL = REFIN		0.1		2	
ICTL Power-Down-Mode Threshold Voltage			REFIN / 100	REFIN / 55	REFIN / 32	V
ICTL Input Bias Current	$0 < V_{ICTL} < V_{REFIN}$		-1		+1	μ A
	ICTL = DCIN = 0, $V_{REFIN} = 3.6V$		-1		+1	
INPUT-CURRENT REGULATION						
Charger-Input Current-Limit Accuracy ($V_{CSSP} - V_{CSSN}$)	CSSS = CSSP	CLS = REF	97	105	113	mV
		CLS = REF x 0.845	81	88	95	
System-Input Current-Limit Accuracy ($V_{CSSP} - V_{CSSS}$)	CSSN = CSSP	CLS = REF	97	105	113	mV
		CLS = REF x 0.845	81	88	95	
CSSP/CSSS/CSSN Input Voltage Range			8		28	V
CSSP Input Current	$V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{DCIN} = 6V$		-1		+1	μ A
	$V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{DCIN} = 8V, 28V$		700		1200	
CSSS/CSSN Input Current	$V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{DCIN} = 6V$		-1		+1	μ A
	$V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{DCIN} = 8V, 28V$		-1		+1	
CLS Input Range			$V_{REF} / 2$		V_{REF}	V
CLS Input Bias Current	CLS = REF		-1		+1	μ A
IINP Transconductance	$V_{CSSP} - V_{CSSS} = 102mV$, CSSN = CSSP		2.5	2.8	3.1	μ A/mV
IINP Output Current	$V_{CSSP} - V_{CSSN} = 200mV$, $V_{IINP} = 0V$		350			μ A
	$V_{CSSP} - V_{CSSS} = 200mV$, $V_{IINP} = 0V$		350			
IINP Output Voltage	$V_{CSSP} - V_{CSSN} = 200mV$, IINP float		3.5			V
	$V_{CSSP} - V_{CSSS} = 200mV$, IINP float		3.5			

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		8		28	V
DCIN Undervoltage Lockout	DCIN falling	4	6.2		V
	DCIN rising		6.3	7.85	
DCIN Quiescent Current	8.0V < V _{DCIN} < 28V		3.5	6	mA
BATT Input Voltage Range		0		19	V
BATT Input Bias Current	DCIN = 0		0.1	1	μA
	V _{BATT} = 2V to 19V		300	500	
LDO Output Voltage	No load	5.3	5.4	5.5	V
LDO Load Regulation	0 < I _{LDO} < 10mA		70	150	mV
LDO Undervoltage Lockout	V _{DCIN} = 8V, LDO rising	4.00	5.0	5.25	V
REFERENCE					
REF Output Voltage	I _{REF} = 0μA	4.076	4.096	4.116	V
REF Load Regulation	0 < I _{REF} < 500μA		5	10	mV
REF Undervoltage-Lockout Trip Point	V _{REF} falling		3.1	3.9	V
REFIN Input Range		2.5		3.6	V
REFIN UVLO Rising			1.9	2.2	V
REFIN UVLO Hysteresis			50		mV
REFIN Input Bias Current	V _{DCIN} = 18V		50	100	μA
	DCIN = 0, V _{REFIN} = 3.6V	-1		+1	
SWITCHING REGULATOR					
Cycle-by-Cycle Step-Up Maximum Current-Limit Sense Voltage	V _{DCIN} = 12V, V _{BATT} = 16.8V	135	150	165	mV
Cycle-by-Cycle Step-Down Maximum Current-Limit Sense Voltage	V _{DCIN} = 19V, V _{BATT} = 16.8V	135	150	165	mV
Step-Down On-Time	V _{DCIN} = 18V, V _{BATT} = 16.8V	2.2	2.4	2.6	μs
Minimum Step-Down Off-Time	V _{DCIN} = 18V, V _{BATT} = 16.8V	0.15	0.4	0.50	μs
Step-Up Off-Time	V _{DCIN} = 12V, V _{BATT} = 16.8V	1.6	1.8	2.0	μs
Minimum Step-Up On-Time	V _{DCIN} = 12V, V _{BATT} = 16.8V	0.15	0.3	0.40	μs

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MOSFET DRIVERS					
VHP - VHN Output Voltage	$8V < V_{VHP} < 28V$, no load	4.5	5	5.5	V
VHN Load Regulation	$0 < I_{VHN} < 10mA$		70	150	mV
DHI On-Resistance High	$I_{SOURCE} = 10mA$		2	5	Ω
DHI On-Resistance Low	$I_{SINK} = 10mA$		1	3	Ω
VHP Input Bias Current	$DCIN = 0$		0.1	1	μA
	$V_{DCIN} = 18V$		1.3	2	mA
BLKP Input Bias Current	$ICTL = 0$		0.1	2	μA
	$V_{ICTL} = V_{REFIN} = 3.3V$		100	400	
DLOV Supply Current	DBST low		5	10	μA
DBST On-Resistance High	$I_{SOURCE} = 10mA$		2	5	Ω
DBST On-Resistance Low	$I_{SINK} = 10mA$		1	3	Ω
ERROR AMPLIFIERS					
GMV Amplifier Loop Transconductance	$V_{CTL} = REF_{IN}$, $V_{BATT} = 16.8V$	0.05	0.1	0.20	$\mu A/mV$
GMI Amplifier Loop Transconductance	$ICTL = REF_{IN}$, $V_{CSIP} - V_{CSIN} = 72mV$	1.8	2.4	3.0	$\mu A/mV$
GMS Amplifier Loop Transconductance	$V_{CLS} = REF$, $V_{CSSP} - V_{CSSN} = 102mV$, $V_{CSSP} = V_{CSSS}$	1.2	1.7	2.2	$\mu A/mV$
	$V_{CLS} = REF$, $V_{CSSP} - V_{CSSS} = 102mV$, $V_{CSSP} = V_{CSSN}$	1.2	1.7	2.2	
CCV Output Current	$V_{CTL} = REF_{IN}$, $V_{BATT} = 15.8V$	50			μA
	$V_{CTL} = REF_{IN}$, $V_{BATT} = 17.8V$			-50	
CCI Output Current	$ICTL = REF_{IN}$, $V_{CSIP} - V_{CSIN} = 0mV$	150			μA
	$ICTL = REF_{IN}$, $V_{CSIP} - V_{CSIN} = 150mV$			-150	
CCS Output Current	$CLS = REF$, $V_{CSSP} = V_{CSSN}$, $V_{CSSP} = V_{CSSS}$	100			μA
	$CLS = REF$, $V_{CSSP} - V_{CSSN} = 200mV$, $V_{CSSP} - V_{CSSS} = 200mV$			-100	
CCI/CCS/CCV Clamp Voltage	$1.1V < V_{CCV} < 3.5V$, $1.1V < V_{CCS} < 3.5V$, $1.1V < V_{CCI} < 3.5V$	100	300	500	mV

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS					
ASNS Output-Voltage Low	$V_{IINP} = GND$, $I_{SINK} = 1mA$			0.4	V
ASNS Output-Voltage High	$V_{IINP} = 4V$, $I_{SOURCE} = 1mA$	LDO - 0.5			V
ASNS Current Detect	V_{IINP} rising	1.1	1.15	1.2	V
	Hysteresis		50		mV
\overline{SHDN} Input Bias Current	$V_{\overline{SHDN}} = 0$ to V_{REFIN}	-1		+1	μA
	$DCIN = 0$, $V_{REFIN} = 5V$, $V_{\overline{SHDN}} = 0$ to V_{REFIN}	-1		+1	
\overline{SHDN} Threshold	\overline{SHDN} falling, $V_{REFIN} = 2.8V$ to $3.6V$	22	23.5	25	% of $REFIN$
\overline{SHDN} Hysteresis			1		% of $REFIN$
CELLS Input Low Voltage				0.75	V
CELLS Float Voltage		40	50	60	% of $REFIN$
CELLS Input High Voltage		$REFIN - 0.75V$			V
CELLS Input Bias Current	$CELLS = 0$ to $REFIN$	-2		+2	μA

Electrical Characteristics

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION					
VCTL Range		0		3.6	V
Battery Regulation Voltage Accuracy	$V_{VCTL} = V_{LDO} (2 \text{ cells})$	-0.8		+0.8	%
	$V_{VCTL} = V_{LDO} (3 \text{ cells})$	-0.8		+0.8	
	$V_{VCTL} = V_{LDO} (4 \text{ cells})$	-0.8		+0.8	
	$V_{VCTL} = V_{REFIN} (2 \text{ cells})$	-1.2		+1.2	
	$V_{VCTL} = V_{REFIN} (3 \text{ cells})$	-1.2		+1.2	
	$V_{VCTL} = V_{REFIN} (4 \text{ cells})$	-1.2		+1.2	
	$V_{VCTL} = V_{REFIN} / 20 (2 \text{ cells})$	-1.4		+1.4	
	$V_{VCTL} = V_{REFIN} / 20 (3 \text{ cells})$	-1.4		+1.4	
	$V_{VCTL} = V_{REFIN} / 20 (4 \text{ cells})$	-1.4		+1.4	
VCTL Default Threshold	VCTL rising	4.0		4.2	V
CHARGE-CURRENT REGULATION					
ICTL Range		0		3.6	V
Quick-Charge-Current Accuracy	$V_{ICTL} = V_{REFIN}$	66		80	mV
	$V_{ICTL} = V_{REFIN} \times 0.8$	53		65	
	$V_{ICTL} = V_{REFIN} \times 0.583$	38		48	
BATT/CSIP/CSIN Input Voltage Range		0		19	V
CSIP Input Current	$ICTL = REFIN$			600	μA
ICTL Power-Down-Mode Threshold Voltage		$REFIN / 100$		$REFIN / 32$	V
INPUT-CURRENT REGULATION					
Charger-Input Current-Limit Accuracy ($V_{CSSP} - V_{CSSN}$)	$CSSS = CSSP$	CLS = REF	95	115	mV
		CLS = REF $\times 0.845$	79	97	
System-Input Current-Limit Accuracy ($V_{CSSP} - V_{CSSS}$)	$CSSN = CSSP$	CLS = REF	95	115	mV
		CLS = REF $\times 0.845$	79	97	
CSSP/CSSS/CSSN Input Voltage Range		8		28	V
CSSP Input Current	$V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{DCIN} = 8V, 28V$			1200	μA
CLS Input Range		$V_{REF} / 2$		V_{REF}	V
IINP Transconductance	$V_{CSSP} - V_{CSSS} = 102mV, CSSN = CSSP$	2.5		3.1	$\mu A/mV$
IINP Output Current	$V_{CSSP} - V_{CSSN} = 200mV, V_{IINP} = 0V$	350			μA
	$V_{CSSP} - V_{CSSS} = 200mV, V_{IINP} = 0V$	350			
IINP Output Voltage	$V_{CSSP} - V_{CSSN} = 200mV, IINP \text{ float}$	3.5			V
	$V_{CSSP} - V_{CSSS} = 200mV, IINP \text{ float}$	3.5			

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND LINEAR REGULATOR					
DCIN Input Voltage Range		8		28	V
DCIN Undervoltage Lockout	DCIN falling	4			V
	DCIN rising			7.85	
DCIN Quiescent Current	$8.0V < V_{DCIN} < 28V$			6	mA
BATT Input Voltage Range		0		19	V
BATT Input Bias Current	$V_{BATT} = 2V$ to $19V$			500	μA
LDO Output Voltage	No load	5.3		5.5	V
LDO Undervoltage Lockout	$V_{DCIN} = 8V$, LDO rising	4.00		5.25	V
REFERENCE					
REF Output Voltage	$I_{REF} = 0\mu A$	4.060		4.132	V
REF Load Regulation	$0 < I_{REF} < 500\mu A$			10	mV
REF Undervoltage-Lockout Trip Point	V_{REF} falling			3.9	V
REFIN Input Range		2.5		3.6	V
REFIN UVLO Rising				2.2	V
REFIN Input Bias Current	$V_{DCIN} = 18V$			100	μA
SWITCHING REGULATOR					
Cycle-by-Cycle Step-Up Maximum Current-Limit Sense Voltage	$V_{DCIN} = 12V$, $V_{BATT} = 16.8V$	130		170	mV
Cycle-by-Cycle Step-Down Maximum Current-Limit Sense Voltage	$V_{DCIN} = 19V$, $V_{BATT} = 16.8V$	130		170	mV
Step-Down On-Time	$V_{DCIN} = 18V$, $V_{BATT} = 16.8V$	2.2		2.6	μs
Minimum Step-Down Off-Time	$V_{DCIN} = 18V$, $V_{BATT} = 16.8V$	0.15		0.50	μs
Step-Up Off-Time	$V_{DCIN} = 12V$, $V_{BATT} = 16.8V$	1.6		2.0	μs
Minimum Step-Up On-Time	$V_{DCIN} = 12V$, $V_{BATT} = 16.8V$	0.15		0.40	μs
MOSFET DRIVERS					
VHP - VHN Output Voltage	$8V < V_{VHP} < 28V$, no load	4.5		5.5	V
VHN Load Regulation	$0 < I_{VHN} < 10mA$			150	mV
DHI On-Resistance High	$I_{SOURCE} = 10mA$			5	Ω
DHI On-Resistance Low	$I_{SINK} = 10mA$			3	Ω
VHP Input Bias Current	$V_{DCIN} = 18V$			2	mA
BLKP Input Bias Current	$V_{ICTL} = V_{REFIN} = 3.3V$			400	μA
DLOV Supply Current	DBST low			10	μA
DBST On-Resistance High	$I_{SOURCE} = 10mA$			5	Ω
DBST On-Resistance Low	$I_{SINK} = 10mA$			3	Ω

Electrical Characteristics (continued)

(Circuit of Figure 2, $V_{DCIN} = V_{CSSP} = V_{CSSN} = V_{CSSS} = V_{VHP} = 18V$, $V_{BATT} = V_{CSIP} = V_{CSIN} = V_{BLKP} = 12V$, $V_{REFIN} = 3.0V$, $V_{ICTL} = 0.75 \times V_{REFIN}$, $V_{CTL} = LDO$, $CELLS = FLOAT$, $GND = PGND = 0$, $V_{DLOV} = 5.4V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.) (Note 1)

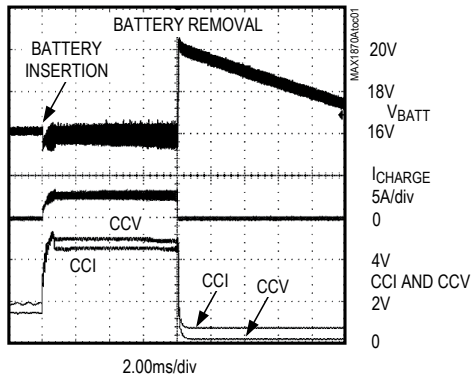
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS					
GMV Amplifier Loop Transconductance	$V_{CTL} = REFIN$, $V_{BATT} = 16.8V$	0.05		0.20	$\mu A/mV$
GMI Amplifier Loop Transconductance	$ICTL = REFIN$, $V_{CSIP} - V_{CSIN} = 72mV$	1.8		3.0	$\mu A/mV$
GMS Amplifier Loop Transconductance	$V_{CLS} = REF$, $V_{CSSP} - V_{CSSN} = 102mV$, $V_{CSSP} = V_{CSSS}$	1.2		2.2	$\mu A/mV$
	$V_{CLS} = REF$, $V_{CSSP} - V_{CSSS} = 102mV$, $V_{CSSP} = V_{CSSN}$	1.2		2.2	
CCV Output Current	$V_{CTL} = REFIN$, $V_{BATT} = 15.8V$	50			μA
	$V_{CTL} = REFIN$, $V_{BATT} = 17.8V$			-50	
CCI Output Current	$ICTL = REFIN$, $V_{CSIP} - V_{CSIN} = 0mV$	150			μA
	$ICTL = REFIN$, $V_{CSIP} - V_{CSIN} = 150mV$			-150	
CCS Output Current	$CLS = REF$, $V_{CSSP} = V_{CSSN}$, $V_{CSSP} = V_{CSSS}$	100			μA
	$CLS = REF$, $V_{CSSP} - V_{CSSN} = 200mV$, $V_{CSSP} - V_{CSSS} = 200mV$			-100	
CCI/CCS/CCV Clamp Voltage	$1.1V < V_{CCV} < 3.5V$, $1.1V < V_{CCS} < 3.5V$, $1.1V < V_{CCI} < 3.5V$	100		500	mV
LOGIC LEVELS					
ASNS Output-Voltage Low	$V_{IINP} = GND$, $I_{SINK} = 1mA$			0.4	V
ASNS Output-Voltage High	$V_{IINP} = 4V$, $I_{SOURCE} = 1mA$	LDO - 0.5			V
ASNS Current Detect	V_{IINP} rising	1.1	1.15	1.2	V
\overline{SHDN} Threshold	\overline{SHDN} falling, $V_{REFIN} = 2.8V$ to $3.6V$	22		25	% of $REFIN$
CELLS Input Low Voltage				0.75	V
CELLS Float Voltage		40		60	% of $REFIN$
CELLS Input High Voltage		$REFIN - 0.75V$			V

Note 1: Specifications to $-40^{\circ}C$ are guaranteed by design, not production tested.

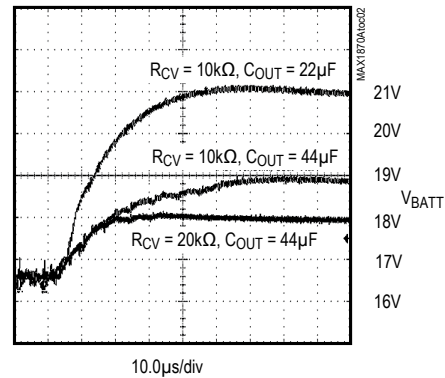
Typical Operating Characteristics

(Circuit of Figure 1, $V_{DCIN} = 16V$, $CELLS = REF_{IN}$, $V_{CLS} = V_{REF}$, $V_{ICTL} = V_{REFIN} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

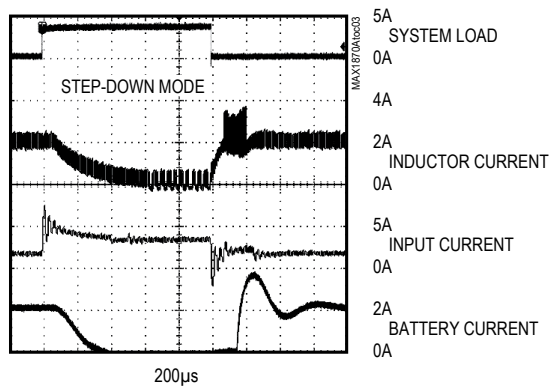
BATTERY INSERTION AND REMOVAL



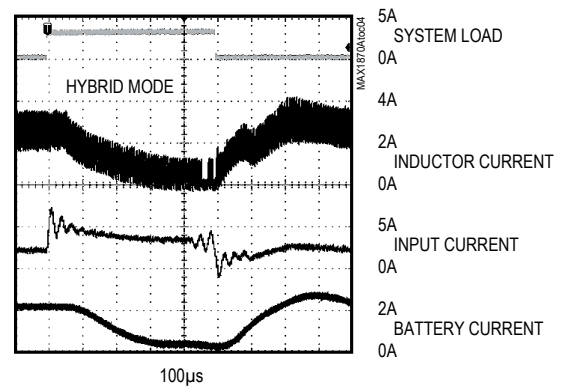
BATTERY-REMOVAL RESPONSE



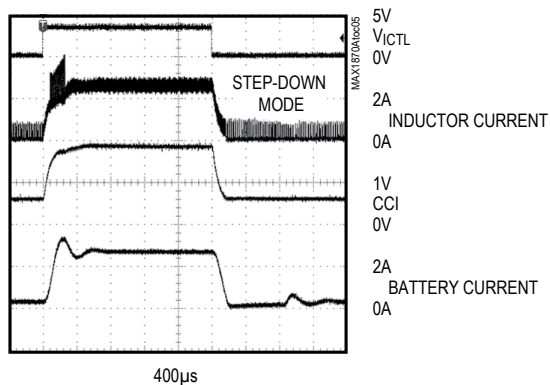
SYSTEM LOAD-TRANSIENT RESPONSE



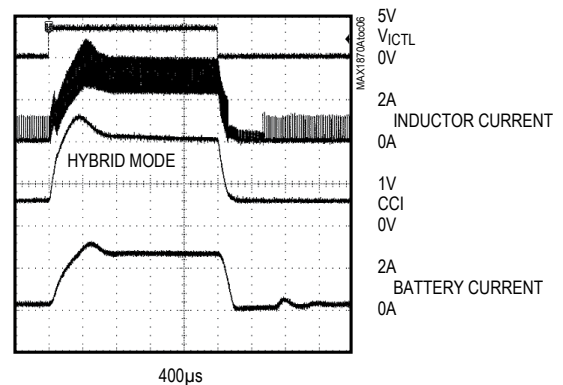
SYSTEM LOAD-TRANSIENT RESPONSE



CHARGE-CURRENT STEP RESPONSE

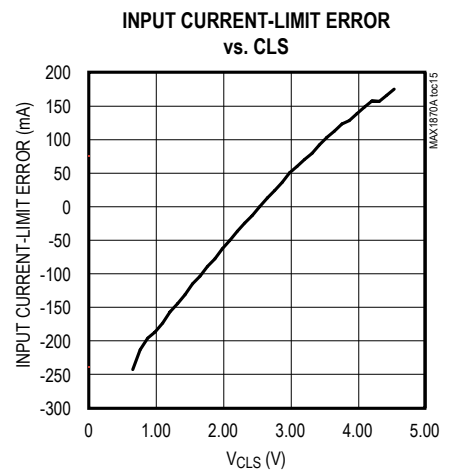
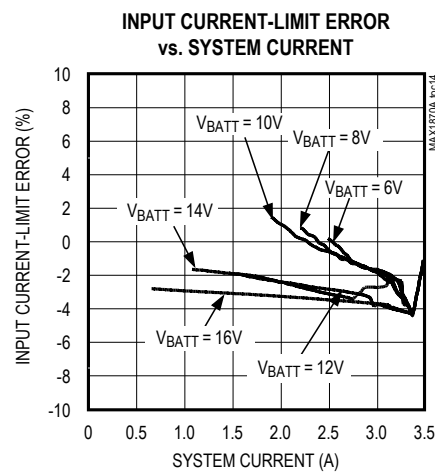
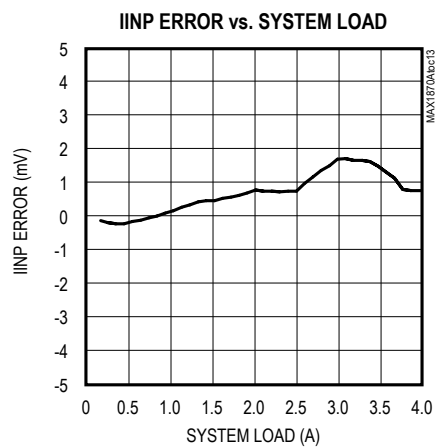
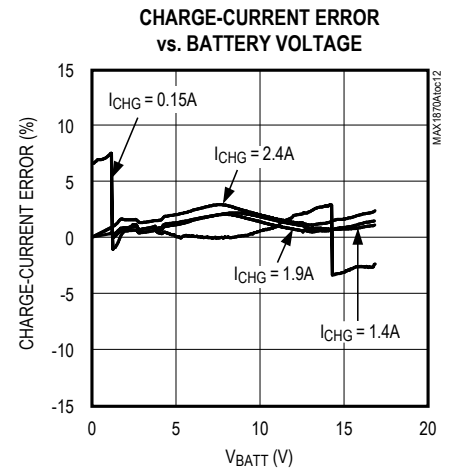
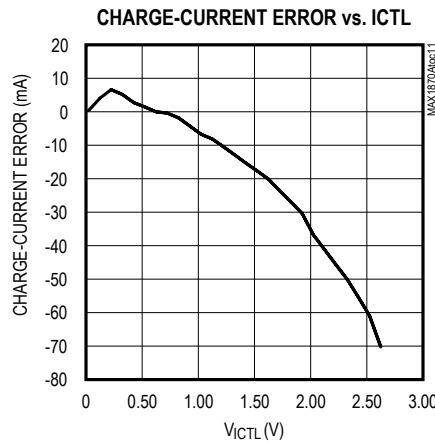
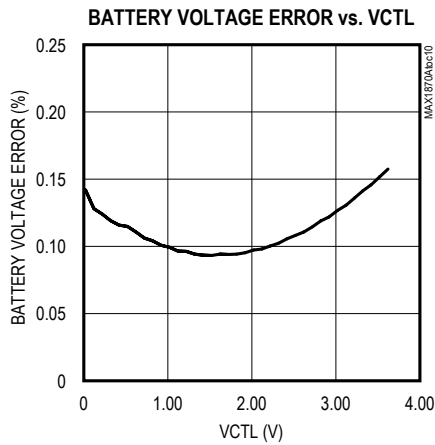
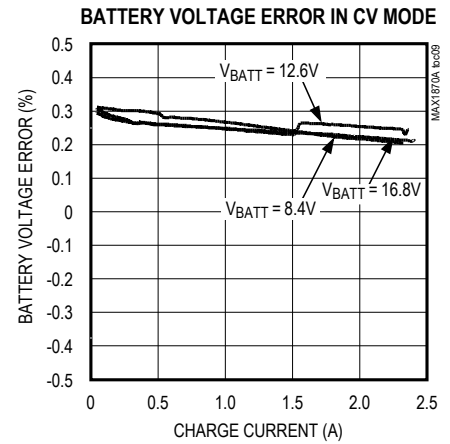
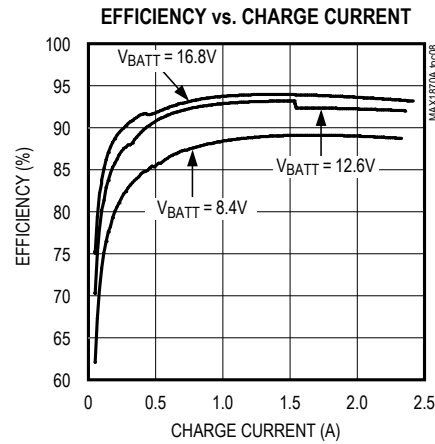
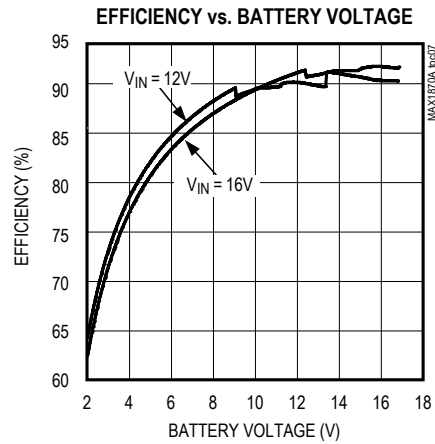


CHARGE-CURRENT STEP RESPONSE



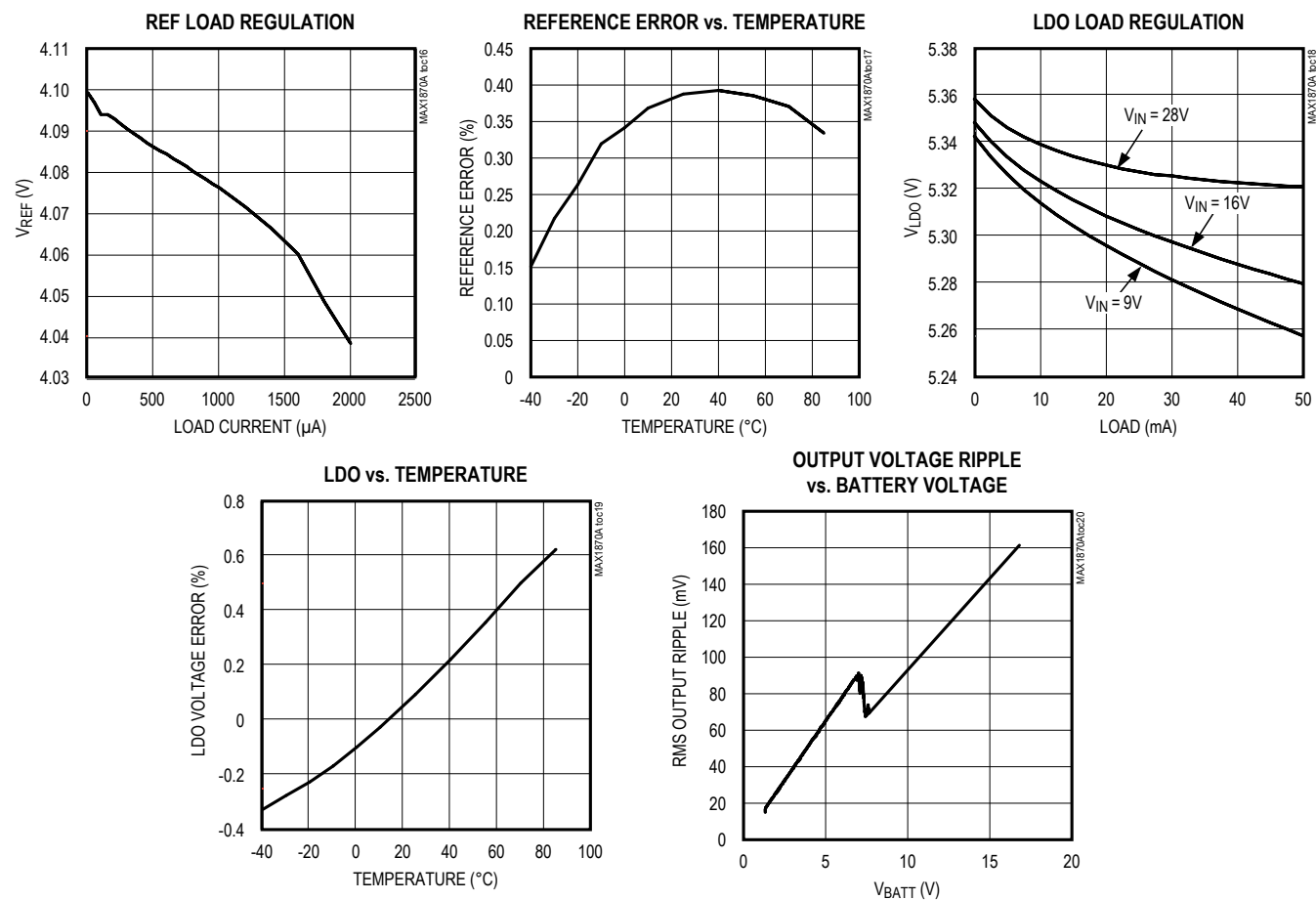
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{DCIN} = 16V$, CELLS = REFIN, $V_{CLS} = V_{REF}$, $V_{ICTL} = V_{REFIN} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



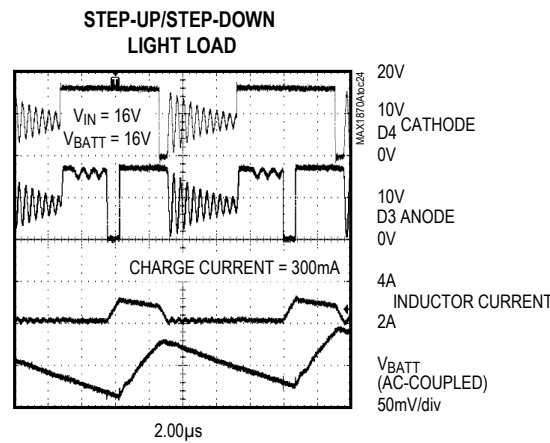
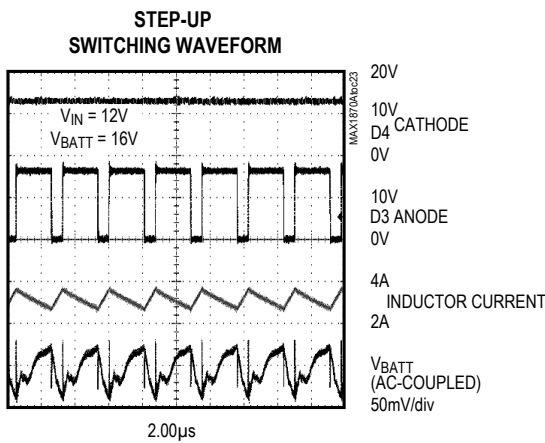
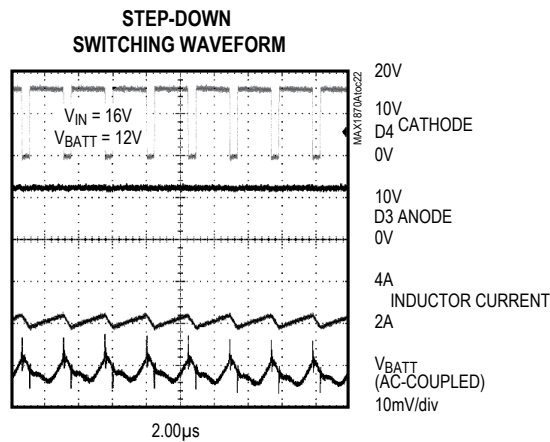
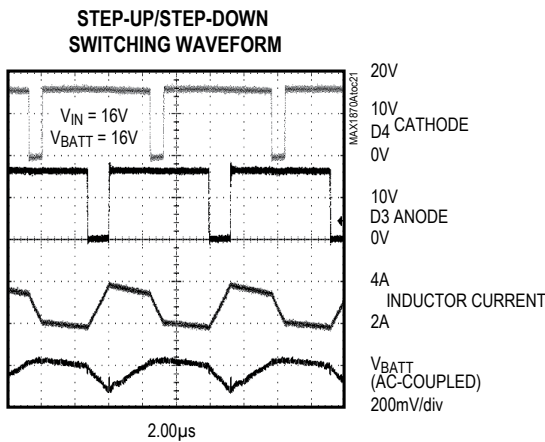
Typical Operating Characteristics (continued)

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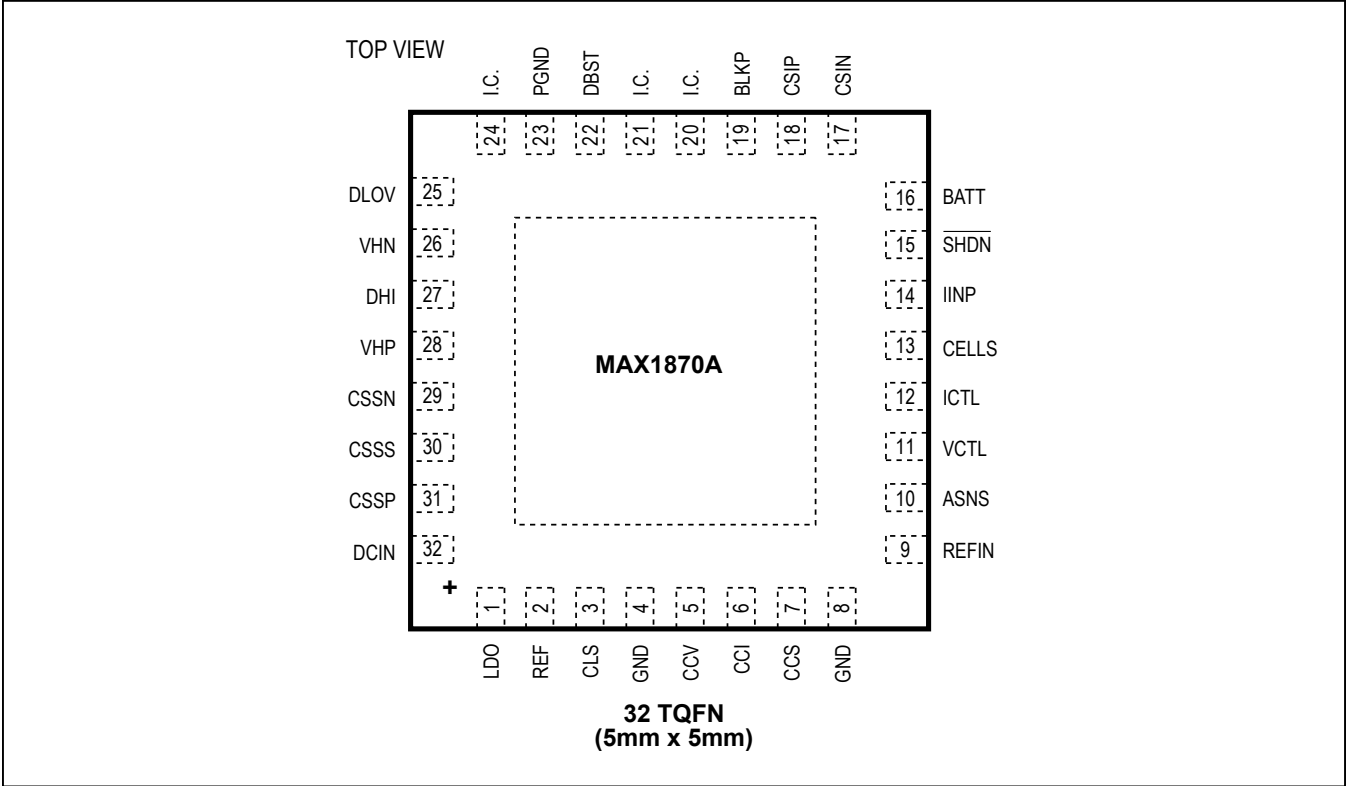


Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{DCIN} = 16V$, $CELLS = REF_{IN}$, $V_{CLS} = V_{REF}$, $V_{ICTL} = V_{REFIN} = 3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	LDO	Device Power Supply. Output of the 5.4V linear regulator supplied from DCIN. Bypass LDO to GND with a 1μF or greater ceramic capacitor.
2	REF	4.096V Voltage Reference. Bypass REF to GND with a 1μF or greater ceramic capacitor.
3	CLS	Source Current-Limit Input. Voltage input for setting the current limit of the input source. See the <i>Setting the Input Current Limit</i> section.
4, 8	GND	Analog Ground
5	CCV	Voltage Regulation Loop Compensation Point. Connect a 10kΩ resistor in series with a 0.01μF capacitor to GND.
6	CCI	Charge-Current Regulation Loop Compensation Point. Connect a 0.01μF capacitor to GND.
7	CCS	Input-Current Regulation Loop Compensation Point. Connect a 0.01μF capacitor to GND.
9	REFIN	Reference Input. ICTL and VCTL are ratiometric with respect to REFIN for increased accuracy.
10	ASNS	Adapter Sense Output. Logic output is high when input current is greater than 1.5A (using 30mΩ sense resistors and a 10kΩ resistor from IINP to GND).
11	VCTL	Charge-Voltage Control Input. Drive VCTL from 0 to VREFIN to adjust the charge voltage from 4V to 4.4V per cell. See the <i>Setting the Charge Voltage</i> section.
12	ICTL	Charge-Current Control Input. Drive ICTL from VREFIN / 32 to VREFIN to adjust the charge current. See the <i>Setting the Charge Current</i> section. Drive ICTL to GND to disable charging.

Pin Description (continued)

PIN	NAME	FUNCTION
13	CELLS	Cell-Count Selection Input. Connect CELLS to GND for two Li+ cells. Float CELLS for three Li+ cells, or connect CELLS to REFIN for four Li+ cells.
14	IINP	Input-Current Monitor Output. IINP is a replica of the input current sensed by the MAX1870. It represents the sum of the current consumed by the charger and the current consumed by the system. IINP has a transconductance of 2.8 μ A/mV.
15	$\overline{\text{SHDN}}$	Shutdown Comparator Input. Pull $\overline{\text{SHDN}}$ low to stop charging. Optionally connect a thermistor to stop charging when the battery temperature is too hot.
16	BATT	Battery-Voltage Feedback Input
17	CSIN	Charge Current-Sense Negative Input
18	CSIP	Charge Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN. Connect a 2.2 μ F capacitor from CSIP to GND.
19	BLKP	Power Connection for Current-Sense Amplifier. Connect BLKP to BATT.
20, 21	I.C.	Internally Connected. Do not connect this pin.
22	DBST	Step-Up Power MOSFET (NMOS) Gate-Driver Output
23	PGND	Power Ground
24	I.C.	Internally Connected. Do not connect this pin.
25	DLOV	Low-Side Driver Supply. Bypass DLOV with a 1 μ F capacitor to GND.
26	VHN	Power Connection for the High-Side MOSFET Driver. Bypass VHP to VHN with a 1 μ F or greater ceramic capacitor.
27	DHI	High-Side Power MOSFET (PMOS) Driver Output. Connect to the gate of the high-side step-down MOSFET.
28	VHP	Power Connection for the High-Side MOSFET Driver. Bypass VHP to VHN with a 1 μ F or greater ceramic capacitor.
29	CSSN	Negative Terminal for Current-Sense Resistor for Charger Current. Connect a 2.2 μ F capacitor from CSSN to GND.
30	CSSS	Negative Terminal for Current-Sense Resistor for System Load Current
31	CSSP	Positive Terminal for Input Current-Sense Resistors. Connect a current-sense resistor from CSSP to CSSN. Connect an equivalent sense resistor from CSSP to CSSS.
32	DCIN	DC Supply Voltage Input. Bypass DCIN with a 1 μ F or greater ceramic capacitor to power ground.
—	Paddle	Paddle. Connect to GND.

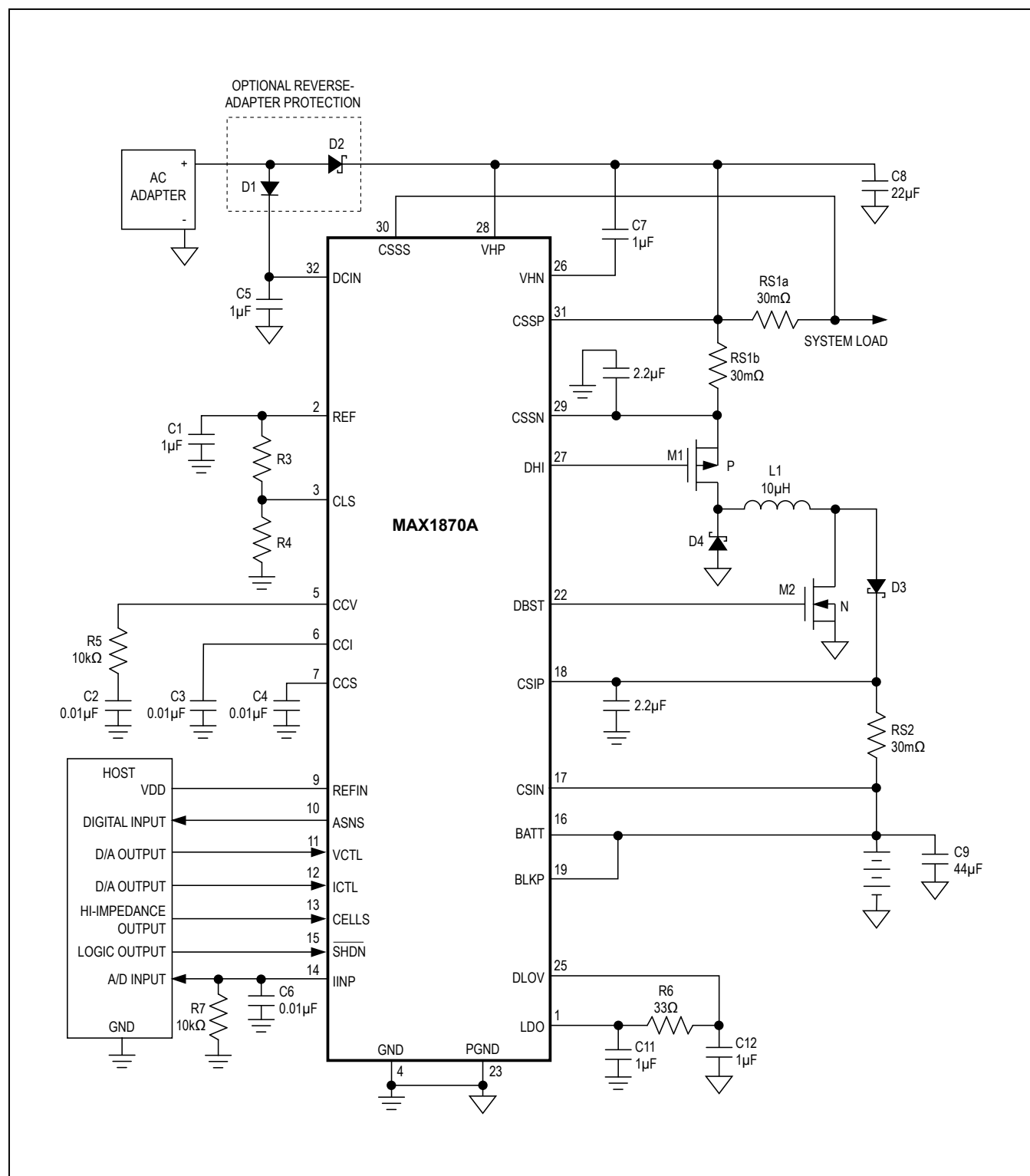


Figure 1. μC-Controlled Typical Application Circuit

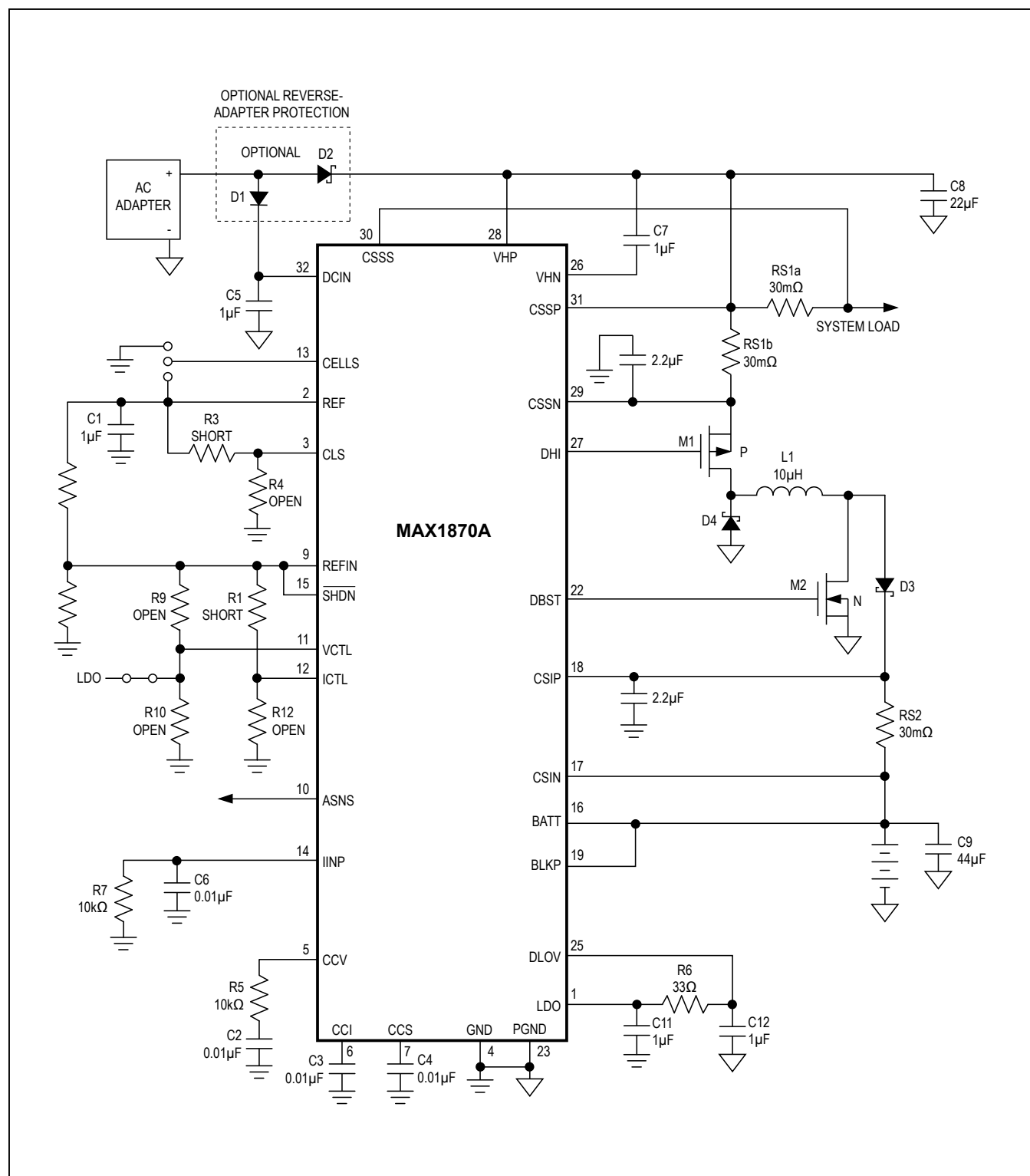


Figure 2. Stand-Alone Typical Application Circuit

Detailed Description

The MAX1870A includes all of the functions necessary to charge Li+, NiMH, and NiCd batteries. A high-efficiency H-bridge topology DC-DC converter controls charge voltage and current. A proprietary control scheme offers improved efficiency and smaller inductor size compared to conventional H-bridge controllers and operates from input voltages above and below the battery voltage. The MAX1870A includes analog control inputs to limit the AC adapter current, charge current, and battery voltage. An analog output (IINP) delivers a current proportional to the source current. The *Typical Application Circuit* shown in [Figure 1](#) uses a microcontroller (μC) to control the charge current or voltage, while [Figure 2](#) shows a typical application with the charge voltage and current fixed to specific values for the application. The voltage at ICTL and the value of RS2 set the charge current. The voltage at VCTL and the CELLS inputs set the battery regulation voltage for the charger. The voltage at CLS and the value of R3 and R4 set the source current limit.

The MAX1870A features a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). CCV is the compensation point for the battery voltage regulation loop. CCI and CCS are the compensation points for the battery charge current and supply current loops, respectively. The MAX1870A regulates the adapter current by reducing battery charge current according to system load demands.

Setting the Charge Voltage

The MAX1870A provides high-accuracy regulation of the charge voltage. Apply a voltage to VCTL to adjust the battery-cell voltage limit. Set VCTL to a voltage between 0 and VREFIN for a 10% adjustment of the battery cell voltage, or connect VCTL to LDO for a default setting of 4.2V per cell. The limited adjustment range reduces the sensitivity of the charge voltage to external resistor tolerances. The overall accuracy of the charge voltage is better than ±1% when using ±1% resistors to divide down the reference to establish VCTL. The per-cell battery-termination voltage is a function of the battery chemistry and construction. Consult the battery manufacturer to determine this voltage. Calculate battery voltage using the following equation:

$$V_{BATT} = N_{CELLS} \times \left(4V + 0.4V \times \frac{V_{VCTL}}{V_{REFIN}} \right)$$

where NCELLS is the cell count selected by CELLS. VCTL is ratiometric with respect to REFIN to improve accuracy when using resistive voltage-dividers. Connect CELLS as

Table 1. Cell Connections

CELLS	CELL COUNT
GND	2
Float	3
REFIN	4

shown in [Table 1](#) to charge two, three, or four cells. The cell count can either be hard-wired or software controlled. The internal error amplifier (GMV) maintains voltage regulation (see [Figure 3](#) for the *Functional Diagram*). Connect a 10kΩ resistor in series with a 0.01μF capacitor from CCV to GND to compensate the battery voltage loop. See the [Voltage Loop Compensation](#) section for more information.

Setting the Charge Current

Set the maximum charge current using ICTL and the current-sense resistor RS2 connected between CSIP and CSIN. The current threshold is set by the ratio of VICTL / VREFIN. Use the following equation to program the battery charge current:

$$I_{CHG} = \frac{V_{CSIT}}{RS2} \times \frac{V_{ICTL}}{V_{REFIN}}$$

where VCSIT is the full-scale charge current-sense threshold, 73mV (typ). The input range for ICTL is VREFIN / 32 to VREFIN. To shut down the MAX1870A, force ICTL below VREFIN / 100.

The internal error amplifier (GMI) maintains charge-current regulation (see [Figure 3](#) for the *Functional Diagram*). Connect a 0.01μF capacitor from CCI to GND to compensate the charge-current loop. See the [Charge-Current and Wall-Adapter-Current Loop Compensation](#) section for more information.

Setting the Input-Current Limit

The total input current, from a wall adapter or other DC source, is a function of the system supply current and the battery charge current. The MAX1870A limits the wall adapter current by reducing the charge current when the input current exceeds the input current-limit set point. As the system supply current rises, the available charge current decreases linearly to zero in proportion to the system current. After the charge current has fallen to zero, the MAX1870A cannot further limit the wall adapter current if the system current continues to increase.

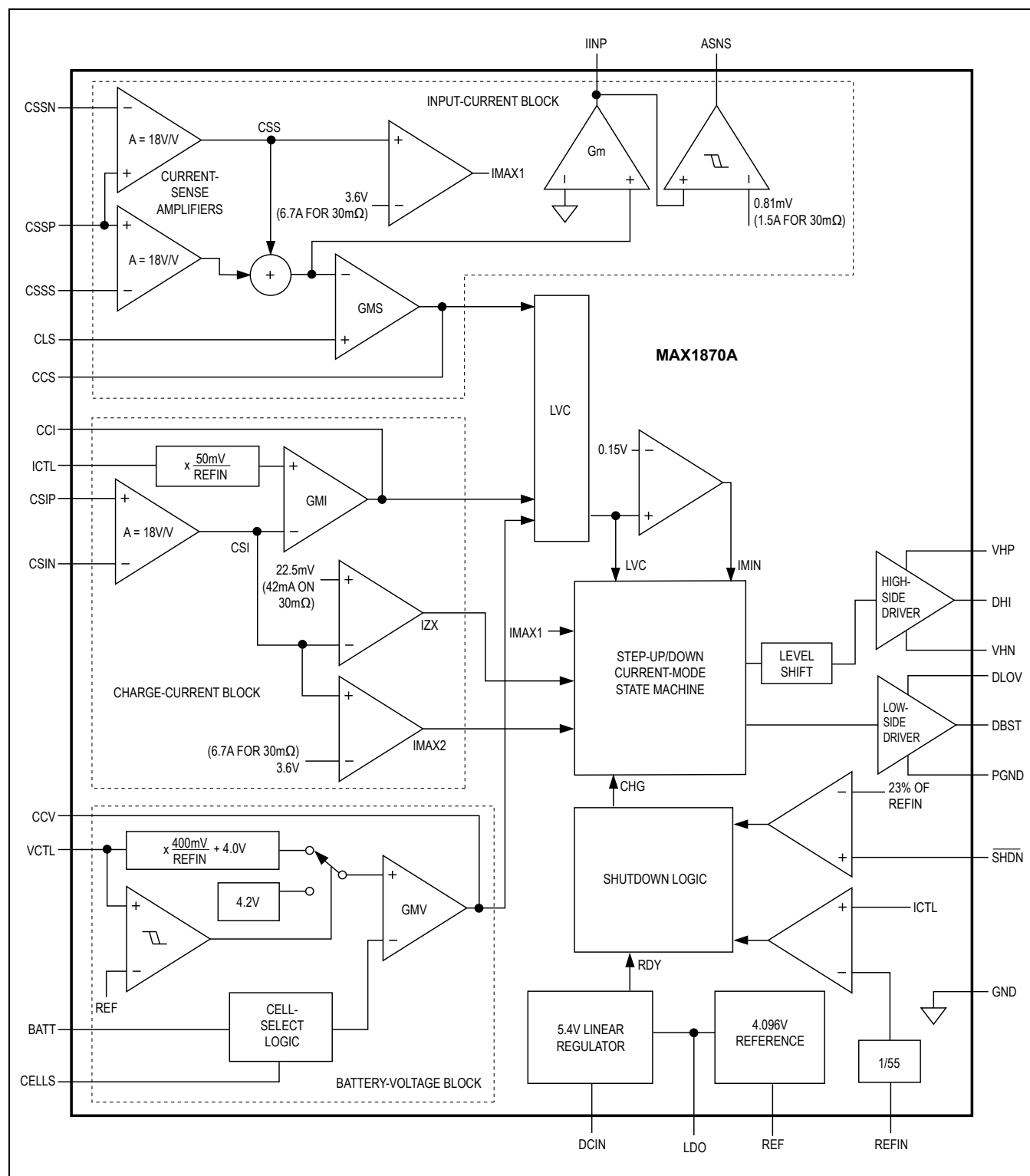


Figure 3. Functional Diagram

The input source current is the sum of the MAX1870A quiescent current, the charger input current, and the system load current. The MAX1870A's 6mA maximum quiescent current is minimal compared to the charge and load currents. The actual wall adapter current is determined as follows:

$$I_{\text{ADAPTER}} = I_{\text{SYS_LOAD}} + \frac{I_{\text{CHARGE}} \times V_{\text{BATT}}}{V_{\text{IN}} \times \eta}$$

where η is the efficiency of the DC-DC converter (85% to 95% typ), $I_{\text{SYS_LOAD}}$ is the system load current, I_{ADAPTER} is the adapter current, and I_{CHARGE} is the charge current.

By controlling the input current, the current requirements of the AC wall adapter are reduced, minimizing system size and cost. Since charge current is reduced to control input current, priority is given to system loads.

An internal amplifier compares the sum of ($V_{\text{CSSP}} - V_{\text{CSSN}}$) and ($V_{\text{CSSP}} - V_{\text{CSSS}}$) to a scaled voltage set by the CLS input. Drive V_{CLS} directly or set with a resistive voltage-divider between REF and GND. Connect CLS to REF for the maximum input current limit of 105mV. Sense resistors RS1a and RS1b set the maximum-allowable wall adapter current. Use the same values for RS1a, RS1b, and RS2. Calculate the maximum wall adapter current as follows:

$$I_{\text{ADAPTER_MAX}} = \frac{V_{\text{CLS}}}{V_{\text{REF}}} \times \frac{V_{\text{CSST}}}{\text{RS1_}}$$

where V_{CSST} is the full-scale source current-sense voltage threshold, and is 105mV (typ). The internal error amplifier (GMS) maintains input-current regulation (see [Figure 3](#) for the *Functional Diagram*). Typically, connect a 0.01 μ F capacitor from CCS to GND to compensate the source current loop (GMS). See the [Charge-Current and Wall-Adapter-Current Loop Compensation](#) section for more information.

Input-Current Measurement

The MAX1870A includes an input-current monitor output, IINP. IINP is a scaled-down replica of the system load current plus the input-referred charge current. The output voltage range for IINP is 0 to 3.5V. The voltage of IINP is proportional to the output current by the following equation:

$$V_{\text{IINP}} = I_{\text{ADAPTER}} \times \text{RS1_} \times G_{\text{IINP}} \times R7$$

where I_{ADAPTER} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of IINP (2.8 μ A/mV typ), and R7 is the resistor connected between IINP and ground.

In the *Typical Application Circuit*, the duty cycle and AC load current affect the accuracy of V_{IINP} (see the [Typical Operating Characteristics](#)).

LDO Regulator

LDO provides a 5.4V supply derived from DCIN. The low-side MOSFET driver is powered by DLOV, which must be connected to LDO as shown in [Figure 1](#). LDO also supplies the 4.096V reference (REF) and most of the internal control circuitry. Bypass LDO to GND with a 1 μ F or greater ceramic capacitor. Bypass DLOV to PGND with a 1 μ F or greater ceramic capacitor.

AC-Adapter Detection

The MAX1870A includes a logic output, ASNS, which indicates AC adapter presence. When the system load draws more than 1.5A (for 30m Ω sense resistors and R7 is 10k Ω), the ASNS logic output pulls high.

Shutdown

When the AC adapter is removed, the MAX1870A shuts down to a low-power state, and typically consumes less than 1 μ A from the battery through the combined load of the CSIP, CSIN, BLKP, and BATT inputs. The charger enters this low-power state when DCIN falls below the undervoltage-lockout (UVLO) threshold of 7.5V.

Alternatively, drive $\overline{\text{SHDN}}$ below 23.5% of V_{REFIN} or drive ICTL below $V_{\text{REFIN}} / 100$ to inhibit charge. This suspends switching and pulls CCI, CCS, and CCV to ground. The LDO, input current monitor, and control logic all remain active in this state.

Step-Up/Step-Down DC-DC Controller

The MAX1870A is a step-up/step-down DC-DC controller. The MAX1870A controls a low-side n-channel MOSFET and a high-side p-channel MOSFET to a constant output voltage with input voltage variation above, near, and below the output. The MAX1870A implements a control scheme that delivers higher efficiency with smaller components and less output ripple when compared with other step-up/step-down control algorithms. This occurs because the MAX1870A operates with lower inductor currents, as shown in [Figure 4](#).

The MAX1870A proprietary algorithm offers the following benefits:

- Inductor current requirements are minimized.
- Low inductor-saturation current requirements allow the use of physically smaller inductors.
- Low inductor current improves efficiency by reducing I^2R losses in the MOSFETs, inductor, and sense resistors.

- Continuous output current for $V_{IN} > 1.4 \times V_{OUT}$ reduces output ripple.

The MAX1870A uses the state machine shown in [Figure 5](#). The controller switches between the states A, B, and C, depending on V_{IN} and V_{BATT} . State D provides PFM operation during light loads. Under moderate and heavy loads the MAX1870A operates in PWM.

Step-Down Operation
($V_{IN} > 1.4 \times V_{BATT}$)

During medium and heavy loads when $V_{IN} > 1.4 \times V_{BATT}$, the MAX1870A alternates between state A and state B, keeping MOSFET M2 off ([Figure 5](#)). [Figure 6](#) shows the inductor current in step-down operation. During this mode, the MAX1870A regulates the step-down off-time. Initially, DHI switches M1 off (state A) and the inductor current ramps down with a di/dt of V_{BATT} / L until a target current is reached (determined by the error integrator). After the target current is reached, DHI switches M1 on (state B), and the inductor current ramps up with a di/dt

of $(V_{IN} - V_{BATT}) / L$. M1 remains on until a step-down on-time timer expires. This on-time is calculated based on the input and output voltage to maintain pseudo-fixed-frequency 400kHz operation. At the end of state B, another step-down off-time (state A) is initiated and the cycle repeats. The off-time is valley regulated according to the error signal. The error signal is set by the charge current or source current if either is at its limit, or the battery voltage if both charge current and source current are below their respective current limits.

During light loads, when the inductor current falls to zero during state A, the controller switches to state D to reduce power consumption and avoid shuttling current in and out of the output.

Step-Up Operation ($V_{IN} < 0.9 \times V_{BATT}$)

When $V_{IN} < 0.9 \times V_{BATT}$, the MAX1870A alternates between state B and state C, keeping MOSFET M1 on. In this mode, the controller looks like a simple step-up controller. [Figure 7](#) shows the inductor current in step-up

Table 2. MAX1870A H-Bridge Controller Advantages

MAX1870A H-BRIDGE CONTROLLER	TRADITIONAL H-BRIDGE CONTROLLER
<ul style="list-style-type: none">• Only 1 MOSFET switched per cycle• Continuous output current in step-down mode	<ul style="list-style-type: none">• 2 MOSFETs switched per cycle• Always discontinuous output current (requires higher inductor currents)

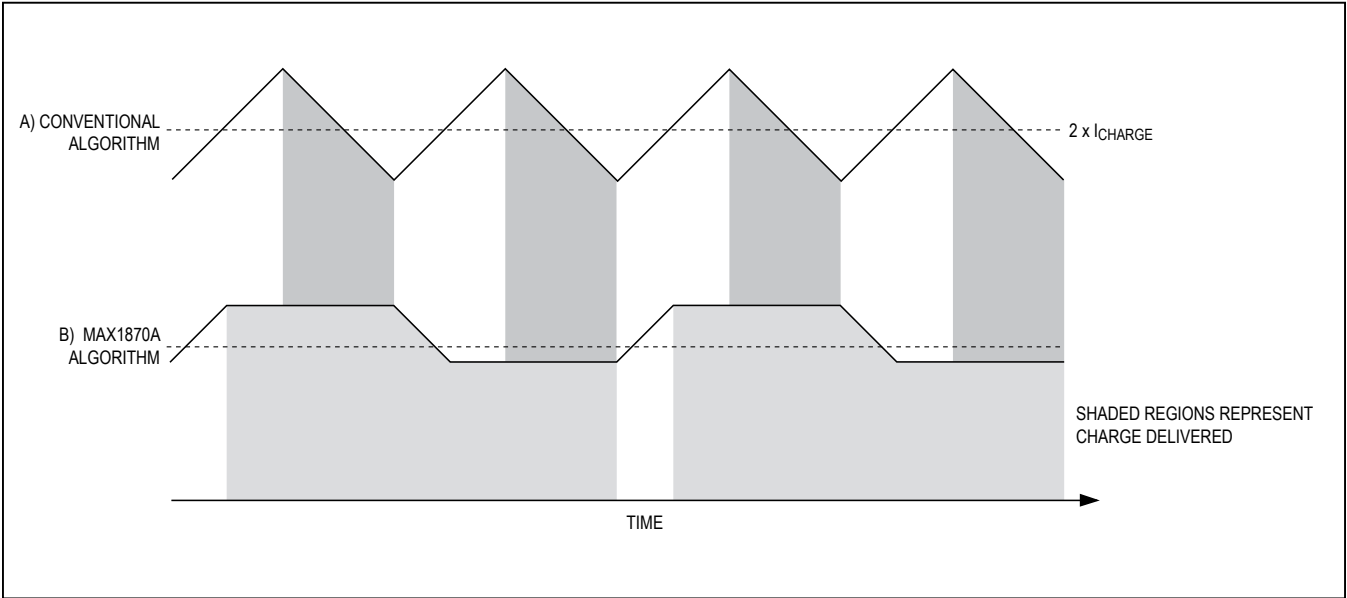


Figure 4. Inductor Current for $V_{IN} = V_{BATT}$

operation. During this mode, the MAX1870A regulates the step-up on-time. Initially DBST switches M2 on (state C) and the inductor current ramps up with a dI/dt of V_{IN} / L . After the inductor current crosses the target current (set by the error integrators), DBST switches M2 off (state B) and the inductor current ramps down with a dI/dt of $(V_{BATT} - V_{IN}) / L$. M2 remains off until a step-up off-time timer expires. This off-time is calculated based on the input and output voltage to maintain 400kHz pseudo-fixed-frequency operation. The step-up on-time is regulated by the error signal, set according to the charge current or source current if either is at its limit, or the battery voltage if both charge current and source current are below their respective current limits.

Step-Up/Step-Down Operation ($0.9 \times V_{BATT} < V_{IN} < 1.4 \times V_{BATT}$)

The MAX1870A features a step-up/step-down mode that eliminates dropout. Figure 8 shows the inductor current in step-up/step-down operation. When V_{IN} is within 10% of V_{BATT} , the MAX1870A alternates through states A, B,

and C, following the order A, B, C, B, A, B, C, etc., with the majority of the time spent in state B. Since more time is spent in state B, the inductor ripple current is reduced, improving efficiency.

The time in state C is peak-current regulated, and the remaining time is spent in state B (Figure 8A). During this operating mode, the average inductor current is approximately 20% higher than the load current.

The time in state A is valley current and the remaining time is spent in state B (Figure 8B). During this mode, the average inductor current is approximately 10% higher than the load current.

Alternative algorithms require inductor currents twice as high, resulting in four times larger I^2R losses and inductors typically four times larger in volume.

IMIN, IMAX, CCMP, and ZCMP

The MAX1870A state machine utilizes five comparators to decide which state to be in and when to switch states (Figure 3). The MAX1870A generates an error signal

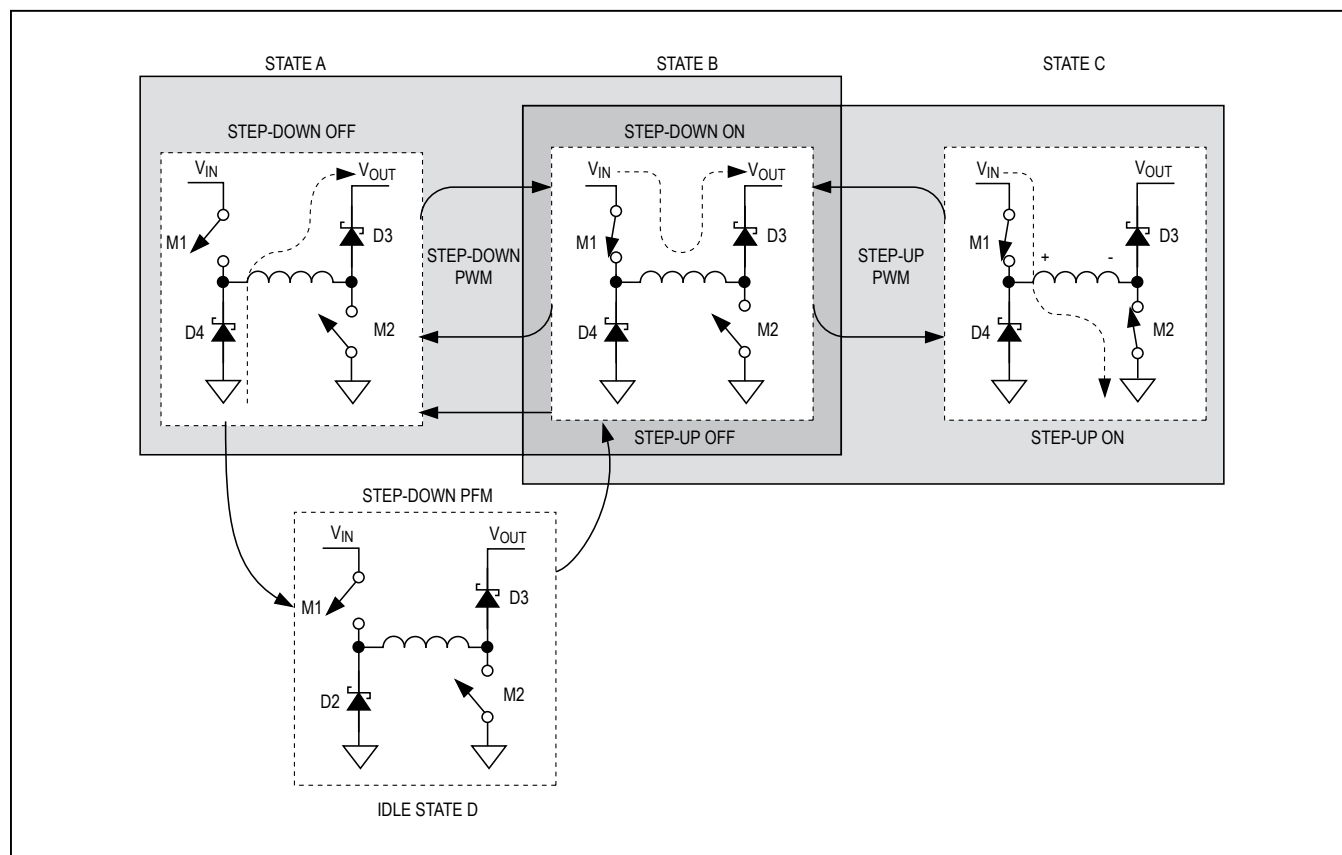


Figure 5. MAX1870A State Machine

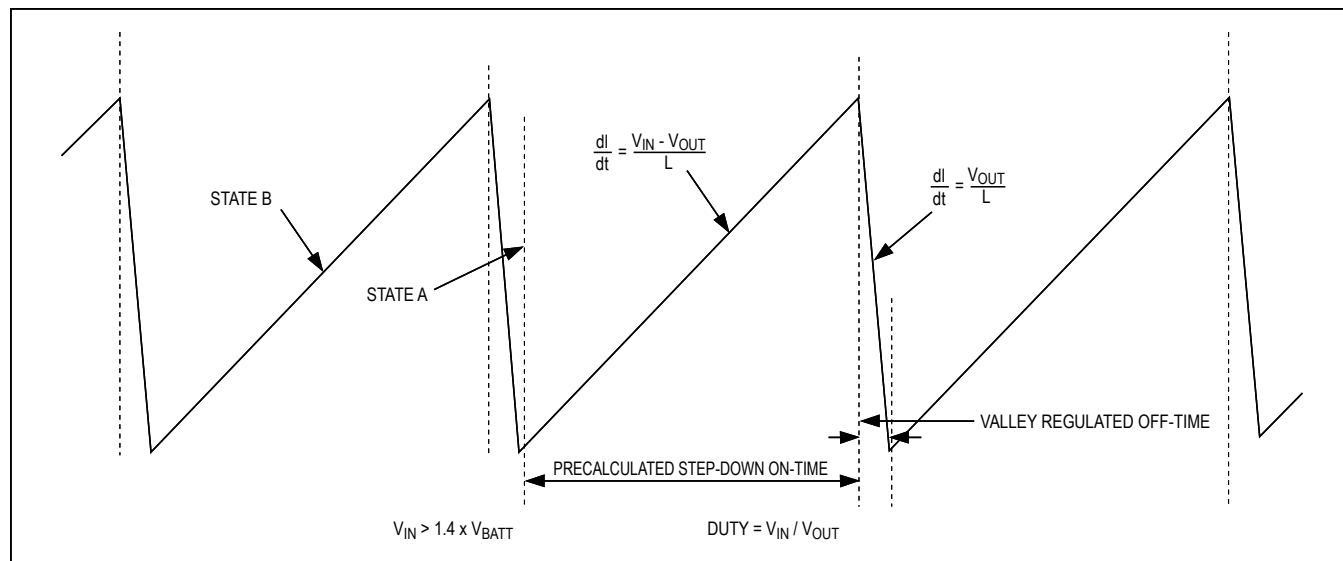


Figure 6. MAX1870A Step-Down Inductor Current Waveform

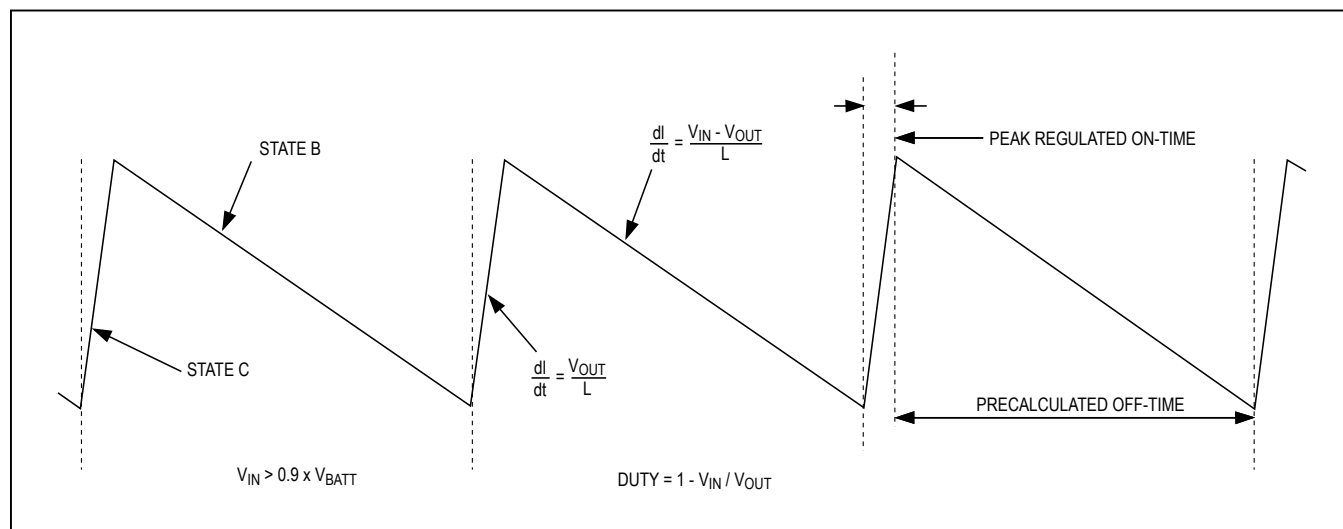


Figure 7. Step-Up Inductor-Current Waveform

based on the integrated error of the input current, charge current, and battery voltage. The error signal, determined by the lowest voltage clamp (LVC), sets the threshold for current-mode regulation. The following comparators are used for regulation:

- IMIN: The MAX1870A operates in discontinuous conduction if LVC is below 0.15V, and does not initiate another step-down on-time. In discontinuous step-up

conduction, the peak current is set by IMIN. The peak inductor current in discontinuous step-up mode:

$$I_{PK} > \frac{V_{IMIN}}{ACSI \times RS2}$$

where VIMIN is the IMIN comparator threshold, 0.15V, and ACSI is the charge current-sense amplifier gain, 18V/V.

- CCMP: CCMP compares the current-mode control point, LVC, to the inductor current. In step-down mode, the off-time (state A) is terminated when the inductor current falls below the current threshold set by LVC. In step-up mode, the on-time (state C) is terminated when the inductor current rises above the current threshold set by LVC.
- IMAX: The IMAX comparators provide a cycle-by-cycle inductor current limit. This circuit compares the inductor current (CSI in step-down mode or CSS in step-up mode) to the internally fixed cycle-by-cycle current limit. The current-sense voltage limit is 200mV. With $RS1_ = RS2 = 30m\Omega$, which corresponds to 6.7A. If the inductor current-sense voltage is greater than V_{IMAX} (200mV), a step-up on-time is terminated or a step-down on-time is not permitted.
- ZCMP: The ZCMP comparator detects when the inductor current crosses zero. If the ZCMP output goes high during a step-down off-time, the MAX1870A switches to the idle state (state D) to conserve power.

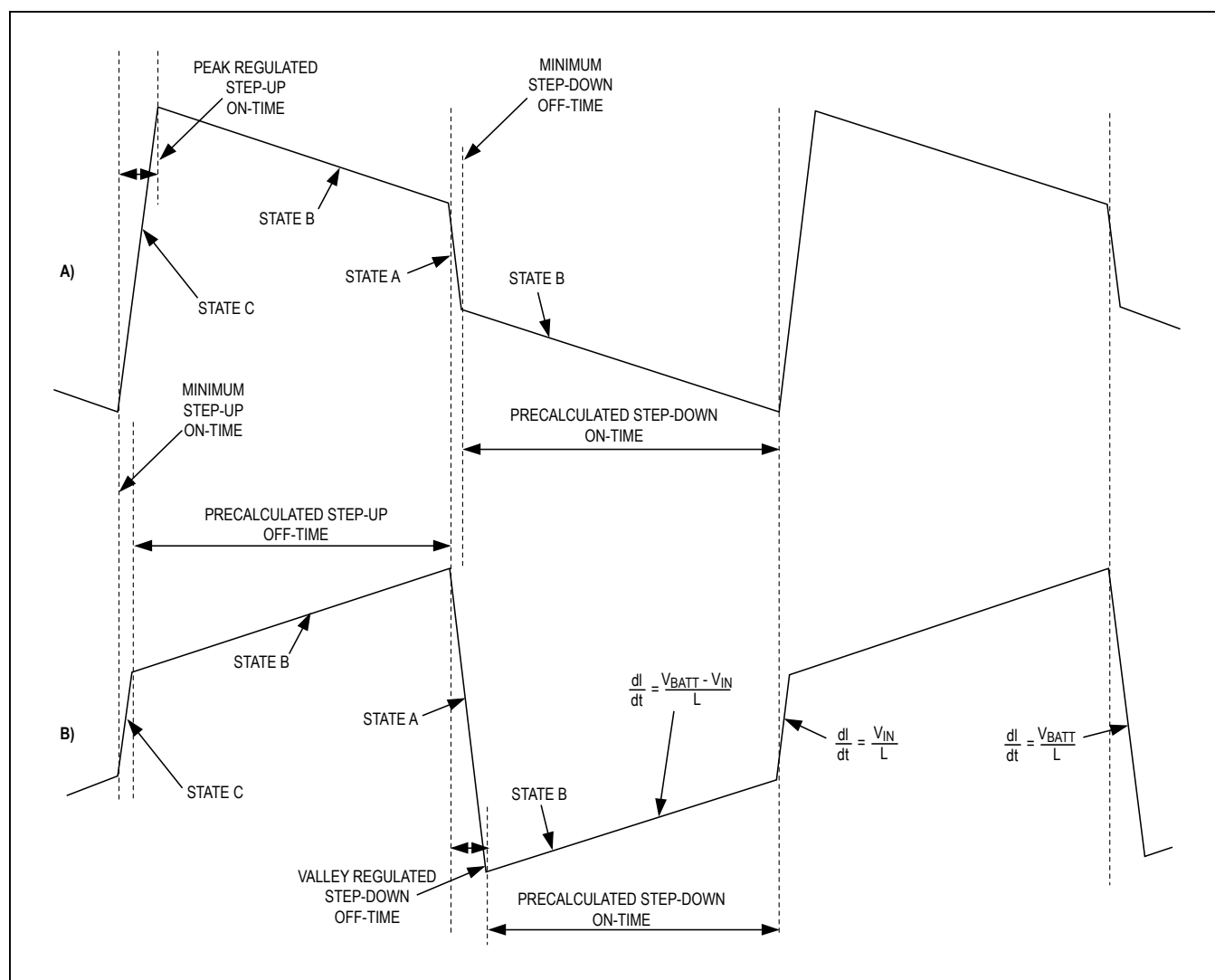


Figure 8. MAX1870A Step-Up/Step-Down Inductor-Current Waveform

Switching Frequency

The MAX1870A includes input and output-voltage feed-forward to maintain pseudo-fixed-frequency (400kHz) operation. The time in state B is set according to the input voltage, output voltage, and a time constant. In step-up/step-down mode the switching frequency is effectively cut in half to allow for both the step-up cycle and the step-down cycle. The switching frequency is typically between 350kHz and 405kHz for V_{IN} between 8V and 28V. See the [Typical Operating Characteristics](#).

Compensation

Each of the three regulation loops (the battery voltage, the charge current, and the input current limit) are compensated separately using the CCV, CCI, and CCS pins, respectively. Compensate the voltage regulation loop with a 10kΩ resistor in series with a 0.01μF capacitor from CCV to GND. Compensate the charge current loop and source current loop with 0.01μF capacitors from CCI to GND and from CCS to GND, respectively.

Voltage Loop Compensation

When regulating the charge voltage, the MAX1870A behaves as a current-mode step-down or step-up power supply. Since a current-mode controller regulates its output current as a function of the error signal, the duty-cycle modulator can be modeled as a GM stage ([Figure 9](#)). Results are similar in step-down, step-up, or step-up/down, with the exception of a load-dependent right-half-plane zero that occurs in step-up mode.

The required compensation network is a pole-zero pair formed with C_{CV} and R_{CV} . C_{CV} is chosen to be large enough that its impedance is relatively small compared to R_{CV} at frequencies near crossover. R_{CV} sets the gain of the error amplifier near crossover. R_{CV} and C_{OUT} determine the crossover frequency and, therefore, the closed-loop response of the system and the response time upon battery removal.

R_{ESR} is the equivalent series resistance (ESR) of the charger's output capacitor (C_{OUT}). R_L is the equivalent charger output load, $R_L = \Delta V_{BATT} / \Delta I_{CHG} = R_{BATT}$. The equivalent output impedance of the GMV amplifier, R_{OGMV} , is greater than 10MΩ. The voltage loop transconductance ($GMV = \Delta I_{CCV} / \Delta V_{BATT}$) scales inversely with the number of cells. $GMV = 0.1\mu A/mV$ for four cells, $0.133\mu A/mV$ for three cells, and $0.2\mu A/mV$ for two cells. The DC-DC converter's transconductance depends upon the charge current-sense resistor $RS2$:

$$GM_{PWM} = \frac{1}{A_{CSI} \times RS2}$$

where $A_{CSI} = 18$, and $RS2 = 30m\Omega$ in [Figure 1](#) and [2](#) so $GM_{PWM} = 1.85A/V$.

Use the following equation to calculate the loop transfer function (LTF):

$$LTF = GM_{PWM} \times \frac{R_{OGMV} \times (1 + sC_{CV} R_{CV})}{(1 + sC_{CV} \times R_{OGMV})} \times \frac{R_L}{(1 + sC_{OUT} \times R_L)} \times GMV \times (1 + sC_{OUT} \times R_{ESR})$$

The poles and zeros of the voltage-loop transfer function are listed from lowest frequency to highest frequency in [Table 3](#).

Near crossover, C_{CV} has much lower impedance than R_{OGMV} . Since C_{CV} is in parallel with R_{OGMV} , C_{CV} dominates the parallel impedance near crossover. Additionally, R_{CV} has a much higher impedance than C_{CV} and dominates the series combination of R_{CV} and C_{CV} , so:

$$\frac{R_{OGMV} \times (1 + sC_{CV} \times R_{CV})}{(1 + sC_{CV} \times R_{OGMV})} \cong R_{CV}, \text{ near crossover}$$

C_{OUT} also has a much lower impedance than R_L near crossover, so the parallel impedance is mostly capacitive and:

$$\frac{R_L}{(1 + sC_{OUT} \times R_L)} \cong \frac{1}{sC_{OUT}}$$

If R_{ESR} is small enough, its associated output zero has a negligible effect near crossover and the loop transfer function can be simplified as follows:

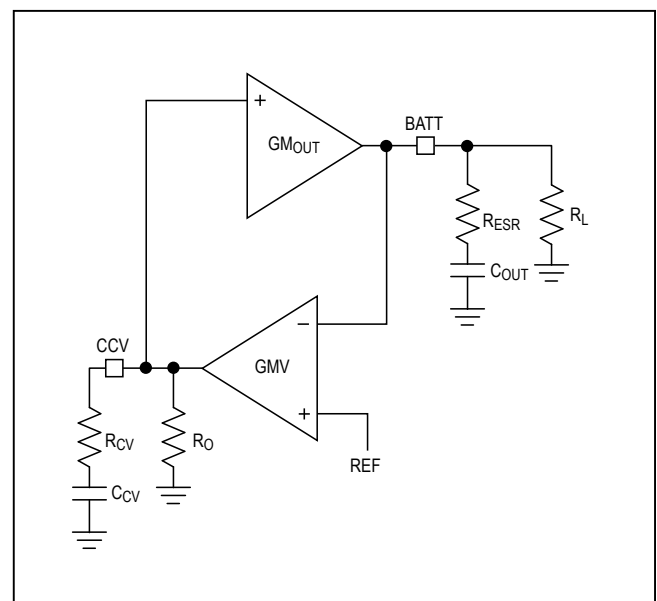


Figure 9. CCV Simplified Loop Diagram

$$LTF = GMPWM \times \frac{R_{CV}}{sC_{OUT}} G_{MV}$$

Setting the LTF = 1 to solve for the unity-gain frequency yields:

$$f_{CO_CV} = GMPWM \times G_{MV} \left(\frac{R_{CV}}{2\pi \times C_{OUT}} \right)$$

For stability, choose a crossover frequency lower than 1/10th of the switching frequency. The crossover frequency must also be below the RHP zero, calculated at maximum charge current, minimum input voltage, and maximum battery voltage.

Choosing a crossover frequency of 13kHz and solving for R_{CV} using the component values listed in [Figure 1](#) yields:

$$\begin{aligned} \text{MODE} &= V_{CC} \text{ (4 cells)} & G_{MV} &= 0.1\mu\text{A/mV} \\ C_{OUT} &= 22\mu\text{F} & GMPWM &= 1.85\text{A/V} \\ V_{BATT} &= 16.8\text{V} & f_{CO_CV} &= 13\text{kHz} \\ R_L &= 0.2\Omega & f_{OSC} &= 400\text{kHz} \end{aligned}$$

$$R_{CV} = \frac{2\pi \times C_{OUT} \times f_{CO_CV}}{G_{MV} \times GMPWM} = 10\text{k}\Omega$$

To ensure that the compensation zero adequately cancels the output pole, select $f_{Z_CV} \leq f_{P_OUT}$.

$$C_{CV} \geq (R_L / R_{CV}) \times C_{OUT}$$

$$C_{CV} \geq 440\text{pF}$$

[Figure 10](#) shows the Bode Plot of the voltage-loop frequency response using the values calculated above.

Charge-Current and Wall-Adapter-Current Loop Compensation

When the MAX1870A regulates the charge current or the wall adapter current, the system stability does not depend on the output capacitance. The simplified schematic in [Figure 11](#) describes the operation of the MAX1870A when the charge-current loop (CCI) is in control. The simplified schematic in [Figure 12](#) describes the operation of the MAX1870A when the source-current loop (CCS) is in control. Since the output capacitor's impedance has little

Table 3. Constant Voltage Loop Poles and Zeros

NO.	NAME	CALCULATION	DESCRIPTION
1	CCV Pole	$f_{P_CV} = \frac{1}{2\pi \times R_{OGMV} C_{CV}}$	Lowest Frequency Pole created by C_{CV} and G_{MV} 's finite output resistance. Since R_{OGMV} is very large ($R_{OGMV} > 10\text{M}\Omega$), this is a low-frequency pole.
2	CCV Zero	$f_{Z_CV} = \frac{1}{2\pi \times R_{CV} C_{CV}}$	Voltage-Loop Compensation Zero. If this zero is lower than the output pole, f_{P_OUT} , then the loop transfer function approximates a single-pole response near the crossover frequency. Choose C_{CV} to place this zero at least 1 decade below crossover to ensure adequate phase margin.
3	Output Pole	$f_{P_OUT} = \frac{1}{2\pi \times R_L C_{OUT}}$	Output Pole Formed with the Effective Load Resistance R_L and the Output Capacitance C_{OUT} . R_L influences the DC gain but does not affect the stability of the system or the crossover frequency.
4	Output Zero	$f_{Z_OUT} = \frac{1}{2\pi \times R_{ESR} C_{OUT}}$	Output ESR Zero. This zero can keep the loop from crossing unity gain if f_{Z_OUT} is less than the desired crossover frequency. Therefore, choose a capacitor with an ESR zero greater than the crossover frequency.
5	RHP Zero	$f_{RHPZ} = \frac{V_{IN}}{2\pi \times L I_L}$ $= \frac{V_{IN}^2}{2\pi \times L I_{OUT} V_{OUT}}$	Step-Up Mode RHP Zero. This zero occurs because of the initial opposing response of a step-up converter. Efforts to increase the inductor current result in an immediate <i>decrease</i> in current delivered, although eventually result in an increase in current delivered. This zero is dependent on charge current and may cause the system to go unstable at high currents when in step-up mode. A right-half-plane zero is detrimental to both phase and gain. To ensure stability under maximum load in step-up mode, the crossover frequency must be lower than half of f_{RHPZ} .

effect on the response of the current loop, only a single pole is required to compensate this loop. ACS_I and ACS_S are the internal gains of the current-sense amplifiers. $RS2$ is the charge current-sense resistor. $RS1a$ and $RS1b$ are the adapter current-sense resistors. $ROGM_I$ and $ROGM_S$ are the equivalent output impedance of the GMI and GMS amplifiers, which are greater than $10M\Omega$. GMI is the charge-current amplifier transconductance ($2.4\mu A/mV$). GMS is the adapter-current amplifier transconductance ($1.7\mu A/mV$). GM_{PWM} is the DC-DC converter transconductance ($1.85A/V$).

Use the following equation to calculate the loop transfer function:

$$LTF = GM_{PWM} \times ACS_ \times RS_ \times GM_ \frac{ROGM_}{1 + sROGM_ \times CC_}$$

which describes a single-pole system. Since $GM_{PWM} =$

$$\frac{1}{ACS_ \times RS_}$$

the loop-transfer function simplifies to:

$$LTF = GM_ \frac{ROGM_}{1 + sROGM_ \times CC_}$$

Use the following equations to calculate the crossover frequency:

$$f_{CO_CI} = \frac{GMI}{2\pi C_{CI}}, f_{CO_CS} = \frac{GMS}{2\pi C_{CS}}$$

For stability, choose a crossover frequency lower than

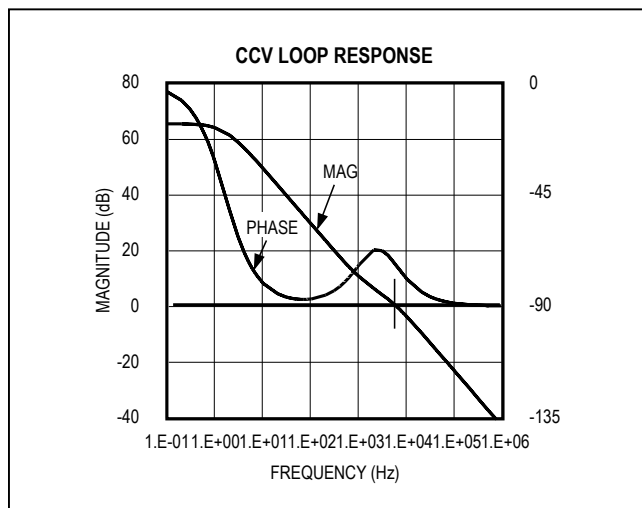


Figure 10. CCV Loop Response

1/10th of the switching frequency and lower than half of the RHP zero.

$$C_{CI} = 10 GMI / (2\pi \times f_{OSC}), C_{CS} = 10 GMS / (2\pi \times f_{OSC})$$

$$f_{RHPZ_WorstCase} = \frac{V_{IN_MIN}}{2\pi \times L I_L} = \frac{V_{IN_MIN}^2}{2\pi L I_{OUTMAX} V_{OUTMAX}}$$

This zero is inversely proportional to charge current and might cause the system to go unstable at high currents when in step-up mode. A right-half-plane zero is detrimental to both phase and gain. To also ensure stability under maximum load in step-up mode, the CCI crossover frequency must also be lower than f_{RHPZ} . The right-half-plane zero does not affect CCS .

Choosing a crossover frequency of 30kHz and using the component values listed in Figure 1 yields C_{CI} and $C_{CS} > 10nF$. Values for C_{CI} / C_{CS} greater than ten times the minimum value may slow down the current loop response excessively. Figure 13 shows the Bode Plot of the input-current frequency response using the values calculated above.

MOSFET Drivers

DHI and DBST are optimized for driving moderately-sized power MOSFETs. Use low-inductance and low-resistance traces from driver outputs to MOSFET gates.

DHI typically sources 1.6A and sinks 0.8A to or from the gate of the p-channel MOSFET. DHI swings from VHP to VHN. VHN is a negative LDO that regulates with respect to VHP to provide high-side gate drive. Connect VHP to DCIN. Bypass VHN with a $1\mu F$ capacitor to VHP.

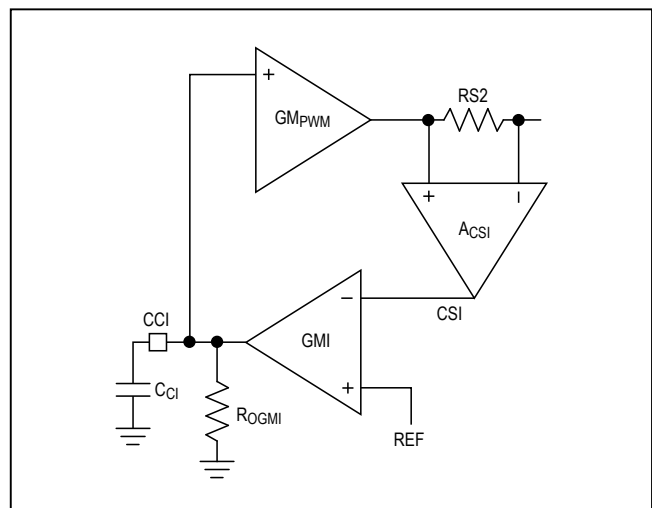


Figure 11. CCI Simplified Loop Diagram

LDO provides a 5.4V supply derived from DCIN and delivers over 10mA. The n-channel MOSFET driver DBST is powered by DLOV and can source 2.5A and sink 5A. Since LDO provides power to the internal analog circuitry, use an RC filter from LDO to DLOV as shown in [Figure 1](#) to minimize noise at LDO. LDO also supplies the 4.096V reference (REF) and most of the internal control circuitry. Bypass LDO with a 1μF or greater capacitor to GND.

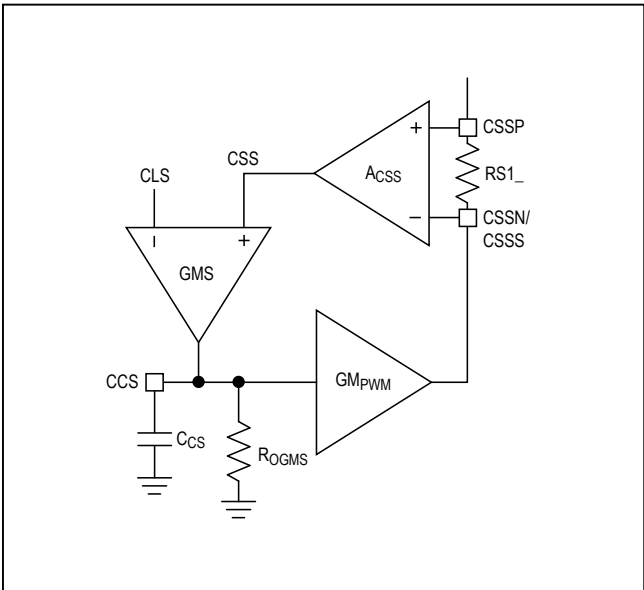


Figure 12. CCS Simplified Loop Diagram

Applications Information

Component Selection

[Table 4](#) lists the recommended components and refers to the circuit of [Figure 1](#). The following sections describe how to select these components.

MOSFETs

The MAX1870A requires one p-channel MOSFET and one n-channel MOSFET. Component substitutions are permissible as long as the on-resistance and gate charge are equal or lower and the voltage, current, and power-dissipation ratings are high enough. If using a lower-power application, scale down the MOSFETs with lower gate charge and the MOSFET's on-resistance can be scaled up. For example, in a system designed to deliver half as much current, MOSFETs selected with twice the on-resistance and half as much gate charge ensure equal or better efficiency, and reduce size and cost. If resistive losses dominate, it can be possible to reduce the gate charge at the cost of on-resistance and still achieve a similar efficiency.

Make sure that the linear regulators can drive the selected MOSFETs. The average current required to drive a given MOSFET is:

$$I_{LDO} = Q_{gM2} \times f_{switch}$$

$$I_{VHN} = Q_{gM1} \times f_{switch}$$

where f_{switch} is 400kHz (typ).

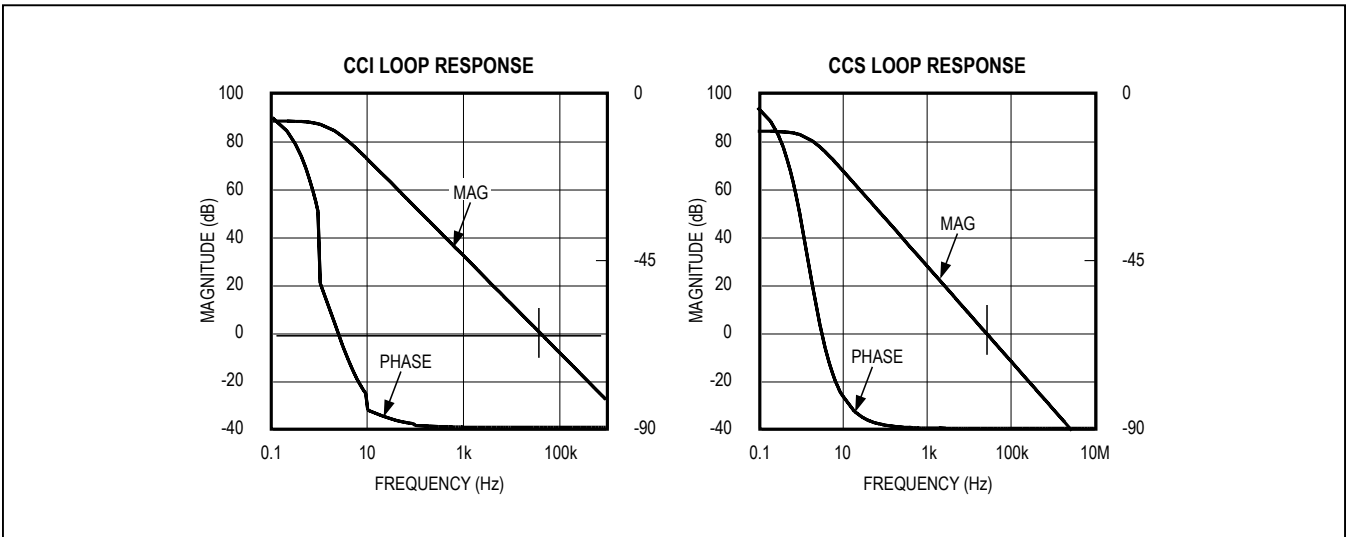


Figure 13. CCI and CCS Loop Response

MOSFET Power Dissipation

Table 5 shows the resistive losses and switching losses in each of the MOSFETs during either step-up or step-down operation. Table 5 provides a first-order estimate, but does not consider second-order effects such as ripple current or nonlinear gate drive.

For typical applications where $V_{BATT} / 2 < V_{IN} < 2 \times V_{BATT}$, the resistive losses are primarily dissipated in M1 since M2 operates at a lower duty cycle. Switching losses are dissipated in M1 when in step-down mode and in M2 when in step-up mode. Ratio the MOSFETs so that resistive losses roughly equal switching losses when at maximum load and typical input/output conditions. The resistive loss equations are a good approximation in hybrid mode (V_{IN} near V_{BATT}). Both M1 and M2 switching losses apply in hybrid mode.

Switching losses can become a heat problem when the maximum AC-adaptor voltage is applied in step-down operation or minimum AC-adaptor voltage is applied with a maximum battery voltage. This behavior occurs because of the squared term in the $CV^2 f$ switching-loss equation. Table 5 provides only an estimate and is not a substitute for breadboard evaluation.

Inductor Selection

Select the inductor to minimize power dissipation in the MOSFETs, inductor, and sense resistors. To optimize resistive losses and RMS inductor current, set the LIR (inductor current ripple) to 0.3. Because the maximum resistive power loss occurs at the step-up boundary of

hybrid mode, select LIR for operating in this mode. Select the inductance according to the following equation:

$$L = \frac{2 \times V_{IN} \times t_{min}}{LIR I_{CHG}}$$

Larger inductance values can be used; however, they contribute extra resistance that can reduce efficiency. Smaller inductance values increase RMS currents and can also reduce efficiency.

Saturation-Current Rating

The inductor must have a saturation current rating high enough so it does not saturate at full charge, maximum output voltage, and minimum input voltage. In step-up operation, the inductor carries a higher current than in step-down operation with the same load. Calculate the inductor saturation current rating by the following equation:

$$I_{SAT} \geq \frac{V_{OUT_MAX} \times I_{CHG_MAX}}{V_{IN_MIN}} + \frac{T \times V_{IN_MIN} \times \left(1 - \frac{V_{IN_MIN}}{V_{OUT_MAX}}\right)}{2 \times L}$$

Input-Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or

Table 4. Component List

DESIGNATION	PART	SPECIFICATIONS
INDUCTORS		
L1	Sumida CDRH104R-100 Sumida CDRH104R-7R0 Sumida CDRH104R-5R2 Sumida CDRH104R-3R8	10μH, 4.4A, 35mΩ power inductor 7μH, 4.8A, 27mΩ power inductor 5.2μH, 5.5A, 22mΩ power inductor 3.8μH, 6A, 13mΩ power inductor
P-CHANNEL MOSFETs		
M1	Siliconix Si4435DY Fairchild FDC602P Fairchild FDS4435A Fairchild FDW256P	P-FET 35mΩ, $Q_G = 17nC$, $V_{DSMAX} = 30V$, 8-pin SO P-FET 35mΩ, $Q_G = 14nC$, $V_{DSMAX} = 20V$, 6-pin SuperSOT P-FET 25mΩ, $Q_G = 21nC$, $V_{DSMAX} = 30V$, 8-pin SO P-FET 20mΩ, $Q_G = 28nC$, $V_{DSMAX} = 30V$, 8-pin TSSOP
N/P-CHANNEL MOSFET PAIRS		
M1/M2	Fairchild FDW2520C (8-pin TSSOP)	N-FET 18mΩ, $Q_G = 14nC$, $V_{DSMAX} = 20V$, P-FET 35mΩ, $Q_G = 14nC$, $V_{DSMAX} = 20V$
N-CHANNEL MOSFETs		
M2	IRF7811W	N-FET, 9mΩ, $Q_G = 18nC$, $V_{DSMAX} = 30V$, 8-pin SO

Table 5. MOSFET Resistive and Switching Losses

DESIGNATION	STEP-DOWN MODE	STEP-UP MODE
	DC LOSSES	
M1	$\left(\frac{V_{BATT}}{V_{DCIN}}\right) \times I_{CHG}^2 \times R_{DS(ON)}$	$\left(\frac{V_{BATT}}{V_{DCIN}} \times I_{CHG}\right)^2 \times R_{DS(ON)}$
D4	$\left(1 - \frac{V_{BATT}}{V_{DCIN}}\right) \times I_{CHG} \times V_{Diode}$	0
M2	0	$\left(1 - \frac{V_{DCIN}}{V_{BATT}}\right) \times \left(\frac{V_{BATT}}{V_{DCIN}} \times I_{CHG}\right)^2 \times R_{DS(ON)}$
D3	$I_{CHG} \times V_{DIODE}$	$I_{CHG} \times V_{DIODE}$
SWITCHING LOSSES		
M1	$\frac{V_{DCIN(MAX)}^2 \times C_{LX} \times f_{SW} \times I_{CHG}}{I_{GATE}}$	0
D4	0	0
M2	0	$\frac{V_{BATT(MAX)}^3 \times C_{LX} \times f_{SW} \times I_{CHG}}{I_{GATE} \times V_{DCIN(MAX)}}$
D3	0	0

Note: C_{LX} is the total parasitic capacitance at the drain terminals of M1 and M2. I_{GATE} is the peak gate-drive source/sink current of M1 or M2.

OS-CON) are preferred due to their resilience to power-up surge currents.

The input capacitors should be sized so that the temperature rise due to ripple current in continuous conduction does not exceed approximately 10°C. Choose a capacitor with a ripple current rating higher than $0.5 \times I_{CHG}$.

Output-Capacitor Selection

The output capacitor absorbs the inductor ripple current in step-down mode, or a peak-to-peak ripple current equal to the inductor current when in step-up or hybrid mode. As such, both capacitance and ESR are important parameters in specifying the output capacitor. The actual amplitude of the ripple is the combination of the two. Ceramic devices are preferable because of their resilience to surge currents. The worst-case output ripple occurs during hybrid mode when the input voltage is at its minimum. See the [Typical Operating Characteristics](#).

Select a capacitor that can handle $0.5 \times I_{CHG} \times V_{BATT} / V_{IN}$ while keeping the rise in capacitor temperature less than 10°C. Also, select the output capacitor to tolerate the surge current delivered from the battery when it is initially plugged into the charger.

Battery-Removal Response

Upon battery removal, the MAX1870A continues to regulate a constant inductor current until the battery voltage, V_{BATT} , exceeds the regulation threshold. The MAX1870A's response time depends on the bandwidth of the CCV loop, f_{CO} (see the [Voltage Loop Compensation](#) section). For applications where battery overshoot is critical, either increase C_{OUT} or increase f_{CO} by increasing R_{CV} . See [Battery Insertion and Removal](#) in the [Typical Operating Characteristics](#).

System Load Transient

The MAX1870A battery charger features a very fast response time to system load transients. Since the input current loop is configured as a single-pole system, the MAX1870A responds quickly to system load transients (see the [System Load-Transient Response](#) graph in the [Typical Operating Characteristics](#)). This reduces the risk of tripping the overcurrent threshold of the wall adapter and minimizes requirements for adapter oversizing.

Layout and Bypassing

Bypass DCIN with a 1 μ F to ground (Figure 1). Optional diodes D1 and D2 protect the MAX1870A when the DC power-source input is reversed. A signal diode for D1 is adequate because DCIN only powers the LDO and the internal reference. Good PC board layout is required to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions—preferably, a pencil sketch showing the placement of the power-switching components and high-current routing. Refer to the PC board layout in the MAX1870A evaluation kit for examples. A ground plane is essential for optimum performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current connections (PGND, DHI, VHP, VHN, BLKP, and DLOV), the bottom layer for quiet connections (CSSP, CSSN, CSSS, CSIP, CSIN, REF, CCV, CCI, CCS, DCIN, LDO and GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

- 1) Place the high-power connections first, with their grounds adjacent:
 - Minimize the current-sense resistor trace lengths, and ensure accurate current sensing with Kelvin connections. Use independent branches for CSSP, CSSS, CSSN, CSIP, and CSIN.
 - Minimize ground trace lengths in the high-current paths.
 - Minimize other trace lengths in the high-current paths.
 - Use > 5mm wide traces for high-current paths.

Ideally, surface-mount power components are flush against one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper, so they do not go through vias. Other high-current paths should also be minimized, but focus primarily on short ground and current-sense connections to eliminate about 90% of all PC board layout problems.

- 2) Place the IC and signal components. Keep the main switching nodes (inductor connections) away from sensitive analog components (current-sense traces and REF capacitor). **Important: the IC must be no further than 10mm from the current-sense resistors.** Keep the gate-drive traces (DHI and DBST) shorter than 20mm, and route them away from the current-sense lines and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. Bypass CSSP, CSSN, CSIN, and CSIP to analog GND to reduce switching noise and maintain input-current and charger-current accuracy. Place the current-sense input filter capacitors under the part, connected directly to GND.
- 3) Use a single-point star ground placed directly below the part. Connect the input ground trace, power ground (subground plane), and normal ground to this node.

Figure 14 shows a partial layout of the power path and components. Refer to the EV kit data sheet for more information.

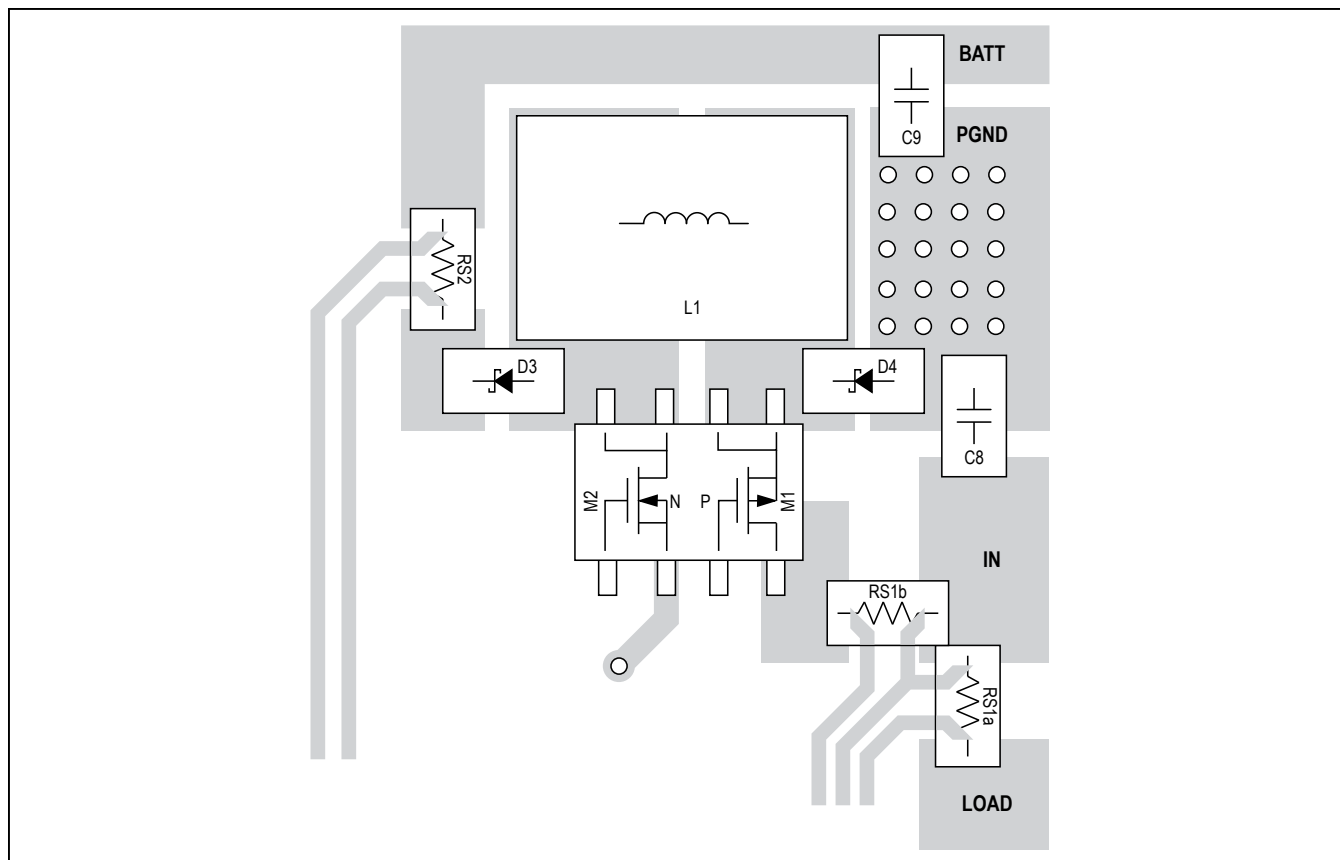


Figure 14. Recommended Layout for the MAX1870A

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1870AETJ	-40°C to +85°C	32 Thin QFN
MAX1870AETJ+	-40°C to +85°C	32 Thin QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

TRANSISTOR COUNT: 6484

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	5/15	Updated <i>Benefits and Features</i> section	1
2	8/15	Updated Figures 1 and 2	14, 15

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