Absolute Maximum Ratings (Note 1)

V_{IN} to PGND .....-0.3V to +65V
EN/UVLO to SGND .....-0.3V to +65V
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
BST to PGND .....-0.3V to +70V
BST to LX.....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +65V
FB, CF, $\overline{RESET}$, SS, MODE, SYNC, RT to SGND .....-0.3V to +6.5V
V_{CC} to SGND.....-0.3V to +6.5V
SGND to PGND.....-0.3V to +0.3V
LX Total RMS Current .....±5.6A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C) (multilayer board)
TQFN (derate 33.3mW/°C above T_A = +70°C).....2666.7mW
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2055+4
Outline Number	**21-0140**
Land Pattern Number	**90-0009**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	30°C/W
Junction to Case (θ_{JC})	2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2kΩ (500kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{MODE} = V_{SYNC} = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		2.8	4.5	µA
Input Quiescent Current	I_{Q_PFM}	V_{FB} = 1V, MODE = RT= open		118		µA
		V_{FB} = 1V, MODE = open		162		
	I_{Q_DCM}	DCM mode, V_{LX} = 0.1V		1.16	1.8	mA
	I_{Q_PWM}	Normal switching mode, f_{SW} = 500kHz, V_{FB} = 0.8V		9.5		

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2kΩ (500kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{MODE} = V_{SYNC} = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.111	
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25ºC	-50	0	+50	nA
LDO						
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, I_{VCC} = 1mA	4.75	5	5.25	V
		1mA ≤ I_{VCC} ≤ 25mA				
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6V	26.5	54	100	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 20mA	4.2			V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.05	4.2	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.65	3.8	3.9	
POWER MOSFET AND BST DRIVER						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A		165	325	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A		80	150	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = V_{IN} - 1V, V_{LX} = V_{PGND} + 1V, T_A = +25ºC	-2		+2	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}	MODE = SGND or MODE = V_{CC}	0.89	0.9	0.91	V
		MODE = open	0.89	0.915	0.936	
FB Input Bias Current	I_{FB}	0 < V_{FB} < 1V, T_A = +25ºC	-50		+50	nA
MODE						
MODE Threshold	V_{M-DCM}	MODE = V_{CC} (DCM mode)	V_{CC} - 1.6			V
	V_{M-PFM}	MODE = open (PFM mode)		V_{CC}/2		
	V_{M-PWM}	MODE = GND (PWM mode)			1.4	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		4.4	5.1	5.85	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		4.9	5.7	6.7	A
Valley Current-Limit Threshold	$I_{SINK-LIMIT}$	MODE = open or MODE = V_{CC}	-0.16	0	+0.16	A
		MODE = GND		-1.8		
PFM Current-Limit Threshold	I_{PFM}	MODE = open	0.6	0.75	0.9	A

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2kΩ (500kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = V_{MODE} = V_{SYNC} = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

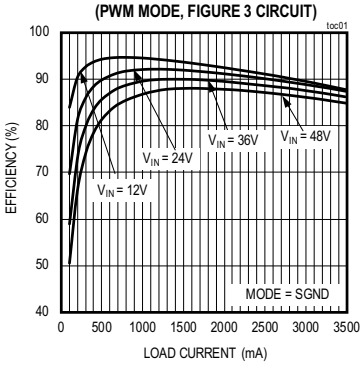
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RT AND SYNC						
Switching Frequency	f_{SW}	R_{RT} = 210kΩ	90	100	110	kHz
		R_{RT} = 102kΩ	180	200	220	
		R_{RT} = 40.2kΩ	475	500	525	
		R_{RT} = 8.06kΩ	1950	2200	2450	
		R_{RT} = OPEN	460	500	540	
SYNC Frequency Capture Range		f_{SW} set bt R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$		0.56	0.58	0.6	V
HICCUP Timeout		(Note 3)		32768		Cycles
Minimum On-Time	t_{ON-MIN}	MAX17504			135	ns
		MAX17504S		55	80	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		160	ns
LX Dead Time				5		ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 1mA			0.4	V
$\overline{RESET}$ Output Leakage Current		T_A = T_J = +25ºC, $V_{\overline{RESET}}$ = 5.5V	-0.1		+0.1	µA
V_{OUT} Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94	%
V_{OUT} Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.2	%
$\overline{RESET}$ Deassertion Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		165		ºC
Thermal Shutdown Hysteresis				10		ºC

Note 2: All limits are 100% tested at +25°C. Limits over temperature are guaranteed by design.
Note 3: See the *Overcurrent Protection/HICCUP Mode* section for more details.

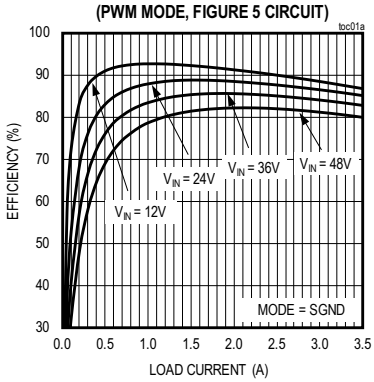
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

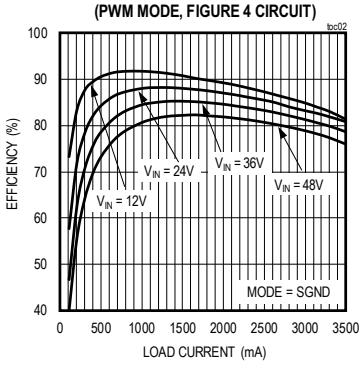
MAX17504 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, FIGURE 3 CIRCUIT)



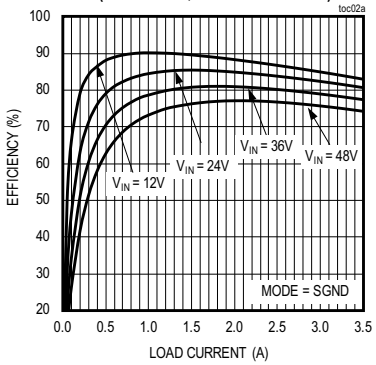
MAX17504S 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, FIGURE 5 CIRCUIT)



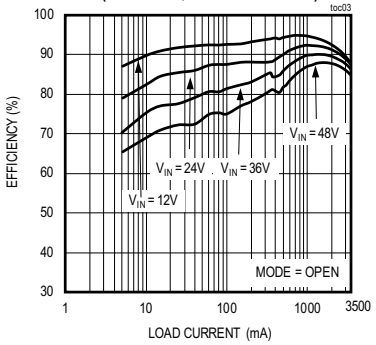
MAX17504 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, FIGURE 4 CIRCUIT)



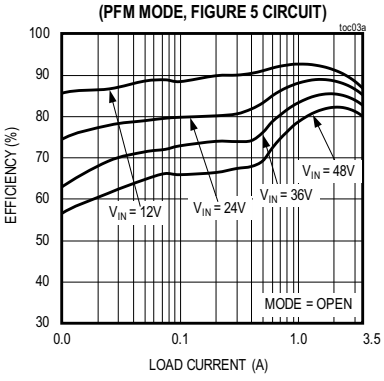
MAX17504S 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PWM MODE, FIGURE 6 CIRCUIT)



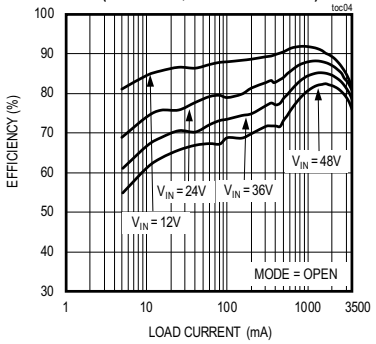
MAX17504 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, FIGURE 3 CIRCUIT)



MAX17504S 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, FIGURE 5 CIRCUIT)



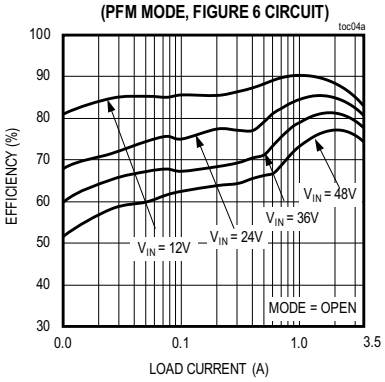
MAX17504 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, FIGURE 4 CIRCUIT)



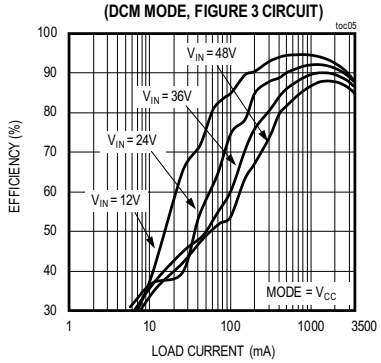
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

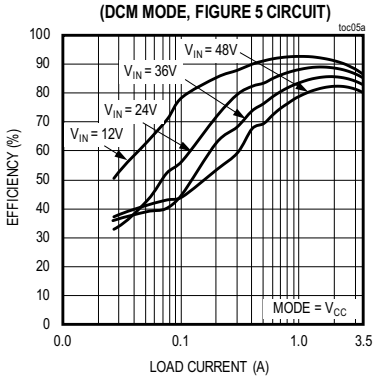
MAX17504S 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (PFM MODE, FIGURE 6 CIRCUIT)



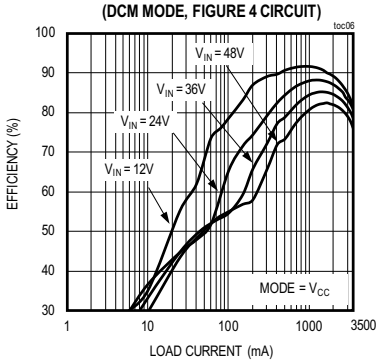
MAX17504 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, FIGURE 3 CIRCUIT)



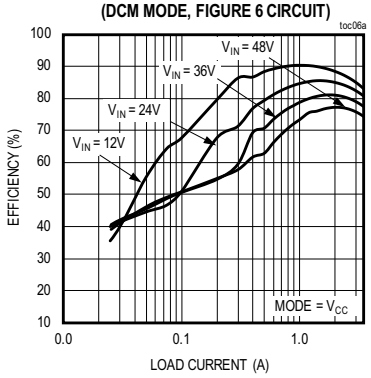
MAX17504S 5V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, FIGURE 5 CIRCUIT)



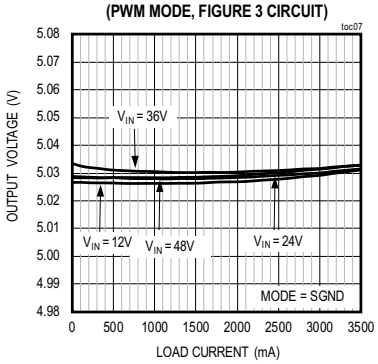
MAX17504 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, FIGURE 4 CIRCUIT)



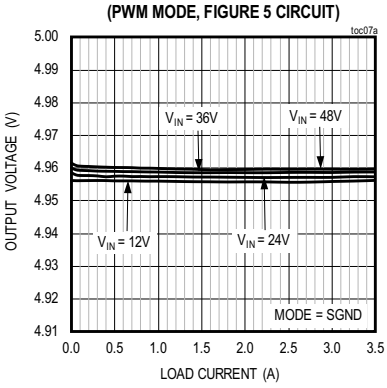
MAX17504S 3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT (DCM MODE, FIGURE 6 CIRCUIT)



MAX17504 5V OUTPUT LOAD AND LINE REGULATION (PWM MODE, FIGURE 3 CIRCUIT)



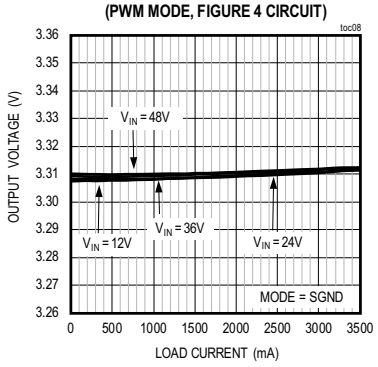
MAX17504S 5V OUTPUT LOAD AND LINE REGULATION (PWM MODE, FIGURE 5 CIRCUIT)



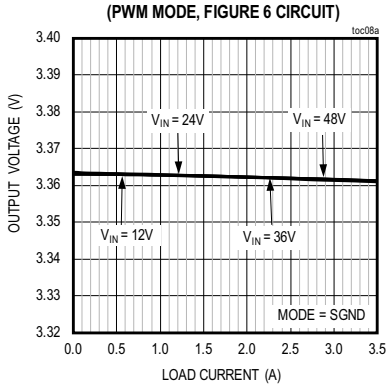
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

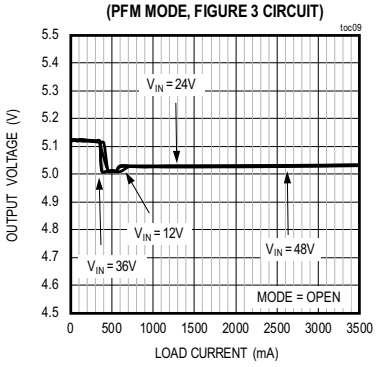
MAX17504 3.3V OUTPUT LOAD AND LINE REGULATION (PWM MODE, FIGURE 4 CIRCUIT)



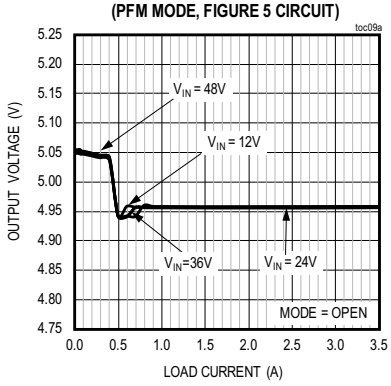
MAX17504S 3.3V OUTPUT LOAD AND LINE REGULATION (PWM MODE, FIGURE 6 CIRCUIT)



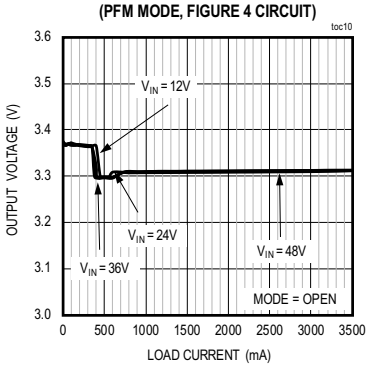
MAX17504 5V OUTPUT LOAD AND LINE REGULATION (PFM MODE, FIGURE 3 CIRCUIT)



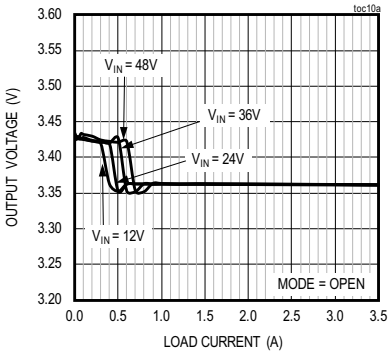
MAX17504S 5V OUTPUT LOAD AND LINE REGULATION (PFM MODE, FIGURE 5 CIRCUIT)



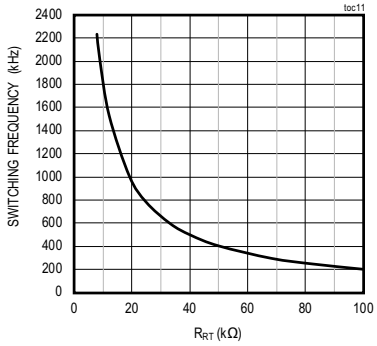
MAX17504 3.3V OUTPUT LOAD AND LINE REGULATION (PFM MODE, FIGURE 4 CIRCUIT)



MAX17504S 3.3V OUTPUT LOAD AND LINE REGULATION (PFM MODE, FIGURE 6 CIRCUIT)



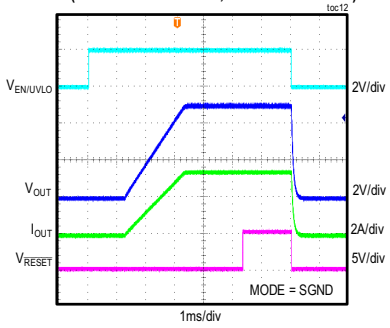
SWITCHING FREQUENCY vs. RT RESISTANCE



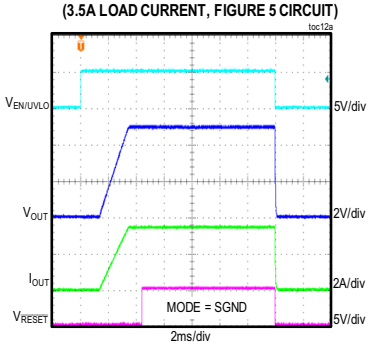
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

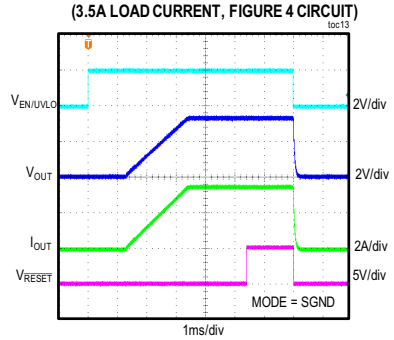
MAX17504 5V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (3.5A LOAD CURRENT, FIGURE 3 CIRCUIT)



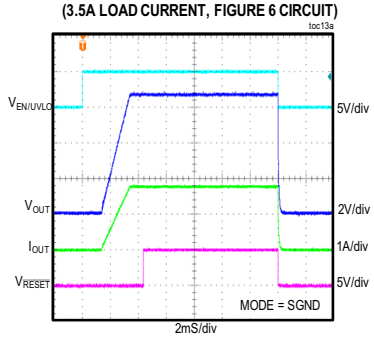
MAX17504S 5V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (3.5A LOAD CURRENT, FIGURE 5 CIRCUIT)



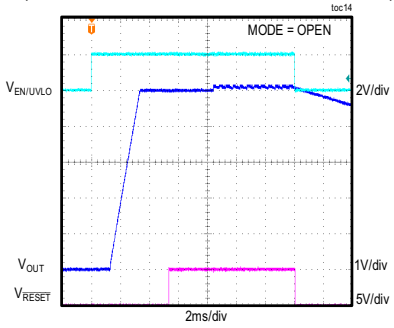
MAX17504 3.3V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO, (3.5A LOAD CURRENT, FIGURE 4 CIRCUIT)



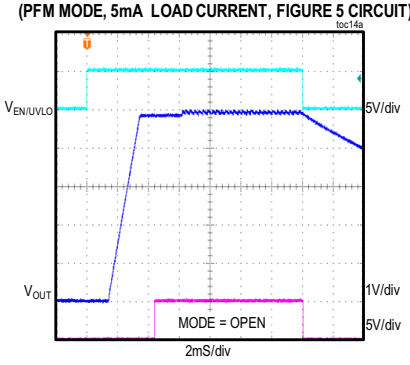
MAX17504S 3.3V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (3.5A LOAD CURRENT, FIGURE 6 CIRCUIT)



MAX17504 5V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (PFM MODE, 5mA LOAD CURRENT, FIGURE 3 CIRCUIT)



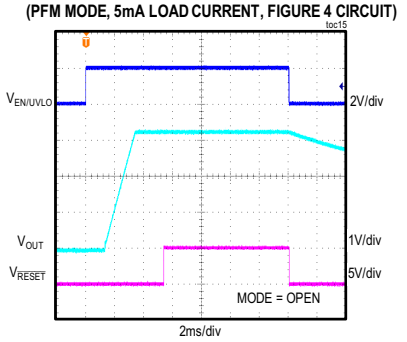
MAX17504S 5V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (PFM MODE, 5mA LOAD CURRENT, FIGURE 5 CIRCUIT)



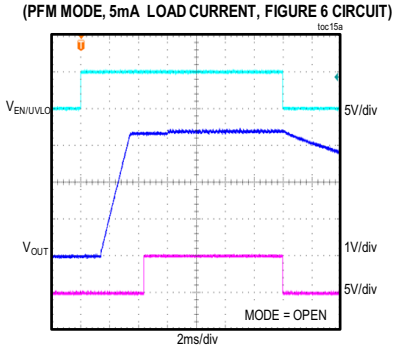
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

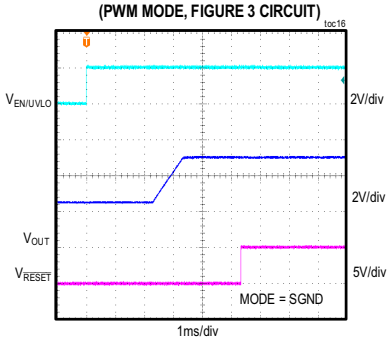
MAX17504 3.3V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (PFM MODE, 5mA LOAD CURRENT, FIGURE 4 CIRCUIT)



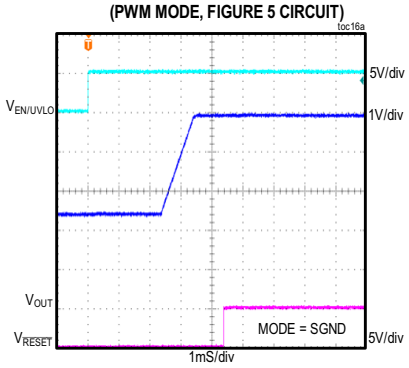
MAX17504S 3.3V OUTPUT SOFT-START/SHUTDOWN FROM EN/UVLO (PFM MODE, 5mA LOAD CURRENT, FIGURE 6 CIRCUIT)



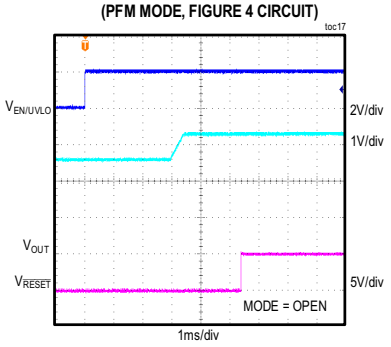
MAX17504 5V OUTPUT SOFT-START WITH 2.5V PREBIAS (PWM MODE, FIGURE 3 CIRCUIT)



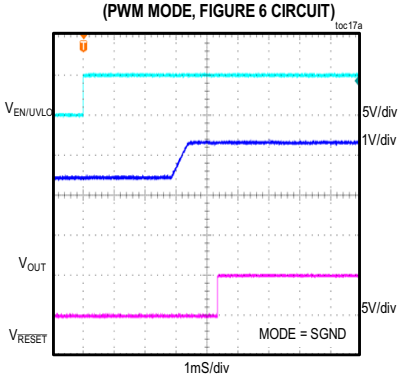
MAX17504S 5V OUTPUT SOFT-START WITH 2.5V PREBIAS (PWM MODE, FIGURE 5 CIRCUIT)



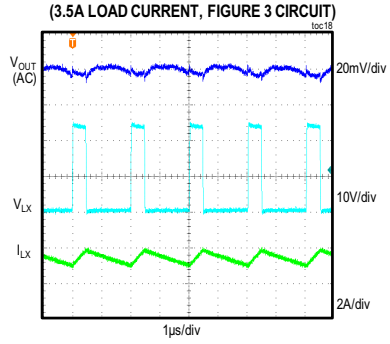
MAX17504 3.3V OUTPUT SOFT-START WITH 2.5V PREBIAS (PFM MODE, FIGURE 4 CIRCUIT)



MAX17504S 3.3V OUTPUT SOFT-START WITH 2.5V PREBIAS (PWM MODE, FIGURE 6 CIRCUIT)



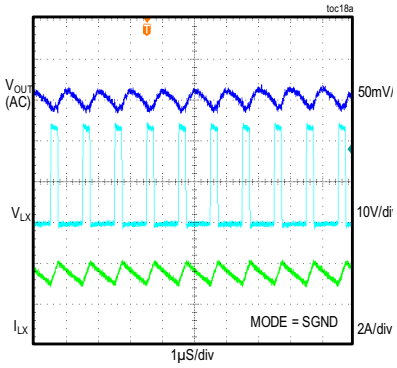
MAX17504 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (3.5A LOAD CURRENT, FIGURE 3 CIRCUIT)



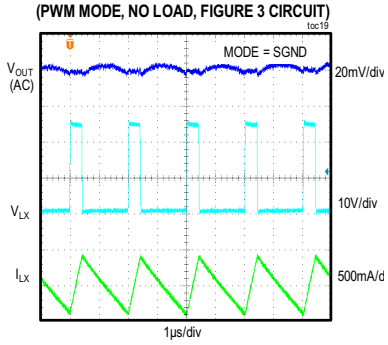
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

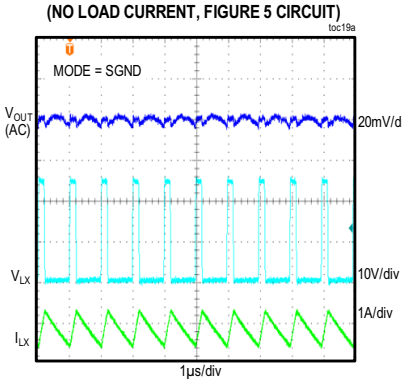
MAX17504S 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (3.5A LOAD CURRENT, FIGURE 5 CIRCUIT)



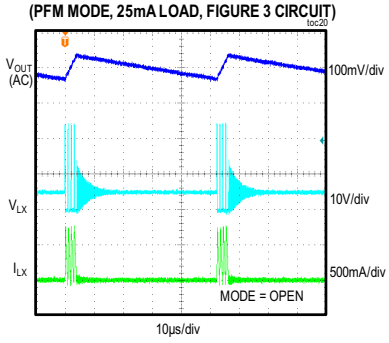
MAX17504 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (PWM MODE, NO LOAD, FIGURE 3 CIRCUIT)



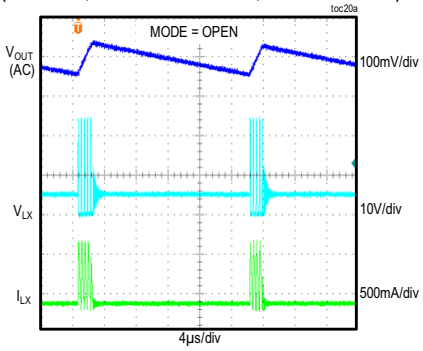
MAX17504S 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (NO LOAD CURRENT, FIGURE 5 CIRCUIT)



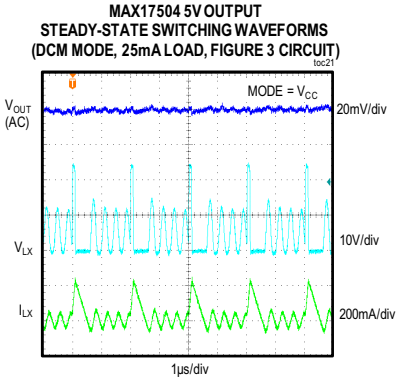
MAX17504 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (PFM MODE, 25mA LOAD, FIGURE 3 CIRCUIT)



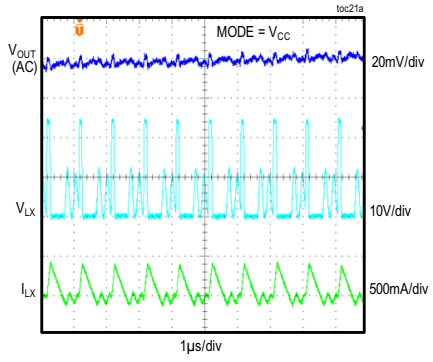
MAX17504S 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (PFM MODE, 25mA LOAD CURRENT, FIGURE 5 CIRCUIT)



MAX17504 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (DCM MODE, 25mA LOAD, FIGURE 3 CIRCUIT)



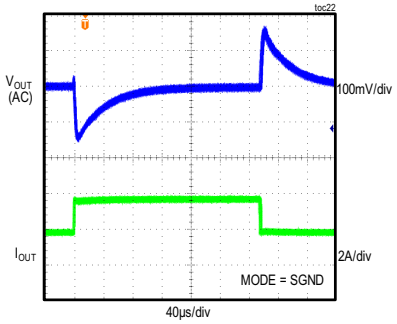
MAX17504S 5V OUTPUT STEADY-STATE SWITCHING WAVEFORMS (DCM MODE, 150mA LOAD CURRENT, FIGURE 5 CIRCUIT)



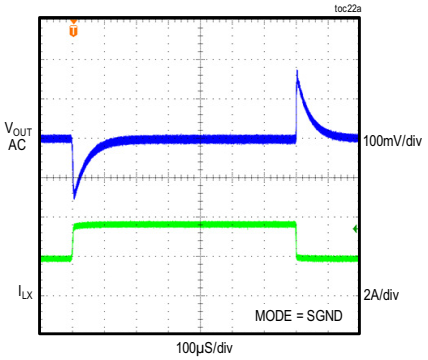
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

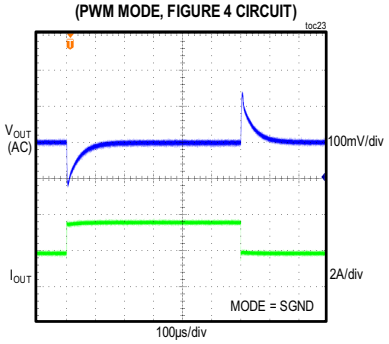
MAX17504 5V OUTPUT LOAD CURRENT STEPPED FROM 1.7`5A TO 3.5A (PWM MODE, FIGURE 3 CIRCUIT)



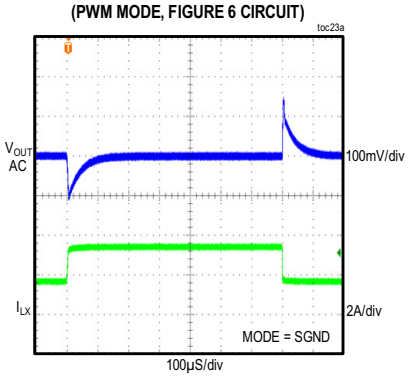
MAX17504S 5V OUTPUT LOAD CURRENT STEPPED FROM 1.75A TO 3.5A (PWM MODE, FIGURE 5 CIRCUIT)



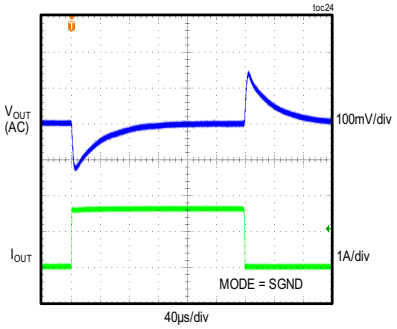
MAX17504 3.3V OUTPUT LOAD CURRENT STEPPED FROM 1.75A TO 3.5A (PWM MODE, FIGURE 4 CIRCUIT)



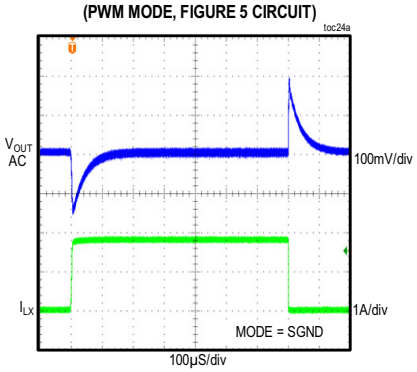
MAX17504S 3.3V OUTPUT LOAD CURRENT STEPPED FROM 1.75A TO 3.5A (PWM MODE, FIGURE 6 CIRCUIT)



MAX17504 5V OUTPUT LOAD CURRENT STEPPED FROM NO LOAD TO 1.75A (PWM MODE, FIGURE 3 CIRCUIT)



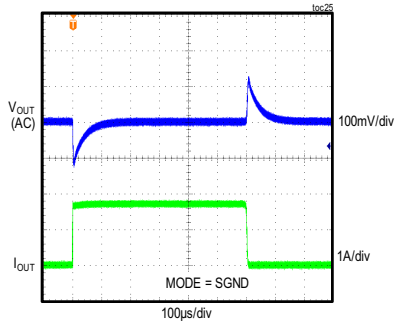
MAX17504S 5V OUTPUT LOAD CURRENT STEPPED FROM NO LOAD TO 1.75A (PWM MODE, FIGURE 5 CIRCUIT)



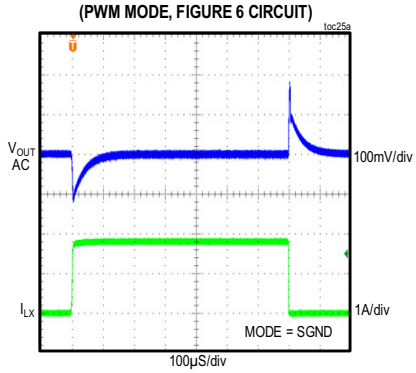
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

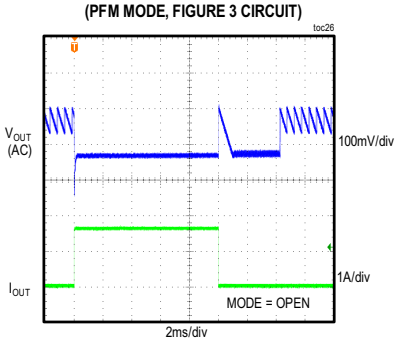
MAX17504 3.3V OUTPUT LOAD CURRENT STEPPED FROM NO LOAD TO 1.75A (PWM MODE, FIGURE 4 CIRCUIT)



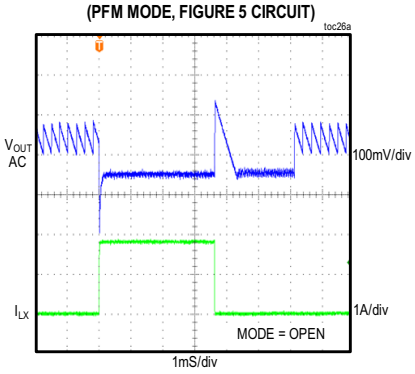
MAX17504S 3.3V OUTPUT LOAD CURRENT STEPPED FROM NO LOAD TO 1.75A (PWM MODE, FIGURE 6 CIRCUIT)



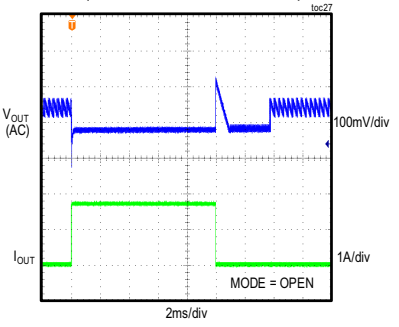
MAX17504 5V OUTPUT LOAD CURRENT STEPPED FROM 5mA TO 1.75A (PFM MODE, FIGURE 3 CIRCUIT)



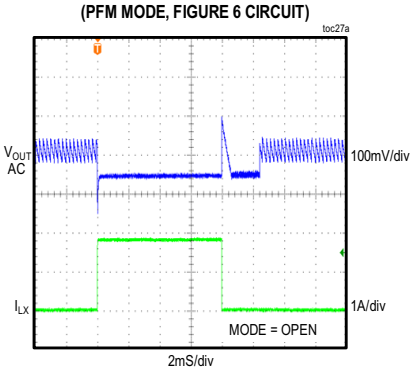
MAX17504S 5V OUTPUT LOAD CURRENT STEPPED FROM 5MA TO 1.75A (PFM MODE, FIGURE 5 CIRCUIT)



MAX17504 3.3V OUTPUT LOAD CURRENT STEPPED FROM 5mA TO 1.75A (PFM MODE, FIGURE 4 CIRCUIT)



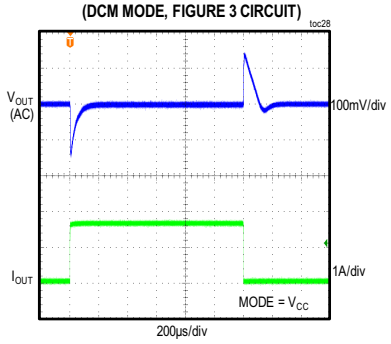
MAX17504S 3.3V OUTPUT LOAD CURRENT STEPPED FROM 5MA TO 1.75A (PFM MODE, FIGURE 6 CIRCUIT)



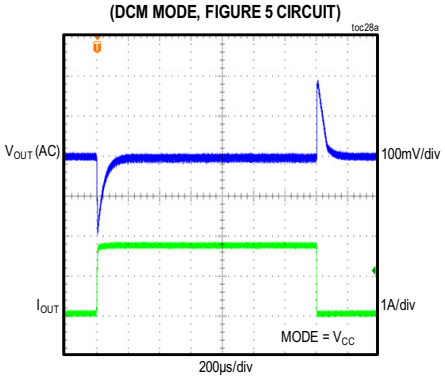
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

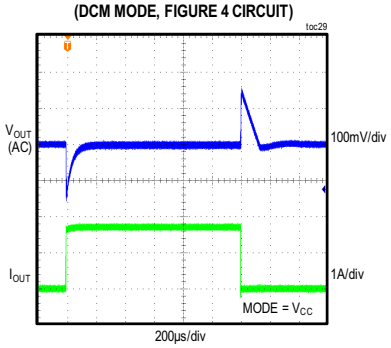
MAX17504 5V OUTPUT LOAD CURRENT STEPPED FROM 50mA TO 1.75A (DCM MODE, FIGURE 3 CIRCUIT)



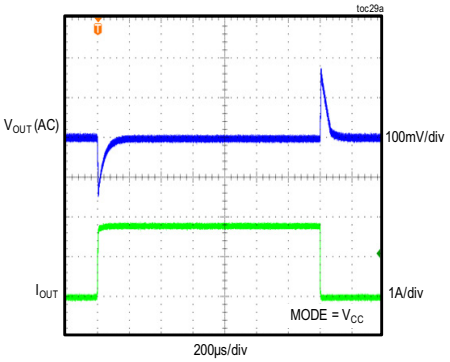
MAX17504S 5V OUTPUT LOAD CURRENT STEPPED FROM 50mA TO 1.75A (DCM MODE, FIGURE 5 CIRCUIT)



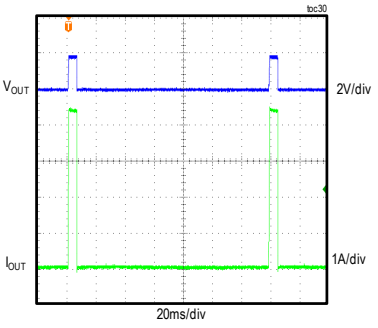
MAX17504 3.3V OUTPUT LOAD CURRENT STEPPED FROM 50mA TO 1.75A (DCM MODE, FIGURE 4 CIRCUIT)



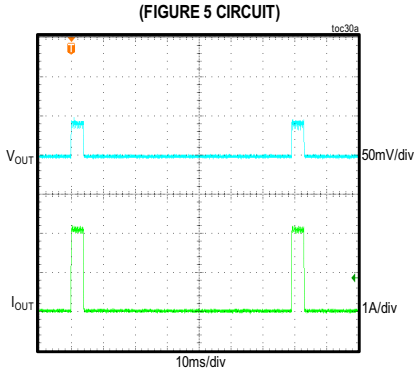
MAX17504S 3.3V OUTPUT LOAD CURRENT STEPPED FROM 50mA TO 1.75A (DCM MODE, FIGURE 6 CIRCUIT)



MAX17504 5V OUTPUT OVERLOAD PROTECTION (FIGURE 3 CIRCUIT)



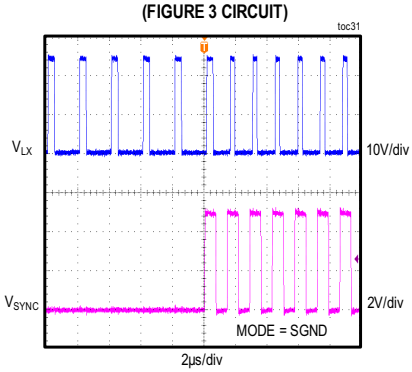
MAX17504S 5V OUTPUT OVERLOAD PROTECTION (FIGURE 5 CIRCUIT)



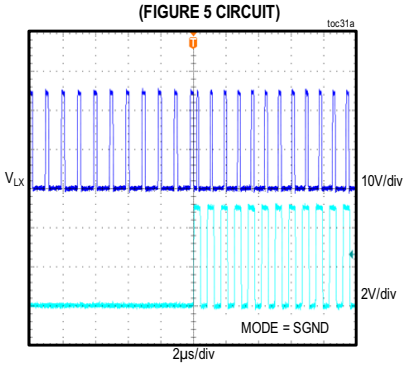
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 12,000pF, RT = MODE = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

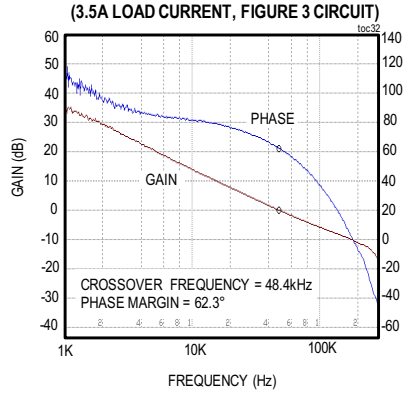
MAX17504 5V OUTPUT APPLICATION OF EXTERNAL CLOCK AT 700kHz (FIGURE 3 CIRCUIT)



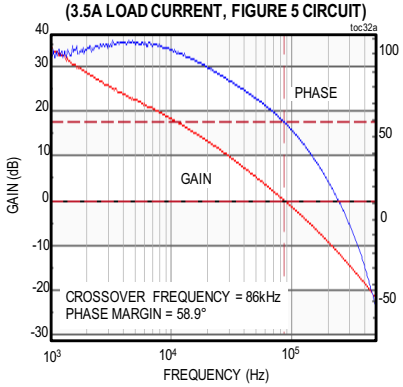
MAX17504S 5V OUTPUT APPLICATION OF EXTERNAL CLOCK AT 1.2MHz, (FIGURE 5 CIRCUIT)



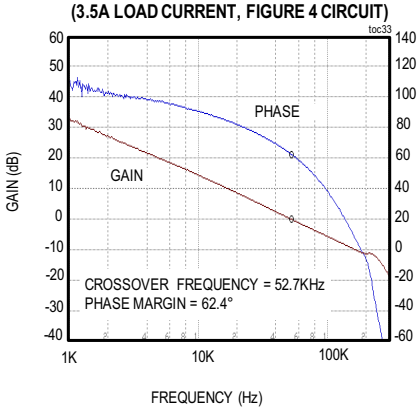
MAX17504 5V OUTPUT BODE PLOT (3.5A LOAD CURRENT, FIGURE 3 CIRCUIT)



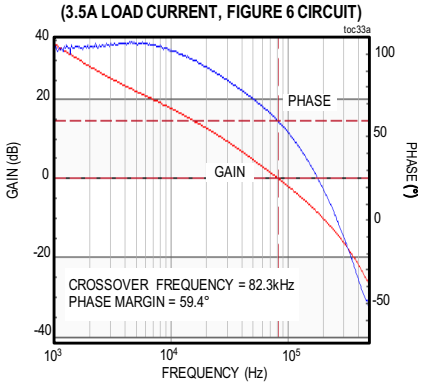
MAX17504S 5V OUTPUT 4 BODE PLOT (3.5A LOAD CURRENT, FIGURE 5 CIRCUIT)



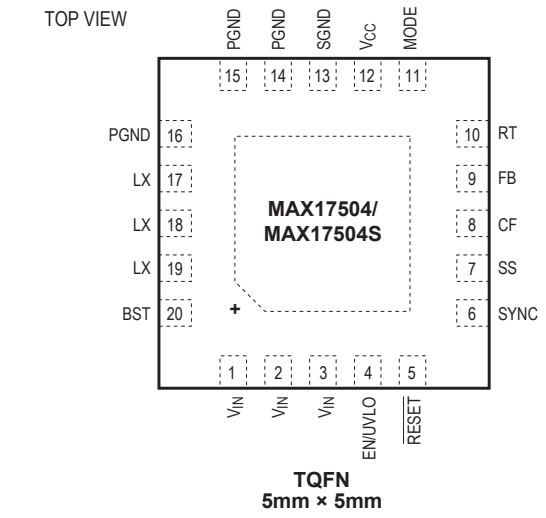
MAX17504 3.3V OUTPUT BODE PLOT (3.5A LOAD CURRENT, FIGURE 4 CIRCUIT)



MAX17504S 3.3V OUTPUT BODE PLOT (3.5A LOAD CURRENT, FIGURE 6 CIRCUIT)



Pin Configuration



TQFN
5mm × 5mm

* EXPOSED PAD (CONNECT TO SIGNAL GROUND).

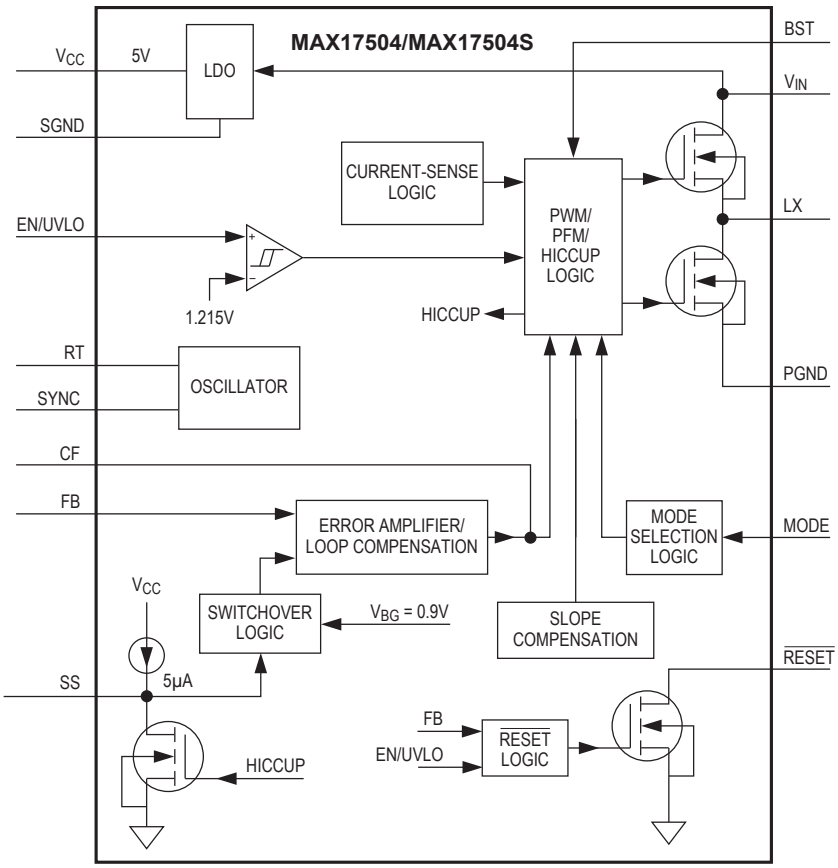
Pin Description

PIN	NAME	FUNCTION
1, 2, 3	V_{IN}	Power-Supply Input. 4.5V to 60V input supply range. Connect the V_{IN} pins together. Decouple to PGND with two 2.2µF capacitors; place the capacitors close to the V_{IN} and PGND pins. Refer to the MAX17504/MAX17504S EV kit data sheet for a layout example.
4	EN/UVLO	Enable/Undervoltage Lockout. Drive EN/UVLO high to enable the output voltage. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the MAX17504/MAX17504S turns on. Pull up to V_{IN} for always on operation.
5	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 clock cycles after FB rises above 95% of its set value.
6	SYNC	The device can be synchronized to an external clock using this pin. See the *External Frequency Synchronization* section for more details.
7	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
8	CF	At switching frequencies lower than 500kHz, connect a capacitor from CF to FB. Leave CF open if the switching frequency is equal to or more than 500kHz. See the *Loop Compensation* section for more details.
9	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
10	RT	Connect a resistor from RT to SGND to set the regulator's switching frequency. Leave RT open for the default 500kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
11	MODE	MODE configures the MAX17504/MAX17504S to operate in PWM, PFM or DCM modes of operation. Leave MODE unconnected for PFM operation (pulse skipping at light loads). Connect MODE to SGND for constant-frequency PWM operation at all loads. Connect MODE to V_{CC} for DCM operation. See the *MODE Setting* section for more details.

Pin Description (continued)

PIN	NAME	FUNCTION
12	V_{CC}	5V LDO Output. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND.
13	SGND	Analog Ground
14, 15, 16	PGND	Power Ground. Connect the PGND pins externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor. Refer to the MAX17504/MAX17504S EV kit data sheet for a layout example.
17, 18, 19	LX	Switching Node. Connect LX pins to the switching side of the inductor.
20	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
—	EP	Exposed pad. Connect to the SGND pin. Connect to a large copper plane below the IC to improve heat dissipation capability. Add thermal vias below the exposed pad. Refer to the MAX17504/MAX17504S EV kit data sheet for a layout example.

Block Diagram



Detailed Description

The MAX17504/MAX17504S high-efficiency, high-voltage, synchronously rectified step-down converter with dual integrated MOSFETs operates over a 4.5V to 60V input. It delivers up to 3.5A and 0.9V to 90% V_{IN} output voltage. Built-in compensation across the output voltage range eliminates the need for external components. The feedback (FB) regulation accuracy over -40°C to +125°C is ±1.1%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node that sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE pin that can be used to operate the device in PWM, PFM, or DCM control schemes. The device integrates adjustable-input undervoltage lockout, adjustable soft-start, open $\overline{RESET}$, and external frequency synchronization features. The MAX17504S offers a lower minimum on-time that allows for higher switching frequencies and a smaller solution size.

Mode Selection (MODE)

The logic state of the MODE pin is latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is open at power-up, the device operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE pin is connected to V_{CC} at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 750mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal blocks and the low-side MOSFET driver. The output of the linear regulator (V_{CC}) should be bypassed with a 2.2µF ceramic capacitor to SGND. The MAX17504/MAX17504S employs an undervoltage lockout circuit that disables the internal linear regulator when V_{CC} falls below 3.8V (typ).

Setting the Switching Frequency (RT)

The switching frequency of the MAX17504/MAX17504S can be programmed from 100kHz to 2.2MHz by using a resistor connected from RT to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 500kHz. See Table 1 for RT resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
500	OPEN
100	210
200	102
400	49.9
1000	19.1
2200	8.06

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.15))}{1 - (f_{SW(MAX)} \times t_{OFF(MAX)})} + (I_{OUT(MAX)} \times 0.175)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where V_{OUT} is the steady-state output voltage, $I_{OUT(MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, $f_{SW(MAX)}$ is the maximum switching frequency, $t_{OFF(MAX)}$ is the worst-case minimum switch off-time (160ns), and $t_{ON(MIN)}$ is the worst-case minimum switch on-time (135ns for the MAX17504, 80ns for the MAX17504S).

External Frequency Synchronization (SYNC)

The internal oscillator of the MAX17504/MAX17504S can be synchronized to an external clock signal on the SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the RT resistor. The minimum external clock pulse-width high should be greater than 50ns. See the RT and SYNC section in the *Electrical Characteristics* table for details.

Overcurrent Protection/HICCUP Mode

The MAX17504/MAX17504S is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 5.1A (typ). A runaway current limit on the high-side switch current at 5.7A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the ON period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, feedback voltage drops to 0.58V (typ) anytime after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under an overload condition, if feedback voltage does not exceed 0.58V, the device switches at half the programmed switching frequency. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The MAX17504/MAX17504S includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high-impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the MAX17504/MAX17504S starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal-Shutdown Protection

Thermal-shutdown protection limits total power dissipation in the MAX17504/MAX17504S. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high ripple current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the MAX17504/MAX17504S input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX17504/MAX17504S: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of 5.1A.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{sw}}\right)$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. For the MAX17504, select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz. For the MAX17504S, select f_C to be 1/10th of f_{SW} if the switching frequency is less than or equal to 1MHz. If the switching frequency is more than 1MHz, select f_C to be 100kHz.

Derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

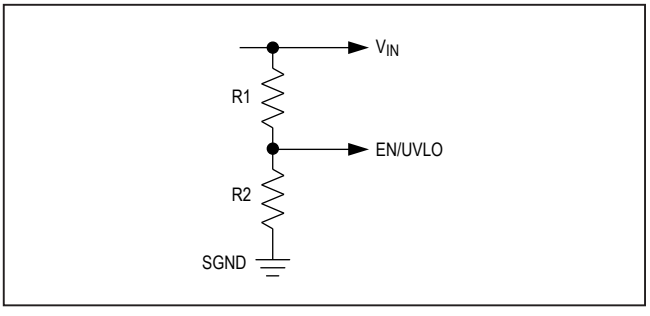


Figure 1. Setting the Input Undervoltage Lockout

Soft-Start Capacitor Selection

The MAX17504/MAX17504S implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = C_{SS}/(5.55 \times 10^{-6})$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to SGND.

Setting the Input Undervoltage Lockout Level

The MAX17504/MAX17504S offers an adjustable input undervoltage lockout level. Set the voltage at which MAX17504/MAX17504S turns ON, with a resistive voltage-divider connected from V_{IN} to SGND. Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the MAX17504/MAX17504S is required to turn ON. Ensure that V_{INU} is higher than 0.8 x V_{OUT}. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

Loop Compensation

The MAX17504/MAX17504S is internally loop compensated. However, if the switching frequency is less than 500kHz, connect a 0402 capacitor, C6, between the CF pin and the FB pin. Use Table 2 to select the value of C6.

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values: Calculate resistor R3 from the output to FB as follows:

$$R3 = \frac{216 \times 10^3}{f_C \times C_{OUT}}$$

where R3 is in kΩ, crossover frequency f_C is in kHz, and output capacitor C_{OUT} is in µF. For the MAX17504, choose f_C to be 1/9th of the switching frequency, f_{SW}, if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz. For the MAX17504S, select f_C to be 1/10th of f_{SW} if the switching frequency is less than or equal to 1MHz. If the switching frequency is more than 1MHz, select f_C to be 100kHz.

Calculate resistor R4 from FB to SGND as follows:

$$R4 = \frac{R3 \times 0.9}{(V_{OUT} - 0.9)}$$

Table 2. C6 Capacitor Value at Various Switching Frequencies

SWITCHING FREQUENCY RANGE (kHz)	C6 (pF)
200 to 300	2.2
300 to 400	1.2
400 to 500	0.75

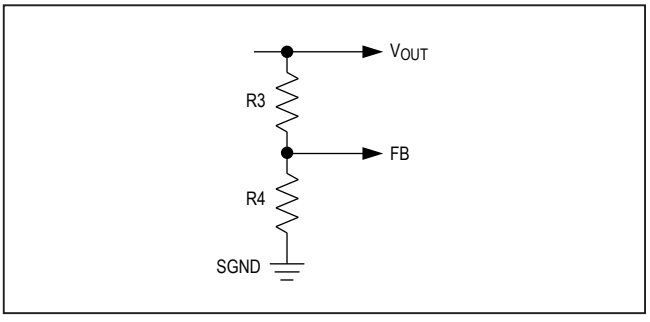


Figure 2. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the total output power, η is the efficiency of the converter, and R_{DCR} is the DC resistance of the inductor. (See the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 30°C/W$$

$$\theta_{JC} = 2°C/W$$

The junction temperature of the MAX17504/MAX17504S can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the equation below:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal management system that ensures that the exposed pad of the MAX17504/MAX17504S is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the MAX17504/MAX17504S can be estimated at any given maximum ambient temperature from the equation below:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperature greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small current loop areas reduce radiated EMI.

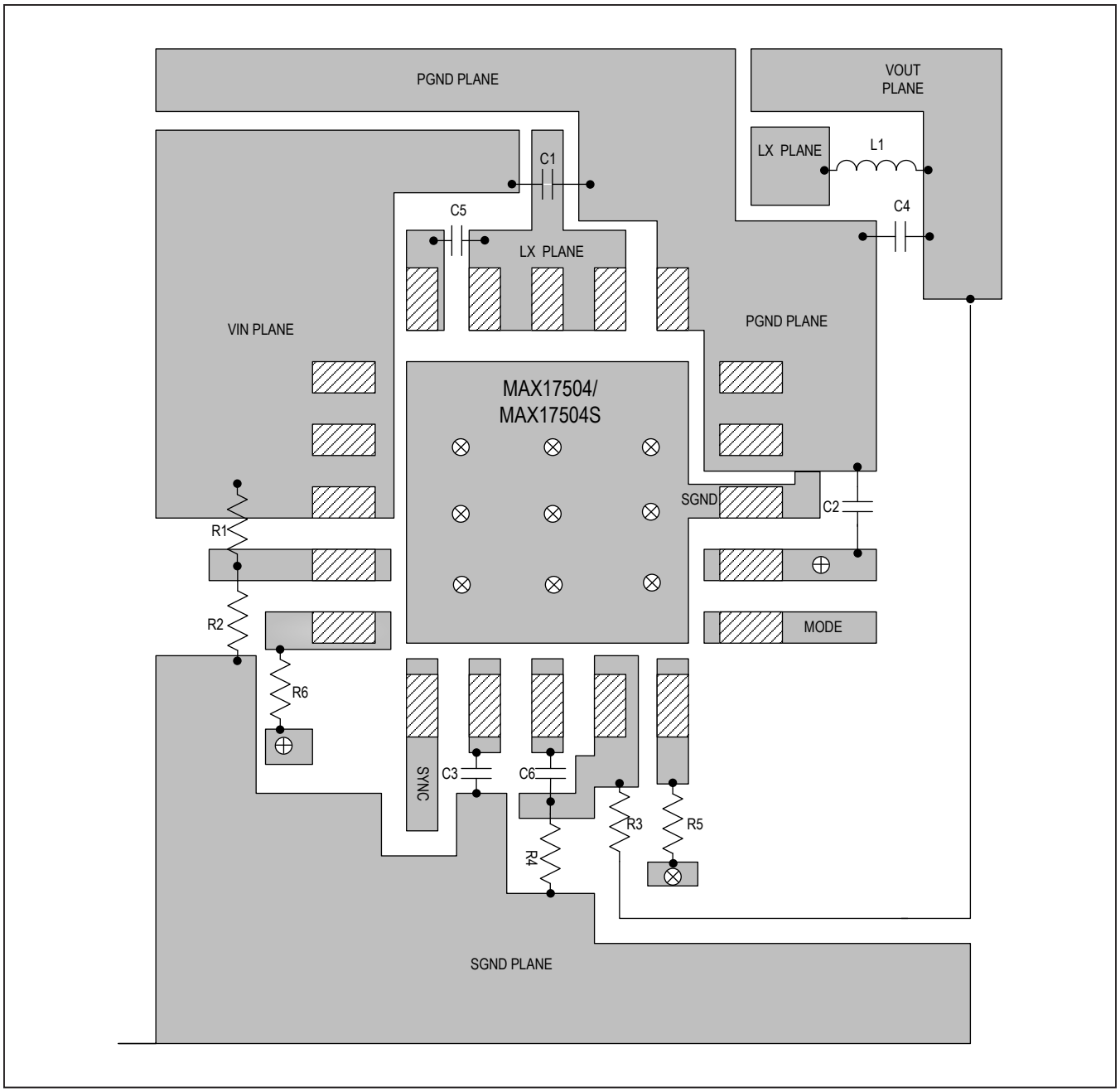
A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and give the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17504 evaluation kit layout available at **www.maximintegrated.com**.

Recommended Component Placement for MAX17504/MAX17504S



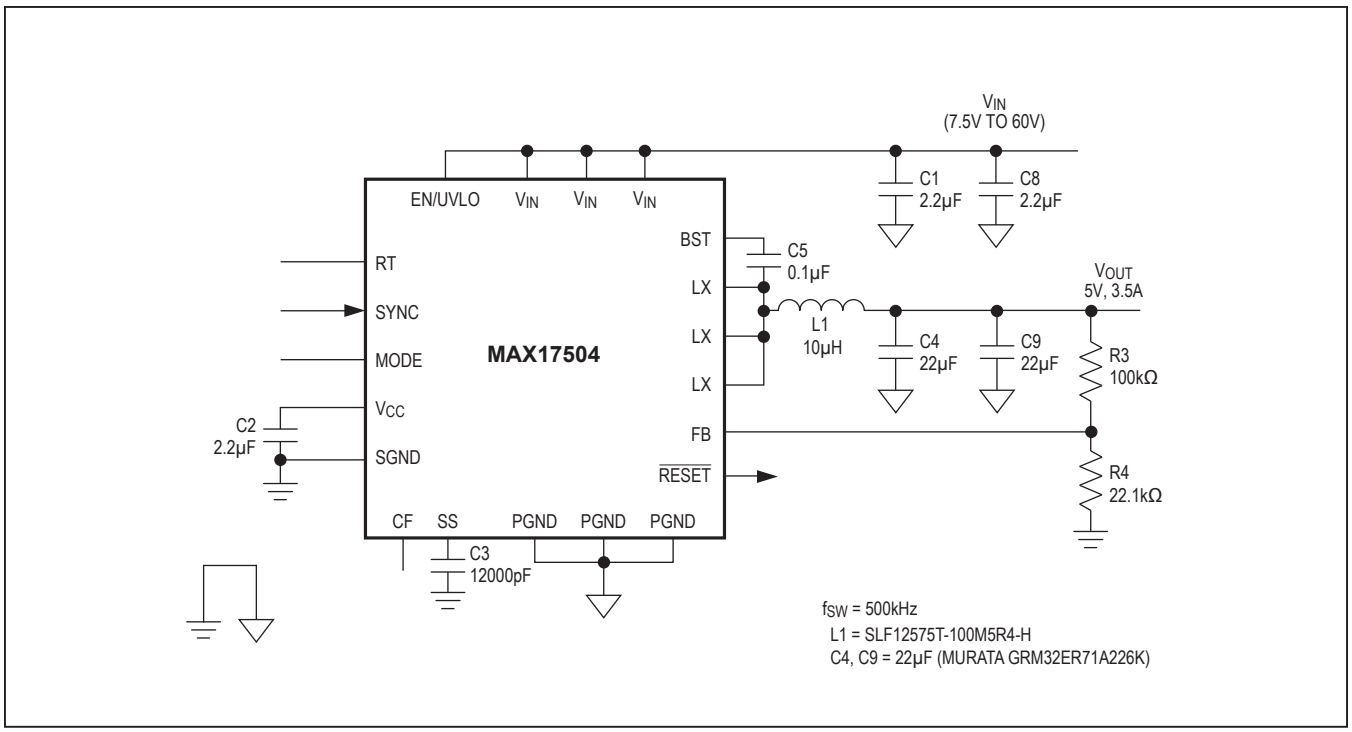


Figure 3. MAX17504 Typical Application Circuit for 5V Output, 500kHz Switching Frequency

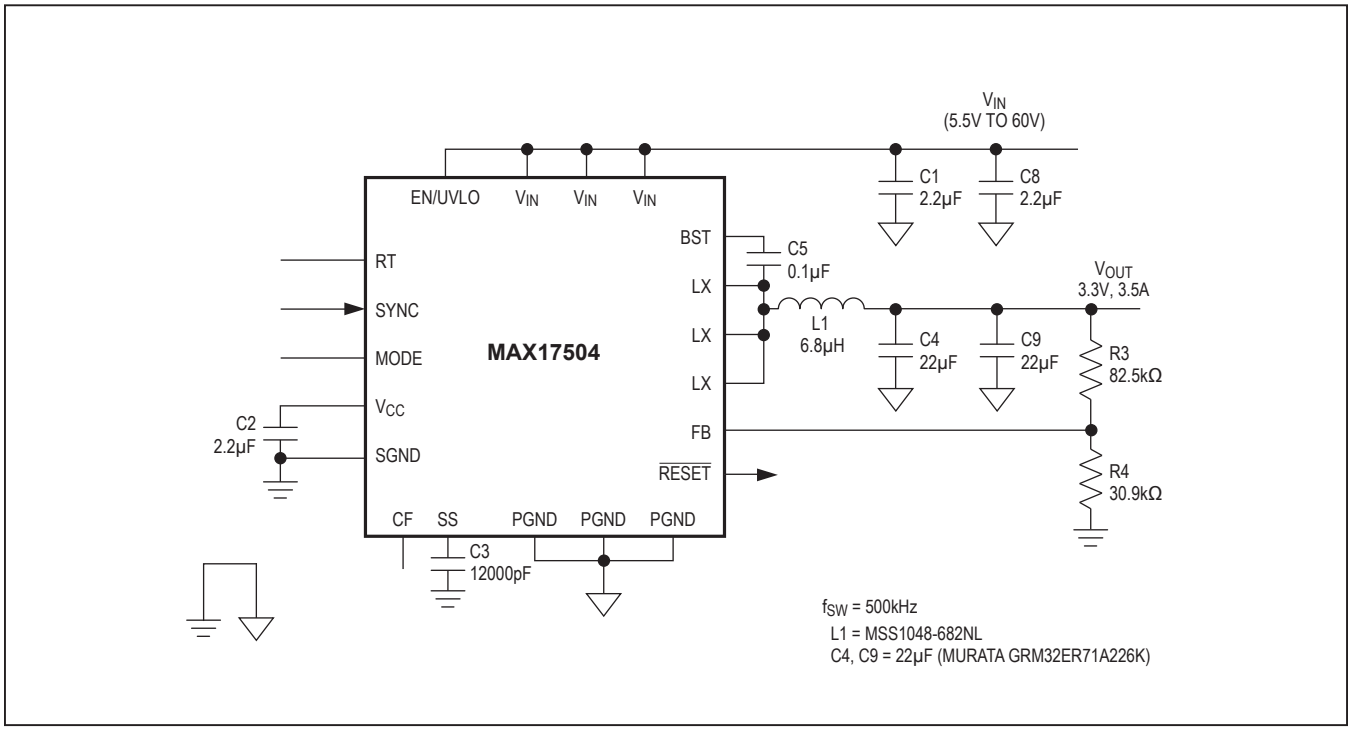


Figure 4. MAX17504 Typical Application Circuit for 3.3V Output, 500kHz Switching Frequency

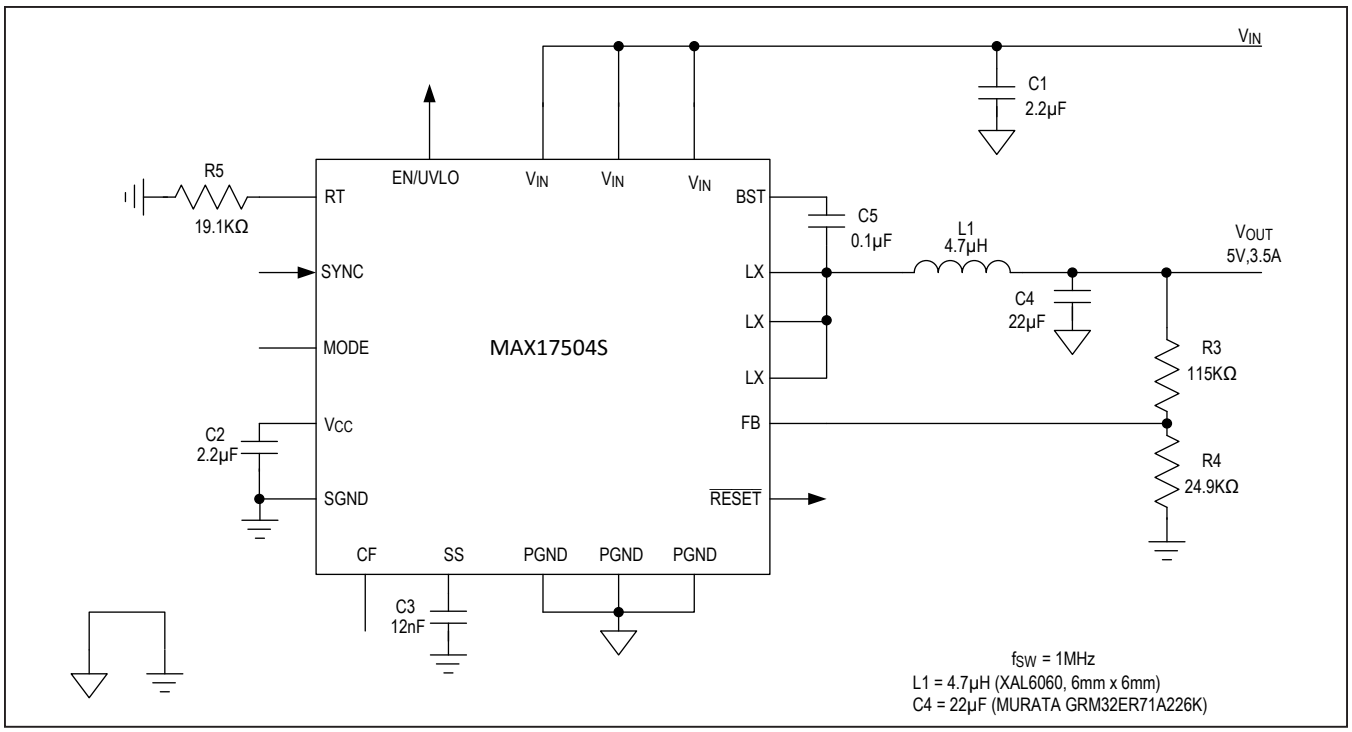


Figure 5. MAX17504S Typical Operating Circuit for 5V Output, 1MHz Switching Frequency

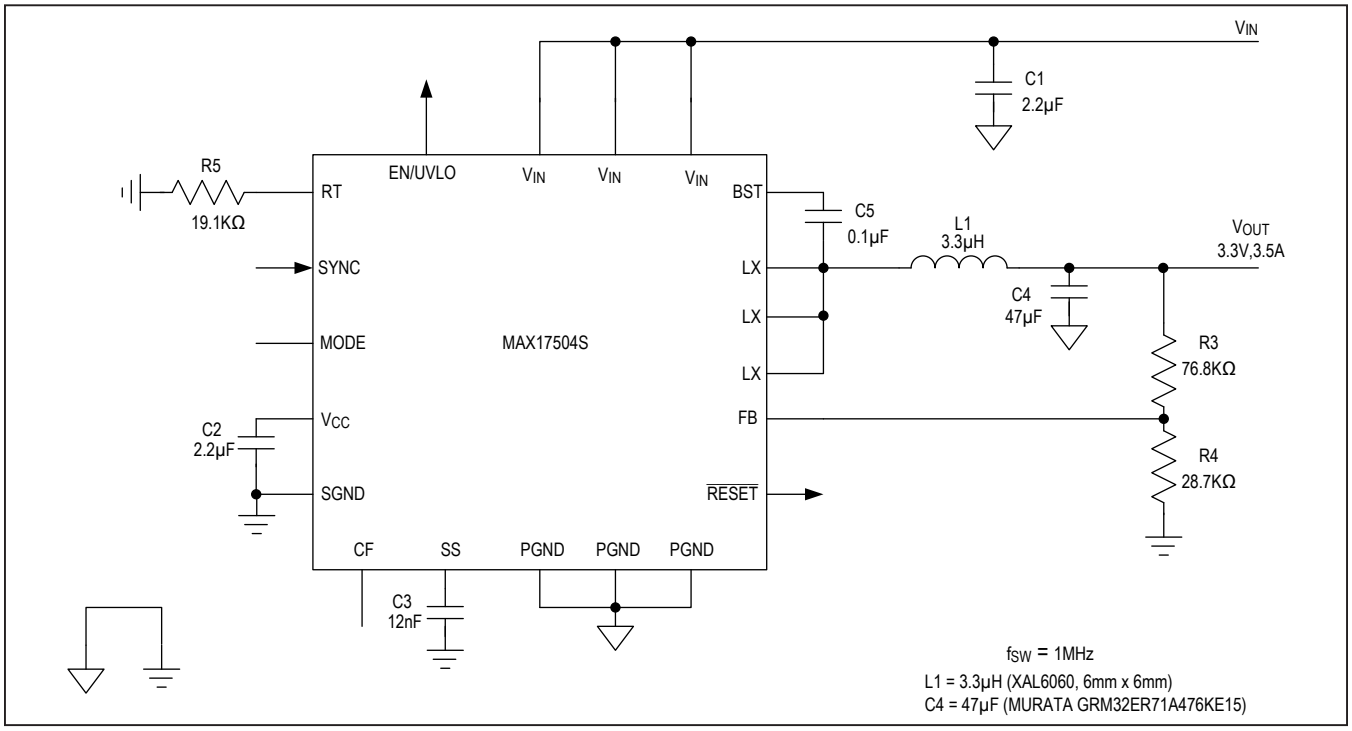


Figure 6. MAX17504S Typical Operating Circuit for 3.3V Output, 1MHz Switching Frequency

Ordering Information

PART	PIN-PACKAGE
MAX17504ATP+	20 TQFN-EP* 5mm x 5mm
MAX17504SATP+	20 TQFN-EP* 5mm x 5mm

Note: *All devices operate over the temperature range of -40ºC to +125ºC, unless otherwise noted.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/13	Initial release	—
1	2/14	Updated TOC32, TOC33, and Typical Application Circuit figures	9, 16, 17
2	10/16	Added MAX17504S to data sheet, updated junction temperature, and added TOCs	1-17
3	5/17	Removed 17504S from data sheet, corrected part numbers in *General Description*, *Benefits and Features*, *Detailed Description*, *Operating Input Voltage Range* sections, updated TOCs 1a, 5, 5a, 6, 7a, 12, 12a, 13, 13a, 14a, 15a, 16a, 17a, 18a, 19a, 20a, 21a, 22, 22a, 23, 23a, 24a, 25a, 26a, 27a, 30a, 32a, Figures 3, 4, 5, and 6, removed *Recommended Component Placement for MAX17504/MAX17504S*	1–26

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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