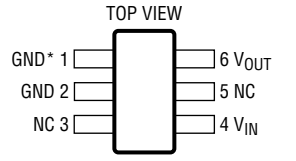
ABSOLUTE MAXIMUM RATINGS (Note 1)

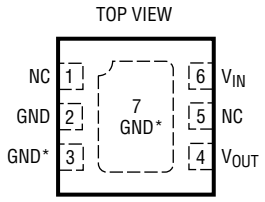
Input Voltage.....±20V
Output Voltage ..... –0.3V to 20V
Output Voltage Above Input Voltage 20V
Specified Temperature Range (Note 2)
Commercial ..... 0°C to 70°C
Industrial .....–40°C to 85°C

Operating Temperature Range (Note 2).. –55°C to 125°C
Output Short Circuit Duration ..... Indefinite
Junction Temperature ..... 150°C
Storage Temperature Range (Note 3)..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)
TSOT-23 (Note 4).....300°C

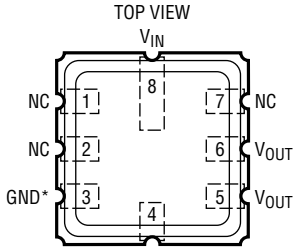
PIN CONFIGURATION



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 230°C/W
*CONNECT PIN TO DEVICE GND (PIN 2)



DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 102°C/W
EXPOSED PAD (PIN 7) MUST BE CONNECTED TO GND



LS8 PACKAGE
8-PIN LEADLESS CHIP CARRIER (5mm × 5mm)
T_{JMAX} = 150°C, θ_{JA} = 125°C/W
*CONNECT PIN TO DEVICE GND (PIN 4)

ORDER INFORMATION

LEAD FREE FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6656ACS6-1.25#TRMPBF	LT6656ACS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-1.25#TRMPBF	LT6656BCS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-1.25#TRMPBF	LT6656AIS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-1.25#TRMPBF	LT6656BIS6-1.25#TRPBF	LTFNK	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACS6-2.048#TRMPBF	LT6656ACS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-2.048#TRMPBF	LT6656BCS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-2.048#TRMPBF	LT6656AIS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-2.048#TRMPBF	LT6656BIS6-2.048#TRPBF	LTFNN	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACS6-2.5#TRMPBF	LT6656ACS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-2.5#TRMPBF	LT6656BCS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-2.5#TRMPBF	LT6656AIS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-2.5#TRMPBF	LT6656BIS6-2.5#TRPBF	LTFGW	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACS6-3#TRMPBF	LT6656ACS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-3#TRMPBF	LT6656BCS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-3#TRMPBF	LT6656AIS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-3#TRMPBF	LT6656BIS6-3#TRPBF	LTFNQ	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACS6-3.3#TRMPBF	LT6656ACS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-3.3#TRMPBF	LT6656BCS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-3.3#TRMPBF	LT6656AIS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-3.3#TRMPBF	LT6656BIS6-3.3#TRPBF	LTFNS	6-Lead Plastic TSOT-23	–40°C to 85°C

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ORDER INFORMATION

LEAD FREE FINISH

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6656ACS6-4.096#TRMPBF	LT6656ACS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-4.096#TRMPBF	LT6656BCS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-4.096#TRMPBF	LT6656AIS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-4.096#TRMPBF	LT6656BIS6-4.096#TRPBF	LTFNV	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACS6-5#TRMPBF	LT6656ACS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656BCS6-5#TRMPBF	LT6656BCS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	0°C to 70°C
LT6656AIS6-5#TRMPBF	LT6656AIS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656BIS6-5#TRMPBF	LT6656BIS6-5#TRPBF	LTFNX	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6656ACDC-1.25#TRMPBF	LT6656ACDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-1.25#TRMPBF	LT6656BCDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-1.25#TRMPBF	LT6656AIDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-1.25#TRMPBF	LT6656BIDC-1.25#TRPBF	LFNM	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-2.048#TRMPBF	LT6656ACDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-2.048#TRMPBF	LT6656BCDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-2.048#TRMPBF	LT6656AIDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-2.048#TRMPBF	LT6656BIDC-2.048#TRPBF	LFNP	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-2.5#TRMPBF	LT6656ACDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-2.5#TRMPBF	LT6656BCDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-2.5#TRMPBF	LT6656AIDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-2.5#TRMPBF	LT6656BIDC-2.5#TRPBF	LFGX	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656AIDC-2.8#TRMPBF	LT6656AIDC-2.8#TRPBF	LHQX	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-3#TRMPBF	LT6656ACDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-3#TRMPBF	LT6656BCDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-3#TRMPBF	LT6656AIDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-3#TRMPBF	LT6656BIDC-3#TRPBF	LFNR	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-3.3#TRMPBF	LT6656ACDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-3.3#TRMPBF	LT6656BCDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-3.3#TRMPBF	LT6656AIDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-3.3#TRMPBF	LT6656BIDC-3.3#TRPBF	LFNT	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-4.096#TRMPBF	LT6656ACDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-4.096#TRMPBF	LT6656BCDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-4.096#TRMPBF	LT6656AIDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-4.096#TRMPBF	LT6656BIDC-4.096#TRPBF	LFNW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656ACDC-5#TRMPBF	LT6656ACDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656BCDC-5#TRMPBF	LT6656BCDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LT6656AIDC-5#TRMPBF	LT6656AIDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LT6656BIDC-5#TRMPBF	LT6656BIDC-5#TRPBF	LFNY	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LEAD FREE FINISH	**PART MARKING***	**PACKAGE DESCRIPTION**		**SPECIFIED TEMPERATURE RANGE**
LT6656AILS8-1.25#PBF†	656125	8-Lead (5mm × 5mm) Ceramic LCC		–40°C to 85°C
LT6656BILS8-1.25#PBF†	656125	8-Lead (5mm × 5mm) Ceramic LCC		–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Contact the factory for parts specified with wider operating temperature ranges.
Contact the factory for information on lead based finish parts.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.
†This product is only offered in trays.

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AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	SPECIFIED TEMPERATURE RANGE	
			0°C TO 70°C	–40°C TO 85°C
			ORDER PART NUMBER*	ORDER PART NUMBER*
1.250V	0.05%	10ppm/°C	LT6656ACS6-1.25	LT6656AIS6-1.25
	0.05%	10ppm/°C	N/A	LT6656AILS8-1.25
	0.10%	20ppm/°C	LT6656BCS6-1.25	LT6656BIS6-1.25
	0.10%	10ppm/°C	LT6656ACDC-1.25	LT6656AIDC-1.25
	0.10%	15ppm/°C	N/A	LT6656BILS8-1.25
	0.20%	20ppm/°C	LT6656BCDC-1.25	LT6656BIDC-1.25
2.048V	0.05%	10ppm/°C	LT6656ACS6-2.048	LT6656AIS6-2.048
	0.10%	20ppm/°C	LT6656BCS6-2.048	LT6656BIS6-2.048
	0.10%	10ppm/°C	LT6656ACDC-2.048	LT6656AIDC-2.048
	0.20%	20ppm/°C	LT6656BCDC-2.048	LT6656BIDC-2.048
2.500V	0.05%	10ppm/°C	LT6656ACS6-2.5	LT6656AIS6-2.5
	0.10%	20ppm/°C	LT6656BCS6-2.5	LT6656BIS6-2.5
	0.10%	10ppm/°C	LT6656ACDC-2.5	LT6656AIDC-2.5
	0.20%	20ppm/°C	LT6656BCDC-2.5	LT6656BIDC-2.5
2.800V	0.10%	10ppm/°C	N/A	LT6656AIDC-2.8
3.000V	0.05%	10ppm/°C	LT6656ACS6-3	LT6656AIS6-3
	0.10%	20ppm/°C	LT6656BCS6-3	LT6656BIS6-3
	0.10%	10ppm/°C	LT6656ACDC-3	LT6656AIDC-3
	0.20%	20ppm/°C	LT6656BCDC-3	LT6656BIDC-3
3.300V	0.05%	10ppm/°C	LT6656ACS6-3.3	LT6656AIS6-3.3
	0.10%	20ppm/°C	LT6656BCS6-3.3	LT6656BIS6-3.3
	0.10%	10ppm/°C	LT6656ACDC-3.3	LT6656AIDC-3.3
	0.20%	20ppm/°C	LT6656BCDC-3.3	LT6656BIDC-3.3
4.096V	0.05%	10ppm/°C	LT6656ACS6-4.096	LT6656AIS6-4.096
	0.10%	20ppm/°C	LT6656BCS6-4.096	LT6656BIS6-4.096
	0.10%	10ppm/°C	LT6656ACDC-4.096	LT6656AIDC-4.096
	0.20%	20ppm/°C	LT6656BCDC-4.096	LT6656BIDC-4.096
5.000V	0.05%	10ppm/°C	LT6656ACS6-5	LT6656AIS6-5
	0.10%	20ppm/°C	LT6656BCS6-5	LT6656BIS6-5
	0.10%	10ppm/°C	LT6656ACDC-5	LT6656AIDC-5
	0.20%	20ppm/°C	LT6656BCDC-5	LT6656BIDC-5

*See Order Information section for complete part number listing.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V (for LT6656-1.25, V_{IN} = 2.2V), C_L = 1µF, I_L = 0,unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Error	LT6656ACS6, LT6656AIS6, LT6656AILS8 LT6656BCS6, LT6656BIS6, LT6656BILS8 LT6656ACDC, LT6656AIDC LT6656BCDC, LT6656BIDC		–0.05 –0.1 –0.1 –0.2		0.05 0.1 0.1 0.2	% % % %
Output Voltage Temperature Coefficient (Note 5)	LT6656A LT6656B	● ●		5 12	10 20	ppm/°C ppm/°C
Line Regulation	V_{IN} = (V_{OUT} + 0.5V) to 18V LT6656-2.048, LT6656-2.5, LT6656-2.8, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●		2	25 40	ppm/V ppm/V
	V_{IN} = 2.2V to 18V LT6656-1.25	●		2	25 40	ppm/V ppm/V
Load Regulation (Note 6)	I_L = 5mA, Sourcing LT6656-2.048, LT6656-2.5, LT6656-2.8, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●		65	150 375	ppm/mA ppm/mA
	I_L = 5mA, Sourcing LT6656S6-1.25, LT6656DC-1.25	●		80	175 425	ppm/mA ppm/mA
	I_L = 5mA, Sourcing LT6656LS8-1.25	●		135	250 500	ppm/mA ppm/mA
Dropout Voltage (Note 7)	V_{IN} – V_{OUT}, ΔV_{OUT} Error ≤ 0.1% I_L = 0 LT6656-2.048, LT6656-2.5, LT6656-2.8, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●		3	10 40	mV mV
	I_L = 5mA, Sourcing LT6656-2.048, LT6656-2.5, LT6656-2.8, LT6656-3, LT6656-3.3, LT6656-4.096, LT6656-5	●		250	370 500	mV mV
Minimum Input Voltage	I_L = 0, ΔV_{OUT} Error ≤ 0.1% LT6656-1.25 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●		 1.35	 1.5 1.6 1.8	 V V V
Supply Current		●		0.85	1.0 1.5	µA µA
Output Short Circuit Current	Short V_{OUT} to GND Short V_{OUT} to V_{IN}			18 4		mA mA
Input Reverse Leakage Current	V_{IN} = –18V, V_{OUT} = GND			80		µA
Reverse Output Current	V_{IN} = GND, V_{OUT} = 18V			30		µA
Output Voltage Noise (Note 8)	0.1Hz to 10Hz 10Hz to 1kHz, LT6656-1.25 10Hz to 1kHz, LT6656-2.5 10Hz to 1kHz, LT6656-5			30 50 80 140		ppm_{P-P} μV_{RMS} μV_{RMS} μV_{RMS}
Turn-On Time	LT6656-1.25, 0.1% Settling LT6656-2.5, 0.1% Settling LT6656-5, 0.1% Settling			15 30 60		ms ms ms

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V (for LT6656-1.25, V_{IN} = 2.2V), C_L = 1µF, I_L = 0,unless otherwise noted.

Long Term Drift of Output Voltage (Note 9)	LT6656S6, LT6656DC LT6656LS8		50 15	ppm/√kHr ppm/√kHr
Hysteresis (Note 10)	LT6656S6, LT6656DC ΔT = 0°C to 70°C ΔT = –40°C to 85°C		 25 70	 ppm ppm
	LT6656LS8 ΔT = 0°C to 70°C ΔT = –40°C to 85°C		 15 55	 ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT6656C is guaranteed to meet specified performance from 0°C to 70°C. The LT6656C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT6656I is guaranteed to meet specified performance from –40°C to 85°C. By design, the LT6656 is guaranteed functional over the operating temperature range of –55°C to 125°C.

Note 3: If the LT6656 is stored outside of the specified temperature range, the output may shift due to hysteresis.

Note 4: The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications section.

Note 5: Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

Note 6: Load regulation is measured with a pulse from no load to the specified load current. Output changes due to die temperature change must be taken into account separately.

Note 7: Excludes load regulation errors.

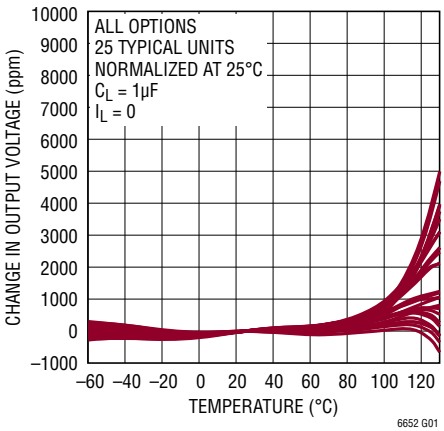
Note 8: Peak-to-peak noise is measured with a 3-pole highpass filter at 0.1Hz and a 4-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. The test time is 10 seconds. RMS noise is measured on a spectrum analyzer in a shielded environment.

Note 9: Long term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly.

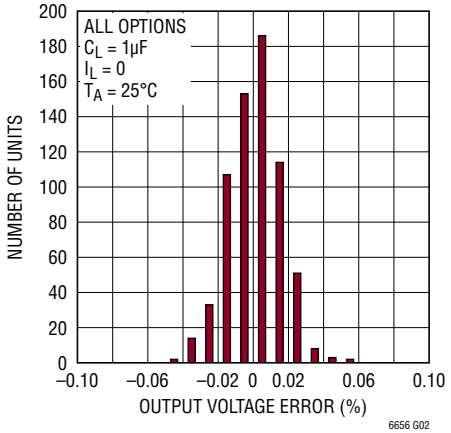
Note 10: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature) hysteresis is usually not a dominant error source. Typical hysteresis is the worst-case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

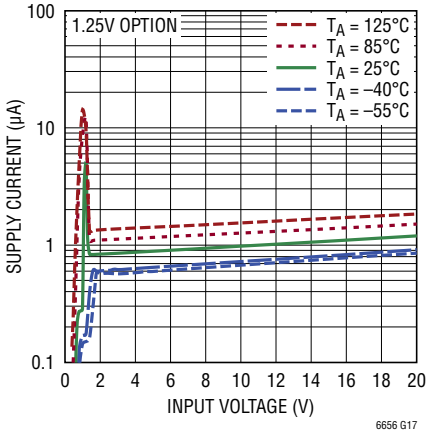
Output Voltage Temperature Drift



Typical V_{OUT} Distribution



Supply Current vs Input Voltage



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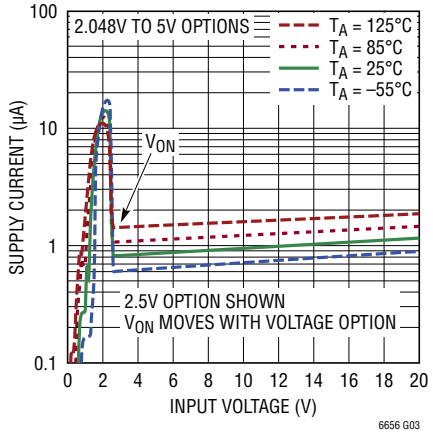
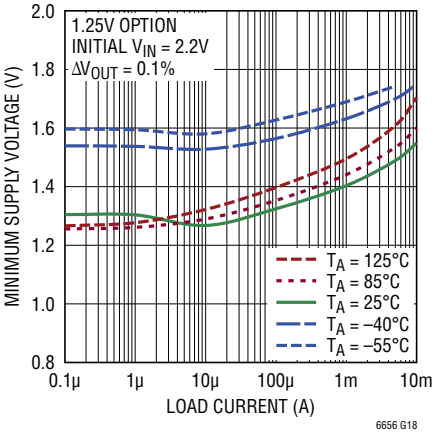
TYPICAL PERFORMANCE CHARACTERISTICS

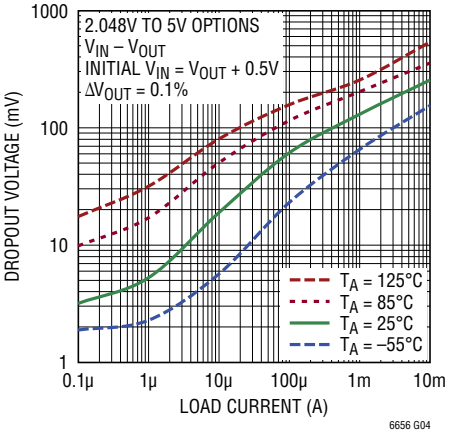
Supply Current vs Input Voltage



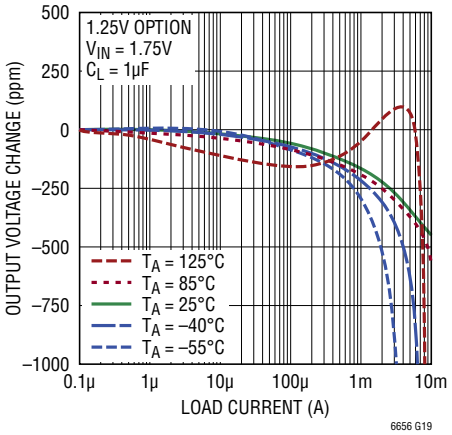
Minimum Supply Voltage vs Load Current



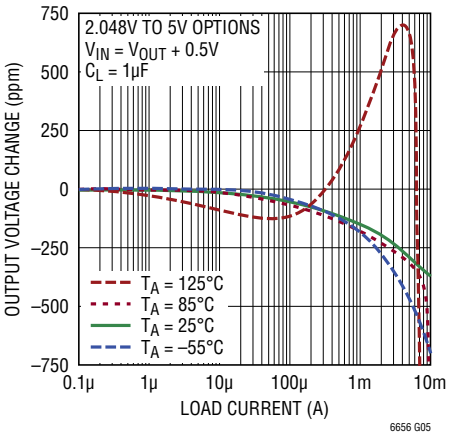
Dropout Voltage vs Load Current



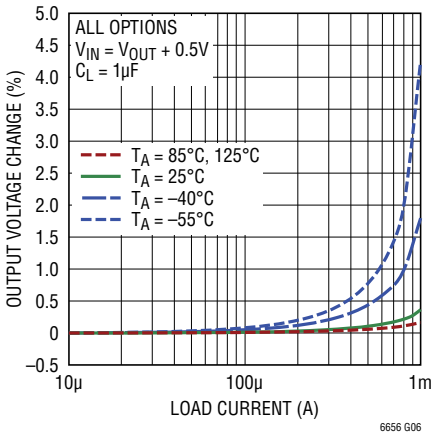
Load Regulation (Sourcing)



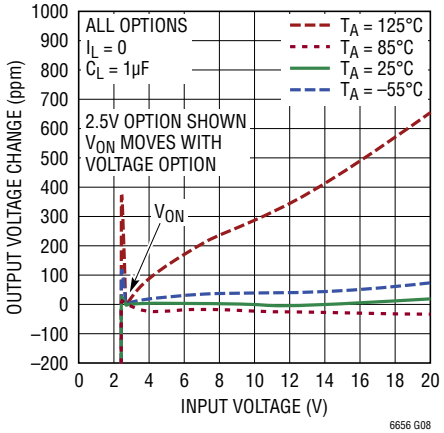
Load Regulation (Sourcing)



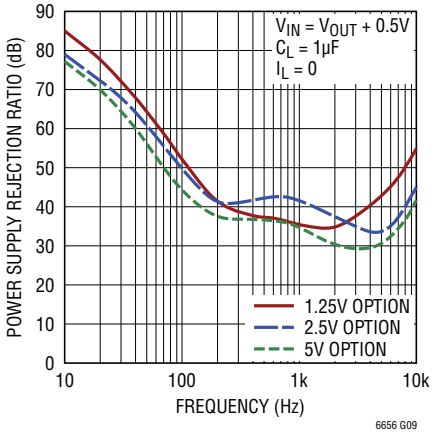
Load Regulation (Sinking)



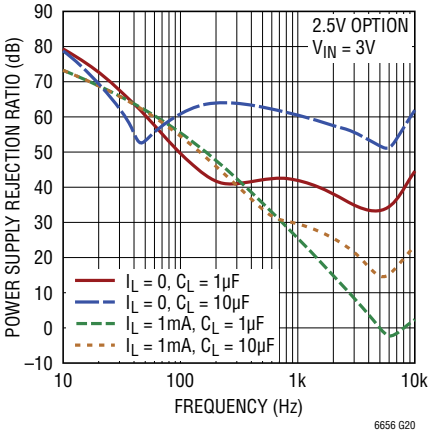
Line Regulation



Power Supply Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



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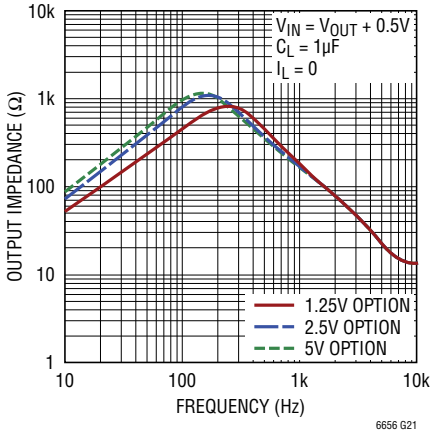
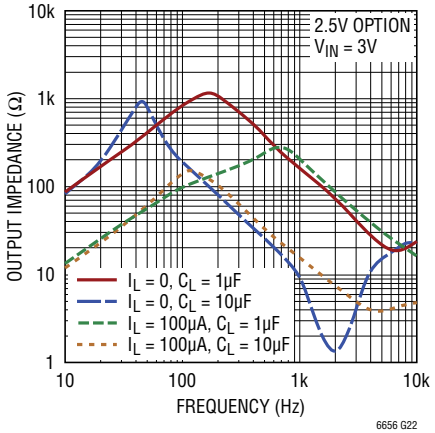
TYPICAL PERFORMANCE CHARACTERISTICS

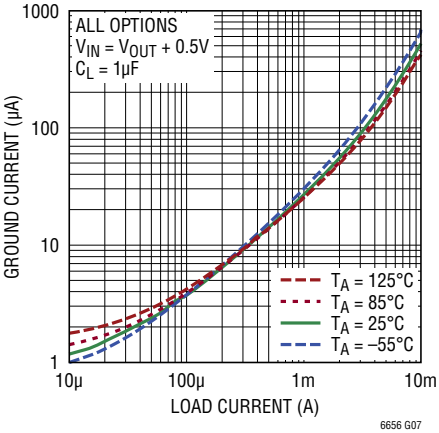
Output Impedance vs Frequency



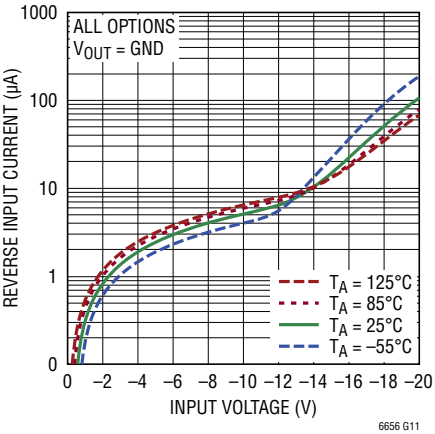
Output Impedance vs Frequency



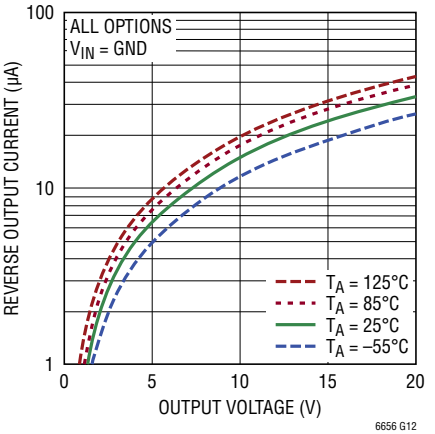
Ground Current vs Load Current



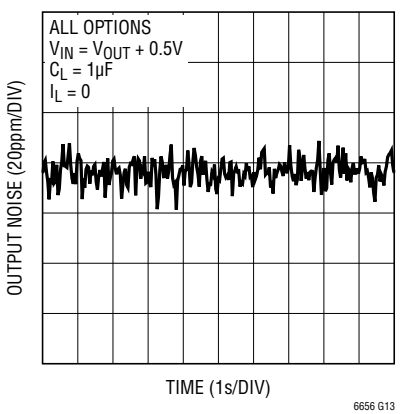
Reverse Input Current



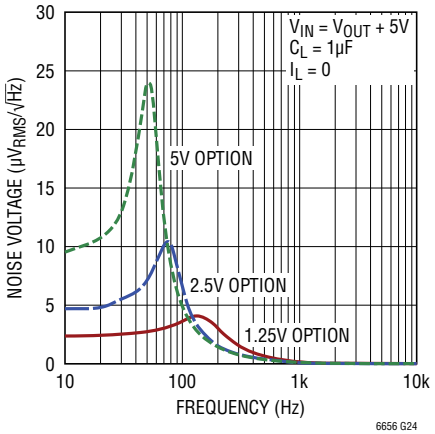
Reverse Output Current



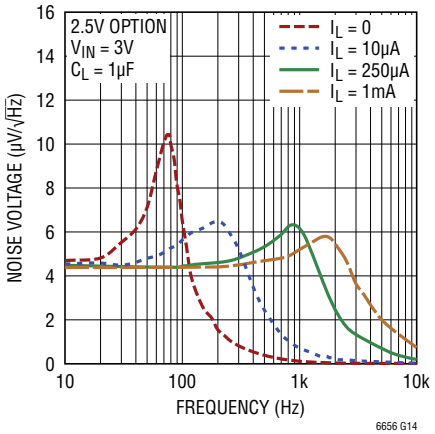
Output Noise 0.1Hz to 10Hz



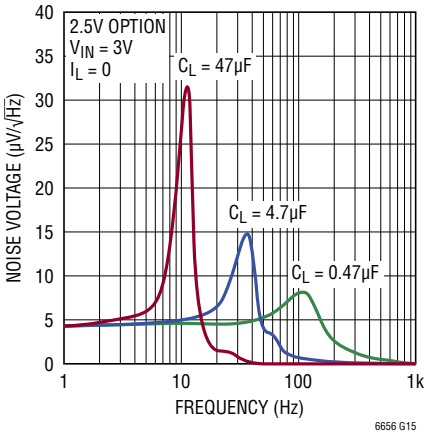
Output Voltage Noise Spectrum



Output Voltage Noise Spectrum vs Load Current



Output Noise Voltage Spectrum vs Load Capacitance



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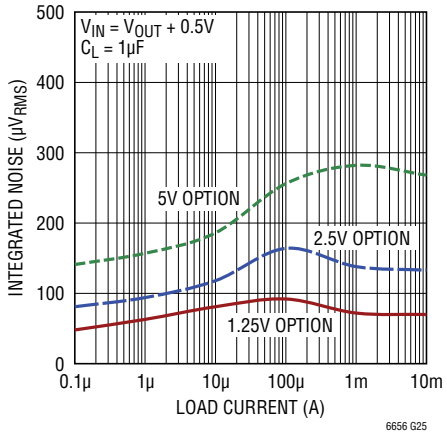
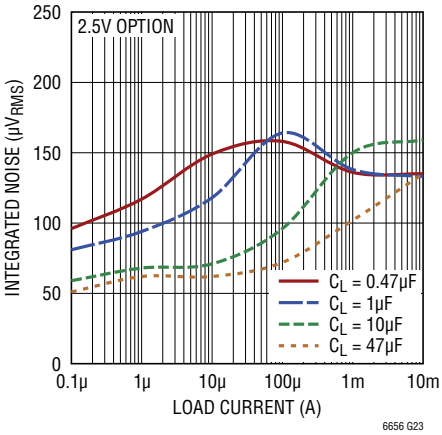
TYPICAL PERFORMANCE CHARACTERISTICS

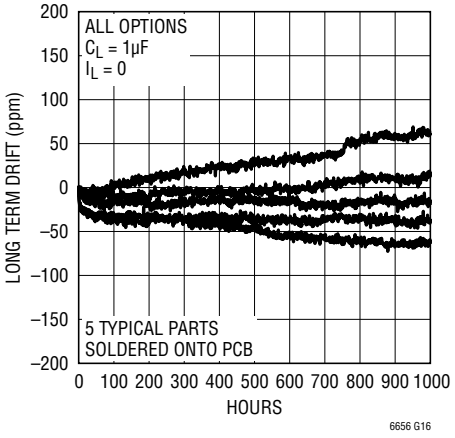
Integrated 10Hz to 1kHz Noise vs Load Current



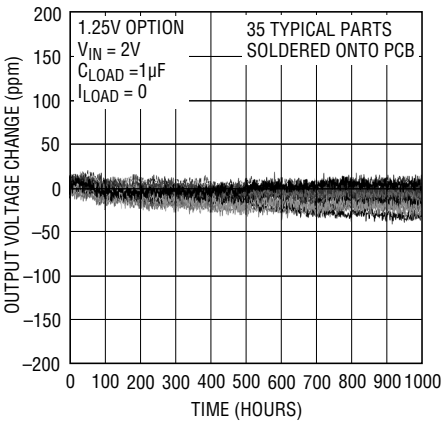
Integrated 10Hz to 1kHz Noise vs Load Current



Long-Term Drift



Long-Term Drift (LS8)



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PIN FUNCTIONS

(TSOT-23/DFN)

GND* (Pin 1/Pin 3): Internal Function. This pin must be tied to ground.

GND (Pin 2/Pin 2): Device Ground.

NC (Pins 3, 5/Pins 1, 5): Not Internally Connected. May be tied to V_{IN}, V_{OUT}, GND or floated.

V_{IN} (Pin 4/Pin 6): Power Supply. The minimum supply varies with output load and voltage option, see the Dropout Voltage specification in the Electrical Characteristics table for further details. The maximum input voltage is 18V. Bypass V_{IN} with a 0.1µF capacitor to ground.

V_{OUT} (Pin 6/Pin 4): Output Voltage. A minimum output capacitor of 1µF is required for stable operation.

GND*(Exposed Pad Pin 7, DFN Only): This pin must be tied to ground.

(LS8)

NC (Pins 1, 2, 7): Not Internally Connected. May be tied to V_{IN}, V_{OUT}, GND or floated.

GND* (Pin 3): Internal Function. This pin must be tied to ground.

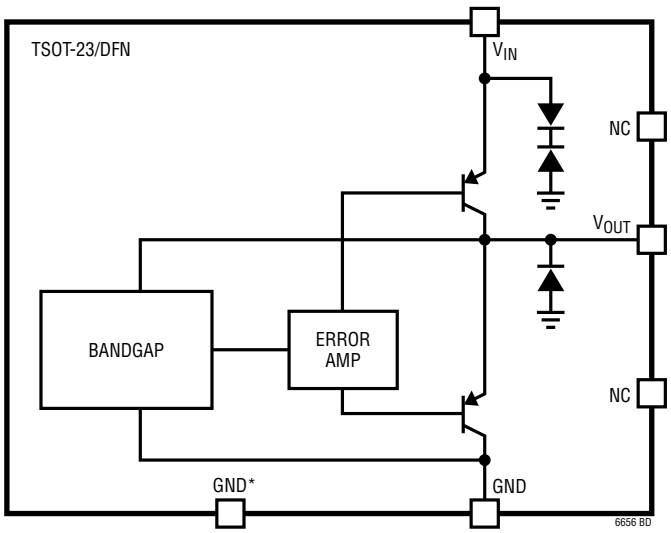
GND (Pin 4): Device Ground.

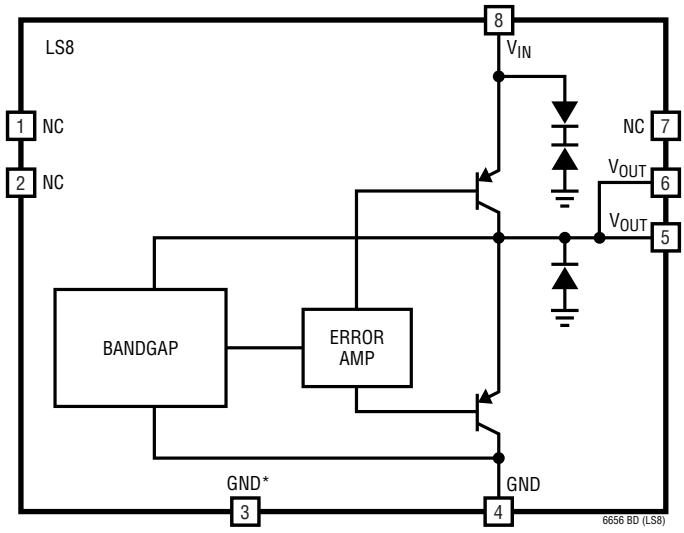
V_{OUT} (Pin 5): Output Voltage. A minimum output capacitor of 1µF is required for stable operation.

V_{OUT} (Pin 6): Output Voltage. Tie to pin 5 for best load regulation.

V_{IN} (Pin 8): Power Supply. Bypass V_{IN} with a 0.1µF capacitor to ground.

BLOCK DIAGRAM





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APPLICATIONS INFORMATION

Long Battery Life

Series references have a large advantage over shunt style references. Shunt references require a resistor from the power supply to operate. This resistor must be chosen to supply the maximum current that can be demanded by the load. When the load is not operating at this maximum current, the shunt reference must always sink this current, resulting in high dissipation and shortened battery life.

The LT6656 series reference does not require a current setting resistor and is specified to operate with any supply from 1.5V to 18V, depending on the output voltage option, load current and operating temperature (see Dropout Voltage and Minimum Input Voltage in the Typical Performance Characteristics). When the load does not demand current, the LT6656 reduces its dissipation and battery life is extended. If the reference is not delivering load current, it dissipates only a few µW, yet the same connection can deliver 5mA of load current when required.

Start-Up

To ensure proper start-up, the output voltage should be between –0.3V and the rated output voltage. If the output load may be driven more than 0.3V below ground, a low forward voltage schottky diode from the output to ground is required. The turn-on characteristics can be seen in Figure 1.

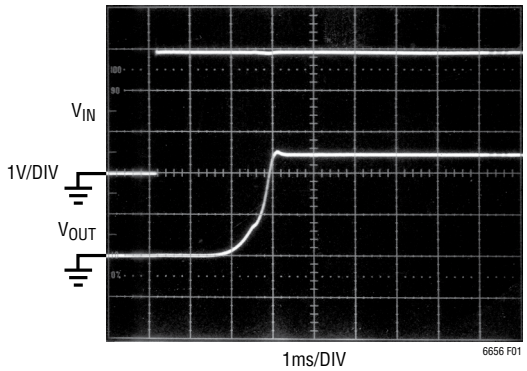

Figure 1. LT6656-2.5 Turn-On Characteristics, C_L = 1µF

Output Voltage Options

The performance of the LT6656 is consistent for the 2.048V to 5V options. The 1.25V option has slightly reduced load regulation, and unlike the higher voltage options, the minimum operating supply voltage is limited by internal circuitry rather than the output voltage.

Parameters that are based on changes in the output voltage, such as load regulation and hysteresis, remain proportional to the output voltage and are specified in relative units, for example, parts per million (ppm). Parameters that are not based on changes in the output voltage, such as supply current and reverse input current, are the same for all options.

The bandwidth of the LT6656 decreases with higher output voltage. This causes parameters that are affected by both bandwidth and output voltage, such as wideband noise and output impedance, to increase less with higher output voltage.

Bypass and Load Capacitance

The LT6656 voltage reference needs a 0.1µF input bypass capacitor placed within an inch of the input pin. An additional 2.2µF capacitor should be used when the source impedance of the input supply is high or when driving heavy loads. The bypassing of other local devices may serve as the required components. The output of the LT6656 requires a capacitance of 1µF or larger. The LT6656 is stable with a wide variety of capacitor types including ceramic, tantalum and electrolytic due to its low sensitivity to ESR (5Ω or less).

The test circuit in Figure 2 was used to test the response and stability of the LT6656 to various load currents. The resultant transient responses can be seen in Figure 3 and Figure 4. The large scale output response to a 500mV input step is shown in Figure 5 with a more detailed photo and description in the Output Settling section.

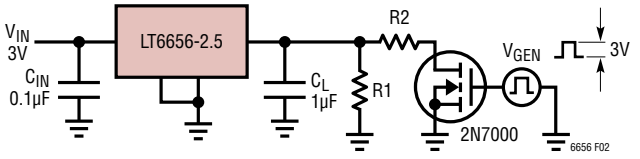

Figure 2. Transient Load Test Circuit

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APPLICATIONS INFORMATION

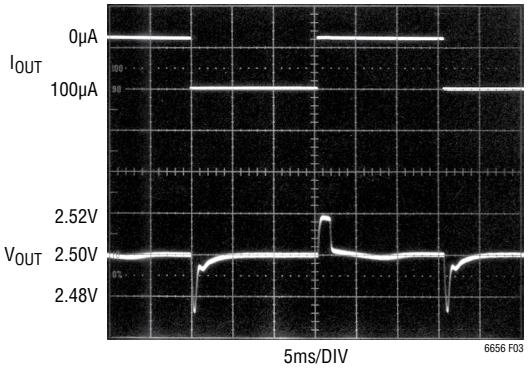

Figure 3. Transient Response, 0µA to 100µA Load Step (R2 = 24.9k, R1 = Open)

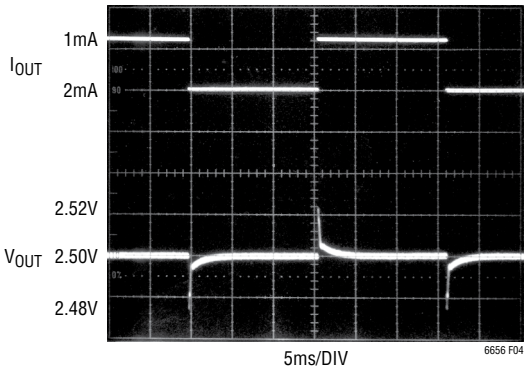

Figure 4. Transient Response, 1mA to 2mA Load Step (R1 = R2 = 2.49k)

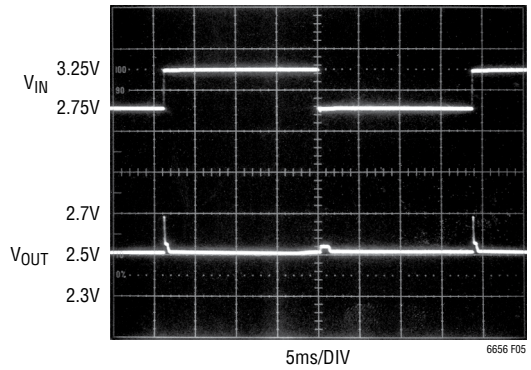

Figure 5. Output Response to 0.5V_{P-P} Step on V_{IN}, C_L = 1µF, I_L = 0

Output Settling

The output of the LT6656 is primarily designed to source current into a load, but is capable of sinking current to aid in output transient recovery. The output stage uses a class B architecture to minimize quiescent current and has a crossover dead band as the output transitions from sourcing to sinking current.

The settling time is typically less than 8ms for output loads up to 5mA, however the time required to settle when the load is turned off or in response to an input transient can be significantly longer due to the dead band (shown in Figure 7). During this interval the output stage is neither sourcing nor sinking current so the settling time is dominated by the ability of the application circuit to discharge the output capacitor to the voltage at which the sourcing circuitry in the output stage reactivates. Larger load currents will decrease the settling time and higher output capacitance will increase the settling time.

In application circuits where the LT6656 is experiencing a load step greater than 5µA, such as an ADC reference and supply implementation, the settling time will typically remain less than 8ms, regardless of the output settling from a previous load step.

The settling time can be estimated by the following equation:

$$\text{Settling time} \approx \frac{2(\text{Deadband})(C_L)}{I_L} + (V_{OUT})(0.8\text{ms/V})$$

The deadband is ≈7mV for the 2.5V option, is proportional to the voltage option (i.e., ≈14mV for the 5V option) and can double due to variations in processing.

The graph in Figure 6 shows the settling time versus load step with no load and with a constant 2µA load applied. Note the settling time can be longer with load steps that are not large enough to activate the sinking side of the output stage.

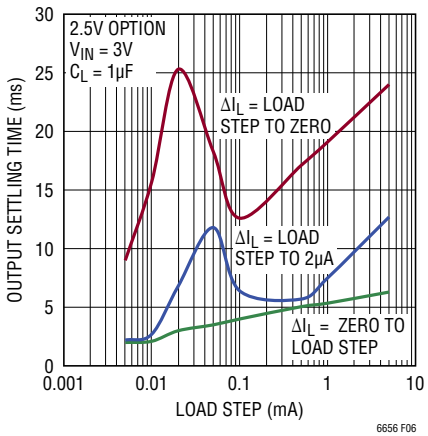

Figure 6. Output Settling Time to 0.05% vs Load Step

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APPLICATIONS INFORMATION

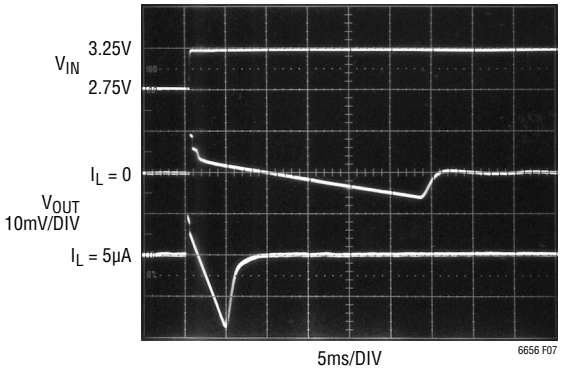

Figure 7. Detailed Output Response to a 0.5V Input Step, $C_{IN} = C_L = 1\mu F$

The photo in Figure 7 shows the output response to a 0.5V input step in both a no-load and 5µA load condition. In the no-load condition only the bias current of the internal bandgap reference (about 400nA) is available to discharge the output capacitor.

Output Noise

Low frequency noise is proportional to the output voltage and is insensitive to output current and moderate levels of output capacitance.

Wideband noise increases less with higher output voltage and is proportional to the bandwidth of the output stage, increasing with higher load current and lower output capacitance.

Peaking in the noise response is another factor contributing to the output noise level for a given frequency range. Noise peaking can be reduced by increasing the size of the output capacitor when driving heavier loads, or conversely, reducing the size of the output capacitor when driving lighter loads. Noise plots in the Typical Performance Curves section show noise spectrum with various load currents and output capacitances.

Internal Protection

The LT6656 incorporates several internal protection features that make it ideal for use in battery powered systems. Reverse input protection limits the input current to typically less than 40µA when either the LT6656 or the battery is installed backwards. In systems where the output can be held up by a backup battery with the input pulled to ground, the reverse output protection of the LT6656 limits the output current to typically less than 30µA. The current versus reverse voltage is shown in the Typical Performance Characteristics section.

Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. A more realistic way to determine long-term drift is to measure it over the time interval of interest. The LT6656 drift data was taken over 100 parts that were soldered onto PC boards in a typical application configuration. The boards were then placed into a constant temperature oven with T_A = 30°C, their outputs scanned regularly and measured with an 8.5 digit DVM. The parts chosen in the Long Term Drift curves in the Typical Performance Characteristics section represent high, low and typical units.

Hysteresis

Hysteresis on the LT6656 is measured in two steps, for example, from 25°C to –40°C to 25°C, then from 25°C to 85°C to 25°C, for the industrial temperature range. After preconditioning by one thermal cycle, this two-step cycle is repeated several times and the maximum hysteresis from all the partial cycles is noted.

Results over both commercial and industrial temperature ranges are shown in Figure 8 and Figure 9. The parts cycled over the higher temperature range have a higher hysteresis than those cycled over the lower range.

Power Dissipation

The LT6656 will not exceed the maximum junction temperature when operating within its specified temperature range of –40°C to 85°C, maximum input voltage of 18V and specified load current of 5mA.

IR Reflow Shift

The different expansion and contraction rates of the materials that make up the LT6656 package may induce small stresses on the die that can cause the output to shift

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APPLICATIONS INFORMATION

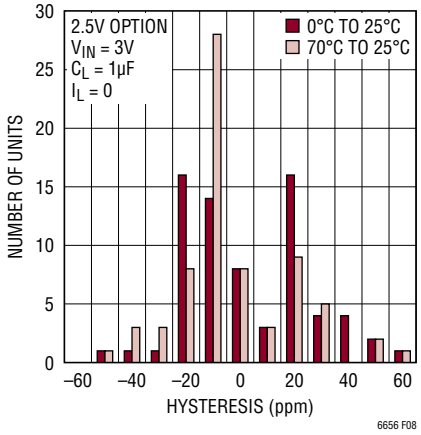

Figure 8. LT6656 S6, DC 0°C to 70°C Hysteresis

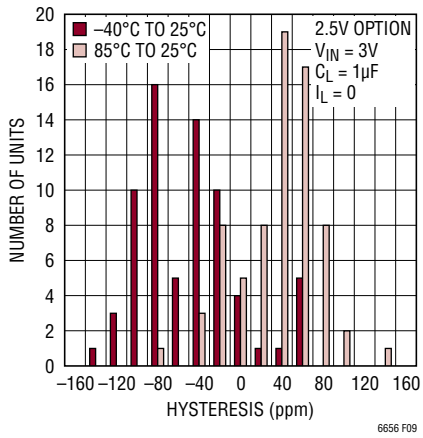

Figure 9. LT6656 S6, DC –40°C to 85°C Hysteresis

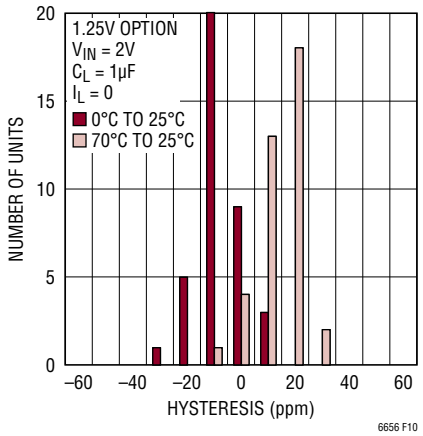

Figure 10. LT6656 LS8 0°C to 70°C Hysteresis

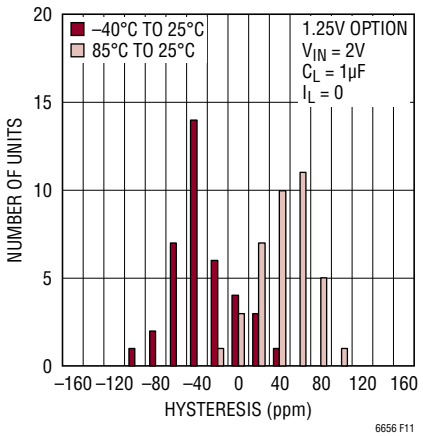

Figure 11. LT6656 LS8 –40°C to 85°C Hysteresis

during IR reflow. Common lead free IR reflow profiles reach over 250°C, considerably more than lead solder profiles. The higher reflow temperature of the lead free parts exacerbates the issue of thermal expansion and contraction causing the output shift to generally be greater than with a leaded reflow process.

The lead free IR reflow profile used to experimentally measure the output voltage shift in the LT6656-2.5 is shown in Figure 12. Similar results can be expected using a convection reflow oven. Figure 13 and Figure 14 show the change in output voltage that was measured for parts that were run through the reflow process for 1 cycle and also 3 cycles. Additional drift of the LT6656 after IR reflow does not vary significantly.

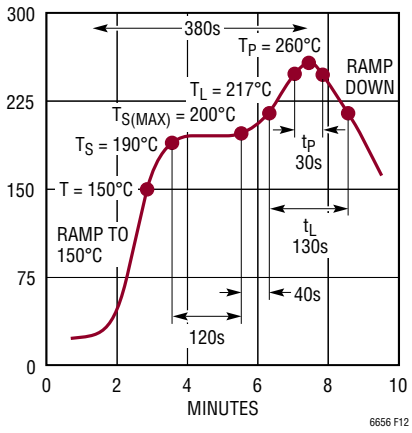

Figure 12. Lead Free Reflow Profile Due to IR Reflow

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APPLICATIONS INFORMATION

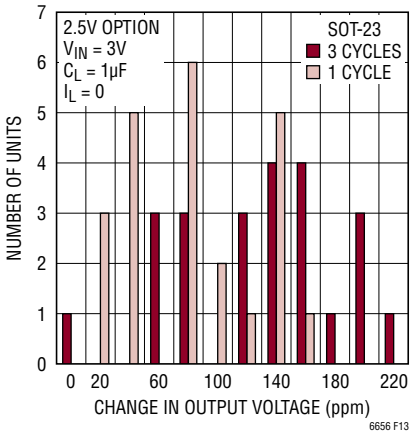

Figure 13. ΔV_{OUT} Due to IR Reflow, Peak Temperature = 260°C, SOT-23

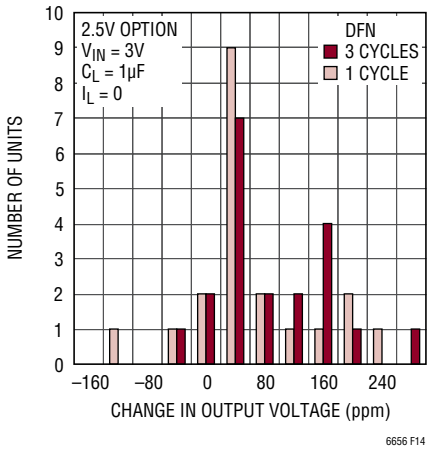

Figure 14. ΔV_{OUT} Due to IR Reflow, Peak Temperature = 260°C, DFN

PC Board Layout

The mechanical stress of soldering a surface mount voltage reference to a PC board can cause the output voltage to shift and temperature coefficient to change.

To reduce the effects of stress-related shifts, position the reference near the short edge of the PC board or in a corner. In addition, slots can be cut into the board on two sides of the device. See Application Note AN82 for more information. http://www.linear.com

The input and output capacitors should be mounted close to the package. The GND and V_{OUT} traces should be as short as possible to minimize the voltage drops caused by load and ground currents. Excessive trace resistance directly impacts load regulation.

Humidity Sensitivity

Plastic mold compounds absorb water. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside, which can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern. However, PC board material may absorb water and apply mechanical stress to the LT6656LS8. Proper board materials and layout are essential.

For best stability, the PC board layout is critical. Change in temperature and position of the PC board, as well as aging, can alter the mechanical stress applied to components soldered to the board. FR4 and similar materials also absorb water, causing the board to swell. Even conformal coating or potting of the board does not always eliminate this effect, though it may delay the symptoms by reducing the rate of absorption. Removing power and ground planes in the PC board under the voltage reference can improve the stability significantly.

Figure 15 shows a tab cut through the PC board on three sides of an LT6656, which significantly reduces stress on the IC, as described in Application Note 82.

An additional advantage of slotting the PC board is that the LT6656 is thermally isolated from surrounding circuitry. This can help reduce thermocouple effects and improve accuracy.

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APPLICATIONS INFORMATION

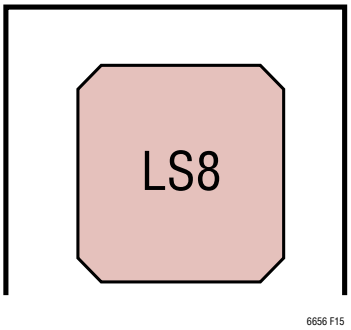

Figure 15. 3-Sided PCB Cutout

TYPICAL APPLICATIONS

Regulator Reference

The robust input and output of the LT6656 along with its high output current make it an excellent precision low power regulator as well as a reference. The LT6656 would be a good match with a small, low power microcontroller. Using the LT6656 as a regulator reduces power consumption, decreases solution size and increases the accuracy of the microcontroller's on board ADC.

Low Power ADC Reference

Low power ADCs draw only a few µAs during their idle period and well over 100µA during conversions. Despite these surges of current, the ADC in reality can have very low power consumption. Figure 17 shows the LTC2480, a low power delta sigma ADC. When the ADC is disabled its quiescent current (I_Q) is roughly 1µA, during conversion the I_Q jumps up to 160µA. In reality, the power consumption is not only based on the I_Q during conversion, but the real power consumption of the ADC is set by the conversion time and the sample rate. The LTC2480 shown in Figure 17 has a conversion time of 160ms which sets the maximum sample rate of 6 samples per second. The maximum sample rate also sets the maximum current consumption to 160µA, but at slower sample rates the ADC will have significantly lower average current draw. If the ADC is sampled at 1 sample per second the average current drawn by the ADC during a 1 second interval would only be 26.4µA. When taking into consideration the current drawn by the reference, the total current draw is only 27.4µA. This system is greatly simplified because the precision reference does not need to be cycled on and off to save power. Furthermore, leaving the reference on continuously eliminates concern for turn-on settling time.

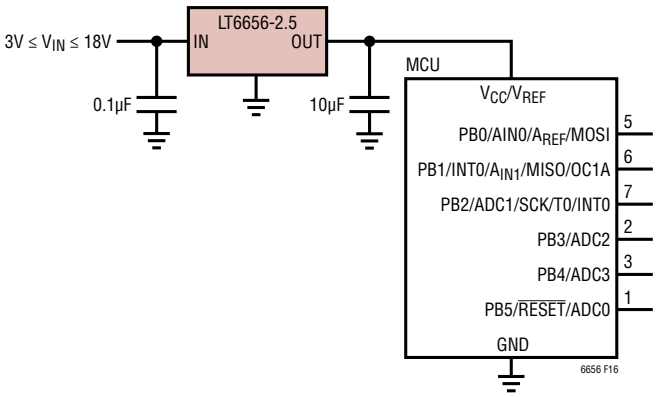

Figure 16. Microcontroller Reference and Regulator

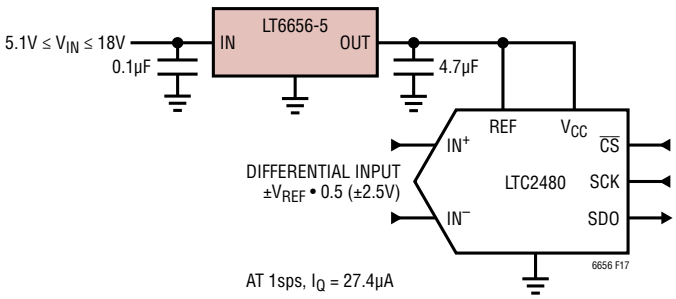

Figure 17. Low Power ADC Reference

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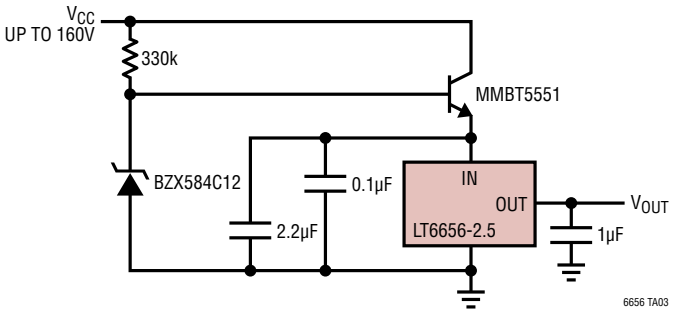
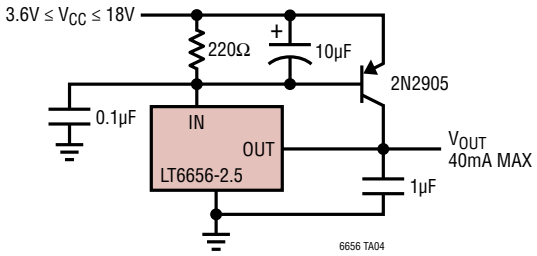
TYPICAL APPLICATIONS

Extended Supply Range Reference



Boosted Output Current Reference



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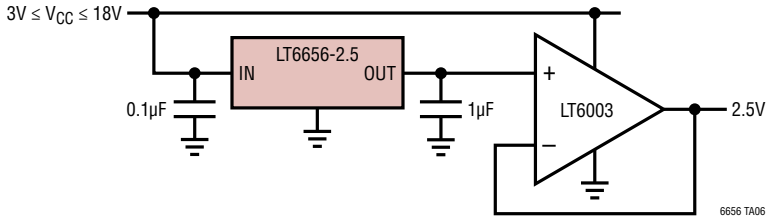
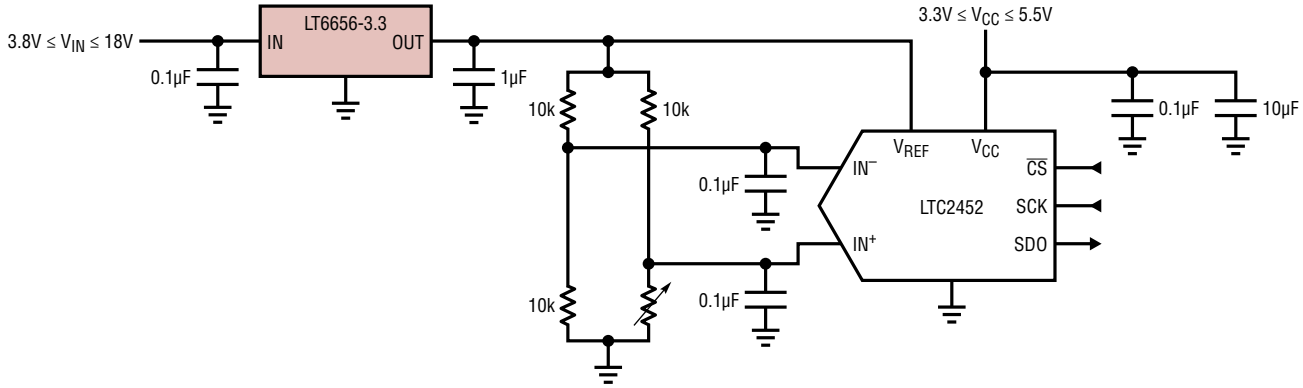
TYPICAL APPLICATIONS

Micropower Regulator, I_Q = 2µA, Sink Up to 8mA



ADC Reference and Bridge Excitation Supply



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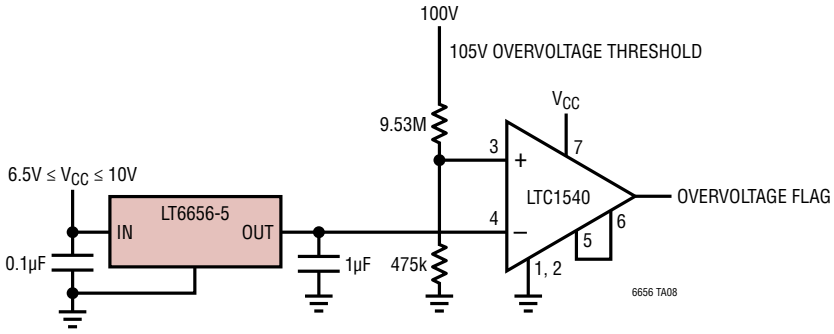
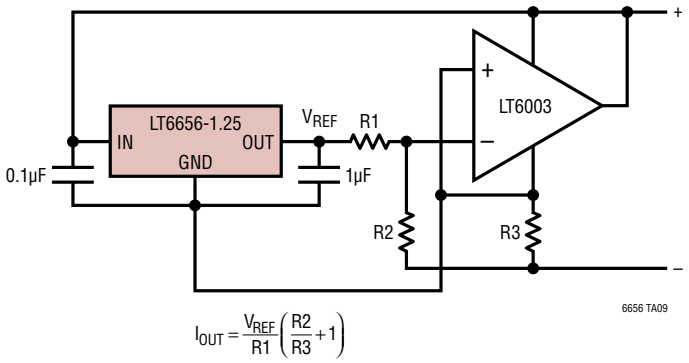
TYPICAL APPLICATIONS

Low Power Precision High Voltage Supply Monitor, I_Q = 1.4µA, High Voltage Supply Load = 10µA

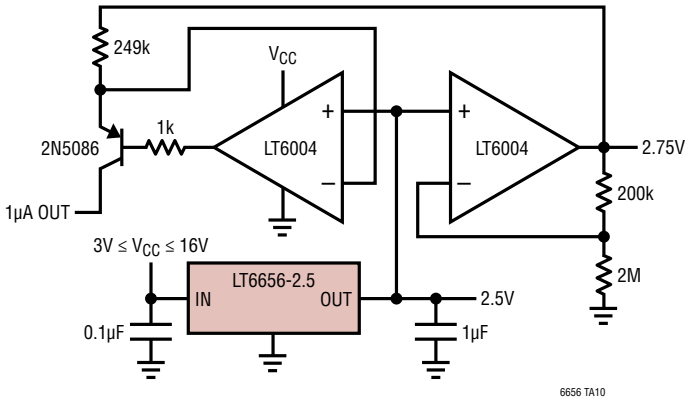


2-Terminal Current Source



$$I_{OUT} = \frac{V_{REF}}{R1}\left(\frac{R2}{R3}+1\right)$$

Precision Current and Boosted Reference, I_Q = 5.5µA



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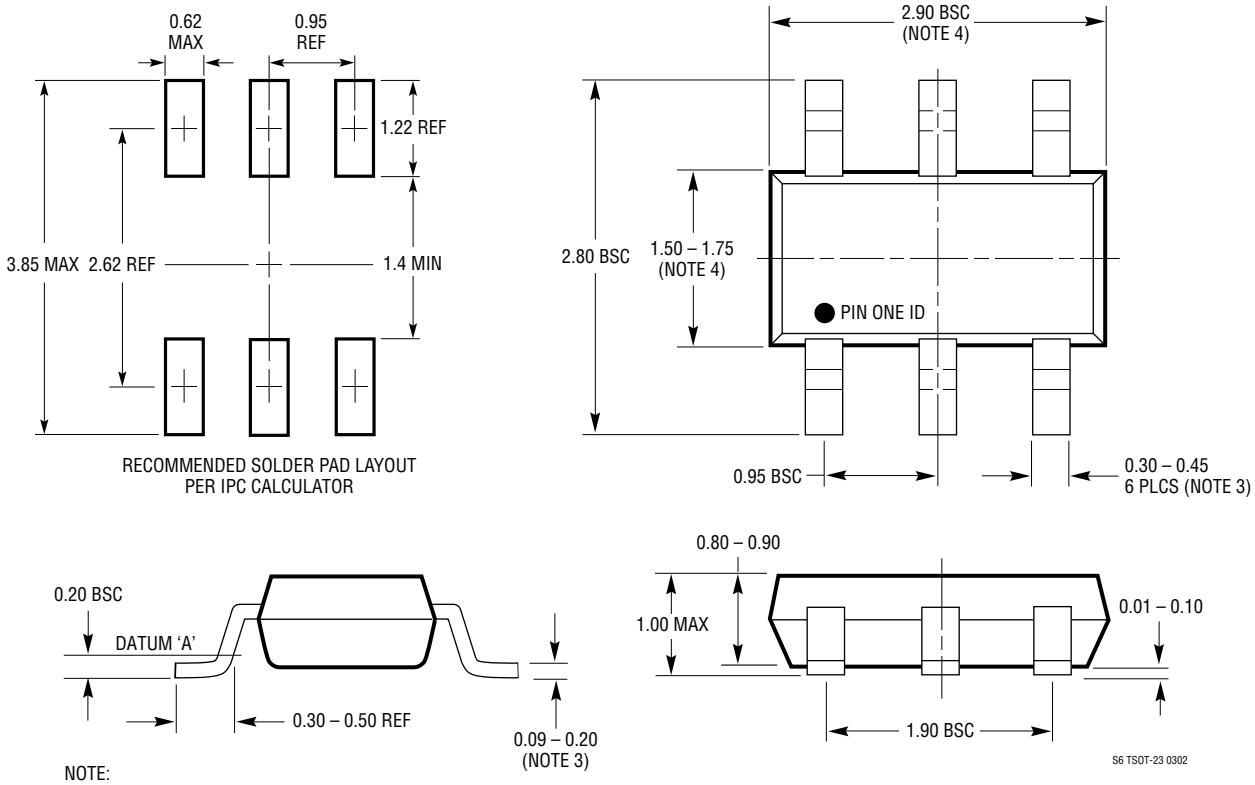
PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

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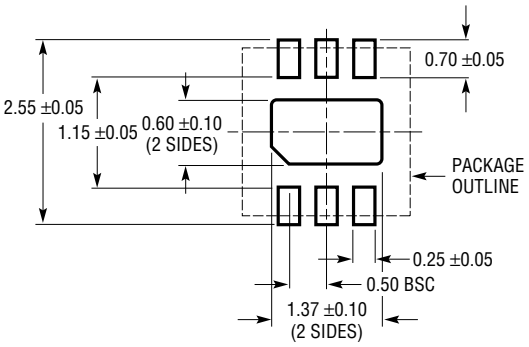
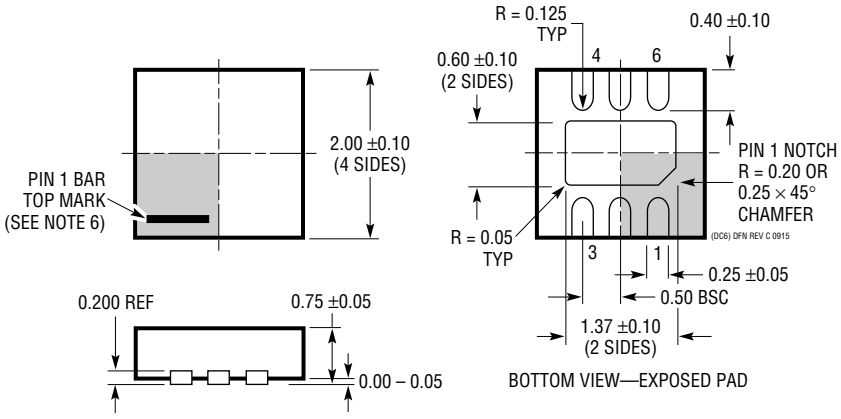
PACKAGE DESCRIPTION

DC6 Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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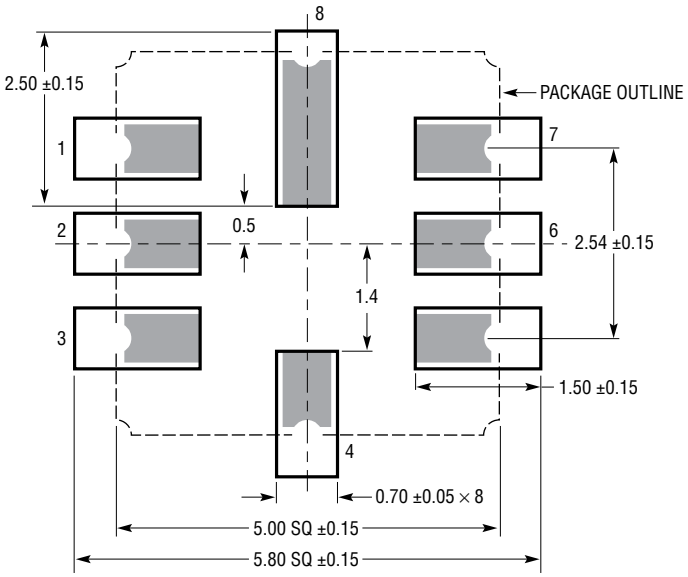
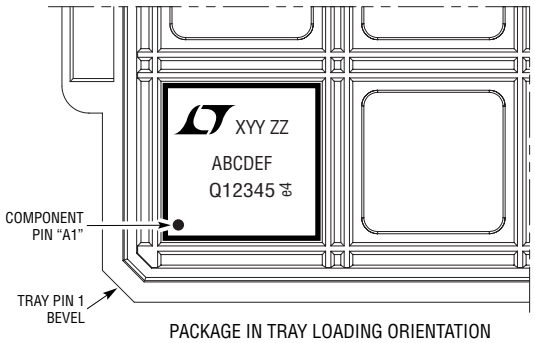
PACKAGE DESCRIPTION

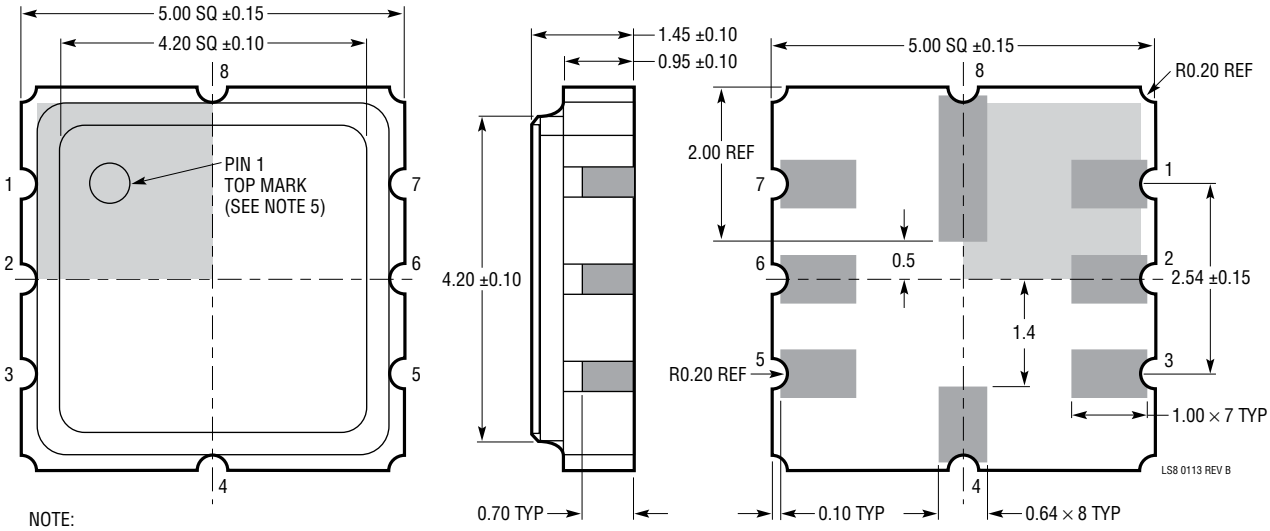
LS8 Package
8-Pin Leadless Chip Carrier (5mm × 5mm)
(Reference LTC DWG # 05-08-1852 Rev B)



APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



PACKAGE IN TRAY LOADING ORIENTATION



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS
   PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/10	Voltage options added (1.25, 2.048, 3, 3.3), reflected throughout the data sheet.	1 to 18
B	05/11	Added 6-lead DFN package reflected throughout the data sheet.	1 to 20
C	11/13	Addition of 1.25V option in the LS8 package.	1 to 4
		Note 10 updated with additional explanation of hysteresis.	6
		Pin Functions updated to show pin numbers and LS8 package.	10
		Block Diagram updated to show pin numbers and LS8 package.	10
		Hysteresis section updated with additional explanation.	13
		Hysteresis graphs updated for SOT23 and LS8 packages.	14
		New section added for Humidity Sensitivity.	15, 16
D	05/21	Additon of the 2.8V option in the DFN package.	1, 3, 4, 5
		Removal of statements under Humidity Sensitivity (3rd paragraph).	15
		Change Figure 15a to Figure 15 and remove Figure 15b.	15, 16
		Adding more related part numbers and descriptions in the Related Parts table.	24

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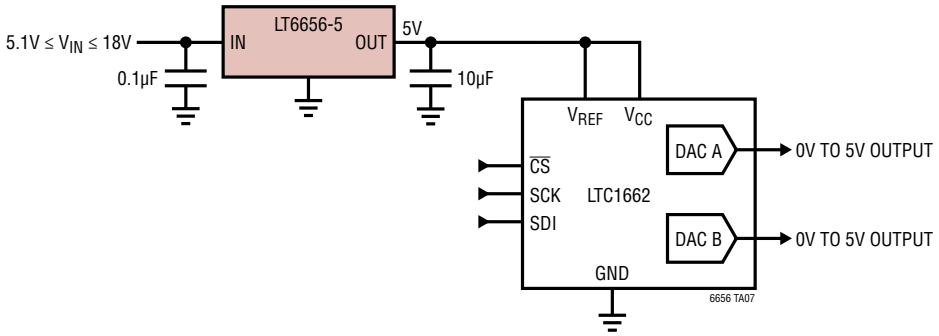
TYPICAL APPLICATION

Reference Regulator for Micropower DAC, Total I_Q = 4.8µA



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1389	Nanopower Precision Shunt Voltage Reference	0.05% Max 10ppm/°C Max, 800nA Supply
LTC1440	Micropower Comparator with Reference	3.7µA Max Supply Current, 1% 1.182V Reference, MSOP, PDIP and SO-8 Packages
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages
LT1461	Micropower Precision LDO Series Reference	3ppm/°C Max Drift, 0°C to 70°C, –40°C to 85°C, –40°C to 125°C Options in SO-8
LT1495	1.5µA Precision Rail-to-Rail Dual Op Amp	1.5µA Max Supply Current, 100pA Max IOS
LTC1540	Nanopower Comparator with Reference	600nA Max Supply Current, 2% 1.182V Reference, MSOP and SO-8 Packages
LT1634	Micropower Precision Shunt Voltage Reference	0.05% Max, 10ppm/°C Max Drift, 1.25V, 2.5V, 4.096V, 5V, 10µA Maximum Supply Current
LT1790	Micropower Precision Series Reference	0.05% Max, 10ppm/°C Max, 60µA Supply, SOT23 Package
LTC1798	6µA Low Dropout Series Reference	Available in Adjustable, 2.5V, 3V, 4.096V and 5V
LT6003	1.6V, 1µA Precision Rail-to-Rail Op Amp	1µA Max Supply Current, 1.6V Minimum Operating Voltage, SOT-23 and DFN Packages
LT6650	Micropower Reference with Buffer Amplifier	0.05% Max, 5.6µA Supply, SOT-23 Package
LT6660	Tiny Micropower Series Reference	0.2% Max, 20ppm/°C Max, 20mA Output Current, 2mm × 2mm DFN
LT6700	Micropower, Low Voltage Dual Comparator with 40mV Reference	6.5µA Supply Current, 1.4V Minimum Operating Voltage
ADR3425	Micropower, High-Accuracy Voltage Reference	100µA Supply Current, ±0.1% Max Initial Accuracy, 8ppm/°C Max drift
ADR3525	Micropower, Precision, Auto Qualified Voltage Reference	AEC-Q100, 100µA Supply Current, ±0.1% Max Initial Accuracy, 5ppm/°C B-Grade Max Drift
ADR5041	Precision Micropower Shunt Mode Voltage Reference	AEC-Q100, SC70 or SOT-23 Package, 50µA to 15mA Supply Current, No External Capacitor Required
AD4000/ AD4001	16-Bit, 2Msps Precision Pseudo Differential or Differential SAR ADC	INL: ±1.0LSB Maximum; 7mW/Msps, 70µW at 10ksps, 14mW at 2Msps from V_{DD} Only
LTC2376-16/ LTC2378-16	18-Bit, 250ksps, Low Power SAR ADC with 102dB SNR	±1.75LSB INL (Max), 2.5V Supply, 3.4mW at 250ksps
LTC2400	24-Bit µPower No Latency ΔΣ™ ADC in SO-8	200µA Supply Current, 12.5% Overrange and Underrange, 50Hz/60Hz Notch Filter with 110dB Min Attenuation
AD7980	16-Bit, 1Msps, PulSAR ADC in MSOP/LFCSP	INL: ±0.6LSB Typ, ±1.25LSB Max, 2.5V Supply with 1.8V/2.5V/3V/5V Logic Interface, 4mW at 1Msps (V_{DD} Only)
AD4695/ AD4696	16-Channel 16-Bit 500ksps SAR ADC	8mW at f_S = 1Msps (AD4696), 4mW at f_S = 500ksps (AD4695 and AD4696)

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