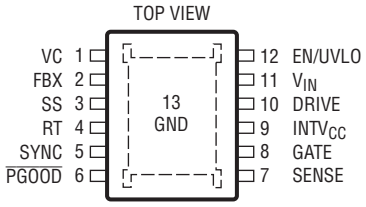
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} 42V
EN/UVLO (Note 2).....42V
DRIVE 42V
$\overline{PGOOD}$.....42V
$INTV_{CC}$.....8V
GATE ..... (Note 3)
SYNC 8V
VC, SS.....3V
RT 1.5V
SENSE.....±0.3V
FBX ..... –3V to 3V
Operating Junction Temperature Range (Note 4)
LT3759E/LT3759I ..... –40°C to 125°C
LT3759H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

θ_{JA} = 35°C/W TO 40°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3759EMSE#PBF	LT3759EMSE#TRPBF	3759	12-Lead Plastic MSOP	–40°C to 125°C
LT3759IMSE#PBF	LT3759IMSE#TRPBF	3759	12-Lead Plastic MSOP	–40°C to 125°C
LT3759HMSE#PBF	LT3759HMSE#TRPBF	3759	12-Lead Plastic MSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, EN/UVLO = 12V, $INTV_{CC}$ = 4.75V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage		●	1.6		42	V
V_{IN} Shutdown I_Q	EN/UVLO < 0.4V EN/UVLO = 1.15V			0.1	1 6	µA µA
V_{IN} Operating I_Q				350	450	µA
DRIVE Shutdown Quiescent Current	EN/UVLO < 0.4V EN/UVLO = 1.15V			0.1 0.1	1 2	µA µA
DRIVE Quiescent Current (Not Switching)	R_T = 27.4kΩ, DRIVE = 6V			2.0	2.5	mA
SENSE Current Limit Threshold		●	46	50	54	mV
SENSE Input Bias Current	Current Out of Pin			–55		µA
Error Amplifier						
FBX Regulation Voltage ($V_{FBX(REG)}$)	FBX > 0V FBX < 0V	● ●	1.580 –0.815	1.6 –0.80	1.620 –0.785	V V
FBX Pin Input Current	FBX = 1.6V FBX = –0.8V		 –10	60	120 10	nA nA
Transconductance g_m ($\Delta I_2/\Delta V_{FBX}$)	FBX = $V_{FBX(REG)}$			240		µs
VC Output Impedance				5		MΩ
FBX Line Regulation [$\Delta V_{FBX(REG)}/(\Delta V_{IN} \bullet V_{FBX(REG)})$]	1.6V < V_{IN} < 42V, FBX >0 1.6V < V_{IN} < 42V, FBX <0			0.02 0.02	0.05 0.05	%/V %/V
VC Current Mode Gain ($\Delta V_{VC}/\Delta V_{SENSE}$)				5		V/V
VC Source Current	FBX = 0V, VC = 1.3V			–13		µA
VC Sink Current	FBX = 1.7V, VC = 1.3V FBX = –0.85V, VC = 1.3V			13 10		µA µA
Oscillator						
Switching Frequency	R_T = 27.4k to GND, V_{FBX} = 1.6V R_T = 86.6k to GND, V_{FBX} = 1.6V R_T = 6.81k to GND, V_{FBX} = 1.6V		270	300 100 1000	330	kHz kHz kHz
R_T Voltage	FBX = 1.6V, –0.8V			1.2		V
GATE Minimum Off-Time				170	200	ns
GATE Minimum On-Time				170	200	ns
SYNC Input Low		●			0.4	V
SYNC Input High		●	1.5			V
SS Pull-Up Current	SS = 0V, Current Out of Pin	●	–14	–10.5	–7	µA
Low Dropout Regulators (DRIVE LDO and V_{IN} LDO)						
DRIVE LDO Regulation Voltage	DRIVE = 6V	●	4.6	4.75	4.9	V
V_{IN} LDO Regulation Voltage	DRIVE = 0V	●	3.6	3.75	3.9	V
DRIVE LDO Current Limit	$INTV_{CC}$ = 4V			60		mA
V_{IN} LDO Current Limit	DRIVE = 0V, $INTV_{CC}$ = 3V			60		mA
DRIVE LDO Load Regulation ($\Delta V_{INTVCC}/V_{INTVCC}$)	0 < I_{INTVCC} < 20mA, DRIVE = 6V		–1	–0.6		%
V_{IN} LDO Load Regulation ($\Delta V_{INTVCC}/V_{INTVCC}$)	DRIVE = 0V, 0 < I_{INTVCC} < 20mA		–1	–0.6		%
DRIVE LDO Line Regulation [$\Delta V_{INTVCC}/(V_{INTVCC} \bullet \Delta V_{IN})$]	1.6V < V_{IN} < 42V, DRIVE = 6V			0.03	0.07	%/V
V_{IN} LDO Line Regulation [$\Delta V_{INTVCC}/(V_{INTVCC} \bullet \Delta V_{IN})$]	DRIVE = 0V, 5V < V_{IN} < 42V			0.03	0.07	%/V
DRIVE LDO Dropout Voltage ($V_{DRIVE} - V_{INTVcc}$)	DRIVE = 4V, I_{INTVCC} = 20mA	●		190	400	mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, EN/UVLO = 12V, $INTV_{CC}$ = 4.75V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} LDO Dropout Voltage (V_{IN} – V_{INTVcc})	V_{IN} = 3V, DRIVE = 0V, I_{INTVCC} = 20mA	●		190	400	mV
$INTV_{CC}$ Undervoltage Lockout Threshold Falling				1.3	1.45	V
$INTV_{CC}$ Current in Shutdown	EN/UVLO = 0V			22		µA
Logic						
EN/UVLO Threshold Voltage Falling		●	1.17	1.22	1.27	V
EN/UVLO Rising Hysteresis				20		mV
EN/UVLO Input Low Voltage	I_{VIN} < 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		1.8	2.2	2.6	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.30V			10	100	nA
FBX Power Good Threshold Voltage	FBX > 0V, $\overline{PGOOD}$ Falling FBX < 0V, $\overline{PGOOD}$ Falling			$V_{FBX(REG)}$ – 0.08 $V_{FBX(REG)}$ + 0.04		V V
FBX Overvoltage Threshold	FBX > 0V, $\overline{PGOOD}$ Rising FBX < 0V, $\overline{PGOOD}$ Rising			$V_{FBX(REG)}$ + 0.12 $V_{FBX(REG)}$ – 0.06		V V
$\overline{PGOOD}$ Output Low (V_{OL})	$I_{\overline{PGOOD}}$ = 250µA			210	300	mV
$\overline{PGOOD}$ Leakage Current	$\overline{PGOOD}$ = 42V				1	µA
$INTV_{CC}$ Minimum Voltage to Enable $\overline{PGOOD}$ Function		●	2.4	2.7	3.0	V
$INTV_{CC}$ Minimum Voltage to Enable SYNC Function		●	2.4	2.7	3.0	V
NMOS Gate Drivers						
GATE Output Rise Time (T_R)	C_L = 3300pF			20		ns
GATE Output Fall Time (T_F)	C_L = 3300pF			20		ns
GATE Output Low (V_{OL})					0.05	V
GATE Output High (V_{OH})			$INTV_{CC}$ – 0.05			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: For V_{IN} below 4V, the EN/UVLO pin must not exceed V_{IN} for proper operation.

Note 3: This pin is for switching purposes. Do not tie directly to a supply.

Note 4: The LT3759E is guaranteed to meet performance specifications from the 0°C to 125°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3759I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3759H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 5: The LT3759 is tested in a feedback loop which servos V_{FBX} to the reference voltages (1.6V and –0.8V) with the VC pin forced to 1.3V.

Note 6: Rise and fall times are measured at 10% and 90% levels.

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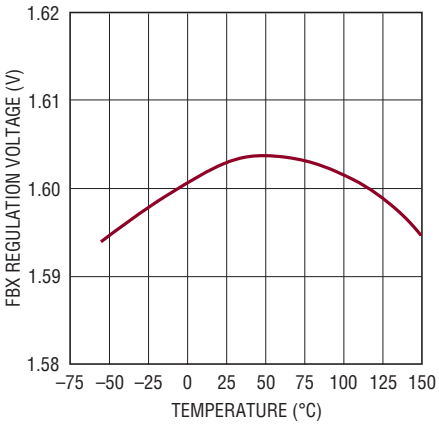
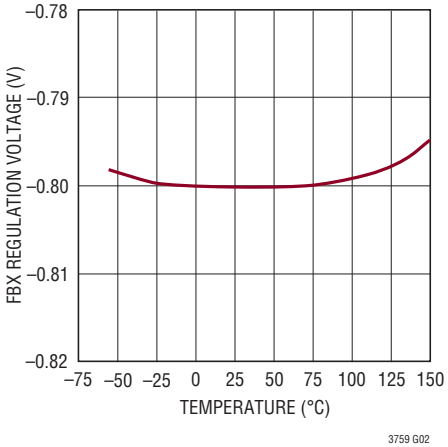
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

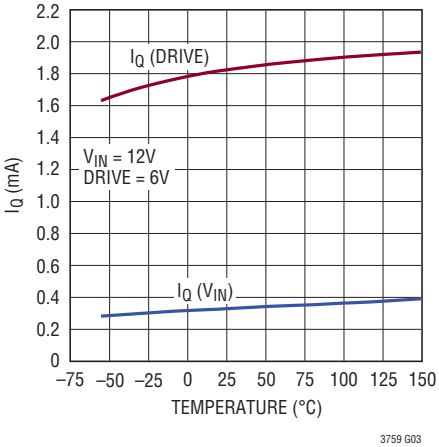
FBX Positive Regulation Voltage vs Temperature



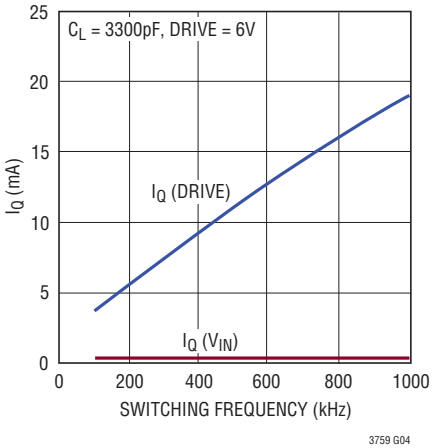
FBX Negative Regulation Voltage vs Temperature



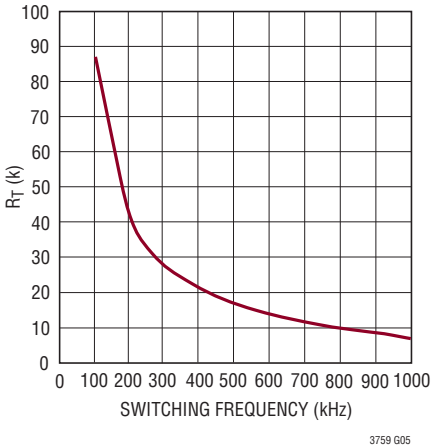
Quiescent Current vs Temperature



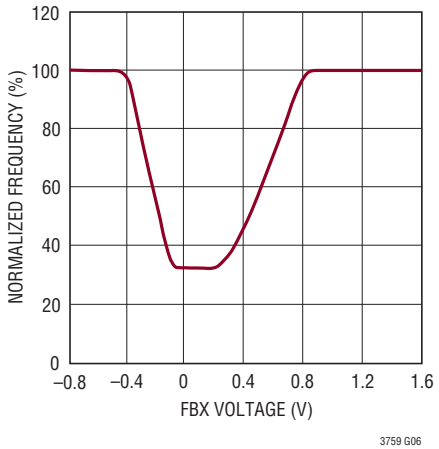
Dynamic Quiescent Current vs Switching Frequency



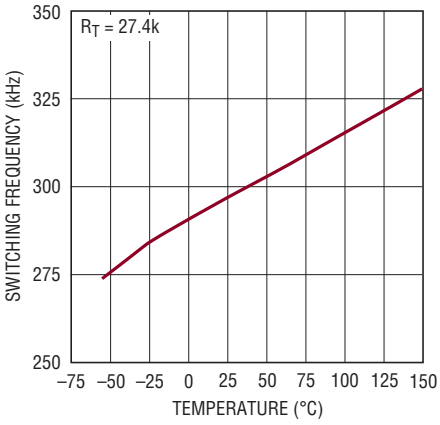
R_T vs Switching Frequency



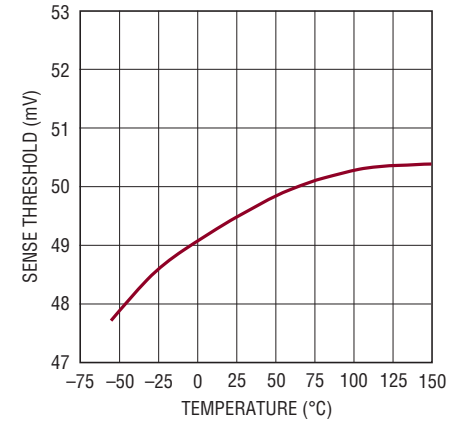
Normalized Switching Frequency vs FBX Voltage



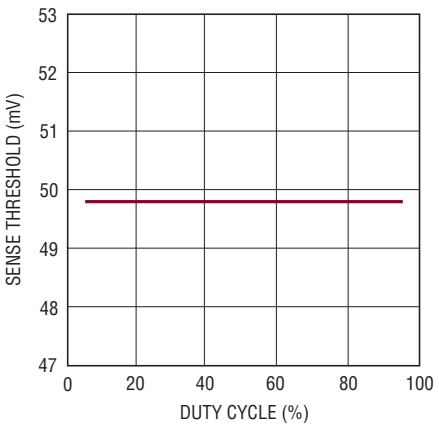
Switching Frequency vs Temperature



SENSE Current Limit Threshold vs Temperature



SENSE Current Limit Threshold vs Duty Cycle



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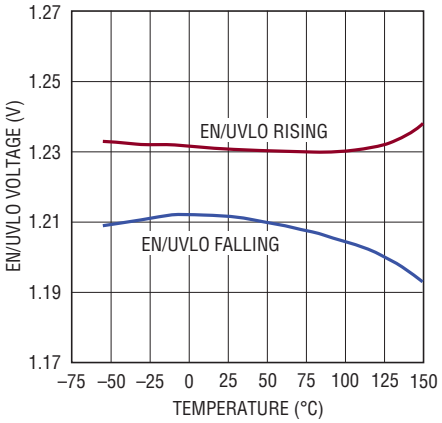
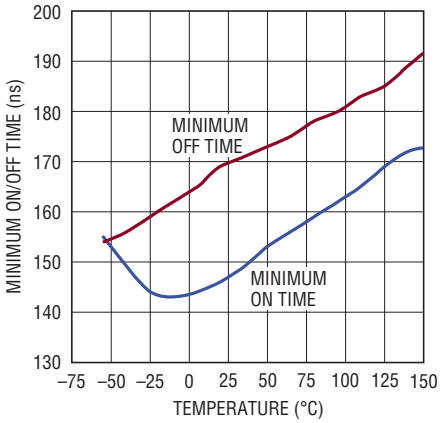
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

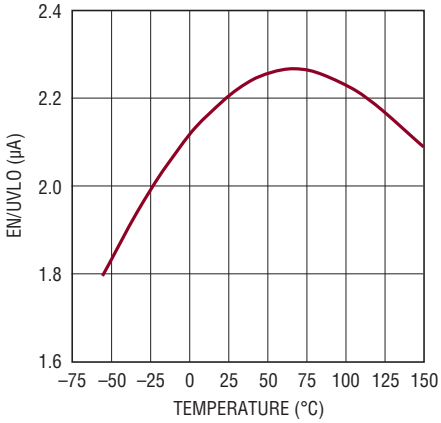
EN/UVLO Threshold vs Temperature



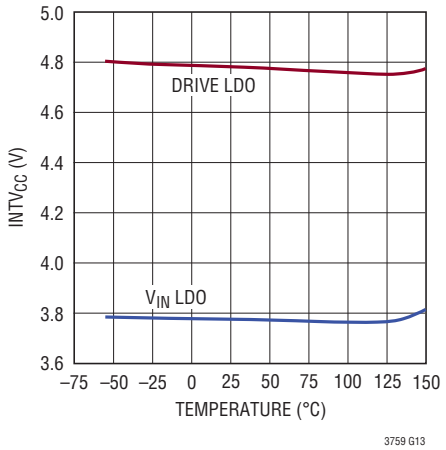
GATE Minimum On- and Off-Times vs Temperature



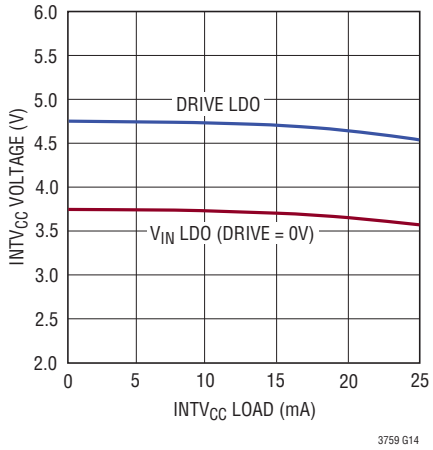
EN/UVLO Hysteresis Current vs Temperature



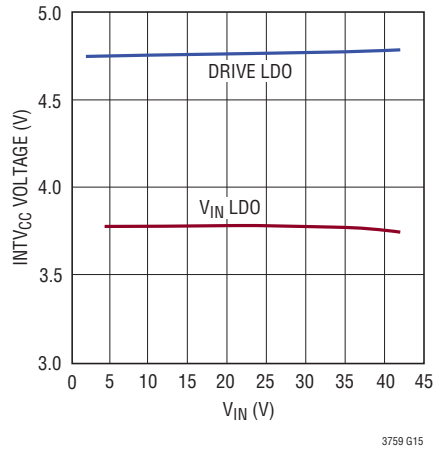
$INTV_{CC}$ vs Temperature



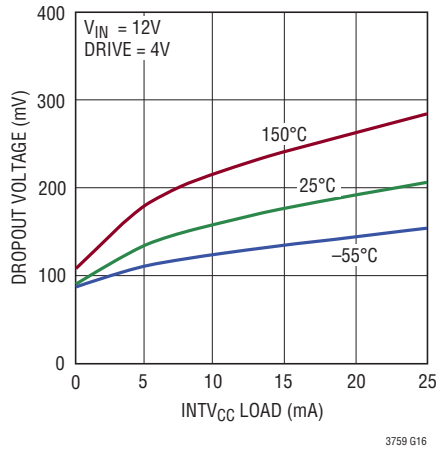
$INTV_{CC}$ Load Regulation



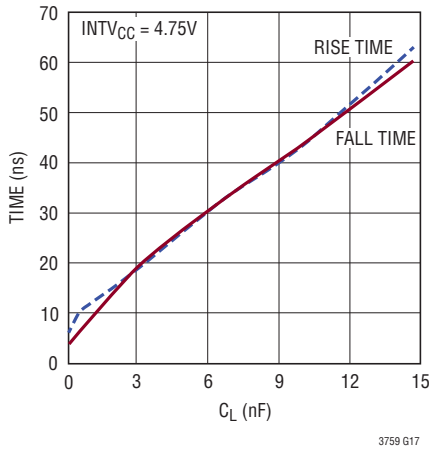
$INTV_{CC}$ Line Regulation



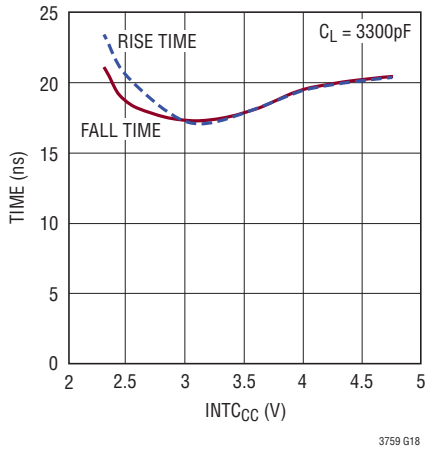
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



Gate Driver Rise and Fall Time vs C_L



Gate Driver Rise and Fall Time vs $INTV_{CC}$



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PIN FUNCTIONS

DRIVE: DRIVE LDO Supply Pin. This pin can be connected to either V_{IN} or a quasi-regulated voltage supply such as a DC converter output. This pin must be bypassed with a minimum of 1µF capacitor placed close to the pin. Tie this pin to V_{IN} if not used.

EN/UVLO: Shutdown and Undervoltage Detect Pin. An accurate 1.22V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2.2µA pull-down current. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

FBX: Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and GND. FBX is the input of two error amplifiers—one configured to regulate a positive output; the other, a negative output. Depending upon topology selected, switching causes the output to ramp positive or negative. The appropriate amplifier takes control while the other becomes inactive. Additionally FBX is input for two window comparators that indicate through the $\overline{PGOOD}$ pin when the output is within 5% of the regulation voltages. FBX also modulates the switching frequency during start-up and fault conditions when FBX is close to GND.

GATE: N-Channel FET Gate Driver Output. Switches between $INTV_{CC}$ and GND. Driven to GND when IC is shut down, during thermal lockout or when $INTV_{CC}$ is below undervoltage threshold.

GND: Exposed Pad. Solder the exposed pad directly to ground plane.

$INTV_{CC}$: Regulated Supply for Internal Loads and Gate Driver. Regulated to 4.75V if powered from DRIVE or regulated to 3.75V if powered from V_{IN}. The $INTV_{CC}$ pin must be bypassed with a minimum of 4.7µF capacitor placed close to the pin.

$\overline{PGOOD}$: Output Ready Status Pin. An open-collector pull down on $\overline{PGOOD}$ asserts when $INTV_{CC}$ is greater than 2.7V and the FBX voltage is within 5% (80mV if V_{FBX} = 1.6V or 40mV if V_{FBX} = –0.8V) of the regulation voltage.

RT: Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND. Do not leave the RT pin open.

SENSE: The Current Sense Input for the Control Loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor in the source of the N-FET. The negative terminal of the current sense resistor should be connected to GND plane close to the IC.

SS: Soft-Start Pin. This pin modulates compensation pin voltage (VC) clamp. The soft-start interval is set with an external capacitor. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to GND by an EN/UVLO undervoltage condition, an $INTV_{CC}$ undervoltage condition or an internal thermal lockout.

SYNC: Frequency Synchronization Pin. Used to synchronize the internal oscillator to an outside clock. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. Tie the SYNC pin to GND if this feature is not used. This signal is ignored during FB frequency foldback or when $INTV_{CC}$ is less than 2.7V.

VC: Error Amplifier Compensation Pin. Used to stabilize the voltage loop with an external RC network.

V_{IN}: Supply Pin for Internal Leads and the V_{IN} LDO Regulator of $INTV_{CC}$. Must be locally bypassed with a minimum of 1µF capacitor placed close to this pin.

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BLOCK DIAGRAM

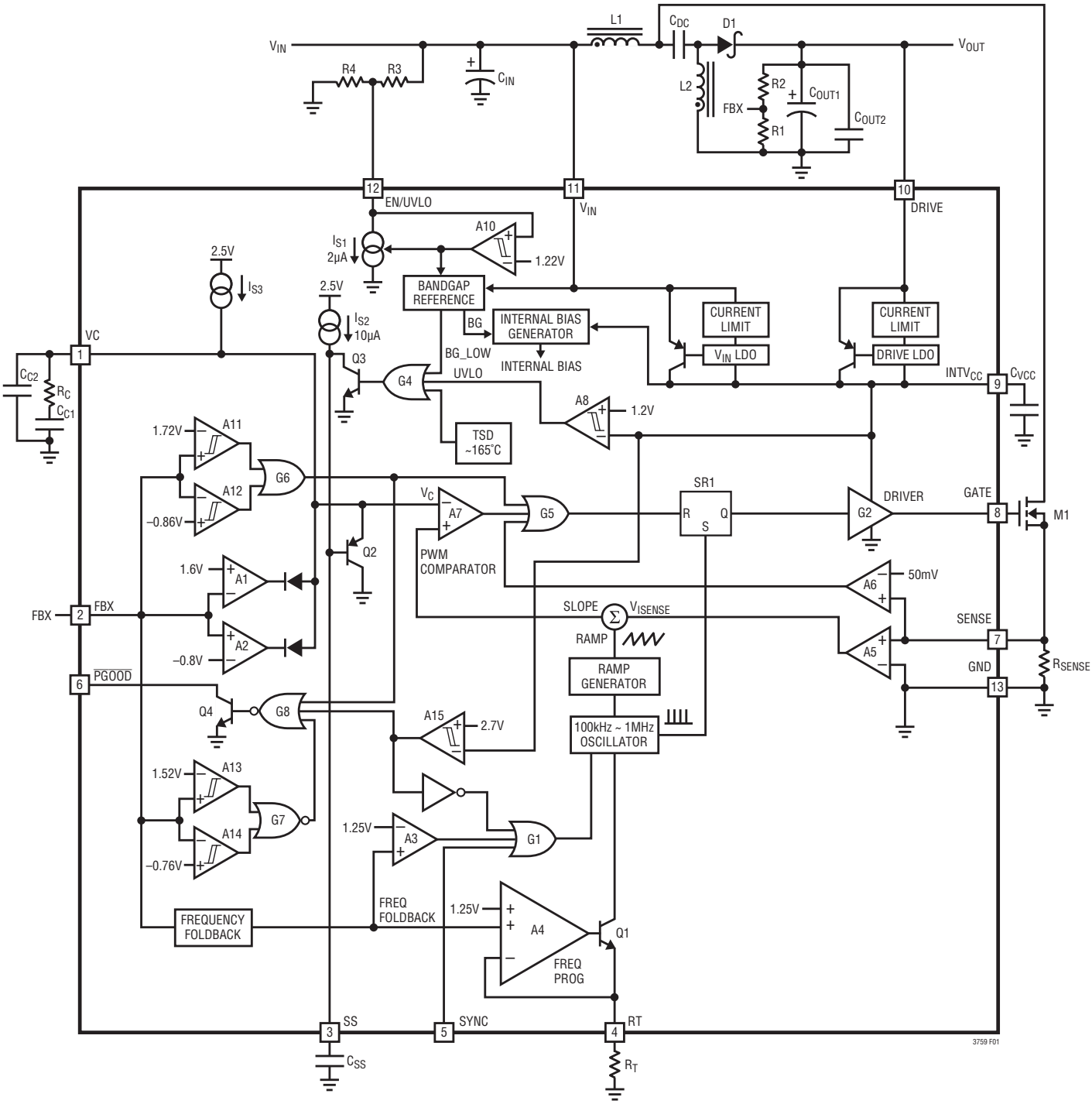

Figure 1. LT3759 Block Diagram Working as a SEPIC Converter

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APPLICATIONS INFORMATION

Main Control Loop

The LT3759 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1.

The start of each oscillator cycle sets the SR latch (SR1) and turns on the external power MOSFET switch M1 through driver G2. The switch current flows through the external current sensing resistor R_{SENSE} and generates a voltage proportional to the switch current. This current sense voltage V_{ISENSE} (amplified by A5) is added to a stabilizing slope compensation ramp and the resulting sum (SLOPE) is fed into the positive terminal of the PWM comparator A7. When SLOPE exceeds the level at the negative input of A7 (VC pin), SR1 is reset, turning off the power switch. The level at the negative input of A7 is set by the error amplifier A1 (or A2) and is an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage (1.6V or –0.8V, depending on the configuration). In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT3759 has a switch current limit function. The current sense voltage is input to the current limit comparator A6. If the SENSE pin voltage is higher than the sense current limit threshold $V_{SENSE(MAX)}$ (50mV, typical), A6 will reset SR1 and turn off M1 immediately.

The LT3759 is capable of generating either positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate positive output voltage, or as an inverting converter to generate negative output voltage. When configured as a SEPIC converter, as shown in Figure 1, the FBX pin is pulled up to the internal bias voltage of 1.6V by a voltage divider (R1 and R2) connected from V_{OUT} to GND. Comparator A2 becomes inactive and comparator A1 performs the inverting amplification from FBX to VC. When the LT3759 is in an inverting configuration, the FBX pin is pulled down to –0.8V by a voltage divider connected from V_{OUT} to GND. Comparator A1 becomes inactive and comparator A2 performs the noninverting amplification from FBX to VC.

The LT3759 has overvoltage protection functions to protect the converter from excessive output voltage overshoot during start-up or recovery from a short-circuit condition. An overvoltage comparator A11 (with 40mV hysteresis) senses when the FBX pin voltage exceeds the positive regulated voltage (1.6V) by 7.5% and turns off M1. Similarly, an overvoltage comparator A12 (with 20mV hysteresis) senses when the FBX pin voltage exceeds the negative regulated voltage (–0.8V) by 7.5% and turns off M1. Both reset pulses are sent to the main RS latch (SR1) through G6 and G5. The external power MOSFET switch M1 is actively held off for the duration of an output overvoltage condition.

Programming Turn-On and Turn-Off Thresholds with EN/UVLO Pin

The EN/UVLO pin controls whether the LT3759 is enabled or is in shutdown state. A micropower 1.22V reference, a comparator A10 and controllable current source I_{S1} allow the user to accurately program the supply voltage at which the IC turns on and off. The falling value can be accurately set by the resistor dividers R3 and R4. When EN/UVLO is above 0.7V, and below the 1.22V threshold, the small pull-down current source I_{S1} (typical 2µA) is active.

The purpose of this current is to allow the user to program the rising hysteresis. The Block Diagram of the comparator and the external resistors is shown in Figure 1. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{VIN(FALLING)} = 1.22 \bullet \frac{(R3+R4)}{R4}$$

$$V_{VIN(RISING)} = 2\mu A \bullet R3 + V_{IN(FALLING)}$$

For applications where the EN/UVLO pin is only used as a logic input, the EN/UVLO pin can be connected directly to the input voltage V_{IN} for always-on operation.

$INTV_{CC}$ Low Dropout Voltage Regulators

The LT3759 features two internal low dropout (LDO) voltage regulators (V_{IN} LDO and DRIVE LDO) powered from different supplies (V_{IN} and DRIVE respectively). Both LDO's regulate the internal $INTV_{CC}$ supply which powers the gate driver and the internal loads, as shown in Figure 1. Both regulators are designed so that current does not flow from $INTV_{CC}$ to the LDO input under a reverse bias condition. DRIVE LDO regulates the $INTV_{CC}$ to 4.75V, while V_{IN} LDO

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APPLICATIONS INFORMATION

regulates the $INTV_{CC}$ to 3.75V. V_{IN} LDO is turned off when the $INTV_{CC}$ voltage is greater than 3.75V (typical). Both LDO's can be turned off if the $INTV_{CC}$ pin is driven by a supply of 4.75V or higher but less than 8V (the $INTV_{CC}$ maximum voltage rating is 8V). A table of the LDO supply and output voltage combination is shown in Table 1.

Table 1. LDO's Supply and Output Voltage Combination (Assuming That the LDO Dropout Voltage is 0.15V)

SUPPLY VOLTAGES		LDO OUTPUT	LDO STATUS (Note 7)
V_{IN}	DRIVE	$INTV_{CC}$	
$V_{IN} \le 3.9V$	$V_{DRIVE} < V_{IN}$	$V_{IN} - 0.15V$	#1 Is ON
	$V_{DRIVE} = V_{IN}$	$V_{IN} - 0.15V$	#1 #2 are ON
	$V_{IN} < V_{DRIVE} < 4.9V$	$V_{DRIVE} - 0.15V$	#2 Is ON
	$4.9V \le V_{DRIVE} \le 42V$	4.75V	#2 Is ON
$3.9V < V_{IN} \le 42V$	$V_{DRIVE} < 3.9V$	3.75V	#1 Is ON
	$V_{DRIVE} = 3.9V$	3.75V	#1 #2 are ON
	$3.9V < V_{DRIVE} < 4.9V$	$V_{DRIVE} - 0.15V$	#2 Is ON
	$4.9V \le V_{DRIVE} \le 42V$	4.75V	#2 Is ON

Note 7: #1 is V_{IN} LDO and #2 is DRIVE LDO

The DRIVE pin provides flexibility to power the gate driver and the internal loads from a supply that is available only when the switcher is enabled and running. If not used, the DRIVE pin should be tied to V_{IN}.

The $INTV_{CC}$ pin must be bypassed to ground immediately adjacent to the $INTV_{CC}$ pin with a minimum of 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

If a low input voltage operation is expected (V_{IN} is 3V or less), low threshold MOSFETs should be used. The LT3759 contains an undervoltage lockout comparator A8 for the internal $INTV_{CC}$ supply. The $INTV_{CC}$ undervoltage (UV) threshold is 1.3V (typical), with 100mV hysteresis, to ensure that the MOSFETs have sufficient gate drive voltage before turning on. The logic circuitry within the LT3759 is also powered from the internal $INTV_{CC}$ supply. When $INTV_{CC}$ is below the UV threshold, the GATE pin will be forced to GND and the soft-start operation will be triggered.

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. The on-chip power dissipation can be a significant concern when a large power MOSFET is being driven at a high frequency and the V_{IN} voltage is high. It is important to limit the power dissipation with proper selection of a MOSFET and/or an operating frequency so the LT3759 does not exceed its maximum junction temperature rating. The junction temperature T_J can be estimated using the following equations:

$$T_J = T_A + P_{IC} \bullet \theta_{JA}$$

T_A = ambient temperature

θ_{JA} = junction-to-ambient thermal resistance

P_{IC} = IC power consumption = $V_{IN} \bullet (I_Q + I_{DRIVE})$

(Assume the DRIVE pin is connected to V_{IN} Supply)

I_Q = V_{IN} operation I_Q = 1.8mA

I_{DRIVE} = average gate drive current = $f \bullet Q_G$

f = switching frequency

Q_G = power MOSFET total gate charge

The LT3759 uses packages with an exposed pad for enhanced thermal conduction. With proper soldering to the exposed pad on the underside of the package and a full copper plane underneath the device, thermal resistance (θ_{JA}) will be about 40°C/W for the MSE package.

The LT3759 has an internal $INTV_{CC}$ I_{DRIVE} current limit function to protect the IC from excessive on-chip power dissipation. If I_{DRIVE} reaches the current limit, $INTV_{CC}$ voltage will fall and may trigger the soft-start.

There is a trade-off between the operating frequency and the size of the power MOSFET (Q_G) in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their most recent low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

Operating Frequency and Synchronization

The choice of operating frequency may be determined by on-chip power dissipation, otherwise it is a trade-off between efficiency and component size. Low frequency

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operation improves efficiency by reducing gate drive current and MOSFET and diode switching losses. However, lower frequency operation requires a physically larger loop inductor. Switching frequency also has implications for loop compensation. The LT3759 uses a constant-frequency architecture that can be programmed over a 100kHz to 1MHz range with a single external resistor from the RT pin to ground, as shown in Figure 1. The RT pin must have an external resistor to GND for proper operation of the LT3759. A table for selecting the value of R_T for a given operating frequency is shown in Table 2.

Table 2. Timing Resistor (R_T) Value

OSCILLATOR FREQUENCY (kHz)	R_T (kΩ)
100	86.6
200	41.2
300	27.4
400	21.0
500	16.5
600	13.7
700	11.5
800	9.76
900	8.45
1000	6.81

The switching frequency of the LT3759 can be synchronized to the positive edge of an external clock source. By providing a digital clock signal into the SYNC pin, the LT3759 will operate at the SYNC clock frequency. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. The SYNC pulse should have a minimum pulse width of 200ns. Tie the SYNC pin to GND if this feature is not used.

Duty Cycle Consideration

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. Minimum on-time is the smallest time duration that the LT3759 is capable of turning on the power MOSFET. This time is generally about 170ns (typical) (see Minimum On-Time in the Electrical Characteristics table). In each switching cycle, the LT3759 keeps the power switch off for at least 170ns (typical) (see Minimum Off-Time in the Electrical Characteristics table).

The minimum on-time and minimum off-time and the switching frequency define the minimum and maximum switching duty cycles a converter is able to generate:

Minimum duty cycle = minimum on-time • frequency

Maximum duty cycle = 1 – (minimum off-time • frequency)

Programming the Output Voltage

The output voltage (V_{OUT}) is set by a resistor divider, as shown in Figure 1. The positive V_{OUT} and negative V_{OUT} are set by the following equations:

$$V_{OUT(POSITIVE)} = 1.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{OUT(NEGATIVE)} = -0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistors R1 and R2 are typically chosen so that the error caused by the current flowing into the FBX pin during normal operation is less than 1% (this translates to a maximum value of R1 at about 158k).

Soft-Start

The LT3759 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

LT3759 addresses this mechanism with the SS pin. As shown in Figure 1, the SS pin reduces the power MOSFET current by pulling down the VC pin through Q2. In this way the SS allows the output capacitor to charge gradually toward its final value while limiting the start-up peak currents.

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Besides start-up, soft-start can also be triggered by $INTV_{CC}$ undervoltage lockout and/or thermal lockout, which causes the LT3759 to stop switching immediately. The SS pin will be discharged by Q3. When all faults are cleared and the SS pin has been discharged below 0.2V, a 10µA current source I_{S2} starts charging the SS pin, initiating a soft-start operation.

The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.25V}{10\mu A}$$

FBX Frequency Foldback

When V_{OUT} is very low during start-up or a short-circuit fault on the output, the switching regulator must operate at low duty cycles to maintain the power switch current within the current limit range, since the inductor current decay rate is very low during switch off time. The minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. So, the switch current will keep increasing through each switch cycle, exceeding the programmed current limit. To prevent the switch peak currents from exceeding the programmed value, the LT3759 contains a frequency foldback function to reduce the switching frequency when the FBX voltage is low (see the Normalized Switching Frequency vs FBX graph in the Typical Performance Characteristics section).

Some frequency foldback waveforms are shown in the Typical Applications section. The frequency foldback function prevents I_L from exceeding the programmed limits because of the minimum on-time.

During frequency foldback, external clock synchronization is disabled to allow the frequency reducing operation to function properly.

Thermal Lockout

If the LT3759 die temperature reaches 165°C (typical), the part will go into thermal lockout. The power switch will be turned off. A soft-start operation will be triggered. The part will be enabled again when the die temperature has dropped by 5°C (nominal).

Loop Compensation

Loop compensation determines the stability and transient performance. The LT3759 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT3759, a series resistor-capacitor network is usually connected from the VC pin to GND. Figure 1 shows the typical VC compensation network. For most applications, the capacitor should be in the range of 470pF to 22nF, and the resistor should be in the range of 5k to 50k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the VC voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

SENSE Pin Programming

For control and protection, the LT3759 measures the power MOSFET current by using a sense resistor (R_{SENSE}) between GND and the MOSFET source. Figure 2 shows a typical wave-form of the sense voltage (V_{SENSE}) across the sense resistor. It is important to use Kelvin traces between the SENSE pin and R_{SENSE}, and to place the IC GND as close as possible to the GND terminal of the R_{SENSE} for proper operation.

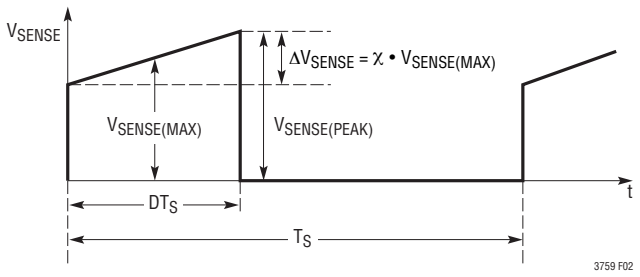

Figure 2. The Sense Voltage During a Switching Cycle

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Due to the current limit function of the SENSE pin, R_{SENSE} should be selected to guarantee that the peak current sense voltage $V_{SENSE(PEAK)}$ during steady state normal operation is lower than the SENSE current limit threshold (see the Electrical Characteristics table). Given a 20% margin, $V_{SENSE(PEAK)}$ is set to be 40mV. Then, the maximum switch ripple current percentage can be calculated using the following equation:

$$\chi = \frac{\Delta V_{SENSE}}{40mV - 0.5 \bullet \Delta V_{SENSE}}$$

χ is used in subsequent design examples to calculate inductor value. ΔV_{SENSE} is the ripple voltage across R_{SENSE}.

The LT3759 has internal slope compensation to stabilize the control loop against sub-harmonic oscillation. When the LT3759 operates at a high duty cycle in continuous conduction mode, the SENSE voltage ripple ΔV_{SENSE} (refer to Figure 2) needs to be limited to ensure the internal slope compensation is sufficient to stabilize the control loop. Figure 3 shows the maximum allowed ΔV_{SENSE} over the duty cycle. It is recommended to check and ensure ΔV_{SENSE} is below the curve at the highest duty cycle.

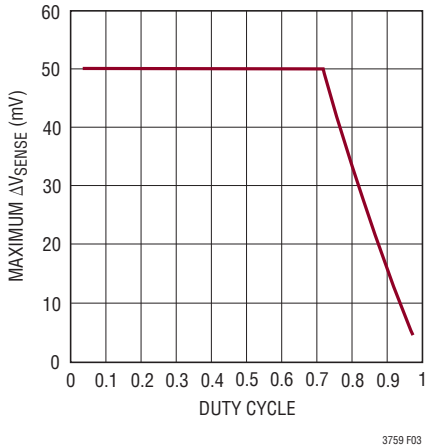

Figure 3. The Maximum Allowed SENSE Voltage Ripple vs Duty Cycle

The LT3759 switching controller incorporates 100ns timing interval to blank the ringing on the current sense signal immediately after M1 is turned on. This ringing is caused by the parasitic inductance and capacitance of the PCB trace, the sense resistor, the diode, and the MOSFET. The 100ns timing interval is adequate for most of the LT3759 applications. In the applications that have very large and long ringing on the current sense signal, a small RC filter can be added to filter out the excess ringing. Figure 4 shows the RC filter on SENSE pin. It is usually sufficient to choose 22Ω for R_{FLT} and 2.2nF to 10nF for C_{FLT}. Keep R_{FLT}'s resistance low. Remember that there is 50µA (typical) flowing out of the SENSE pin. Adding R_{FLT} will affect the SENSE current limit threshold:

$$V_{SENSE_ILIM} = 50mV - 50\mu A \bullet R_{FLT}$$

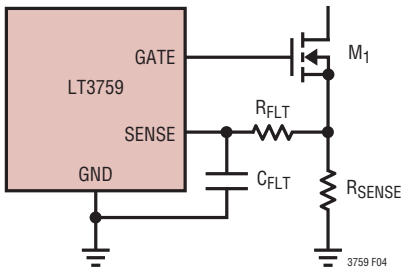

Figure 4. The RC Filter on SENSE pin

APPLICATION CIRCUITS

The LT3759 can be configured as different topologies. The design procedure for component selection differs somewhat between these topologies. The first topology to be analyzed will be the boost converter, followed by the flyback SEPIC and inverting converters.

Boost Converter: Switch Duty Cycle and Frequency

The LT3759 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

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The selection of switching frequency is the starting point. The maximum frequency that can be used is based on the maximum duty cycle. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM). The equations that follow assume CCM operation.

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

The alternative to CCM, discontinuous conduction mode (DCM) is not limited by duty cycle to provide high conversion ratios at a given frequency. The price one pays is reduced efficiency and substantially higher switching current.

Boost Converter: Inductor and Sense Resistor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Then, the ripple current can be calculated by:

$$\Delta I_L = \chi \bullet I_{L(MAX)} = \chi \bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The constant χ in the preceding equation represents the percentage peak-to-peak ripple current in the inductor, relative to $I_{L(MAX)}$.

The inductor ripple current has a direct effect on the choice of inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls within the range of 0.2 to 0.6.

The peak and RMS inductor current are:

$$I_{L(PEAK)} = I_{L(MAX)} \bullet \left(1 + \frac{\chi}{2}\right)$$

$$I_{L(RMS)} = I_{L(MAX)} \bullet \sqrt{1 + \frac{\chi^2}{12}}$$

The inductor used with the LT3759 should have a saturation current rating appropriate to the maximum switch current selected with the R_{SENSE} resistor. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode ramp on SENSE during the switch on-time of approximately 10mV magnitude. The following equation is useful to estimate the inductor value for continuous conduction mode operation:

$$L = \frac{R_{SENSE} \bullet V_{IN(MIN)}}{0.01V \bullet f_{OSC}} \bullet D_{MAX}$$

Set the sense voltage at $I_{L(PEAK)}$ to be the minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{40mV}{I_{L(PEAK)}}$$

Boost Converter: Power MOSFET Selection

Important parameters for the power MOSFET include the drain-source voltage rating (V_{DS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$), the gate to source and gate to drain charges (Q_{GS} and Q_{GD}), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{\theta JC}$ and $R_{\theta JA}$).

The power MOSFET will see full output voltage, plus a diode forward voltage, and any additional ringing across its drain-to-source during its off-time. It is recommended

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to choose a MOSFET whose BV_{DSS} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = I^2_{L(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX}$$

$$+V^2_{OUT} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet \frac{f}{1A}$$

The first term in the preceding equation represents the conduction losses in the devices, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A \bullet P_{FET} \bullet \theta_{JA}$$

$$= T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desirable. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage plus any additional ringing across its anode-to-cathode during the on-time. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = I_{L(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{L(MAX)}$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A \bullet P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 5.

The choice of component(s) begins with the maximum

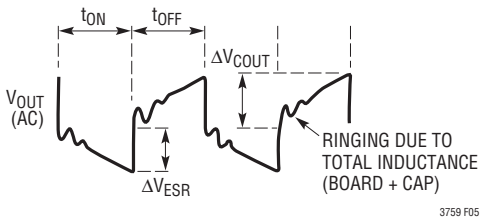

Figure 5. The Output Ripple Waveform of a Boost Converter

acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will

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change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 5. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \geq I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

FLYBACK CONVERTER APPLICATIONS

The LT3759 can be configured as a flyback converter for the applications where the converters have multiple outputs, high output voltages or isolated outputs. Figure 6 shows a simplified flyback converter.

The flyback converter has a very low parts count for multiple outputs, and with prudent selection of turns ratio, can have high output/input voltage conversion ratios with a desirable duty cycle. However, it has low efficiency due to the high peak currents, high peak voltages and consequent power loss. The flyback converter is commonly used for an output power of less than 50W.

The flyback converter can be designed to operate either in continuous or discontinuous mode. Compared to continuous mode, discontinuous mode has the advantage of smaller transformer inductances and easy loop compensation, and the disadvantage of higher peak-to-average current and lower efficiency. In the high output voltage applications, the flyback converters can be designed to operate in discontinuous mode to avoid using large transformers.

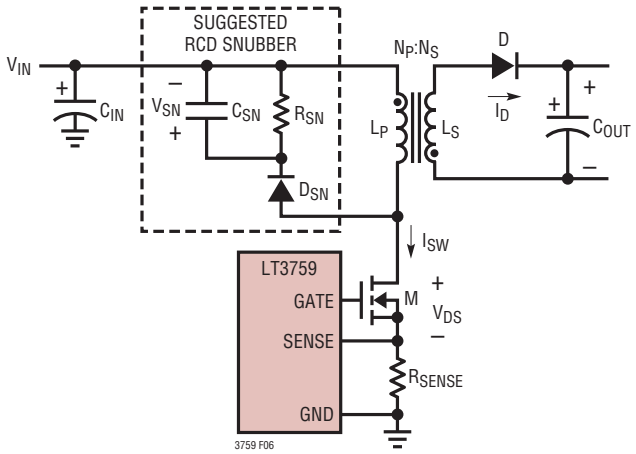

Figure 6. A Simplified Flyback Converter

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Flyback Converter: Switch Duty Cycle and Turns Ratio

The flyback converter conversion ratio in the continuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{1-D}$$

where N_S/N_P is the second to primary turns ratio.

Figure 7 shows the waveforms of the flyback converter in discontinuous mode operation. During each switching period T_S, three subintervals occur: DT_S, $D2T_S$, $D3T_S$. During DT_S, M is on, and D is reverse-biased. During $D2T_S$, M is off, and L_S is conducting current. Both L_P and L_S currents are zero during $D3T_S$.

The flyback converter conversion ratio in the discontinuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{D2}$$

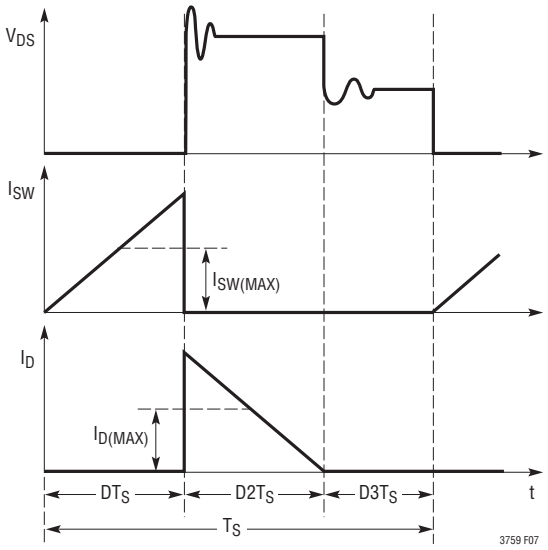

Figure 7. Waveforms of the Flyback Converter in Discontinuous Mode Operation

According to the preceding equations, the user has relative freedom in selecting the switch duty cycle or turns ratio to suit a given application. The selections of the duty cycle and the turns ratio are somewhat iterative processes, due to the number of variables involved. The user can choose either a duty cycle or a turns ratio as the start point. The following trade-offs should be considered when selecting the switch duty cycle or turns ratio, to optimize the converter performance. A higher duty cycle affects the flyback converter in the following aspects:

- Lower MOSFET RMS current $I_{SW(RMS)}$, but higher MOSFET V_{DS} peak voltage
- Lower diode peak reverse voltage, but higher diode RMS current $I_{D(RMS)}$
- Higher transformer turns ratio (N_P/N_S)

The choice,

$$\frac{D}{D+D2} = \frac{1}{3}$$

(for discontinuous mode operation with a given D3) gives the power MOSFET the lowest power stress (the product of RMS current and peak voltage). However, in the high output voltage applications, a higher duty cycle may be adopted to limit the large peak reverse voltage of the diode. The choice,

$$\frac{D}{D+D2} = \frac{2}{3}$$

(for discontinuous mode operation with a given D3) gives the diode the lowest power stress (the product of RMS current and peak voltage). An extreme high or low duty cycle results in high power stress on the MOSFET or diode, and reduces efficiency. It is recommended to choose a duty cycle, D, between 20% and 80%.

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Flyback Converter: Transformer Design for Discontinuous Mode Operation

The transformer design for discontinuous mode of operation is chosen as presented here. According to Figure 7, the minimum D3 ($D3_{MIN}$) occurs when the converter has the minimum V_{IN} and the maximum output power (P_{OUT}). Choose $D3_{MIN}$ to be equal to or higher than 10% to guarantee the converter is always in discontinuous mode operation (choosing higher D3 allows the use of low inductances, but results in a higher switch peak current).

The user can choose a D_{MAX} as the start point. Then, the maximum average primary currents can be calculated by the following equation:

$$I_{LP(MAX)} = I_{SW(MAX)} = \frac{P_{OUT(MAX)}}{D_{MAX} \bullet V_{IN(MIN)} \bullet \eta}$$

where η is the converter efficiency.

If the flyback converter has multiple outputs, $P_{OUT(MAX)}$ is the sum of all the output power.

The maximum average secondary current is:

$$I_{LS(MAX)} = I_{D(MAX)} = \frac{I_{OUT(MAX)}}{D2}$$

where:

$$D2 = 1 - D_{MAX} - D3$$

the primary and secondary RMS currents are:

$$I_{LP(RMS)} = 2 \bullet I_{LP(MAX)} \bullet \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{LS(RMS)} = 2 \bullet I_{LS(MAX)} \bullet \sqrt{\frac{D2}{3}}$$

According to Figure 7, the primary and secondary peak currents are:

$$I_{LP(PEAK)} = I_{SW(PEAK)} = 2 \bullet I_{LP(MAX)}$$

$$I_{LS(PEAK)} = I_{D(PEAK)} = 2 \bullet I_{LS(MAX)}$$

The primary and second inductor values of the flyback converter transformer can be determined using the following equations:

$$L_P = \frac{D^2_{MAX} \bullet V^2_{IN(MIN)} \bullet \eta}{2 \bullet P_{OUT(MAX)} \bullet f_{OSC}}$$

$$L_S = \frac{D2^2 \bullet (V_{OUT} + V_D)}{2 \bullet I_{OUT(MAX)} \bullet f_{OSC}}$$

The primary to second turns ratio is:

$$\frac{N_P}{N_S} = \sqrt{\frac{L_P}{L_S}}$$

Flyback Converter: Snubber Design

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases a snubber circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. There are different snubber circuits, and Application Note 19 is a good reference on snubber design. An RCD snubber is shown in Figure 6.

The snubber resistor value (R_{SN}) can be calculated by the following equation:

$$R_{SN} = 2 \bullet \frac{V^2_{SN} - V_{SN} \bullet V_{OUT} \bullet \frac{N_P}{N_S}}{I^2_{SW(PEAK)} \bullet L_{LK} \bullet f_{OSC}}$$

where V_{SN} is the snubber capacitor voltage. A smaller V_{SN} results in a larger snubber loss. A reasonable V_{SN} is 2 to 2.5 times of:

$$\frac{V_{OUT} \bullet N_P}{N_S}$$

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L_{LK} is the leakage inductance of the primary winding, which is usually specified in the transformer characteristics. L_{LK} can be obtained by measuring the primary inductance with the secondary windings shorted. The snubber capacitor value (C_{CN}) can be determined using the following equation:

$$C_{CN} = \frac{V_{SN}}{\Delta V_{SN} \bullet R_{CN} \bullet f_{OSC}}$$

where ΔV_{SN} is the voltage ripple across C_{CN}. A reasonable ΔV_{SN} is 5% to 10% of V_{SN}. The reverse voltage rating of D_{SN} should be higher than the sum of V_{SN} and $V_{IN(MAX)}$.

Flyback Converter: Sense Resistor Selection

In a flyback converter, when the power switch is turned on, the current flowing through the sense resistor (I_{SENSE}) is:

$$I_{SENSE} = I_{LP}$$

Set the sense voltage at $I_{LP(PEAK)}$ to be the minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{40mV}{I_{LP(PEAK)}}$$

Flyback Converter: Power MOSFET Selection

For the flyback configuration, the MOSFET is selected with a V_{DC} rating high enough to handle the maximum V_{IN}, the reflected secondary voltage and the voltage spike due to the leakage inductance. Approximate the required MOSFET V_{DC} rating using:

$$BV_{DSS} > V_{DS(PEAK)}$$

where:

$$V_{DS(PEAK)} = V_{IN(MAX)} + V_{SN}$$

The power dissipated by the MOSFET in a flyback converter is:

$$P_{FET} = I^2_{M(RMS)} \bullet R_{DS(ON)} + 2 \bullet V^2_{DS(PEAK)} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f_{OSC}/1A$$

The first term in this equation represents the conduction losses in the device, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

Flyback Converter: Output Diode Selection

The output diode in a flyback converter is subject to large RMS current and peak reverse voltage stresses. A fast switching diode with a low forward drop and a low reverse leakage is desired. Schottky diodes are recommended if the output voltage is below 100V.

Approximate the required peak repetitive reverse voltage rating V_{RRM} using:

$$V_{RRM} > \frac{N_S}{N_P} \bullet V_{IN(MAX)} + V_{OUT}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Flyback Converter: Output Capacitor Selection

The output capacitor of the flyback converter has a similar operation condition as that of the boost converter. Refer to the Boost Converter: Output Capacitor Selection section for the calculation of C_{OUT} and ESR_{COUT}.

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APPLICATIONS INFORMATION

The RMS ripple current rating of the output capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(COUT),DISCONTINUOUS} \geq I_{O(MAX)} \bullet \sqrt{\frac{4-(3\bullet D2)}{3\bullet D2}}$$

Flyback Converter: Input Capacitor Selection

The input capacitor in a flyback converter is subject to a large RMS current due to the discontinuous primary current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The RMS ripple current rating of the input capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(CIN),DISCONTINUOUS} \geq \frac{P_{OUT(MAX)}}{V_{IN(MIN)}\bullet \eta} \bullet \sqrt{\frac{4-(3\bullet D_{MAX})}{3\bullet D_{MAX}}}$$

SEPIC CONVERTER APPLICATIONS

The LT3759 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 1. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}+V_D}{V_{IN}} = \frac{D}{1-D}$$

In continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT}+V_D}{V_{IN(MIN)}+V_{OUT}+V_D}$$

SEPIC Converter: Inductor and Sense Resistor Selection

As shown in Figure 1, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)} = I_{IN(MAX)} = I_{O(MAX)} \frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2(MAX)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to I_{L1} + I_{L2} when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)} = I_{L1(MAX)} + I_{L2(MAX)}$$

$$= I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)}$, as shown in Figure 8. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)}$$

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APPLICATIONS INFORMATION

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW}$$

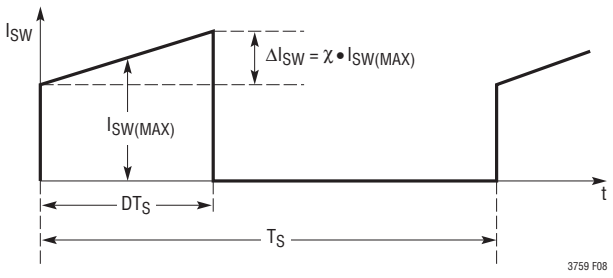

Figure 8. The Switch Current Waveform of a SEPIC Converter

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.2 to 0.4.

Choose an inductor value based on operating frequency, input and output voltage to provide a current mode ramp on SENSE during the switch on-time of approximately 10mV magnitude. The inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

$$= \frac{R_{SENSE} \bullet V_{IN(MIN)}}{0.5 \bullet 0.01V \bullet f_{OSC}} \bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 100µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

$$= \frac{R_{SENSE} \bullet V_{IN(MIN)}}{0.01V \bullet f_{OSC}} \bullet D_{MAX}$$

In a SEPIC converter, when the power switch is turned on, the current flowing through the sense resistor (I_{SENSE}) is the switch current.

Set the sense voltage at $I_{SENSE(PEAK)}$ to be minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{40mV}{I_{SW(PEAK)}}$$

SEPIC Converter: Power MOSFET Selection

For the SEPIC configuration, choose a MOSFET with a V_{DC} rating higher than the sum of the output voltage and input voltage by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a SEPIC converter is:

$$P_{FET} = I^2_{SW(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX}$$

$$+ (V_{IN(MIN)} + V_{OUT})^2 \bullet I_{SW(MAX)}$$

$$\bullet C_{RSS} \bullet \frac{f_{OSC}}{1A}$$

The first term in this equation represents the conduction losses in the device, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

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APPLICATIONS INFORMATION

For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA}$$

$$= T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter. Please refer to the Boost Converter, Output Capacitor Selection and Boost Converter, Input Capacitor Selection sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 1) should be rated for the maximum input voltage:

$$C_{DC} \geq V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} \geq I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT3759 can be configured as a dual-inductor inverting topology, as shown in Figure 9. The V_{OUT} to V_{IN} ratio is:

$$\frac{V_{OUT} - V_D}{V_{IN}} = \frac{D}{1 - D}$$

In continuous conduction mode (CCM).

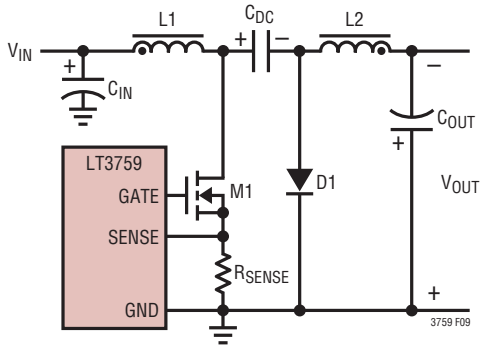

Figure 9. A Simplified Inverting Converter

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APPLICATIONS INFORMATION

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_D}{V_{OUT} - V_D - V_{IN(MIN)}}$$

Inverting Converter: Inductor, Sense Resistor, Power MOSFET, Output Diode and Input Capacitor Selections

The selections of the inductor, sense resistor, power MOSFET, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f_{OSC} \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 9) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Board Layout

The high speed operation of the LT3759 demands careful attention to board layout and component placement. The exposed pad of the package is the only GND terminal of the IC, and is important for thermal management of the IC. Therefore, it is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground plane of the board. For the LT3759 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths with higher di/dt. The following high di/dt loops of different topologies should be kept as tight as possible to reduce inductive ringing:

- In boost configuration, the high di/dt loop contains the output capacitor, the sensing resistor, the power MOSFET and the Schottky diode.

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APPLICATIONS INFORMATION

- In flyback configuration, the high di/dt primary loop contains the input capacitor, the primary winding, the power MOSFET and sensing resistor. The high di/dt secondary loop contains the output capacitor, the secondary winding and the output diode.
- In SEPIC configuration, the high di/dt loop contains the power MOSFET, sense resistor, output capacitor, Schottky diode and the coupling capacitor.
- In inverting configuration, the high di/dt loop contains power MOSFET, sense resistor, Schottky diode and the coupling capacitor.

Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing, which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided, and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET.

The small-signal components should be placed away from high frequency switching nodes. For optimum load regulation and true remote sensing, the top of the output voltage sensing resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LT3759 in order to keep the high impedance FBX node short.

Figure 10 shows the suggested layout of 1.8V to 3.3V input, 5V/2A Output Boost Converter.

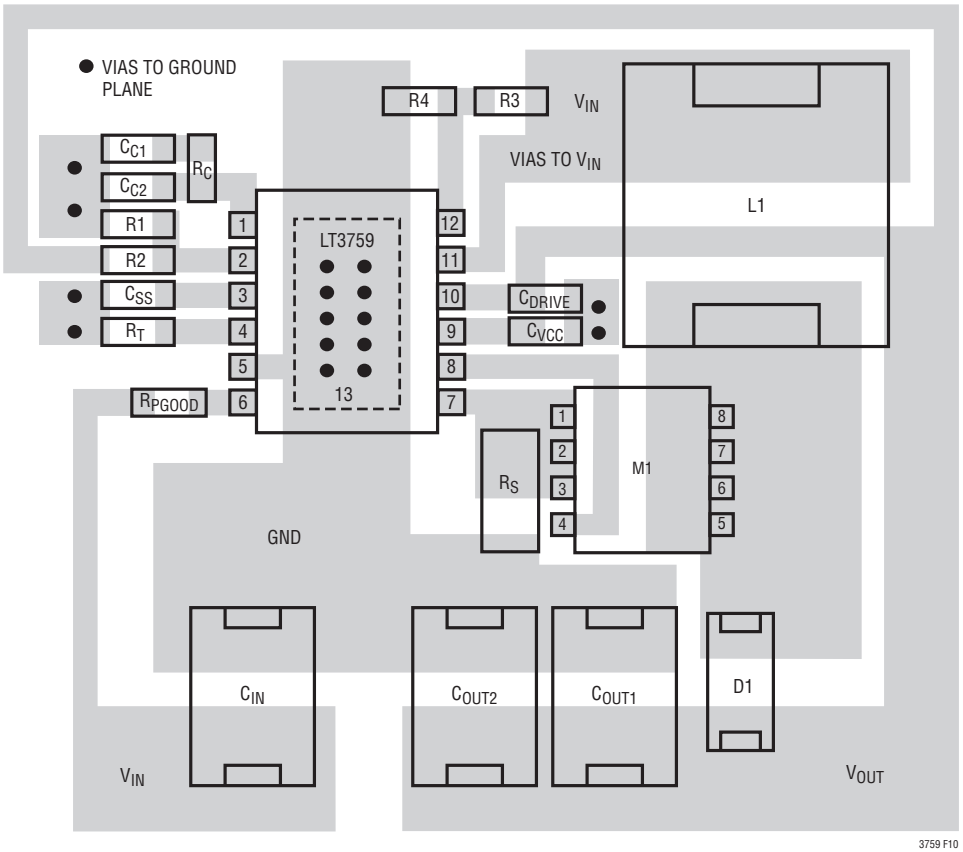

Figure 10. The Suggested Boost Converter Layout

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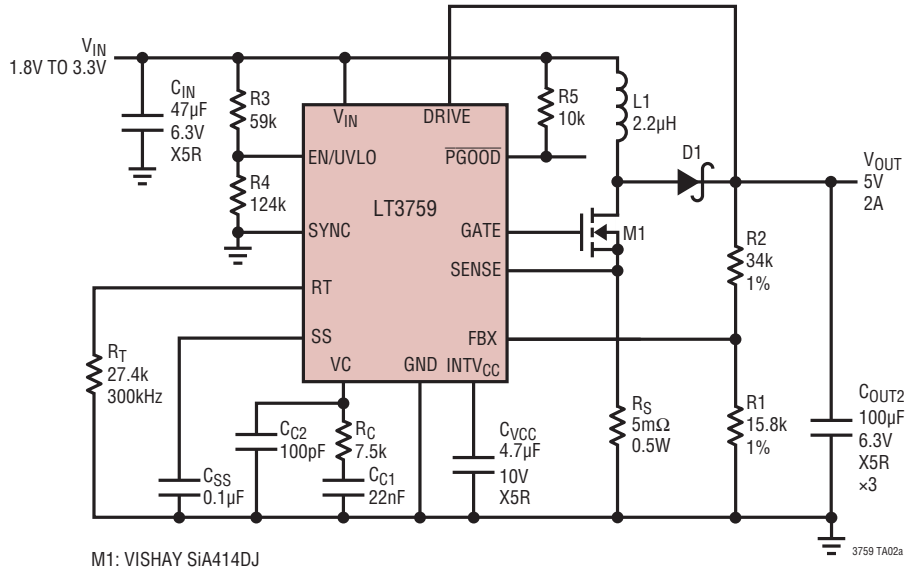
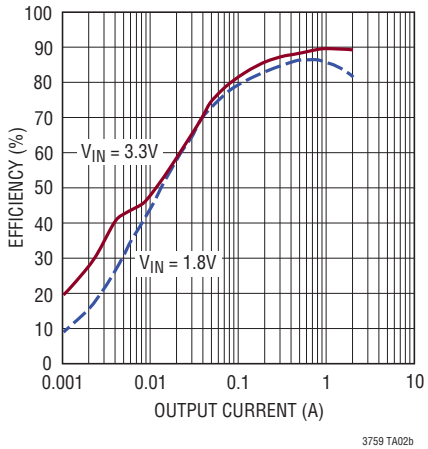
TYPICAL APPLICATIONS

1.8V to 3.3V Input, 5V/2A Output Boost Converter

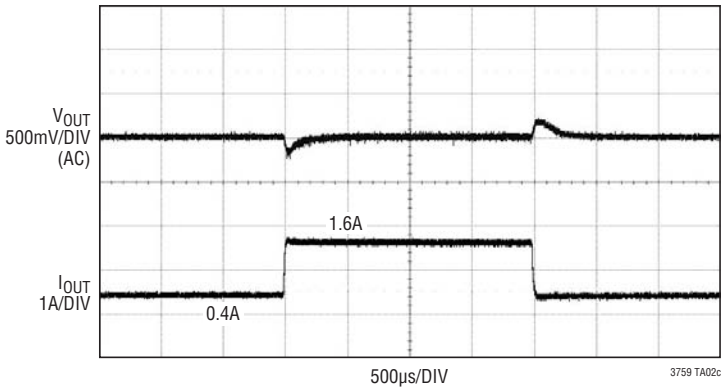


M1: VISHAY SiA414DJ
L1: TOKO FDA1055-2R2M
D1: VISHAY 6CWQ06FN

Efficiency vs Output Current



Load Step Response at V_{IN} = 2.5V



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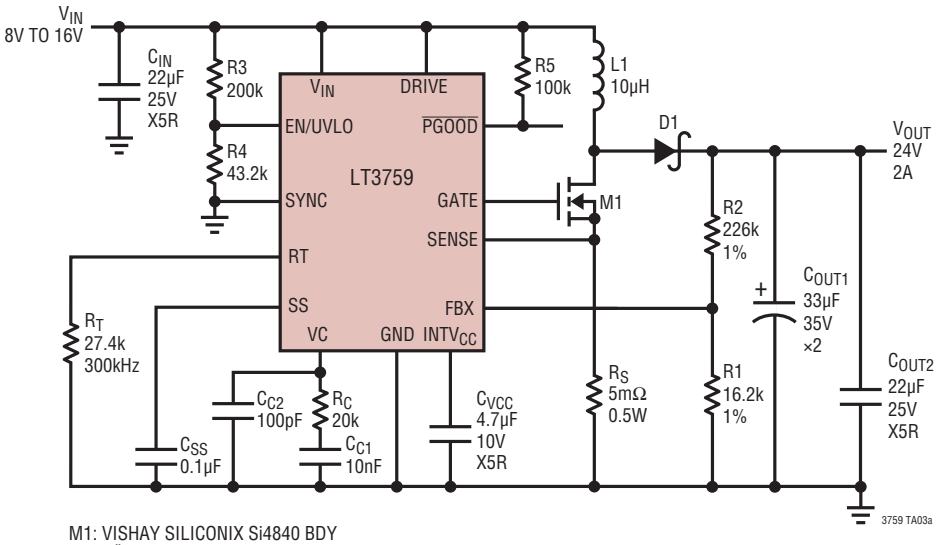
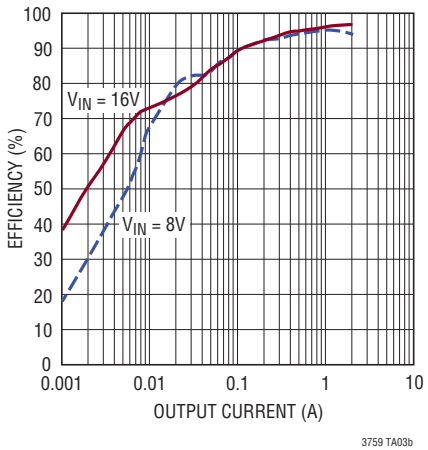
TYPICAL APPLICATIONS

8V to 16V Input, 24V/2A Output Boost Converter

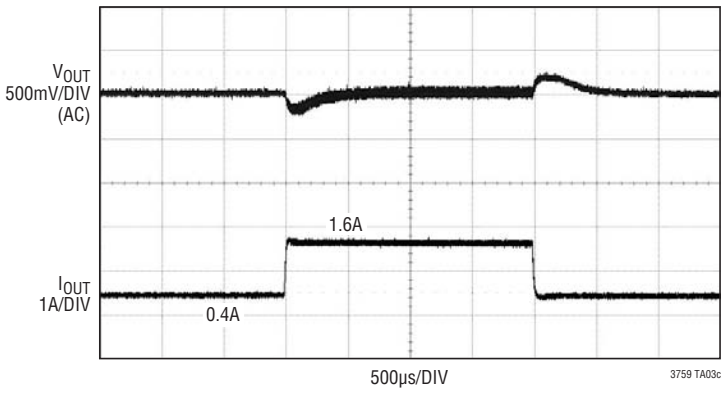


M1: VISHAY SILICONIX Si4840 BDY
L1: WÜRTH ELEKTRONIK 7443321000
D1: VISHAY 6CWQ06FN

Efficiency vs Output Current



Load Step Response at V_{IN} = 12V



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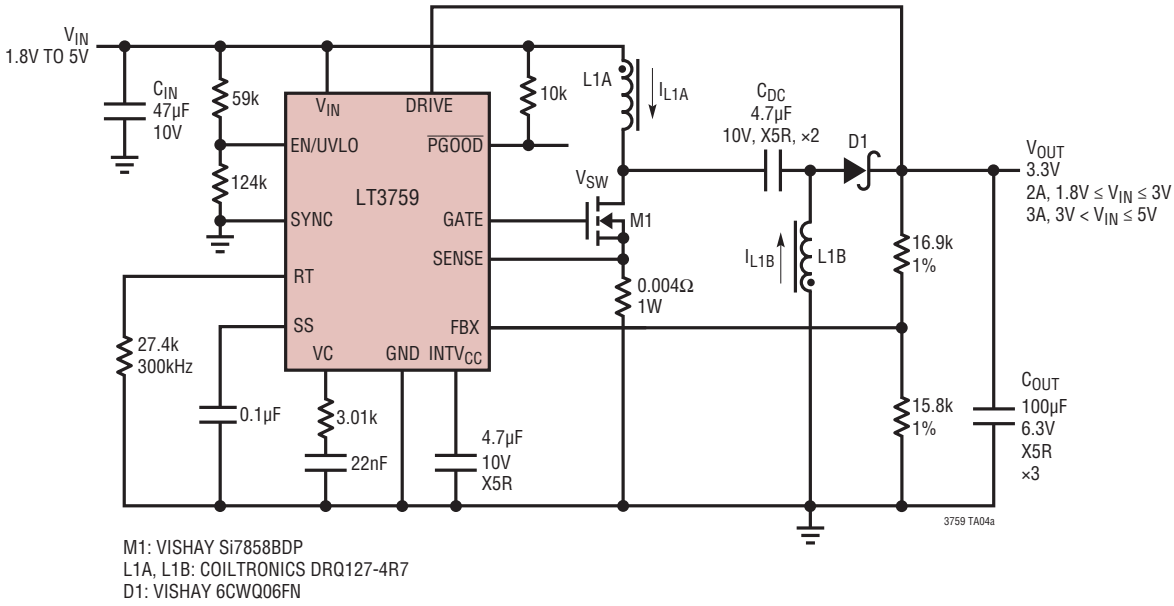
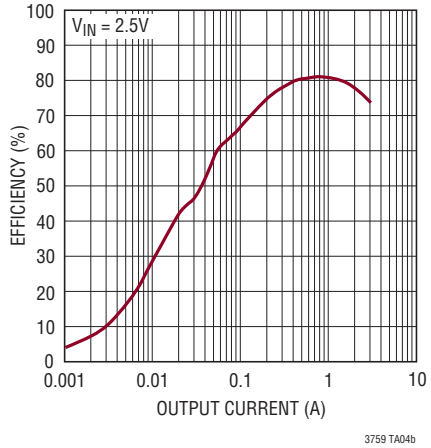
TYPICAL APPLICATIONS

1.8V to 5V Input, 3.3V/3A Output SEPIC Converter

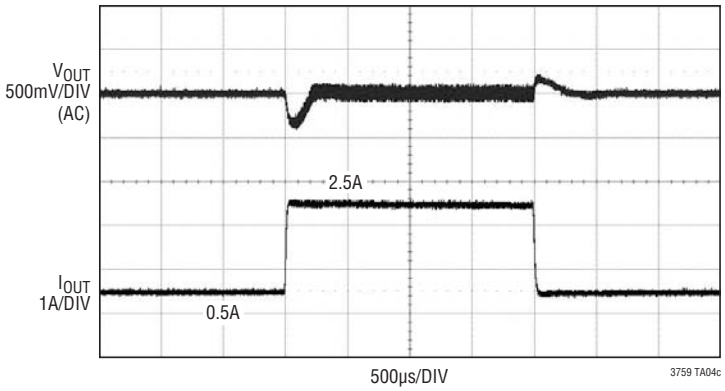


M1: VISHAY Si7858BDP
L1A, L1B: COILTRONICS DRQ127-4R7
D1: VISHAY 6CWQ06FN

Efficiency vs Output Current



Load Step Response at V_{IN} = 2.5V



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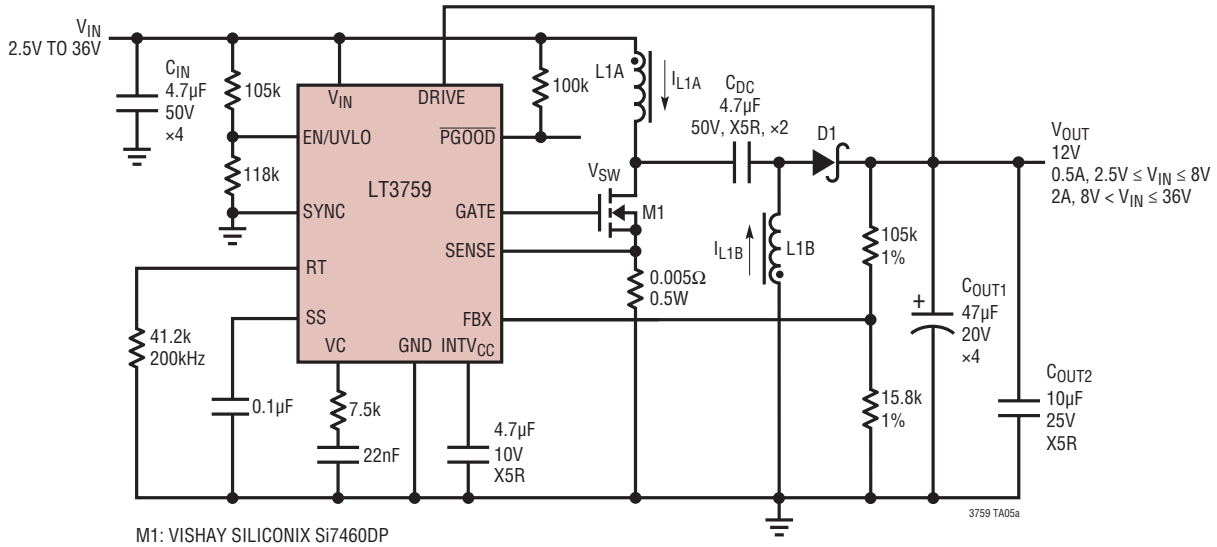
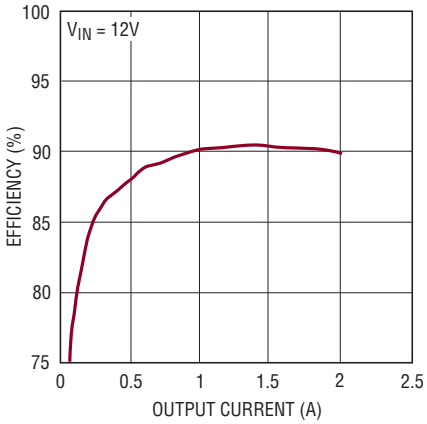
TYPICAL APPLICATIONS

2.5V to 36V Input, 12V/1A Output SEPIC Converter (Automotive 12V Regulator)

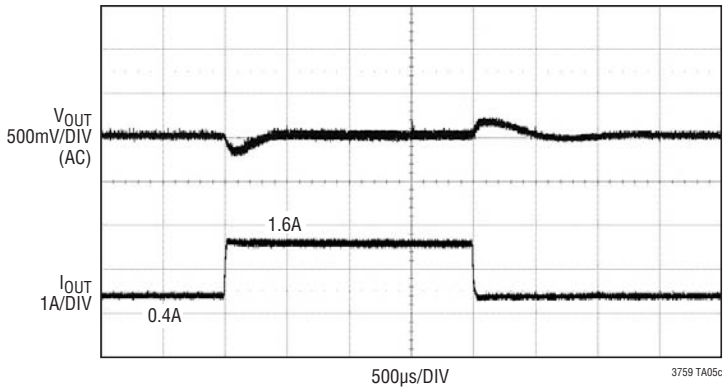


M1: VISHAY SILICONIX Si7460DP
L1A, L1B: COILTRONICS DRQ127-150
D1: VISHAY 6CWQ06FN

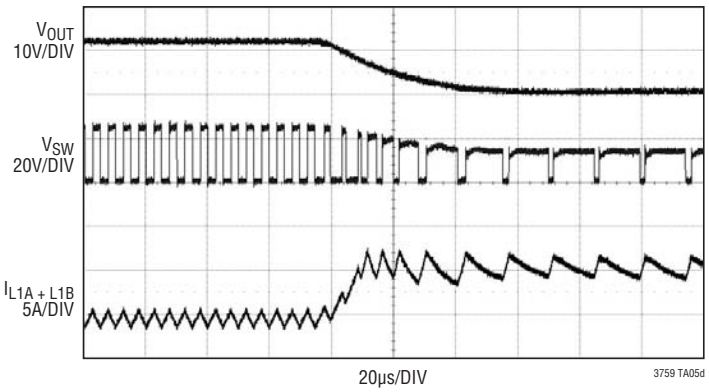
Efficiency vs Output Current



Load Step Response at V_{IN} = 12V



Frequency Foldback Waveforms When Output Short-Circuits



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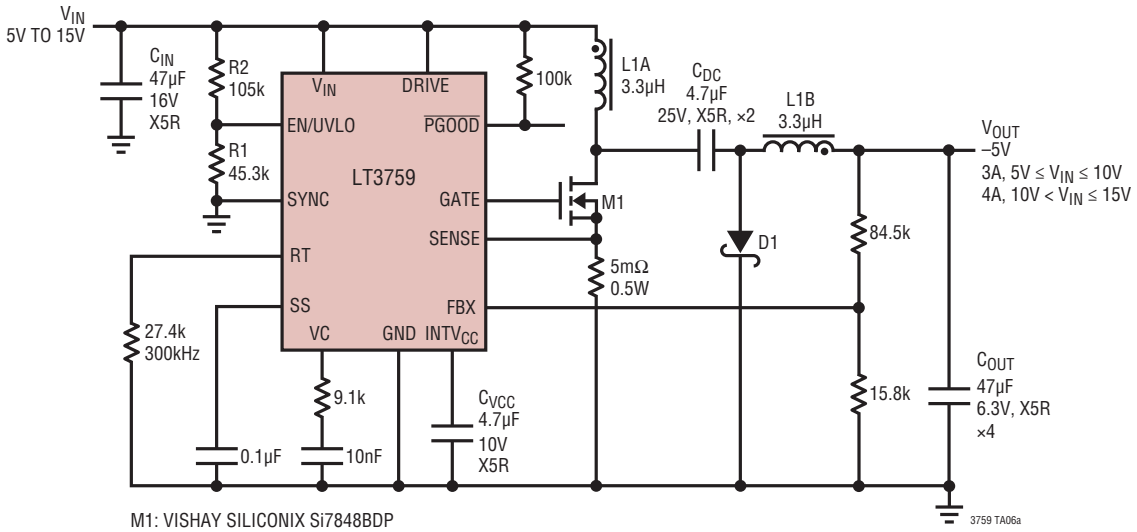
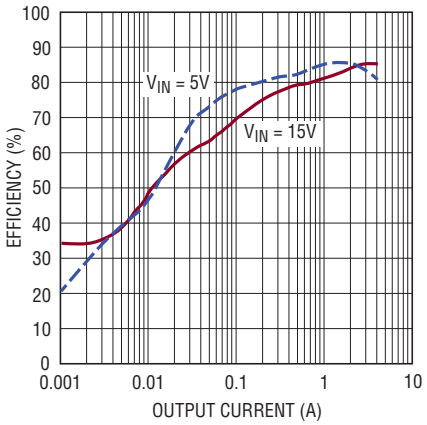
TYPICAL APPLICATIONS

5V to 15V Input, –5V/3A Output Inverting Converter

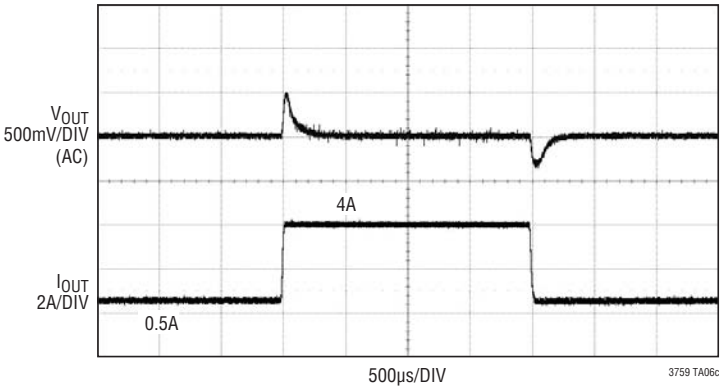


M1: VISHAY SILICONIX Si7848BDP
L1A, L1B: COILTRONICS DRQ127-3R3
D1: VISHAY 6CWQ03FN

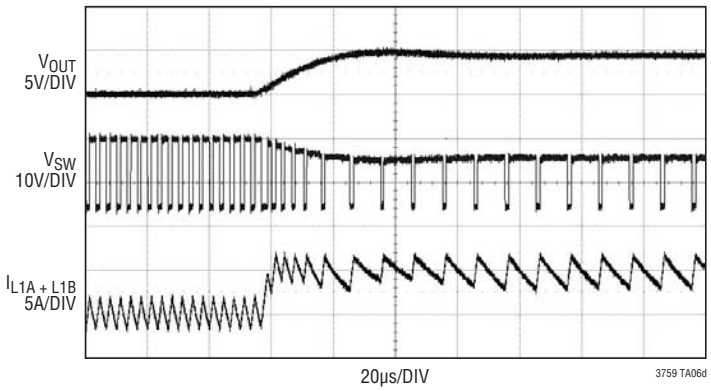
Efficiency vs Output Current



Load Step Response at V_{IN} = 10V



Frequency Foldback Waveforms When Output Short-Circuits



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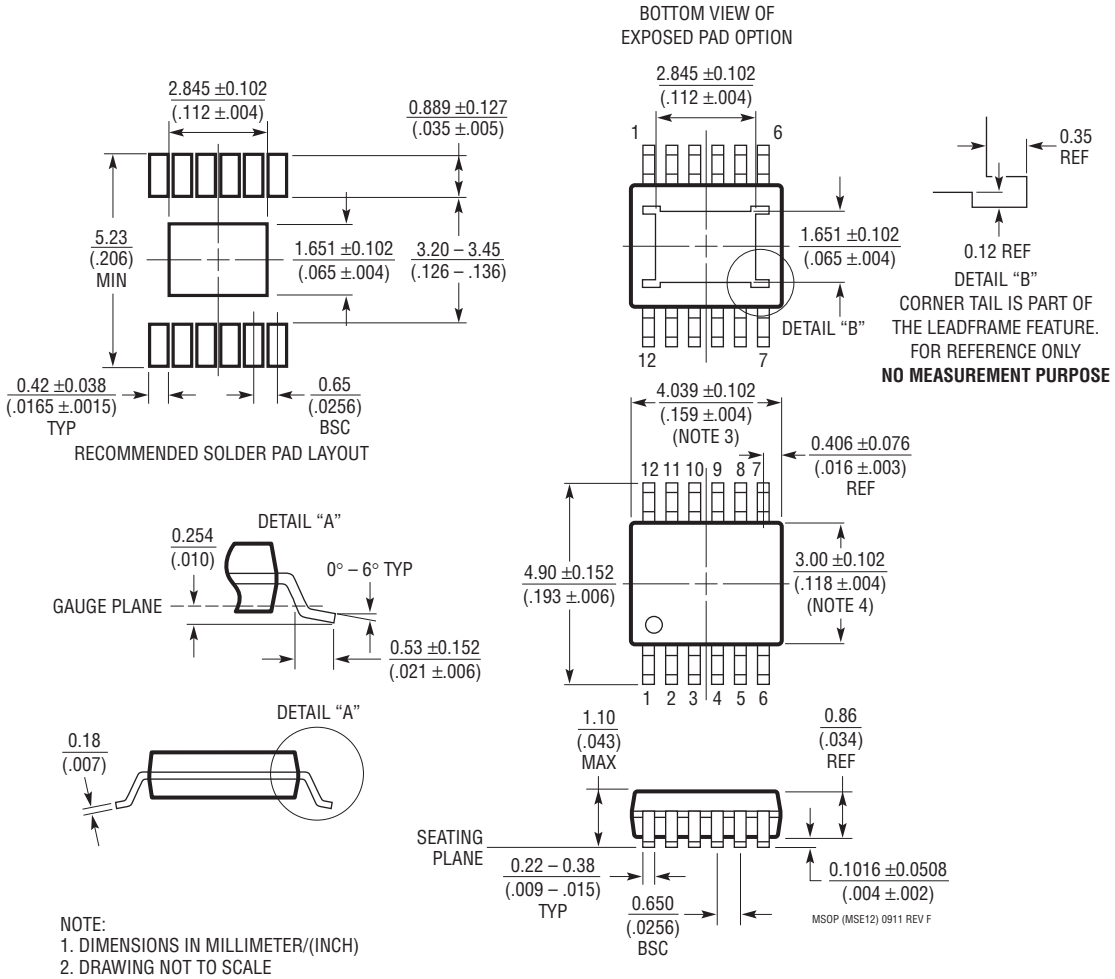
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/11	SS Pull-Up Current MIN and TYP values updated and $INTV_{CC}$ Current in Shutdown TYP value updated in Electrical Characteristics table.	3, 4
		Revised Typical Application drawing TA02a	25
B	4/12	Revised Typical Applications Schematic TA01a	1
		Added UN/UVLO Rising Spec	4
C	1/13	Corrected M1 part number on Typical Application	25

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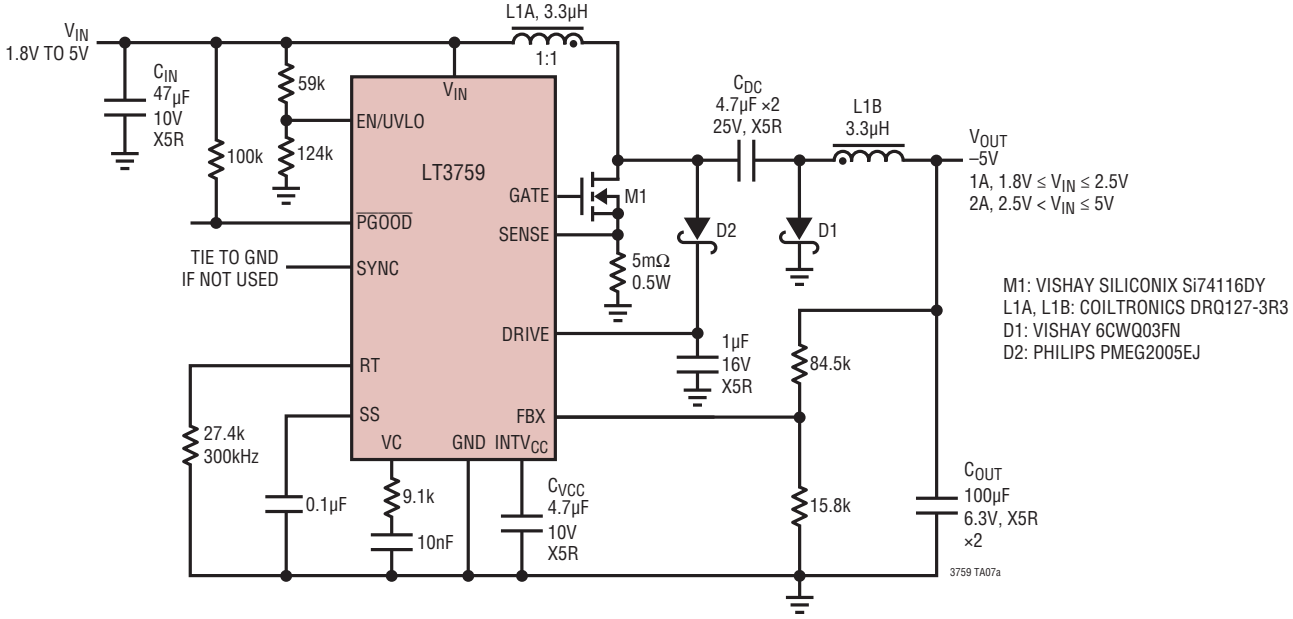
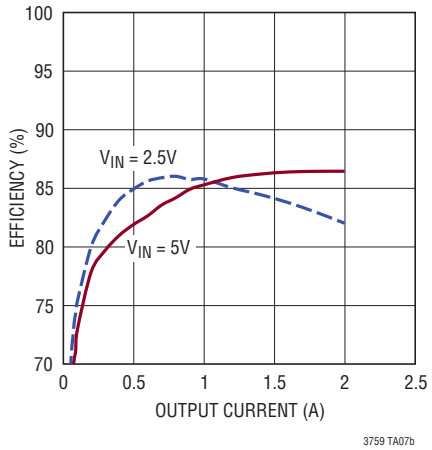
TYPICAL APPLICATION

1.8V to 5V Input, –5V/2A Output Inverting Converter



Efficiency vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3757	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3758	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3957	Boost, Flyback, SEPIC and Inverting Converter with 5A, 40V Switch	3V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN Package
LT3958	Boost, Flyback, SEPIC and Inverting Converter with 3.3A, 84V Switch	5V ≤ V_{IN} ≤ 80V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN Package
LTC3872	No R_{SENSE} Boost Controller	2.75V ≤ V_{IN} ≤ 9.8V, TSOT-23 and 2mm × 3mm DFN-8

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