available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.
Two pins are dedicated to the overcurrent protection/monitoring: CEXT and OLF. The overcurrent protection circuit works dynamically: as soon as an overload is detected in either LNB output, the output is shut-down for a time Toff determined by the capacitor connected between CEXT and GND. Simultaneously the OLF pin, that is an open collector diagnostic output flag, from HIGH IMPEDANCE state goes LOW.
After the time has elapsed, the output is resumed for a time t_{on}=1/15t_{off} (typ.) and OLF goes in HIGH IMPEDANCE. If the overload is still present, the protection circuit will cycle again through t_{off} and ton until the overload is removed. Typical t_{on}+t_{off} value is 1200ms when a 4.7µF external capacitor is used.
This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up even with highly capacitive loads on LNB outputs.
The device is packaged in Multiwatt15 for thru-holes mounting and in PowerSO-20 for surface mounting. When a limited functionality in a smaller package matches design needs, a range of cost-effective PowerSO-10 solutions is also offered. All versions have built-in thermal protection against overheating damage.

(*): External components are needed to comply to level 2.x and above (bidirectiona) DiSEqC™ bus hardware requirements. DiSEqC™ is a trademark or EUTELSAT.

PIN CONFIGURATION (top view)

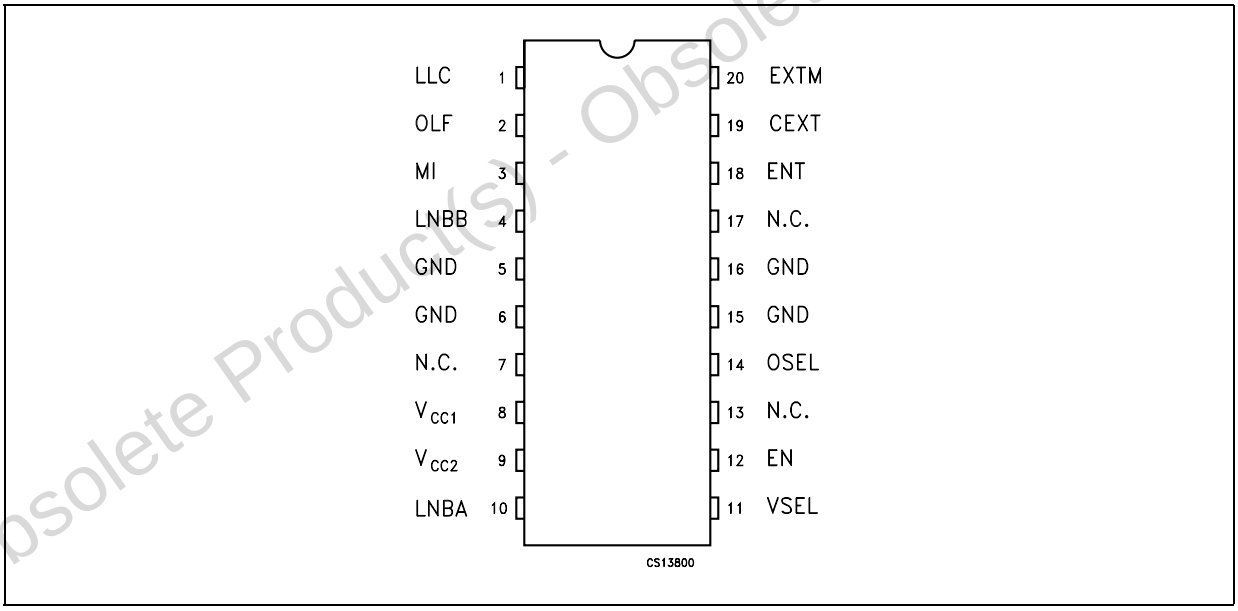


TABLE A: PIN CONFIGURATIONS

PIN N°	SYMBOL	NAME	FUNCTION
1	LLC	Line Length Compens. (1V typ)	Logic control input: see truth table
2	OLF	Over Load Flag	Logic output (open collector). Normally in HIGH IMPEDANCE, goes LOW when current or thermal overload occurs
3	MI	Master Input	In stand-by mode, the voltage on MI is routed to LNBA pin. Can be left open if bypass function is not needed
4	LNBB	Output Port	See truth tables for voltage and port selection
5, 6, 15, 16	GND	Ground	Circuit Ground. It is internally connected to the die frame
7, 13	N.C.	Not Connected	
8	V_{CC1}	Supply Input 1	15V to 27V supply. It is automatically selected when V_{OUT} = 13 or 14V
9	V_{CC2}	Supply Input 2	22V to 27V supply. It is automatically selected when V_{OUT} = 18 or 19V
10	LNBA	Output Port	See truth table voltage and port selection. In stand-by mode this port is powered by the MI pin via the internal Bypass Switch
11	V_{SEL}	Output Voltage Selection: 13 or 18V (typ)	Logic control input: see truth table
12	EN	Port Enable	Logic control input: see truth table
14	OSEL	Port Selection	Logic control input: see truth table
18	ENT	22KHz Tone Enable	Logic control input: see truth table
19	CEXT	External Capacitor	Timing Capacitor used by the Dynamic Overload protection. Typical application is 4.7µF for a 1200ms cycle
20	EXTM	External Modulator	External Modulation Input. Needs DC decoupling to the AC source. if not used, can be left open.

NOTE: the limited pin availability of the PowerSO-10 package leads to drop some functions.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter[2]	Value	Unit
V_I	DC Input Voltage (V_{CC1}, V_{CC2}, MI)	28	V
I_O	Output Current (LNBA, LNBB)	Internally Limited	mA
V_I	Logic Input Voltage (ENT, EN OSEL, VSEL, LLC)	-0.5 to 7	V
I_{SW}	Bypass Switch Current	900	mA
P_D	Power Dissipation at T_{case} < 85°C	3	W
T_{stg}	Storage Temperature Range	-40 to +150	°C
T_{op}	Operating Junction Temperature Range	-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	15	°C/W

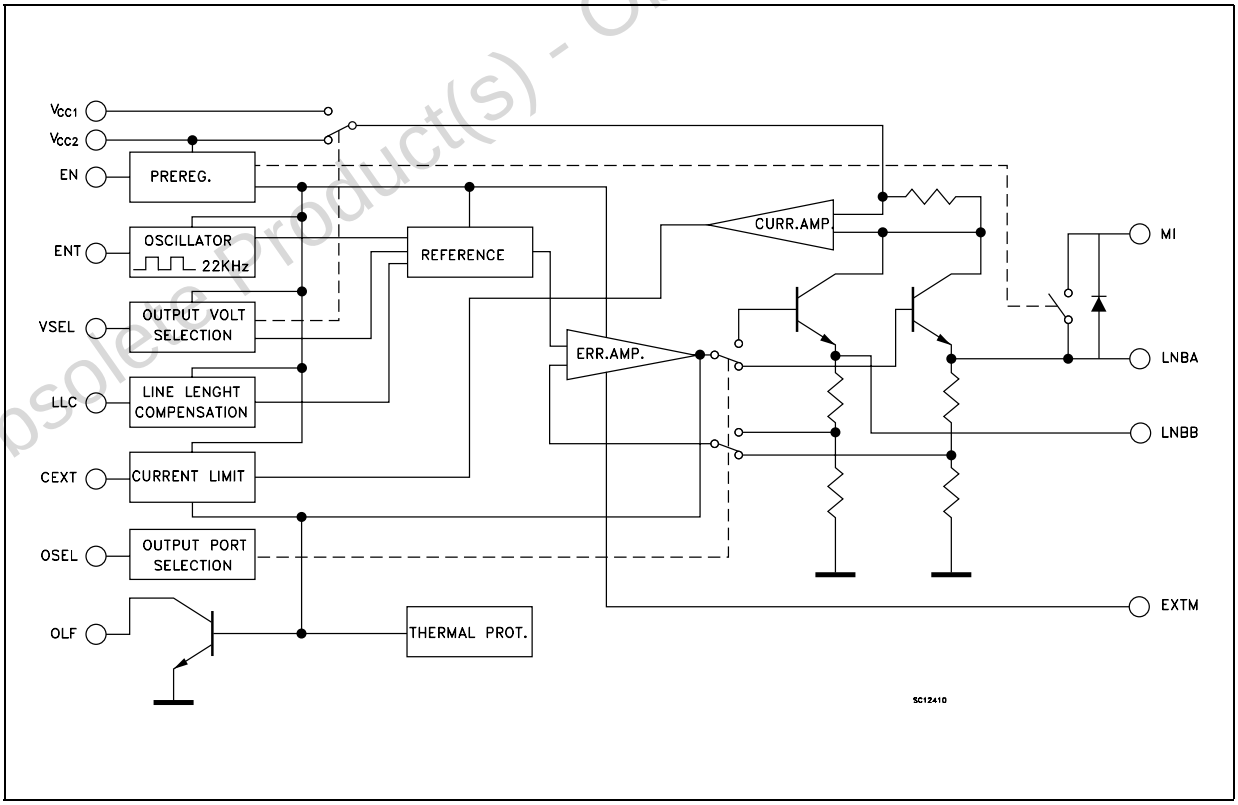
LOGIC CONTROLS TRUTH TABLE

CONTROL I/O	PIN NAME	L	H
OUT	OLF	$I_{OUT} > I_{OMAX}$ or $T_j > 150°C$	$I_{OUT} < I_{OMAX}$
IN	ENT	22KHz tone OFF	22KHz tone ON
IN	EN	See Table Below	See Table Below
IN	OSEL	See Table Below	See Table Below
IN	VSEL	See Table Below	See Table Below
IN	LLC	See Table Below	See Table Below

EN	OSEL	VSEL	LLCO	V_{LNBA}	V_{LNBB}
L	X	X	X	V_{MI} - 0.4V (typ.)	Disabled
H	L	L	L	13V (typ.)	Disabled
H	L	H	L	18V (typ.)	Disabled
H	L	L	H	14V (typ.)	Disabled
H	L	H	H	19V (typ.)	Disabled
H	H	L	L	Disabled	13V (typ.)
H	H	H	L	Disabled	18V (typ.)
H	H	L	H	Disabled	14V (typ.)
H	H	H	H	Disabled	19V (typ.)

NOTE: All logic input pins have internal pull-down resistor (typ. = 250KΩ)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS FOR LNBK SERIES (T_J = 0 to 85°C, C_I = 0.22µF, C_O =0.1µF, EN=H, ENT=L, LLC=L, V_{IN1}=16V, V_{IN2}=23V I_{OUT}=50mA, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN1}	V_{CC1} Supply Voltage	I_O = 400 mA ENT=H, VSEL=L, LLC=L	15		27	V
		I_O = 400 mA ENT=H, VSEL=L, LLC=H	16		27	V
V_{IN2}	V_{CC2} Supply Voltage	I_O = 400 mA ENT=H, VSEL=L, LLC=L	22		27	V
		I_O = 400 mA VSEL=L, LLC=H	23		27	V
V_{O1}	Output Voltage	I_O = 400 mA VSEL=L, LLC=L	17.3	18	18.7	V
		I_O = 400 mA ENT=H, VSEL=L, LLC=H		19		V
V_{O2}	Output Voltage	I_O = 400 mA VSEL=L, LLC=L	12.5	13	13.5	V
		I_O = 400 mA ENT=H, VSEL=L, LLC=H		14		V
ΔV_O	Line Regulation	V_{IN1}=15 to 18V V_{OUT}=13V		5	50	mV
		V_{IN2}=22 to 25V V_{OUT}=18V		5	50	mV
ΔV_O	Load Regulation	V_{IN1}=V_{IN2}=22V V_{OUT}=13 or 18V I_O = 0 to 3A		65	150	mV
SVR	Supply Voltage Rejection	V_{IN1} = V_{IN2} = 23 ± 0.5V_{ac} f_{ac} = 120 Hz,		45		dB
I_{MAX}	Output Current Limiting		500	650	800	mA
t_{OFF}	Dynamic Overload protection OFF Time	Output Shorted C_{EXT} =4.7µF		1100		ms
t_{ON}	Dynamic Overload protection ON Time	Output Shorted C_{EXT} =4.7µF		t_{OFF}/15		ms
f_{TONE}	Tone Frequency	ENT=H	20	22	24	KHz
A_{TONE}	Tone Amplitude	ENT=H	0.55	0.72	0.9	Vpp
D_{TONE}	Tone Duty Cycle	ENT=H	40	50	60	%
t_r, t_f	Tone Rise and Fall Time	ENT=H	5	10	15	µs
G_{EXTM}	External Modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 40KHz		5		
V_{EXTM}	External Modulation Input Voltage	AC Coupling			400	mVpp
Z_{EXTM}	External Modulation Impedance	f = 10Hz to 40KHz		400		Ω
V_{SW}	Bypass Switch Voltage Drop (MI to LNBA)	EN=L, I_{SW}=300mA, V_{CC2}-V_{MI}=4V		0.35	0.6	V
V_{OL}	Overload Flag Pin Logic LOW	I_{OL}=8mA		0.28	0.5	V
I_{OZ}	Overload Flag Pin OFF State Leakage Current	V_{OH} = 6V			10	µA
V_{IL}	Control Input Pin Logic LOW				0.8	V
V_{IH}	Control Input Pin Logic HIGH		2.5			V
I_{IH}	Control Pins Input Current	V_{IH} = 5V		20		µA
I_{CC}	Supply Current	Output Disabled (EN=L)		0.3	1	mA
		ENT=H, I_{OUT}=500mA		3.1	6	mA
I_{OBK}	Output Backward Current	EN=L V_{LNBA} = V_{LNBB} = 18V V_{IN1} = V_{IN2} = 22V or floating		0.2	3	mA
T_{SHDN}	Temperature Shutdown Threshold			150		°C

TYPICAL CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 1 : Output Voltage vs Output Current

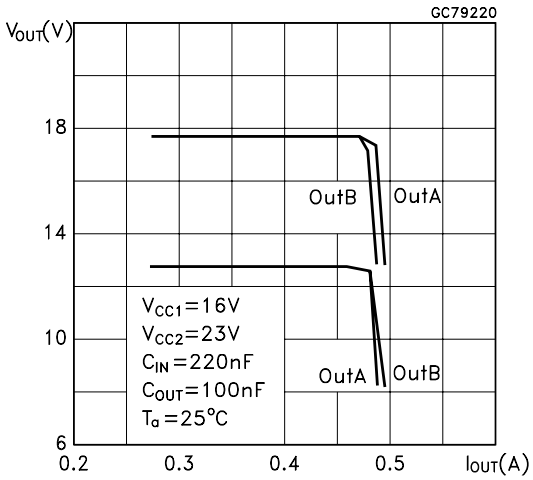


Figure 2 : Tone Duty Cycle vs Temperature

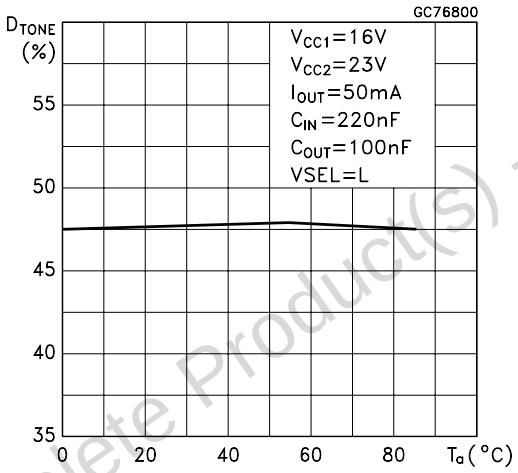


Figure 3 : Tone Fall Time vs Temperature

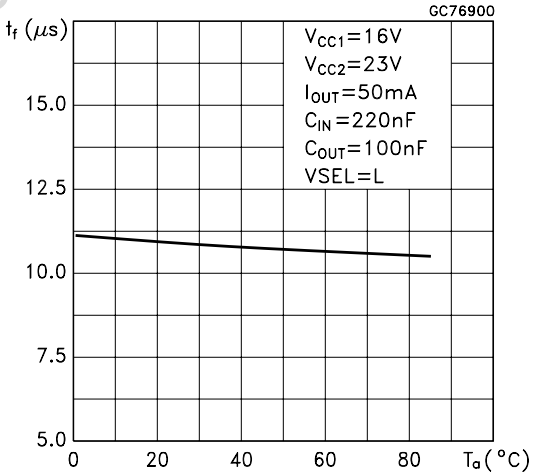


Figure 4 : Tone Frequency vs Temperature

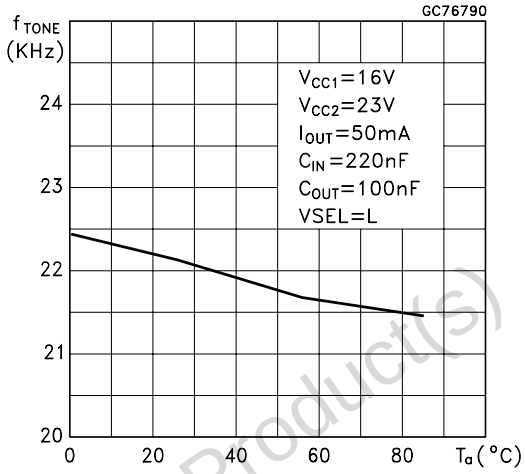


Figure 5 : Tone Rise Time vs Temperature

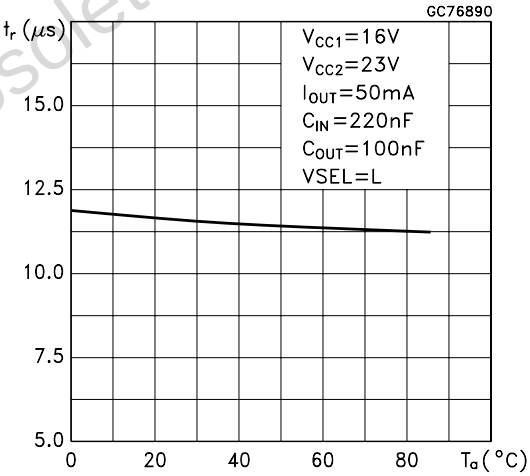


Figure 6 : Tone Amplitude vs Temperature

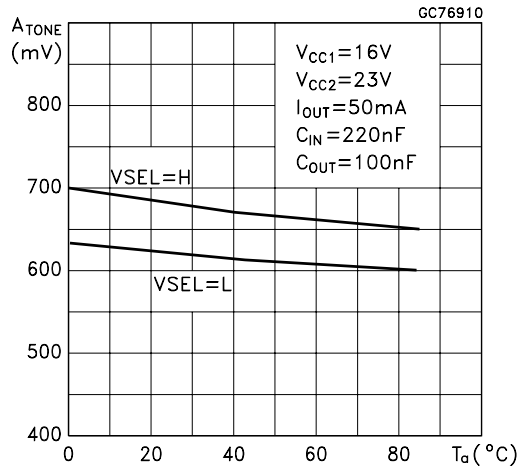


Figure 7 : S.V.R. vs Frequency

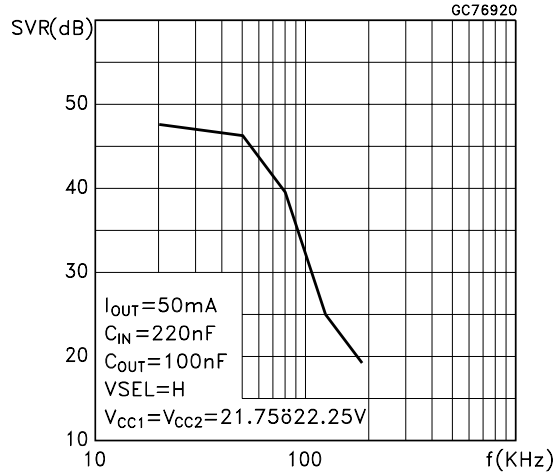


Figure 8 : External Modulation vs Temperature

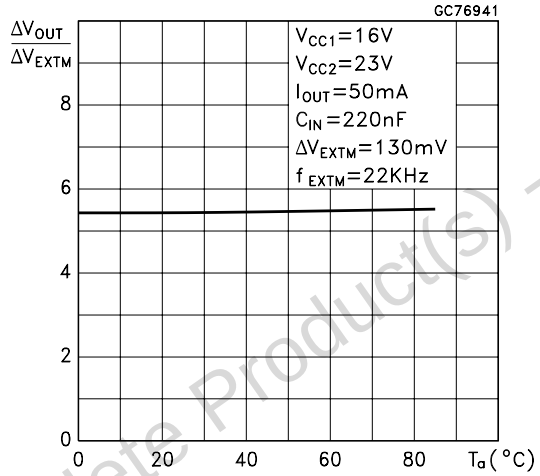


Figure 9 : Bypass Switch Drop vs Output Current

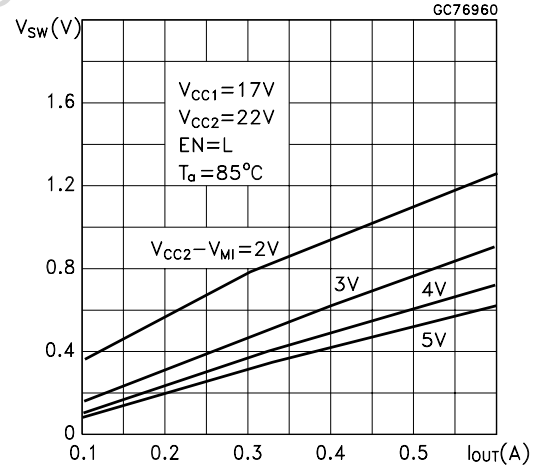


Figure 10 : LNBA External Modulation gain vs Frequency

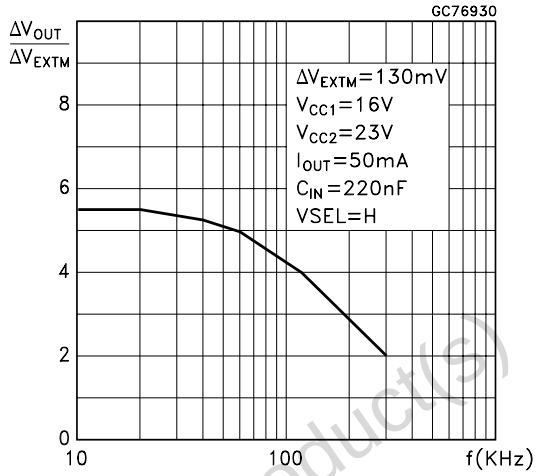


Figure 11 : Bypass switch Drop vs Output Current

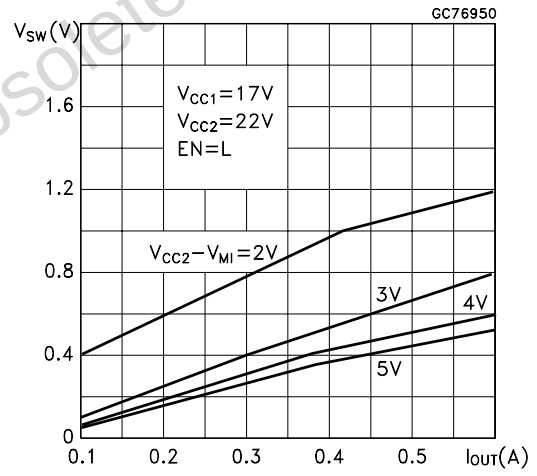


Figure 12 : overload Flag pin Logic LOW vs Flag Current

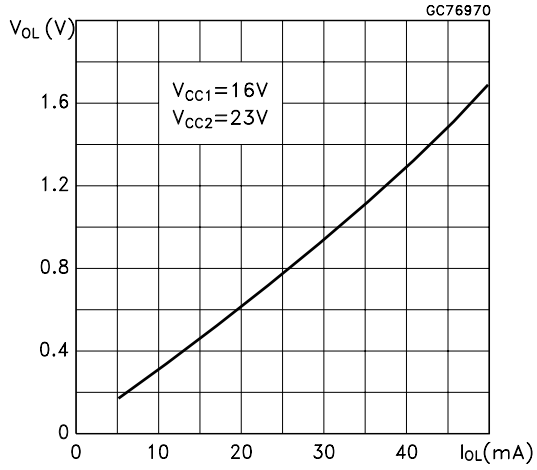


Figure 13 : Supply Voltage vs Temperature

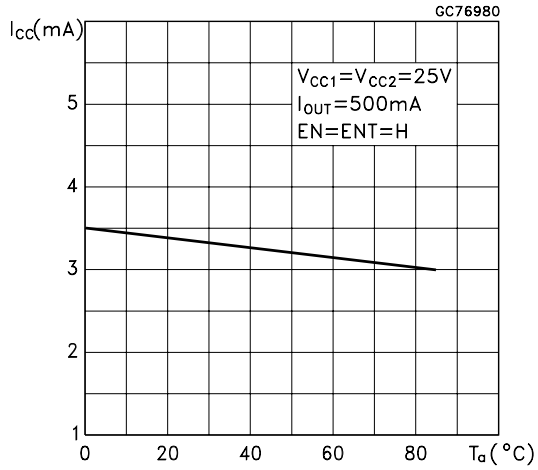


Figure 14 : Supply Current vs Temperature

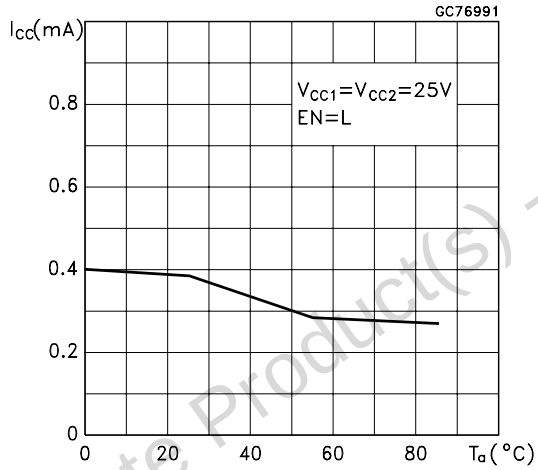


Figure 15 : Dynamic Overload protection (I_{SC} vs Time)

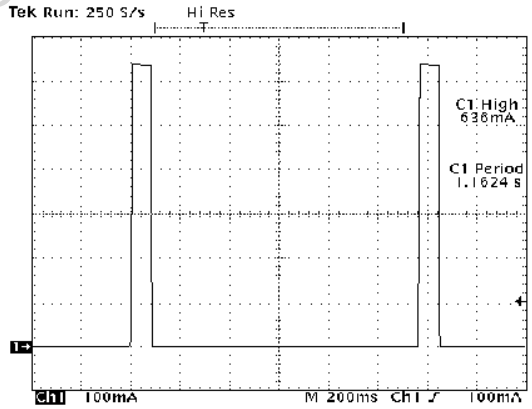


Figure 16 : Tone Enable

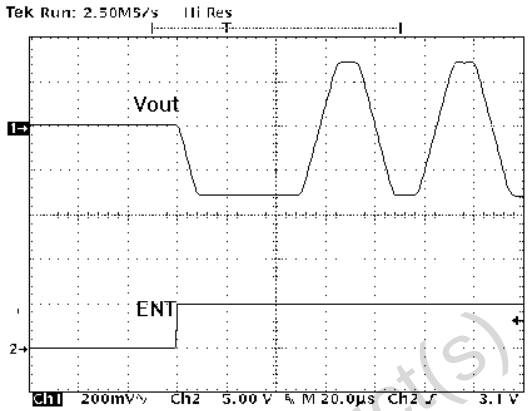


Figure 17 : Tone Disable

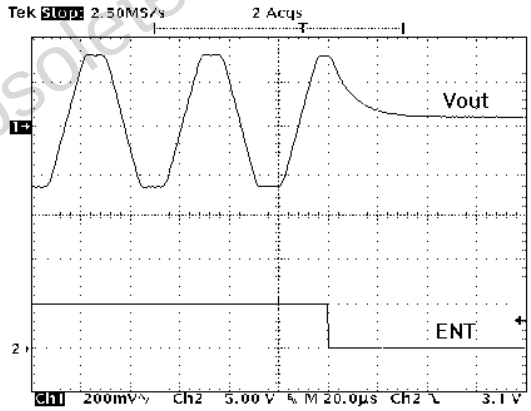


Figure 18 : 22KHz Tone

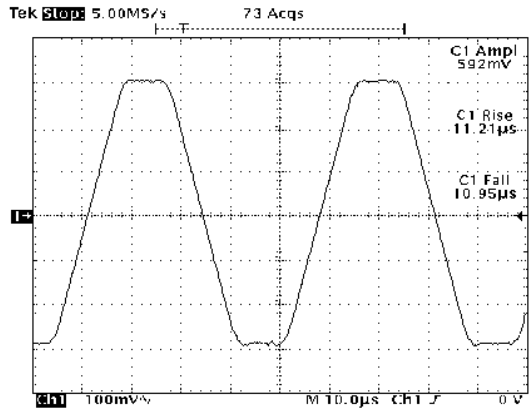


Figure 19 : Enable Time

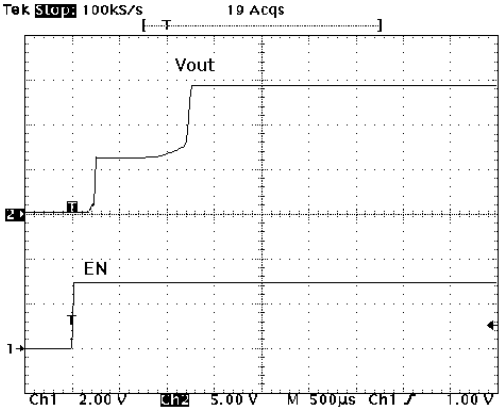


Figure 20 : Disable Time

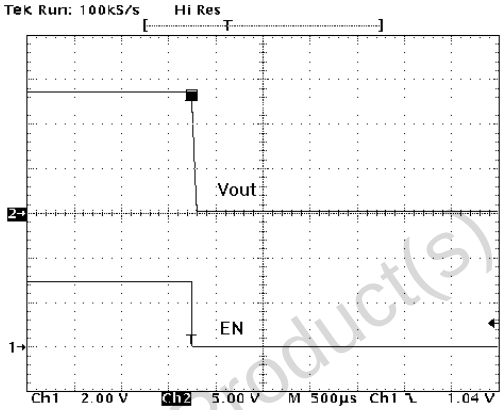


Figure 21 : 18V to 13V Change

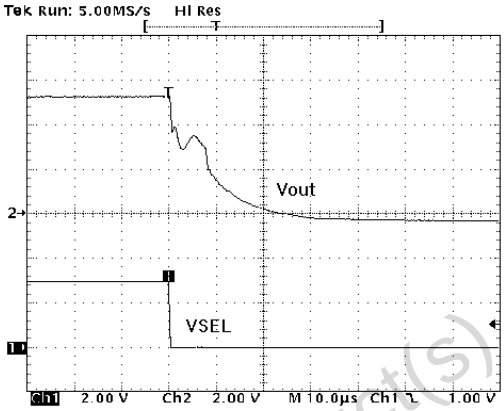
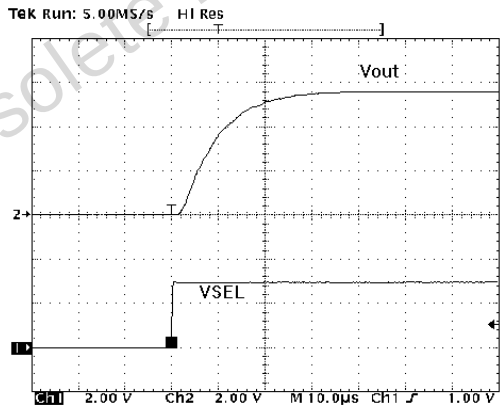
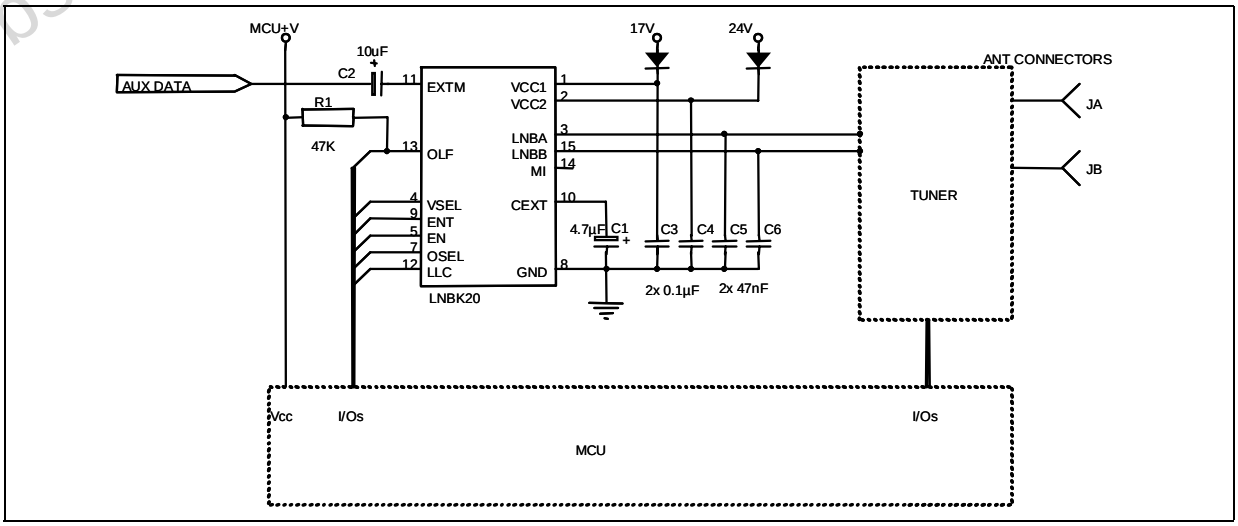


Figure 22 : 18V to 13V Change

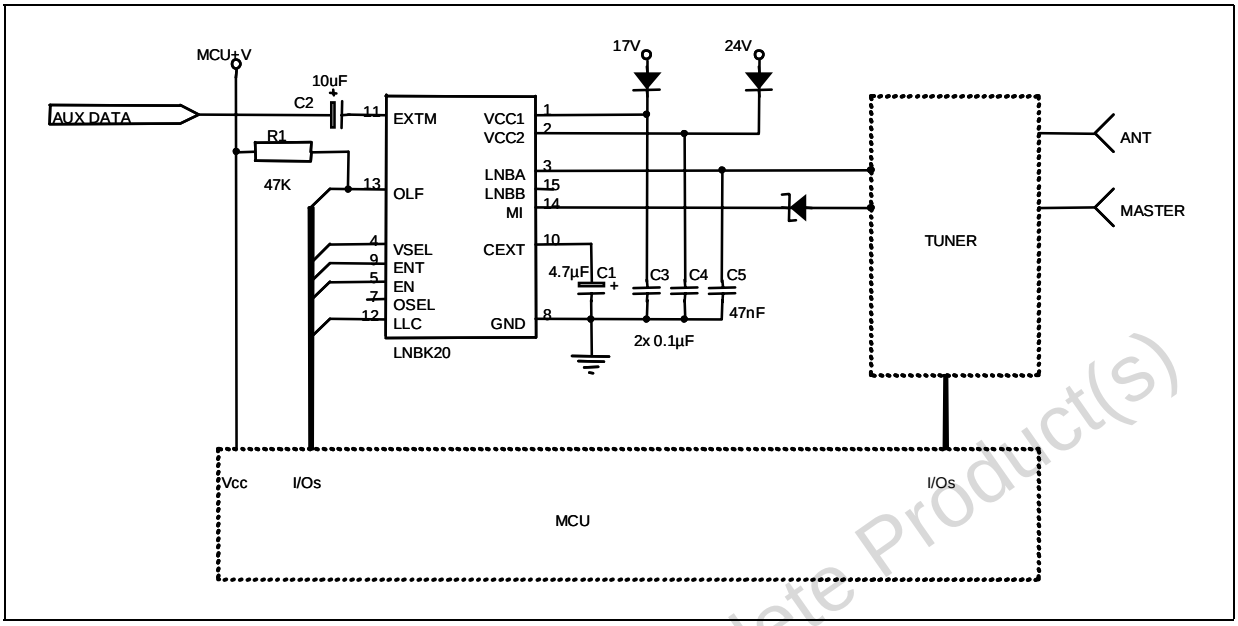


TYPICAL APPLICATION SCHEMATICS

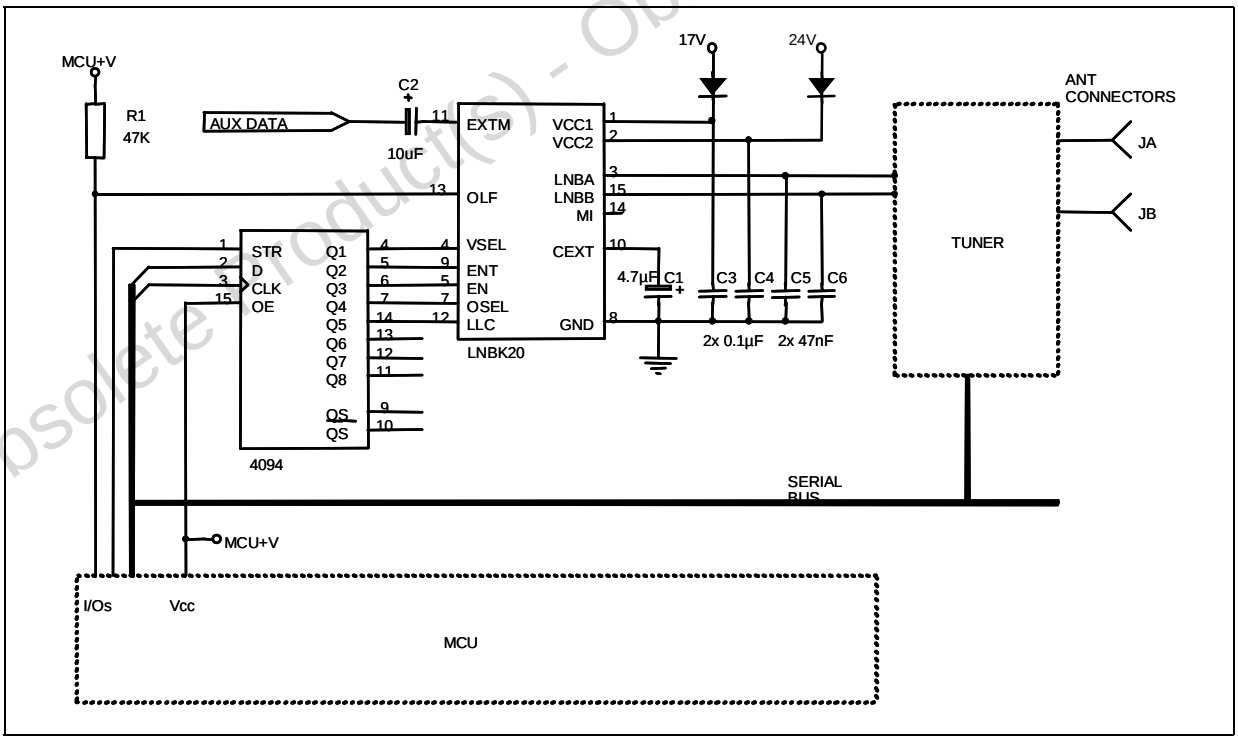
TWO ANTENNA PORTS RECEIVER



SINGLE ANTENNA RECEIVER WITH MASTER RECEIVER PORT



USING SERIAL BUS TO SAVE MPU I/Os



THERMAL DESIGN NOTE

During normal operation, this device dissipates some power. At maximum rated output current (400mA), the voltage drop on the linear regulator lead to a total dissipated power that is of about 2W. The heat generated requires a suitable heatsink to keep the junction temperature below the over temperature protection threshold. Assuming a 40°C temperature inside the Set-Top-Box case, the total Rthj-amb has to be less than 43°C/W.

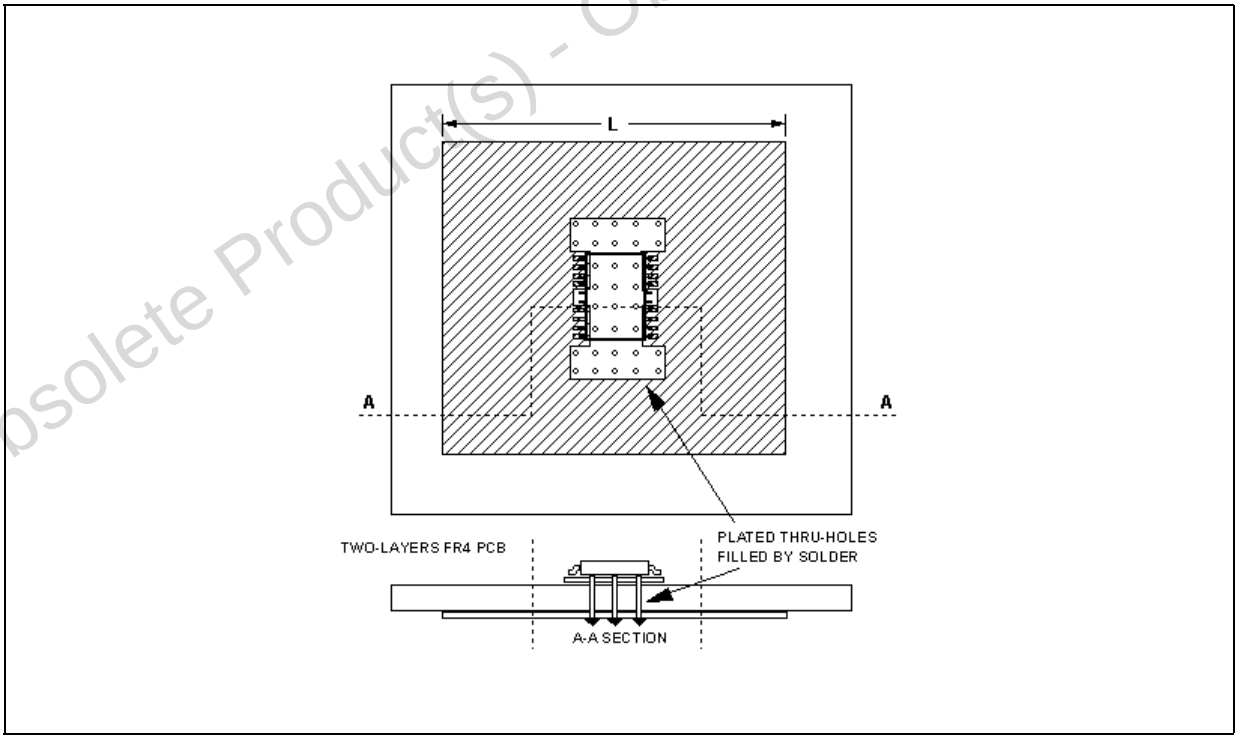
While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

The SO-20 package of this IC has 4 GND pins that are not just intended for electrical GND connection, but also to provide a low thermal resistance path between the silicon chip and the PCB heatsink. Given an Rthj-c equal to 15°C/W, a maximum of 28°C/W are left to the PCB heatsink. This figure is achieved if a minimum of 25cm^2 copper area is placed just below the IC body. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In both cases, the thermal path between the IC GND pins and the dissipating copper area must exhibit a low thermal resistance.

In figure 4, it is shown a suggested layout for the SO-20 package with a dual layer PCB, where the IC Ground pins and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when L=50mm, achieves an Rthc-a of about 28°C/W.

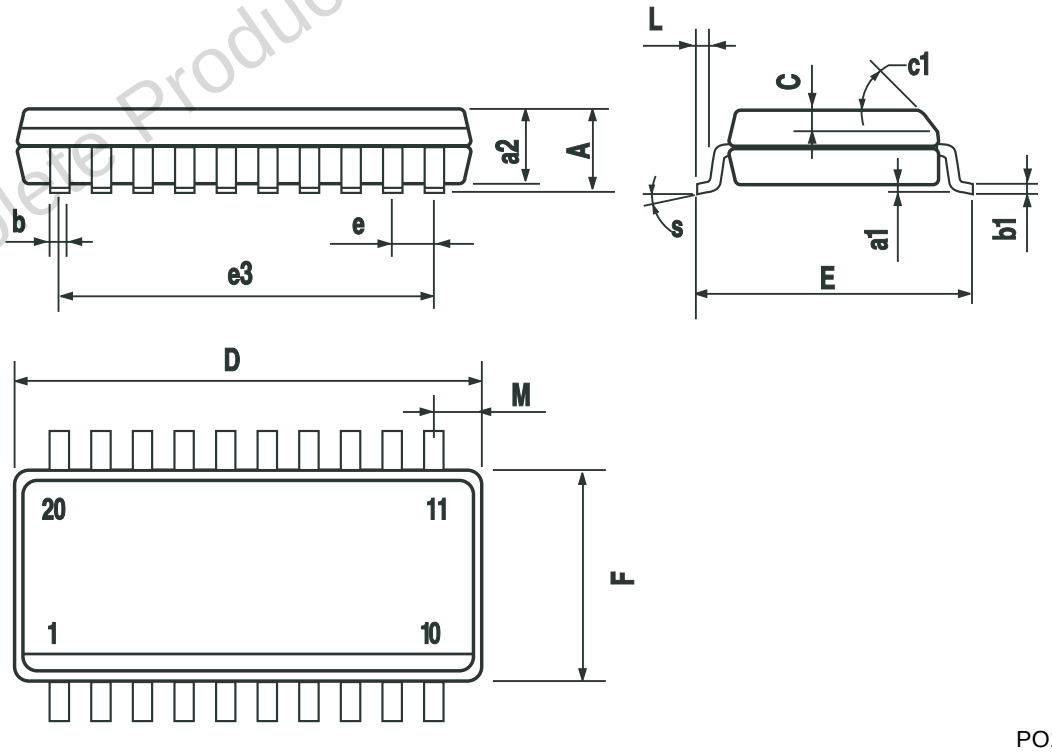
Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground pins approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

SO-20 SUGGESTED PCB HEATSINK LAYOUT



SO-20 MECHANICAL DATA

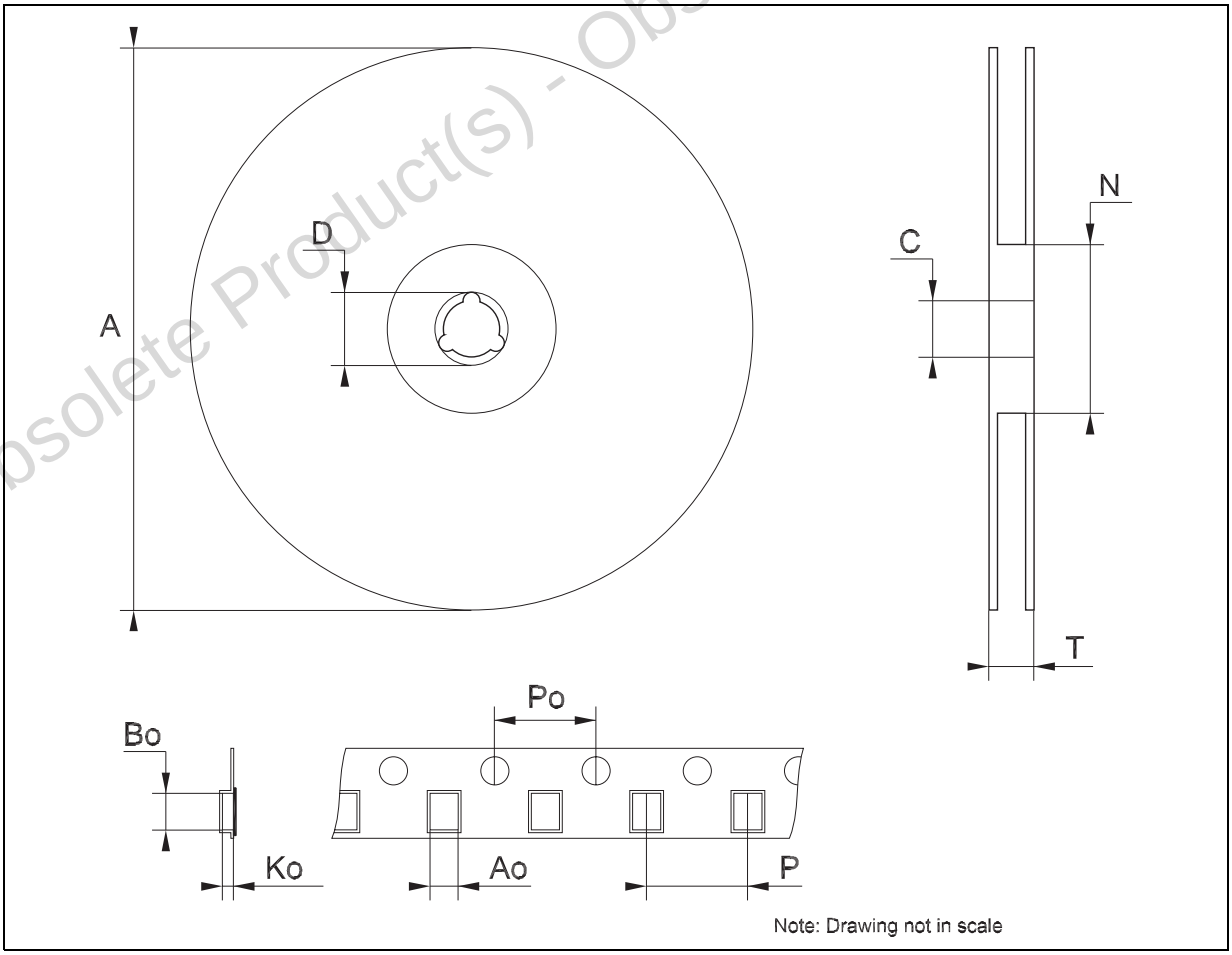
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

Tape & Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale