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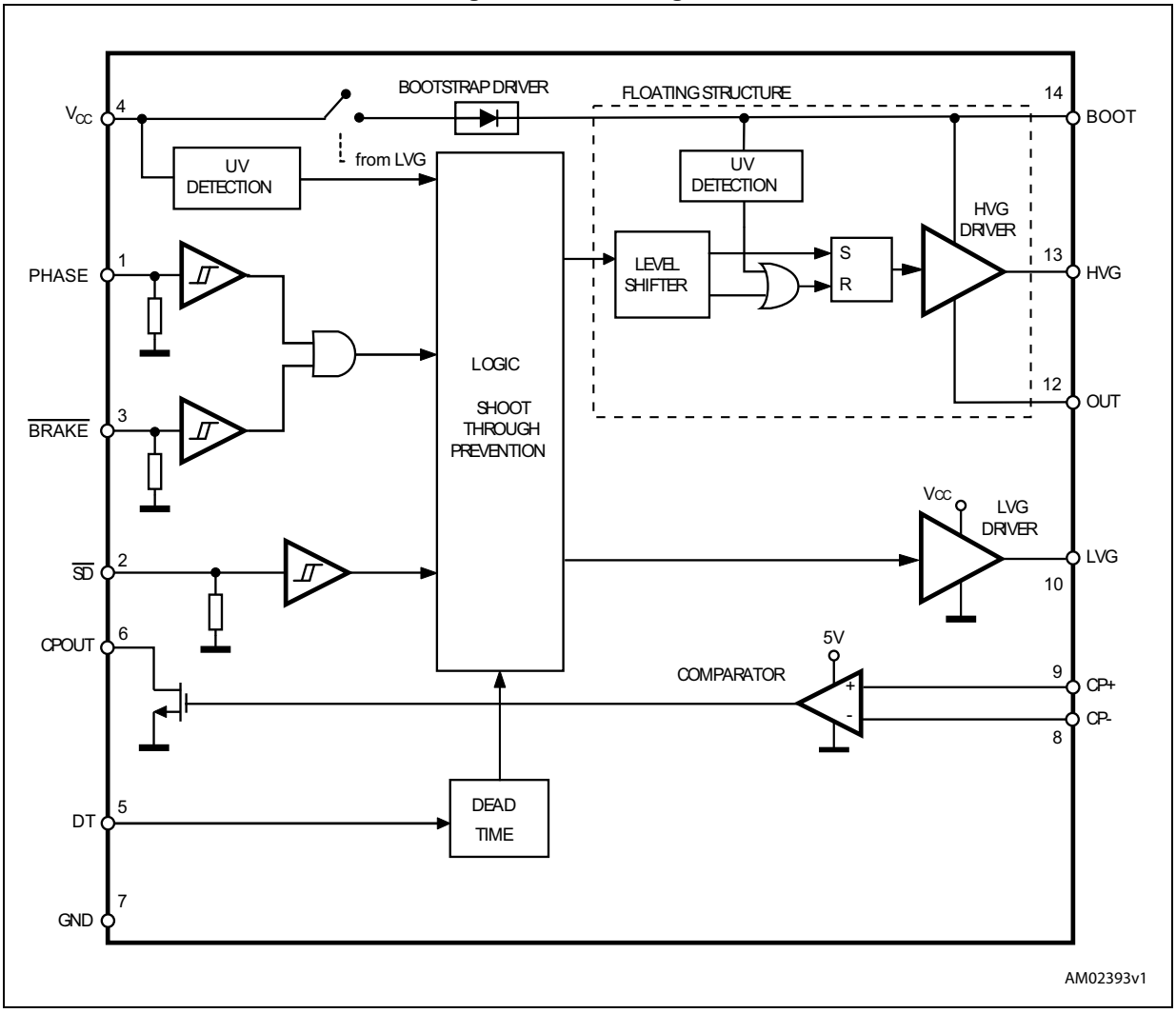
1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

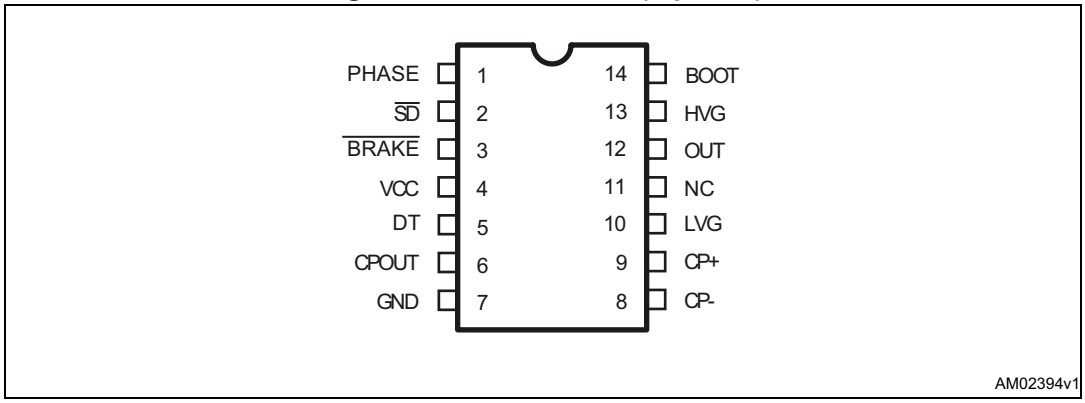


Table 1. Pin description

Pin no.	Pin name	Type	Function
1	PHASE	I	Driver logic input (active high)
2	$\overline{SD}$(1)	I	Shutdown input (active low)
3	$\overline{BRAKE}$	I	Driver logic input (active low)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	CPOUT	O	Comparator output (open drain)
7	GND	P	Ground
8	CP-	I	Comparator negative input
9	CP+	I	Comparator positive input
10	LVG(1)	O	Low-side driver output
11	NC		Not connected
12	OUT	P	High-side (floating) common voltage
13	HVG(1)	O	High-side driver output
14	BOOT	P	Bootstrapped supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Truth table

Table 2. Truth table

Inputs			Outputs	
$\overline{SD}$	PHASE	$\overline{BRAKE}$	LVG	HVG
L	X(1)	X(1)	L	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

1. X: don't care.

In the L6393 IC the two input signals PHASE and $\overline{BRAKE}$ are fed into an AND logic port and the resulting signal is in phase with the high-side output HVG and in opposition of phase with the low-side output LVG. This means that if $\overline{BRAKE}$ is kept to a high level, the PHASE signal drives the half bridge in phase with the HVG output and in opposition of phase with the LVG output. If $\overline{BRAKE}$ is set to a low level, the low-side output LVG is always ON and the high-side output HVG is always OFF, whatever the PHASE signal. This kind of logic interface provides the possibility to control the power stages using the PHASE signal to select the current direction in the bridge and the $\overline{BRAKE}$ signal to perform current slow decay on the low-sides.

From the point of view of the logic operations the two signals PHASE and $\overline{BRAKE}$ are completely equivalent, that means the two signals can be exchanged without any change in the behavior on the resulting output signals (see *Figure 1*).

Note: The deadtime between the turn-OFF of one power switch and the turn-ON of the other power switch is defined by the resistor connected between the DT pin and the ground.

4 Electrical data

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	-0.3	21	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Bootstrap voltage	-0.3	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	-0.3	V_{CC} + 0.3	V
V_{CP+}	Comparator positive input voltage	-0.3	V_{CC} + 0.3	V
V_{CP-}	Comparator negative input voltage	-0.3	V_{CC} + 0.3	V
V_i	Logic input voltage	-0.3	15	V
V_{od}	Open drain voltage	-0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		800	mW
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	SO-14	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient max.	120	°C/W

4.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
V_{CC}	4	Supply voltage		10	20	V
V_{BO} (1)	14 - 12	Floating supply voltage		9.8	20	V
V_{OUT}	12	DC output voltage		- 9 (2)	580	V
V_{CP-}	8	Comparator negative input voltage	$V_{CP+} \leq 2.5$ V		V_{CC} (3)	V
V_{CP+}	9	Comparator positive input voltage	$V_{CP-} \leq 2.5$ V		V_{CC} (3)	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{BO} = V_{BOOT} - V_{OUT}$
2. LVG off. V_{CC} = 10 V. Logic is operational if V_{BOOT} > 5 V, refer to AN2785 for more details.
3. At least one of the comparator's input must be lower than 2.5 V to guarantee proper operation.

5 Electrical characteristics

5.1 AC operation

Table 6. AC operation electrical characteristics (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
AC operation							
t_{on}	1, 3 vs. 10, 13	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V V_{BOOT} = V_{CC} C_L = 1 nF V_i = 0 to 3.3 V see *Figure 3*	50	125	200	ns
t_{off}		High/low-side driver turn-off propagation delay		50	125	200	ns
t_{sd}	2 vs. 10, 13	Shutdown to high/low-side propagation delay		50	125	200	ns
MT		Delay matching, HS and LS turn-on/off				30	ns
DT	5	Deadtime setting range(1)	R_{DT} = 0, C_L = 1 nF	0.1	0.18	0.25	µs
			R_{DT} = 37 kΩ, C_L = 1 nF, C_{DT} = 100 nF	0.48	0.6	0.72	
			R_{DT} = 136 kΩ, C_L = 1 nF, C_{DT} = 100 nF	1.35	1.6	1.85	
			R_{DT} = 260 kΩ, C_L = 1 nF, C_{DT} = 100 nF	2.6	3.0	3.4	
MDT		Matching deadtime (2)	R_{DT} = 0 Ω; C_L = 1 nF			80	ns
			R_{DT} = 37 kΩ; C_L = 1 nF; C_{DT} = 100 nF			120	
			R_{DT} = 136 kΩ; C_L = 1 nF; C_{DT} = 100 nF			250	
			R_{DT} = 260 kΩ; C_L = 1 nF; C_{DT} = 100 nF			400	
t_r	10, 13	Rise time	C_L = 1 nF		75	120	ns
t_f		Fall time	C_L = 1 nF		35	70	ns

1. See *Figure 4.*
2. MDT = I DT_{LH} - DT_{HL} I see *Figure 5 on page 12.*

Figure 3. Timing

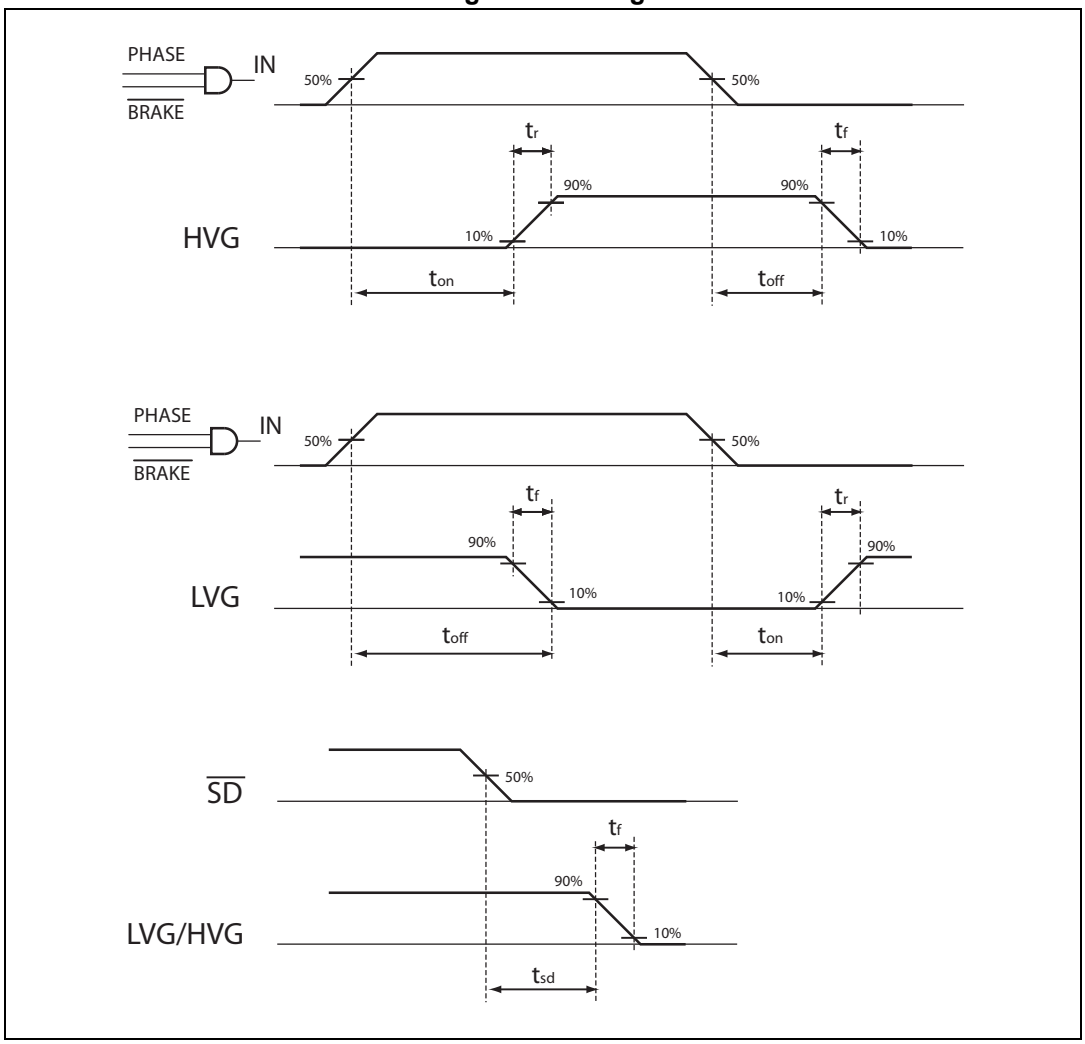
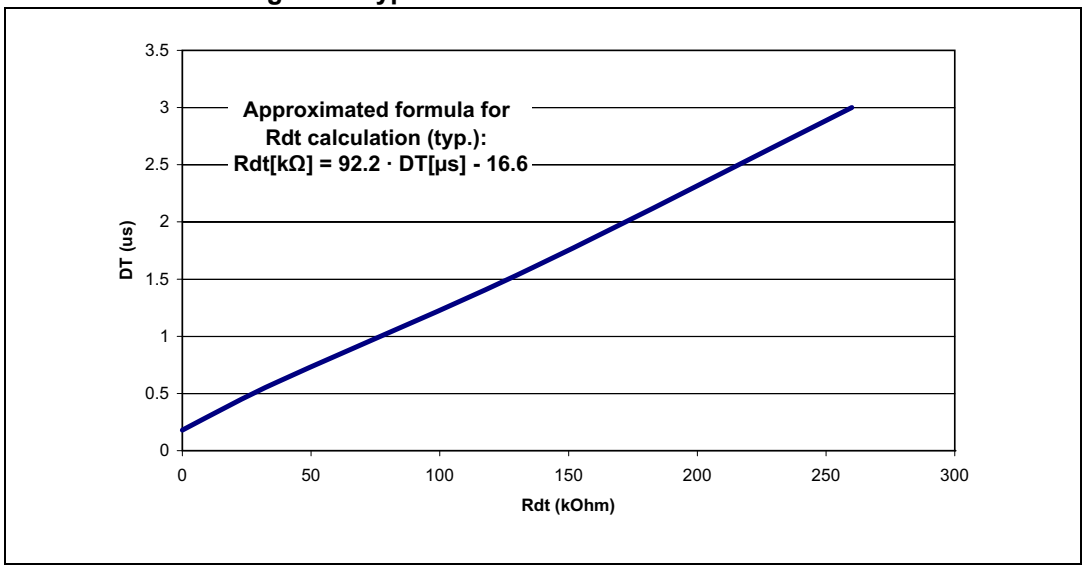


Figure 4. Typical deadtime vs. DT resistor value



5.2 DC operation

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low supply voltage section							
V_{CC_hys}	4	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}		V_{CC} UV turn-ON threshold		9	9.5	10	V
V_{CC_thOFF}		V_{CC} UV turn-OFF threshold		7.6	8	8.4	
I_{QCCU}		Undervoltage quiescent supply current	V_{CC} = 7 V; $\overline{SD}$ = 5 V; PHASE and $\overline{BRAKE}$ = GND; R_{DT} = 0 Ω; CP + = GND; CP - = 0.5 V		110	150	µA
I_{QCC}		Quiescent current	V_{CC} = 15 V; $\overline{SD}$ = 5 V; PHASE and $\overline{BRAKE}$ = GND; R_{DT} = 0 Ω; CP + = GND; CP - = 0.5 V		600	1000	
Bootstrapped supply voltage section(1)							
V_{BO_hys}	14	V_{BO} UV hysteresis		0.8	1.0	1.2	V
V_{BO_thON}		V_{BO} UV turn-ON threshold		8.2	9	9.8	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		7.3	8	8.7	V
I_{QBOU}		Undervoltage V_{BOOT} quiescent current	V_{BO} = 7 V $\overline{SD}$ = 5 V; PHASE and $\overline{BRAKE}$ = 5 V; R_{DT} = 0 Ω; CP + = GND; CP - = 0.5 V		40	100	µA
I_{QBO}		V_{BOOT} quiescent current	V_{BO} = 15 V $\overline{SD}$ = 5 V; PHASE and $\overline{BRAKE}$ = 5 V; R_{DT} = 0 Ω; CP + = GND; CP - = 0.5 V		140	210	
I_{LK}		High voltage leakage current	V_{hvg} = V_{OUT} = V_{BOOT} = 600 V			10	
R_{DSon}		Bootstrap driver on resistance(2)	LVG ON		120		Ω
Driving buffers section							
I_{so}	10, 13	High/low-side source short-circuit current	V_{IN} = V_{ih} (t_p < 10 µs)	200	290		mA
I_{si}		High/low-side sink short-circuit current	V_{IN} = V_{il} (t_p < 10 µs)	250	430		mA
Logic inputs							
V_{il}	1, 2, 3	Low level logic threshold voltage		0.8		1.1	V
V_{ih}		High level logic threshold voltage		1.9		2.25	V

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = +25 °C) (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{PHASEh}	1	PHASE logic “1” input bias current	PHASE = 15 V	20	40	100	µA
I_{PHASEl}		PHASE logic “0” input bias current	PHASE = 0 V			1	
I_{BRAKEh}	3	$\overline{BRAKE}$ logic “1” input bias current	$\overline{BRAKE}$ = 15 V	20	40	100	
I_{BRAKEl}		$\overline{BRAKE}$ logic “0” input bias current	$\overline{BRAKE}$ = 0 V			1	
I_{SDh}	2	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V	10	30	100	
I_{SDl}		$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V			1	

1. $V_{BO} = V_{BOOT} - V_{OUT}$.
2. R_{DSon} is tested in the following way:
   $R_{DSon} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1(V_{CC},V_{BOOT1}) - I_2(V_{CC},V_{BOOT2})]$ where I_1 is the pin 14 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

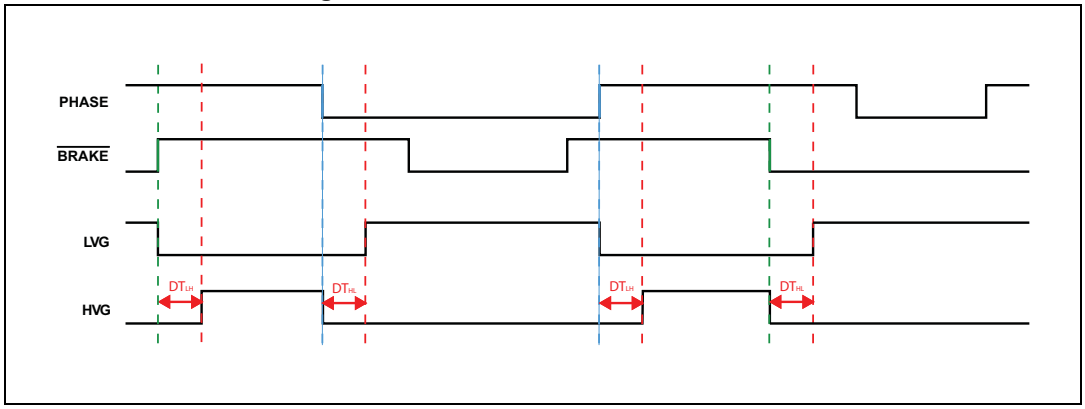
Table 8. Sense comparator (V_{CC} = 15 V, T_J = +25 °C)(1)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	8, 9	Input offset voltage		-15		15	mV
I_{ib}		Input bias current	V_{CP+} = 1 V			1	µA
V_{ol}	6	Open drain low level output voltage	I_{od} = - 3 mA			0.5	V
t_{d_comp}		Comparator delay	R_{pu} = 100 kΩ to 5 V; V_{CP-} = 0.5 V		90	130	ns
SR	6	Slew rate	C_L = 180 pF, R_{pu} = 5 kΩ		60		V/µs

1. The comparator is disabled when V_{CC} is in UVLO condition.

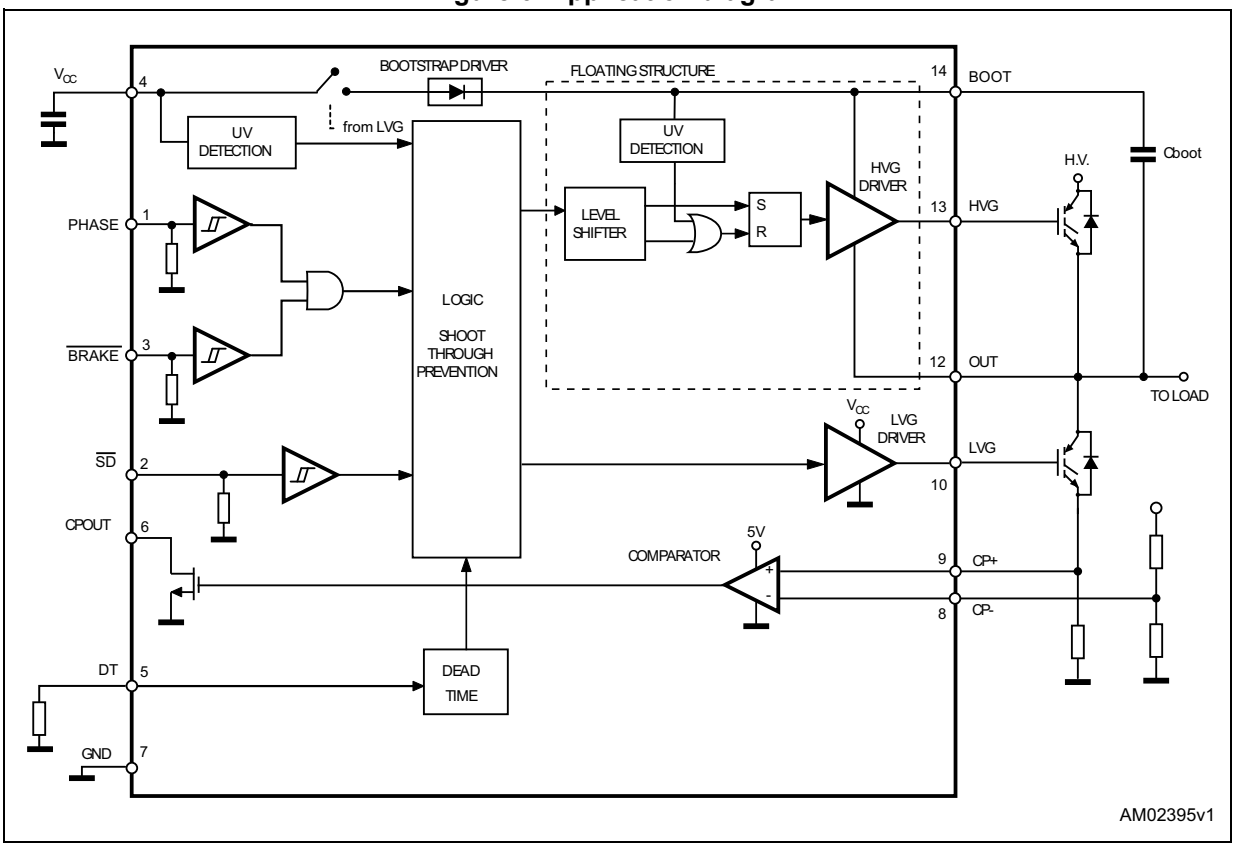
6 Waveform definition

Figure 5. Deadtime waveform definition



7 Typical application diagram

Figure 6. Application diagram



8 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 7*.a). In the L6393 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 7*.b. An internal charge pump (*Figure 7*.b) provides the DMOS driving voltage.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOSFET can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOSFET total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} \gg C_{EXT}$$

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

E.g.: HVG steady state consumption is lower than 200 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has a great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOSFET, R_{DSon} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

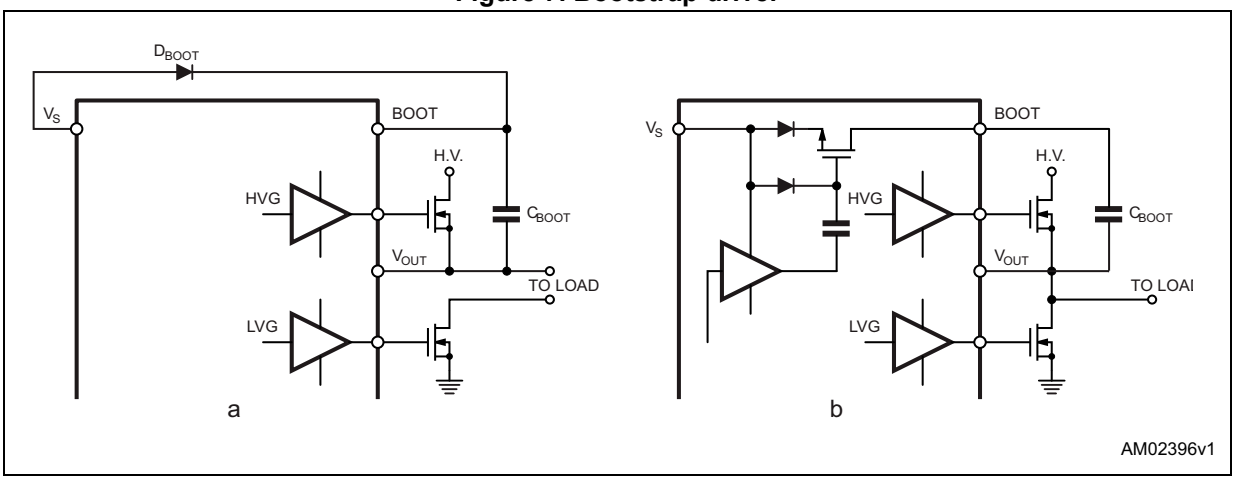
For example: using a power MOSFET with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu S} \cdot 120\Omega \sim 0.7V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 7. Bootstrap driver



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

SO-14 package information

Figure 8. SO-14 package outline

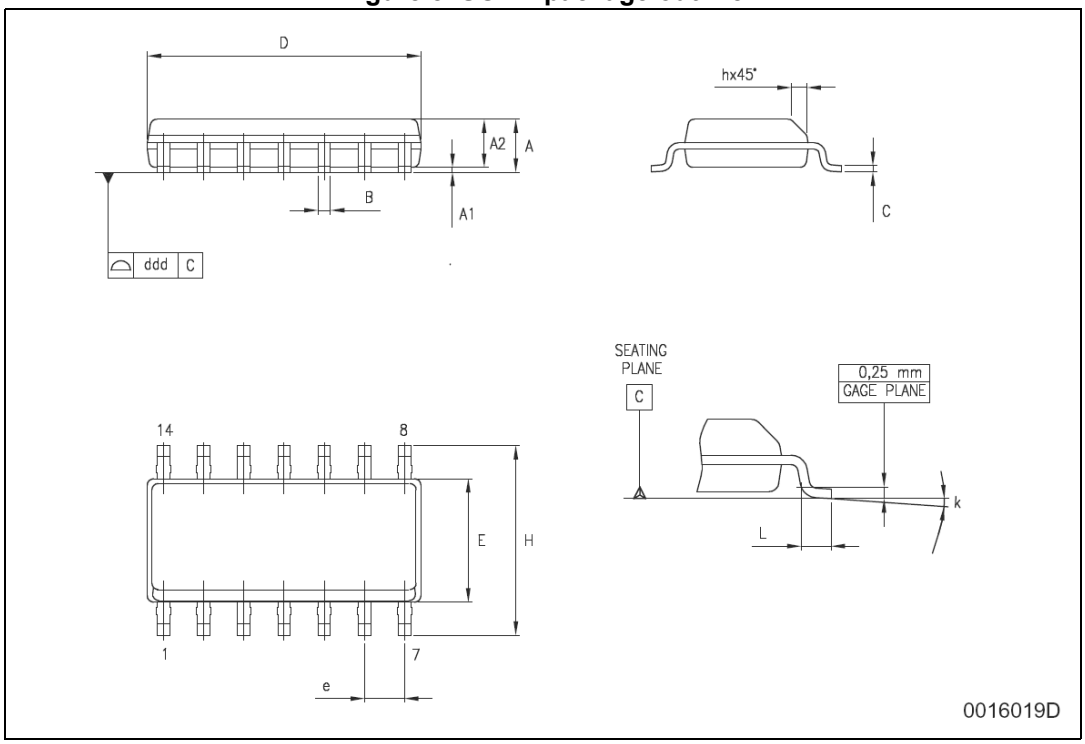
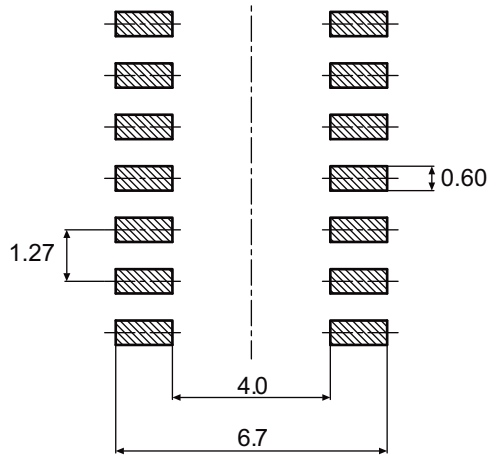


Table 9. SO-14 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

Figure 9. SO-14 footprint



10 Order codes

Table 10. Order codes

Order codes	Package	Packaging
L6393D	SO-14	Tube
L6393DTR		Tape and reel

11 Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Mar-2008	1	Initial release
18-Mar-2008	2	Cover page updated
17-Nov-2009	3	Updated: Cover page, *Table 4 on page 6*, *Table 6 on page 7*, *Table 7 on page 8*, *Table 8 on page 10*, *Table 9 on page 11*
11-Aug-2010	4	Updated: *Table 1 on page 1, Table 5 on page 7 and Table 7 on page 10.*
18-Sep-2015	5	Removed DIP-14 package from the entire document. Updated *Table 3 on page 6* (added ESD parameter and value, removed note below *Table 3*). Updated *Table 4 on page 6* (updated $R_{th(JA)}$ value). Updated *Table 7 on page 10* (updated V_{il} and V_{ih} parameters and values, updated note *2.* below *Table 7* - replaced V_{CBOOTx} by V_{BOOTx}). Updated *Table 8 on page 11* (added conditions to title and note *1.*). Named and numbered *Equation 1 on page 14*, *Equation 2 on page 14* and *Equation 3 on page 15* . Updated *Section 9 on page 16* (added/updated titles, reversed order of *Figure 8* and *Table 9*, updated header of *Table 9*, added *Figure 9*). Updated *Table 10 on page 18* (moved from page 1 to page 18, added and updated titles). Updated cross-references throughout document. Minor modifications throughout document.