TABLE OF CONTENTS

Document Number: DS-000038
Revision: 1.0

Document Number: DS-000038
Revision: 1.0

SPECIFICATIONS

TABLE 1. ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{DD} = 1.8 to 3.3 V, SCK = 3.072 MHz, C_{LOAD} = 30 pF unless otherwise noted. Typical specifications are not guaranteed.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PERFORMANCE							
Directionality				Omni			
Sensitivity		1 kHz, 94 dB SPL	−27	−26	−25	dB FS	
Signal-to-Noise Ratio (SNR)				65		dBA	
Equivalent Input Noise (EIN)				29		dBA SPL	
Acoustic Dynamic Range		Derived from EIN and acoustic overload point		87		dB	
Digital Dynamic Range		Derived from EIN and full-scale acoustic level		91		dB	
Frequency Response		Low frequency −3 dB point		50		Hz	1
		High frequency −3 dB point		>20		kHz	
Total Harmonic Distortion (THD)		105 dB SPL		0.3	1	%	
Power-Supply Rejection (PSR)		217 Hz, 100 mVp-p square wave superimposed on VDD = 1.8 V (A-weighted)		−80		dB FS	
Power-Supply Rejection – Swept Sine		1 kHz sine wave		−90		dB FS	
Acoustic Overload Point		10% THD		116		dB SPL	
Full-Scale Digital Input		0 dB FS output		120		dB SPL	
Noise Floor		20 Hz to 20 kHz, A-weighted, rms		−91		dB FS	
POWER SUPPLY							
Supply Voltage (V_{DD})			1.62		3.63	V	
Supply Current (I_S)	V_{DD} = 1.8 V	Normal Mode		1.0	1.4	mA	
		Standby		5	20	µA	
	V_{DD} = 3.3 V	Normal Mode		1.1	1.5	mA	
		Standby		7	24	µA	
DIGITAL FILTER							
Group Delay		Acoustic input to digital output – includes filter and I^2S serial output		$2/f_S$		sec	
Pass Band Ripple					±0.3	dB	
Stop Band Attenuation				58		dB	
Pass Band		fs = 48 kHz		20		kHz	

Note 1: See Figures 4 and 5.

Document Number: DS-000038
Revision: 1.0

TABLE 2. I²S DIGITAL INPUT/OUTPUT

(–40°C < T_A < +85°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	MAX	UNITS	NOTES
DIGITAL INPUT					
Voltage Input Low (V_{OL})		0	0.25 × V_{DD}	V	
Voltage Input High (V_{OH})		0.7 × V_{DD}	V_{DD}	V	
SD DIGITAL OUTPUT					
Voltage Input Low (V_{IL})		0	0.25 × V_{DD}	V	
Voltage Input High (V_{IH})		0.7 × V_{DD}	V_{DD}	V	
Maximum Load	CLK = 3.072 MHz		150	pF	

TABLE 3. SERIAL DATA PORT TIMING SPECIFICATION

(–40°C < TA < +85°C, 1.8 V < VDD < 3.3 V, unless otherwise noted.)

PARAMETER	MIN	MAX	UNITS	NOTES
SCK high (t_{SCH})	50		ns	
SCK low (t_{SCL})	50		ns	
SCK period (t_{SCP})	296		ns	
SCK frequency (f_{SCK})	0.460	3.379	MHz	
WS setup (t_{WSS})	0		ns	
WS hold (t_{WSH})	20		ns	
WS frequency (f_{WS})	7.19	52.8	kHz	

TIMING DIAGRAM

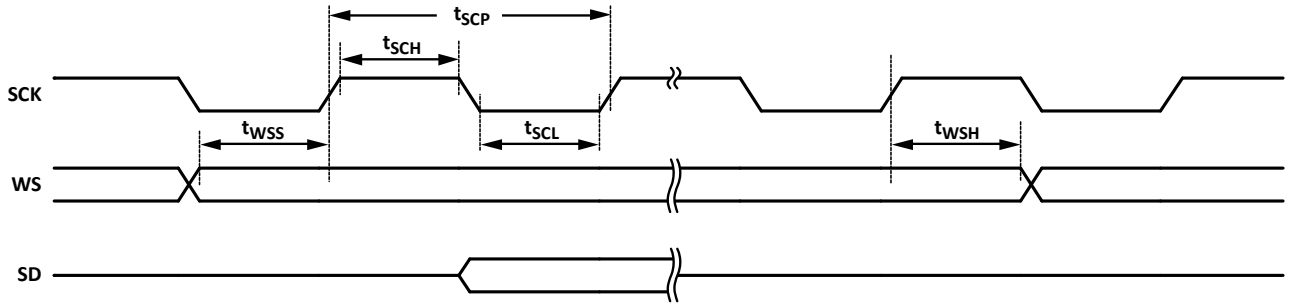


Figure 1. Serial Data Port Timing

Document Number: DS-000038
Revision: 1.0

ABSOLUTE MAXIMUM RATINGS

Stress above those listed as Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

TABLE 4. ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING
Supply Voltage (V_{DD})		−0.3 V to +3.63 V
Digital Pin Input Voltage		−0.3 V to V_{DD} + 0.3 V or 3.63 V, whichever is less
Sound Pressure Level		160 dB
Mechanical Shock		10,000 *g*
Vibration		Per MIL-STD-883 Method 2007, Test Condition B
Temperature Range	Biased	−40°C to +85°C
	Storage	−55°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Document Number: DS-000038
Revision: 1.0

SOLDERING PROFILE

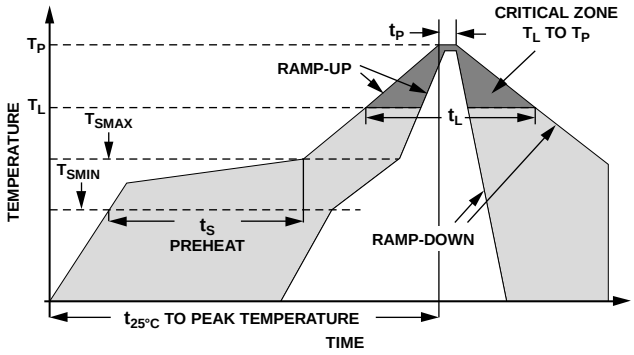


Figure 2. Recommended Soldering Profile Limits

TABLE 5. RECOMMENDED SOLDERING PROFILE

PROFILE FEATURE		Sn63/Pb37	Pb-Free
Average Ramp Rate (T_L to T_P)		1.25°C/sec max	1.25°C/sec max
Preheat	Minimum Temperature (T_{SMIN})	100°C	100°C
	Minimum Temperature (T_{SMIN})	150°C	200°C
	Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)		1.25°C/sec	1.25°C/sec
Time Maintained Above Liquidous (t_L)		45 sec to 75 sec	~50 sec
Liquidous Temperature (T_L)		183°C	217°C
Peak Temperature (T_P)		215°C ±3°C/−3°C	260°C +0°C/−5°C
Time Within +5°C of Actual Peak Temperature (t_P)		20 sec to 30 sec	20 sec to 30 sec
Ramp-Down Rate		3°C/sec max	3°C/sec max
Time +25°C ($t_{25°C}$) to Peak Temperature		5 min max	5 min max

**The reflow profile in Table 5 is recommended for board manufacturing with InvenSense MEMS microphones. All microphones are also compatible with the J-STD-020 profile*

Document Number: DS-000038
Revision: 1.0

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

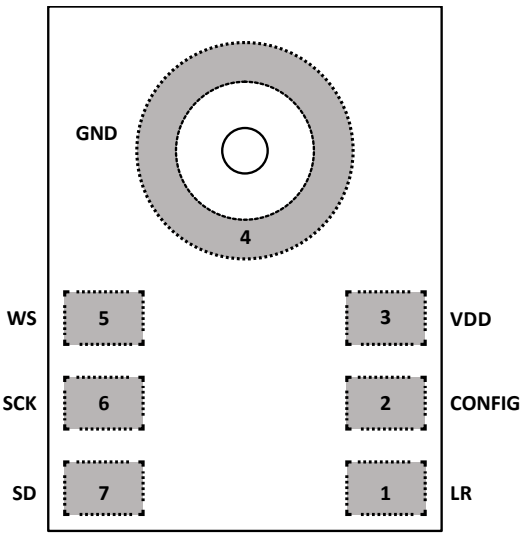


Figure 3. Pin Configuration (Top View, Terminal Side Down)

TABLE 6. PIN FUNCTION DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1	LR	Input	Left/Right channel select. When set low, the microphone outputs its signal in the left channel of the I²S frame. When set high, the microphone outputs its signal in the right channel.
2	CONFIG	Input	Pull to ground. The state of this pin is used at power-up.
3	VDD	Power	Power, 1.62 to 3.63 V. This pin should be decoupled to GND with a 0.1 µF capacitor.
4	GND	Ground	Ground. Connect to ground on the PCB.
5	WS	Input	Serial Data-Word Select for I²S Interface
6	SCK	Input	Serial Data Clock for I²S Interface
7	SD	Output	Serial Data Output for I²S Interface. This pin tri-states when not actively driving the appropriate output channel. The SD trace should have a 100 kΩ pulldown resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs.

Document Number: DS-000038
Revision: 1.0

TYPICAL PERFORMANCE CHARACTERISTICS

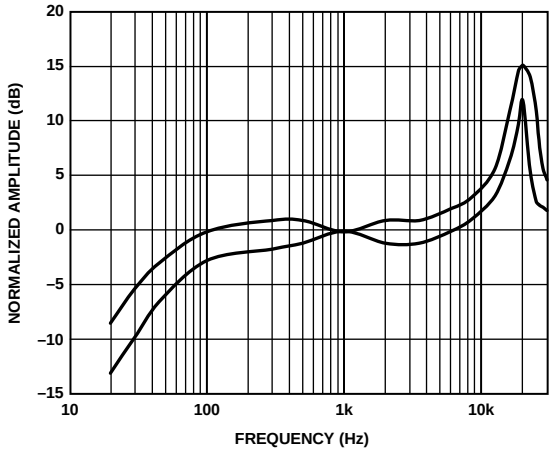


Figure 4. Frequency Response Mask

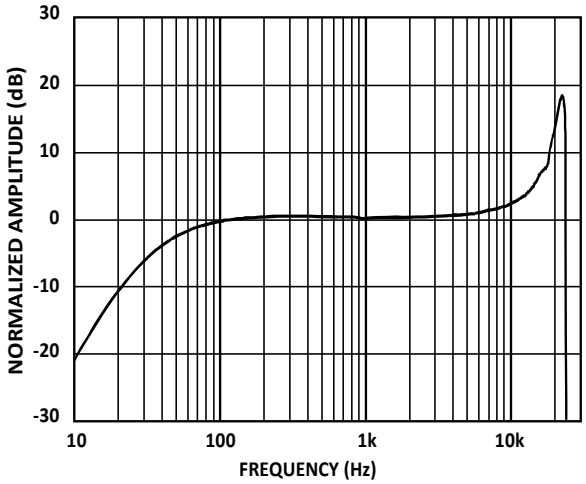


Figure 5. Typical Frequency Response (Measured)

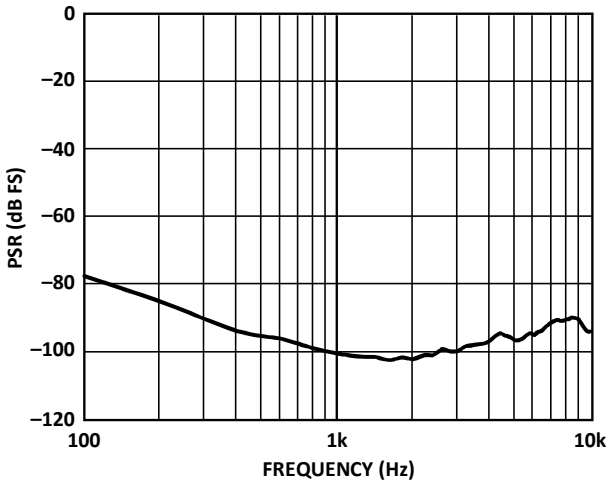


Figure 6. PSR vs. Frequency, 100 mV p-p Swept Sine Wave

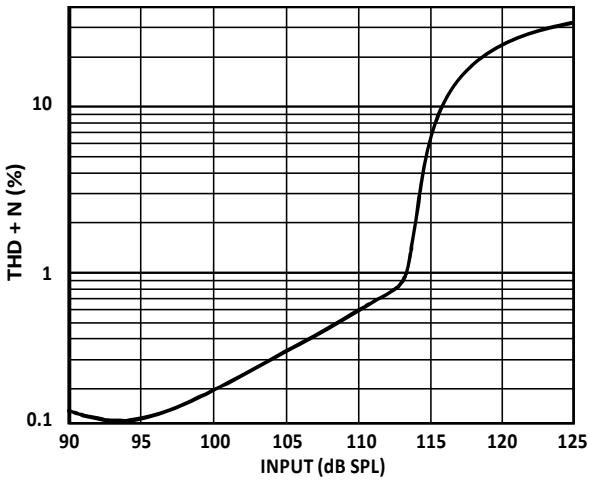


Figure 7. Total Harmonic Distortion + Noise (THD+N) vs. Input SPL

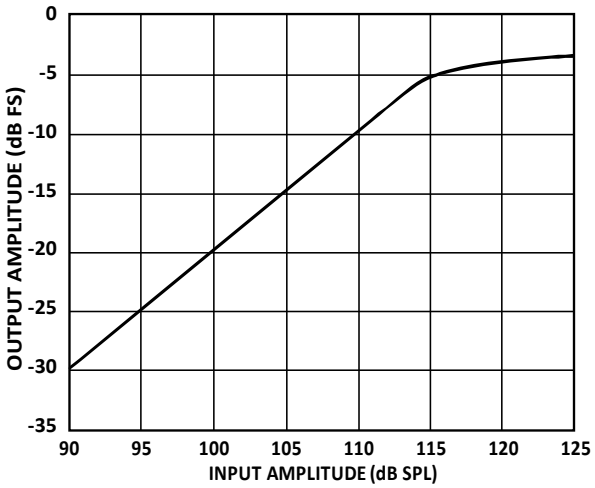


Figure 8. Linearity

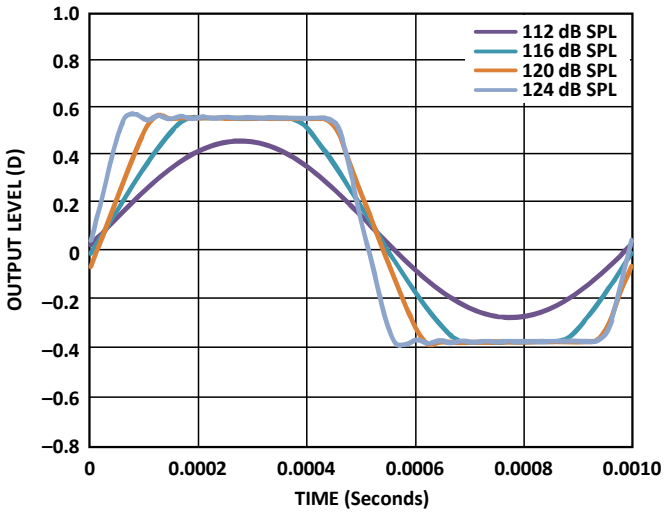


Figure 9. Clipping Characteristics

Document Number: DS-000038
Revision: 1.0

THEORY OF OPERATION

POWER MANAGEMENT

The ICS-43432 has two power states: normal operation, and standby mode.

Startup and Normal Operation

The ICS-43432 will begin to output non-zero data 4462 SCK clock cycles (1.5 ms with f_{SCK} = 3.072 MHz) after initial power-up. The part is in normal operation mode when SCK and WS are active.

Table 7 shows the startup time for different sampling rates.

Table 7. Startup time

f_S (WS frequency)	Startup time
48 kHz	1.5 ms
24 kHz	3.0 ms
16 kHz	4.5 ms
8 kHz	9.0 ms

Standby Mode

The microphone enters standby mode when the frequency of SCK falls below about 1 kHz. It is recommended to enter standby mode by stopping both the SCK and WS clock signals and pulling those signals to ground to avoid drawing current through the WS pin's internal pull-down resistor. The timing for exiting standby mode is the same as normal startup.

It is not recommended to supply active clocks (WS and SCK) to the ICS-43432 while there is no power supplied to VDD, doing this continuously turns on ESD protection diodes, which may affect long-term reliability of the microphone.

Soft Unmute

The ICS-43432 has a soft unmute feature to prevent pops on power-up. From the time that the ICS-43432 starts to output data, the volume will ramp up to the full-scale output level over 256 WS clock cycles. With a 48 kHz sampling rate, this unmute sequence will take about 5.3 ms.

SYNCHRONIZING MICROPHONES

Stereo ICS-43432 microphones are synchronized by the WS signal, so audio captured from two microphones sharing the same clock will be in sync. If the mics are enabled separately, this synchronization may take up to 0.35 ms after the enable signal is asserted while internal data paths are flushed.

I²S DATA INTERFACE

The slave serial data port's format is I²S, 24-bit, twos complement. There must be 64 SCK cycles in each WS stereo frame. The L/R control pin determines whether the ICS-43432 outputs data in the left or right channel. When set to the left channel, the data will be output following WS's falling edge and when set to output on the right channel, data will be output following WS's rising edge.

For a stereo application, the SD pins of the left and right ICS-43432 microphones should be tied together as shown in Figure 10. The format of a stereo I²S data stream is shown in Figure 11. Figure 12 and Figure 13 show the formats of a mono microphone data stream for left and right microphones, respectively.

Data Output Mode

The output data pin (SD) is tri-stated when it is not actively driving I²S output data. SD immediately tristates after the LSB is output so that another microphone can drive the common data line.

Document Number: DS-000038
Revision: 1.0

The SD trace should have a pulldown resistor to discharge the line during the time that all microphones on the bus have tri-stated their outputs. A 100 kΩ resistor is sufficient for this, as shown in Figure 10. If the SD line needs to be discharged faster than a 100 kΩ resistor can, a smaller resistor, such as 10 kΩ, can be used.

Data Word Length

The output data word length is 24 bits per channel.

Data Word Format

The default data format is I²S (twos complement), MSB-first. In this format, the MSB of each word is delayed by one SCK cycle from the start of each half-frame.

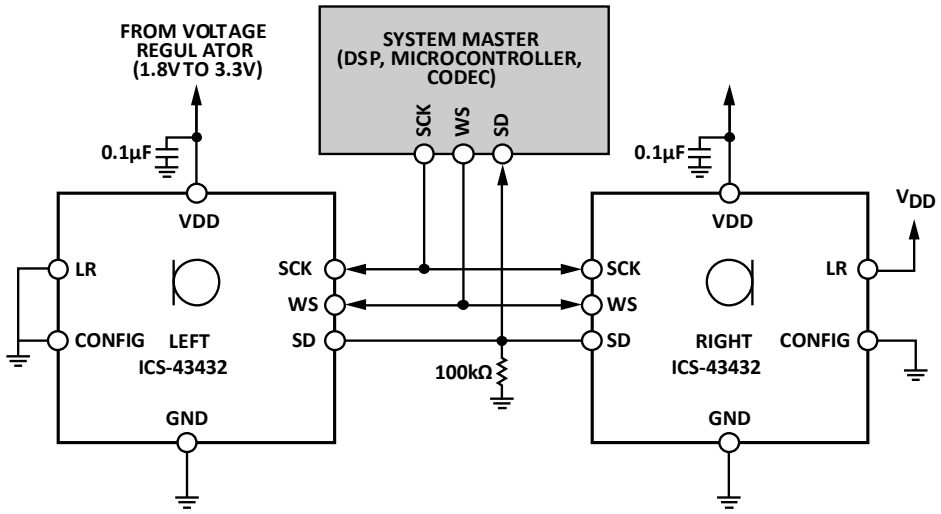


Figure 10. System Block Diagram

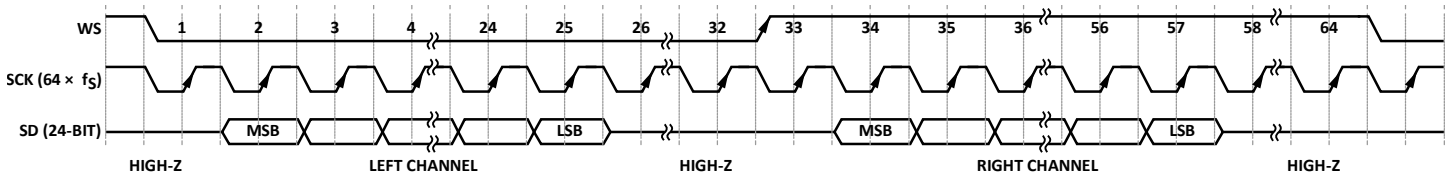


Figure 11. Stereo Output I²S Format

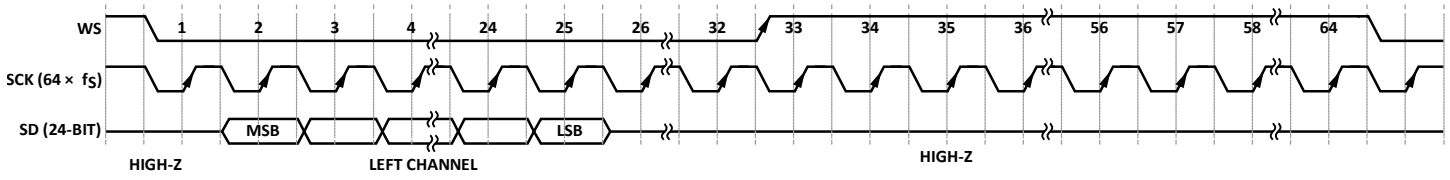


Figure 12. Mono Output I²S Format Left Channel (LR = 0)

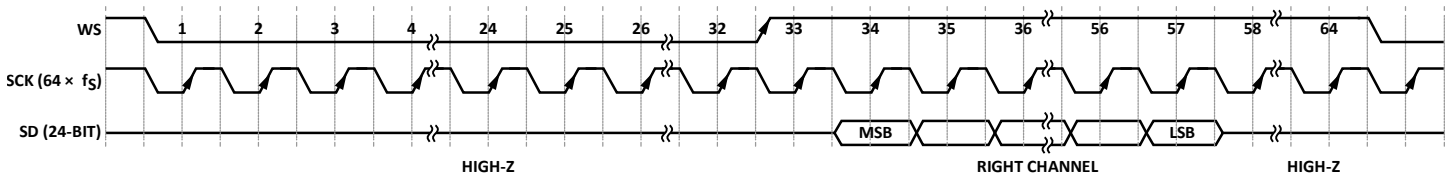


Figure 13. Mono Output I²S Format Right Channel (LR = 1)

Document Number: DS-000038
Revision: 1.0

Data Output Format

The output data word length is 24 bits/channel. The data word format is 2's complement, MSB first.

The output data pin (SD) is tri-stated when it is not actively driving output data. SD will immediately tri-state after the LSB is output so that another microphone can drive the common data line.

DIGITAL MICROPHONE SENSITIVITY

The sensitivity of a digital output microphone is specified in units of dB FS (decibels relative to a full-scale digital output). A 0 dB FS sine wave is defined as a signal whose peak just touches the full-scale code of the digital word (see Figure 5). This measurement convention means that signals with a different crest factor may have an RMS level higher than 0 dB FS. For example, a full-scale square wave has an RMS level of 3 dB FS.

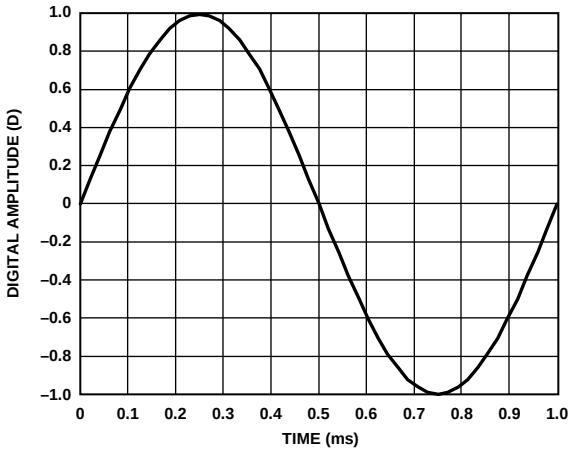


Figure 11. 1 kHz, 0 dB FS Sine Wave

The definition of a 0 dB FS signal must be understood when measuring the sensitivity of the ICS-43432. An acoustic input signal of a 1 kHz sine wave at 94 dB SPL applied to the ICS-43432 results in an output signal with a −26 dB FS level. This means that the output digital word peaks at −26 dB below the digital full-scale level. A common misunderstanding is that the output has an RMS level of −29 dB FS; however, this is not the case because of the definition of a 0 dB FS sine wave.

There is no commonly accepted unit of measurement to express the instantaneous level of a digital signal output from the microphone, as opposed to the RMS level of the signal. Some measurement systems express the instantaneous level of an individual sample in units of D, where 1.0 D is digital full scale (see Figure 11). In this case, a −26 dB FS sine wave has peaks at 0.05 D.

For more information about digital microphone sensitivity, see the AN-1112 Application Note, *Microphone Specifications Explained*.

DIGITAL FILTER CHARACTERISTICS

The ICS-43432 has an internal digital bandpass filter. A high-pass filter eliminates unwanted low frequency signals. A low-pass decimation filter scales the pass band with the sampling frequency and performs required out-of-band noise reduction.

High-Pass Filter

The ICS-43432 incorporates a high-pass filter to remove unwanted dc and very low frequency components. With f_S = 48 kHz, this high pass filter has a −3 dB corner frequency of 3.7 Hz. The cutoff frequency scales with changes in sampling rate.

This digital filter response is in addition to the acoustic high-pass response of the ICS-43432 that has a −3 dB corner of 50 Hz.

Document Number: DS-000038
Revision: 1.0

Low-Pass Decimation Filter

The analog-to-digital converter in the ICS-43432 is a single-bit, high order, sigma-delta (Σ-Δ) running at a high oversampling ratio. The noise shaping of the converter pushes the majority of the noise well above the audio band and gives the microphone a wide dynamic range. However, it does require a good quality low-pass decimation filter to eliminate the high frequency noise.

The pass band of the filter extends to $0.417 \times f_S$ and, in that band, has only 0.04 dB of ripple. The high frequency cutoff of −3 dB occurs at $0.5 \times f_S$. A 48 kHz sampling rate results in a pass band of 20.3 kHz and a half amplitude corner at 24 kHz; the stop-band attenuation of the filter is 58 dB. Note that these filter specifications scale with sampling frequency.

Document Number: DS-000038
Revision: 1.0

APPLICATIONS INFORMATION

SD OUTPUT DRIVE STRENGTH

The SD data output pin must drive a load that includes the PCB trace and the tri-stated inputs of the other ICS-43432 SD pins connected to that same trace. The tri-stated load capacitance of the ICS-43432 SD pin is about 6 pF. The ICS-43432 has been designed to drive a load of 150 pF.

POWER SUPPLY DECOUPLING

For best performance and to avoid potential parasitic artifacts, placing a 0.1 µF ceramic type X7R or better capacitor between Pin 3 (VDD) and ground is strongly recommended. The capacitor should be placed as close to Pin 3 as possible.

The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the ground planes should be made on the far side of the capacitor, as shown in Figure 14.

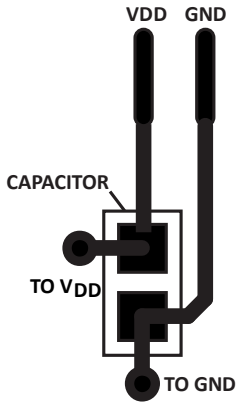


Figure 14. Recommended Power Supply Bypass Capacitor Layout

Document Number: DS-000038
Revision: 1.0

SUPPORTING DOCUMENTS

For additional information, see the following documents.

EVALUATION BOARD USER GUIDE

UG-303, *Bottom-Port I²S Output MEMS Microphone Evaluation Board*

APPLICATION NOTES

AN-100, *MEMS Microphone Handling and Assembly Guide*
AN-1003, *Recommendations for Mounting and Connecting the InvenSense Bottom-Ported MEMS Microphones*
AN-1112, *Microphone Specifications Explained*
AN-1124, *Recommendations for Sealing InvenSense Bottom-Port MEMS Microphones from Dust and Liquid Ingress*
AN-1140, *Microphone Array Beamforming*

Document Number: DS-000038
Revision: 1.0

PCB DESIGN AND LAND PATTERN LAYOUT

The recommended PCB land pattern for the ICS-43432 should be laid out to a 1:1 ratio to the solder pads on the microphone package, as shown in Figure 15. Take care to avoid applying solder paste to the sound hole in the PCB. A suggested solder paste stencil pattern layout is shown in Figure 16. The diameter of the sound hole in the PCB should be larger than the diameter of the sound port of the microphone. A minimum diameter of 0.5 mm is recommended.

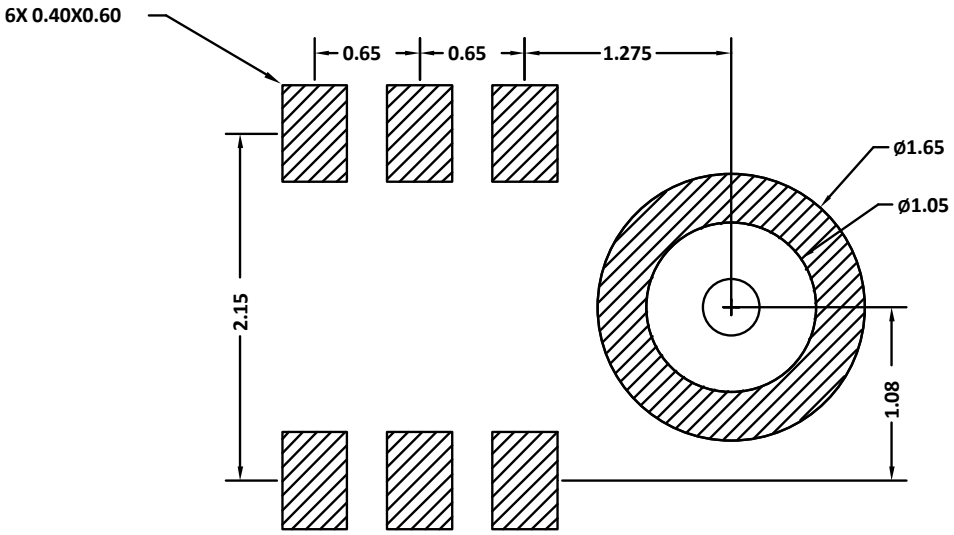


Figure 15. PCB Land Pattern Layout

Dimensions shown in millimeters

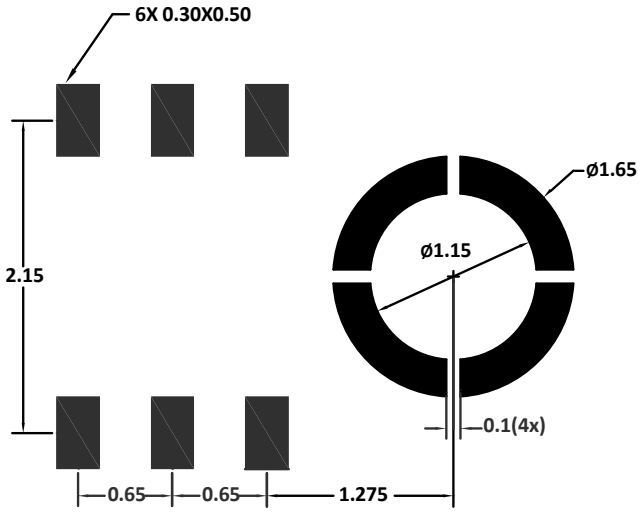


Figure 16. Suggested Solder Paste Stencil Pattern Layout

Dimensions shown in millimeters

PCB MATERIAL AND THICKNESS

The performance of the ICS-43432 is not affected by PCB thickness. The ICS-43432 can be mounted on either a rigid or flexible PCB. A flexible PCB with the microphone can be attached directly to the device housing with an adhesive layer. This mounting method offers a reliable seal around the sound port while providing the shortest acoustic path for good sound quality.

Document Number: DS-000038
Revision: 1.0

HANDLING INSTRUCTIONS

PICK AND PLACE EQUIPMENT

The MEMS microphone can be handled using standard pick-and-place and chip shooting equipment. Take care to avoid damage to the MEMS microphone structure as follows:

- Use a standard pickup tool to handle the microphone. Because the microphone hole is on the bottom of the package, the pickup tool can make contact with any part of the lid surface.
- Do not pick up the microphone with a vacuum tool that makes contact with the bottom side of the microphone. Do not pull air out of or blow air into the microphone port.
- Do not use excessive force to place the microphone on the PCB.

REFLOW SOLDER

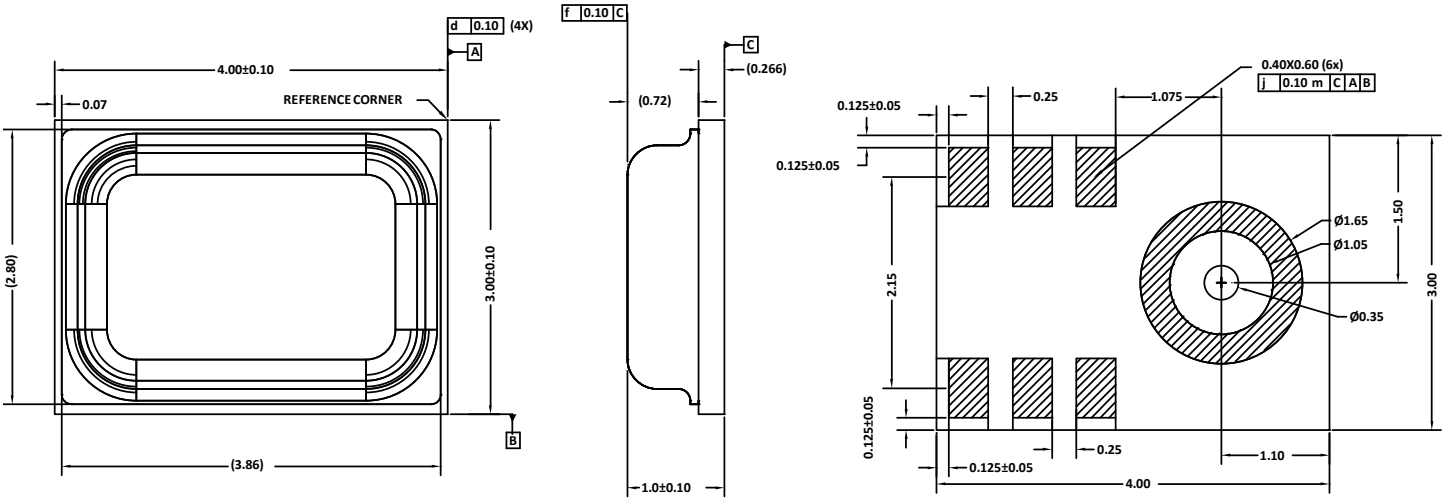
For best results, the soldering profile must be in accordance with the recommendations of the manufacturer of the solder paste used to attach the MEMS microphone to the PCB. It is recommended that the solder reflow profile not exceed the limit conditions specified in Figure 2 and Table 5.

BOARD WASH

When washing the PCB, ensure that water does not make contact with the microphone port. Do not use blow-off procedures or ultrasonic cleaning.

Document Number: DS-000038
Revision: 1.0

OUTLINE DIMENSIONS



TOP VIEW SIDE VIEW BOTTOM VIEW

Figure 17. 7-Terminal Chip Array Small Outline No Lead Cavity
4.00 × 3.00 × 1.00 mm Body
Dimensions shown in millimeters

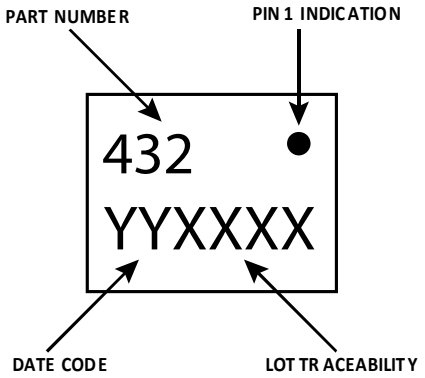


Figure 18. Package Marking Specification (Top View)

ORDERING GUIDE

PART	TEMP RANGE	PACKAGE	QUANTITY	PACKAGING
ICS-43432	–40°C to +85°C	7-Terminal LGA_CAV	4,500	13” Tape and Reel
EV_ICS-43432-FX		Flex Evaluation Board		

Document Number: DS-000038
Revision: 1.0

REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
12/10/2014	1.0	Initial Release

COMPLIANCE DECLARATION DISCLAIMER

InvenSense believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. InvenSense subcontracts manufacturing, and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

InvenSense