High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Relative to GND .....-0.5V to +6.0V
Voltage Range on V+ Relative to GND .....-0.5V to +17V
Voltage Range on SDA, SCL, A0, A1
Relative to GND.....-0.5V to (V_{CC} + 0.5V), not to exceed 6.0V
Voltage Range on RH, RL, RW.....-0.5V to V+
Voltage Range Across RH and RL Pins .....-0.5V to V+

Operating Temperature Range .....-40°C to +100°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020 Specification
Maximum RW Current 1mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +100°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
V+ Voltage	V+	V+ > V_{CC}	+4.5		+15.5	V
Input Logic 1 (SCL, SDA, A0, A1)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, A1)	V_{IL}		-0.3		0.3 x V_{CC}	V
Resistor Inputs (RL, RW, RH)	V_{RES}		-0.3		V+ + 0.3	V
Wiper Current	I_{WIPER}				1	mA

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Current	I_{CC}	(Note 2)		2		mA
	I_{CC2}	(Note 3)		250	350	µA
Standby Supply Current	I_{STBY}	(Note 4)		40	60	µA
V+ Bias Current	I_{V+}				+1	µA
Input Leakage (SDA, SCL, A0, A1)	I_L		-1		+1	µA
Low-Level Output Voltage (SDA)	V_{OL}	3mA sink current	0.0		0.4	V
I/O Capacitance	$C_{I/O}$			5	10	pF
Power-Up Recall Voltage	V_{POR}	(Note 5)	1.6		2.6	V
Power-Up Memory Recall Delay	t_D	(Note 6)			5	ms
Wiper Resistance	R_W	V+ = 15.0V			5000	Ω
End-to-End Resistance (RH to RL)	R_{TOTAL}			10		kΩ
R_{TOTAL} Tolerance		T_A = +25°C	-20		+20	%
R_{TOTAL} Temp Co.		(Note 7)		±200		ppm
CH, CL, CW Capacitance	C_{POT}			10		pF

TEMPERATURE SENSOR CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Error					±5	°C
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Resolution	LSB	Full-scale voltage of 6.5536V		25.6		mV
Input/Supply Accuracy	A_{CC}	At factory setting		0.25	1	% FS (Full Scale)
Input Supply Offset	V_{OS}	(Note 7)		0	5	LSB
Update Rate (Temperature and Supply Conversion Time)	t_{FRAME}			16		ms

VOLTAGE-DIVIDER CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Integral Nonlinearity	INL	(Note 8)	-1		+1	LSB
Differential Nonlinearity	DNL	(Note 9)	-0.5		+0.5	LSB
Zero-Scale Error	ZS_{ERROR}	V+ = 4.5V (Note 10)	0	0.5	2	LSB
Full-Scale Error	FS_{ERROR}	V+ = 4.5V (Note 11)	-2	-0.003	0	LSB
Ratiometric Temp Coefficient	TCV	WR set to 40h		±4		ppm/°C

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 3.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

I²C AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +100°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$. See Figure 3.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 13)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 13)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 13)			400	pF
EEPROM Write Time	t_W	(Note 14)		10	20	ms
Pulse-Width Suppression Time at SDA and SCL Inputs	t_{IN}	(Note 15)		50		ns
A0, A1 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0, A1 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
SDA and SCL Input Buffer Hysteresis				0.05 x V_{CC}		V

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C	50,000			Writes
		T_A = +25°C	200,000			

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.

Note 2: I_{CC} is specified with the following conditions: SCL = 400kHz; SDA pulled up; and RL, RW, RH floating.

Note 3: I_{CC} is specified with the following conditions: SCL, SDA pulled up; RL, RW, RH floating; and temperature sensor on.

Note 4: I_{STBY} is specified with SDA = SCL = V_{CC} = 5.5V, resistor pins floating, and CR2 bit 0 = logic-high.

Note 5: This is the minimum V_{CC} voltage that causes NV memory to be recalled.

Note 6: This is the time from $V_{CC} > V_{POR}$ until initial memory recall is complete.

Note 7: Guaranteed by design.

Note 8: Integral nonlinearity is the deviation of a measured resistor setting value from the expected values at each particular resistor setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting. INL = $[V(RW)_i - (V(RW)_0]$ / LSB(ideal) - i, for i = 0...127.

Note 9: Differential nonlinearity is the deviation of the step-size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position. DNL = $[V(RW)_{i+1} - (V(RW)_i]$ / LSB(ideal) - 1, for i = 0...126.

Note 10: ZS error = code 0 wiper voltage divided by one LSB(ideal).

Note 11: FS error = (code 127 wiper voltage - V+) divided by one LSB (ideal).

Note 12: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard mode timing.

Note 13: CB—total capacitance of one bus line in picofarads.

Note 14: EEPROM write time begins after a STOP condition occurs.

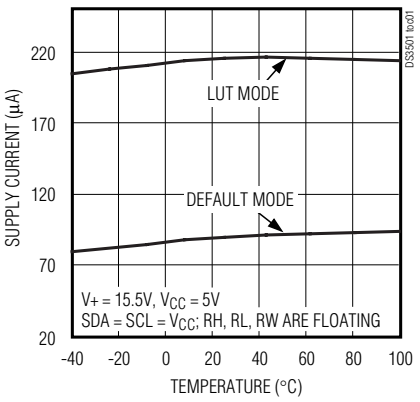
Note 15: Pulses narrower than max are suppressed.

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

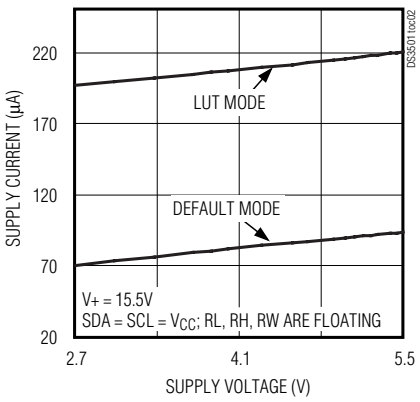
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

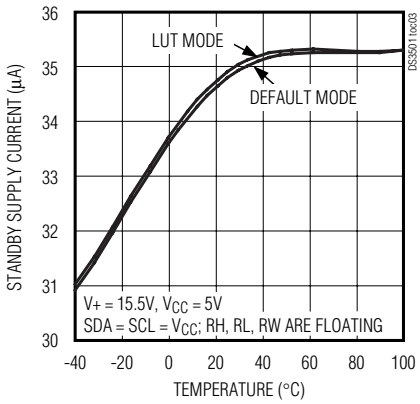
SUPPLY CURRENT vs. TEMPERATURE



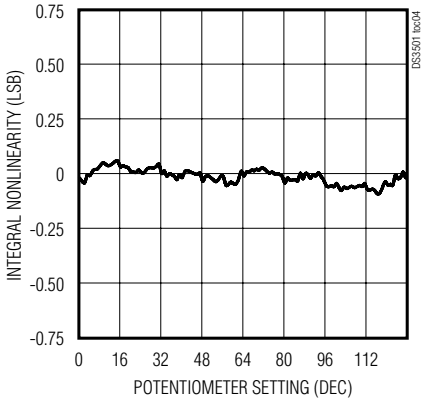
SUPPLY CURRENT vs. SUPPLY VOLTAGE



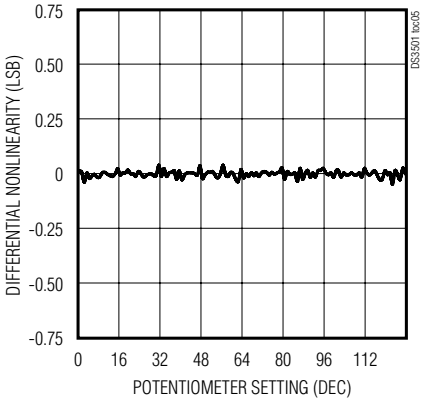
STANDBY SUPPLY CURRENT vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. POTENTIOMETER SETTING



DIFFERENTIAL NONLINEARITY vs. POTENTIOMETER SETTING

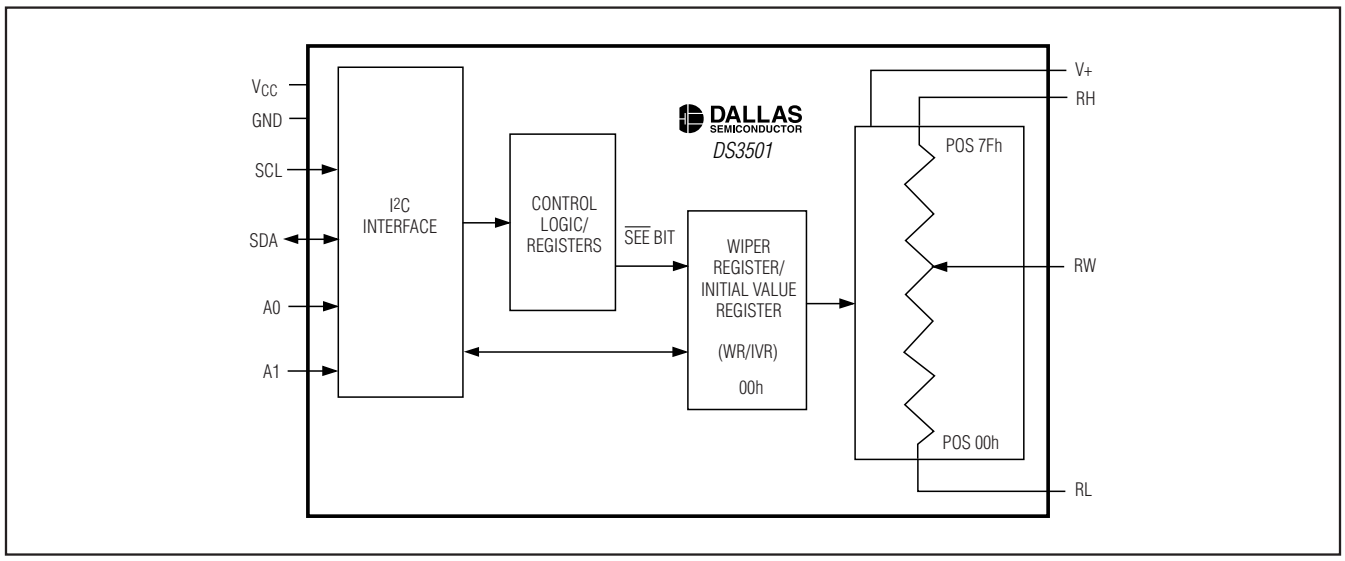


Pin Description

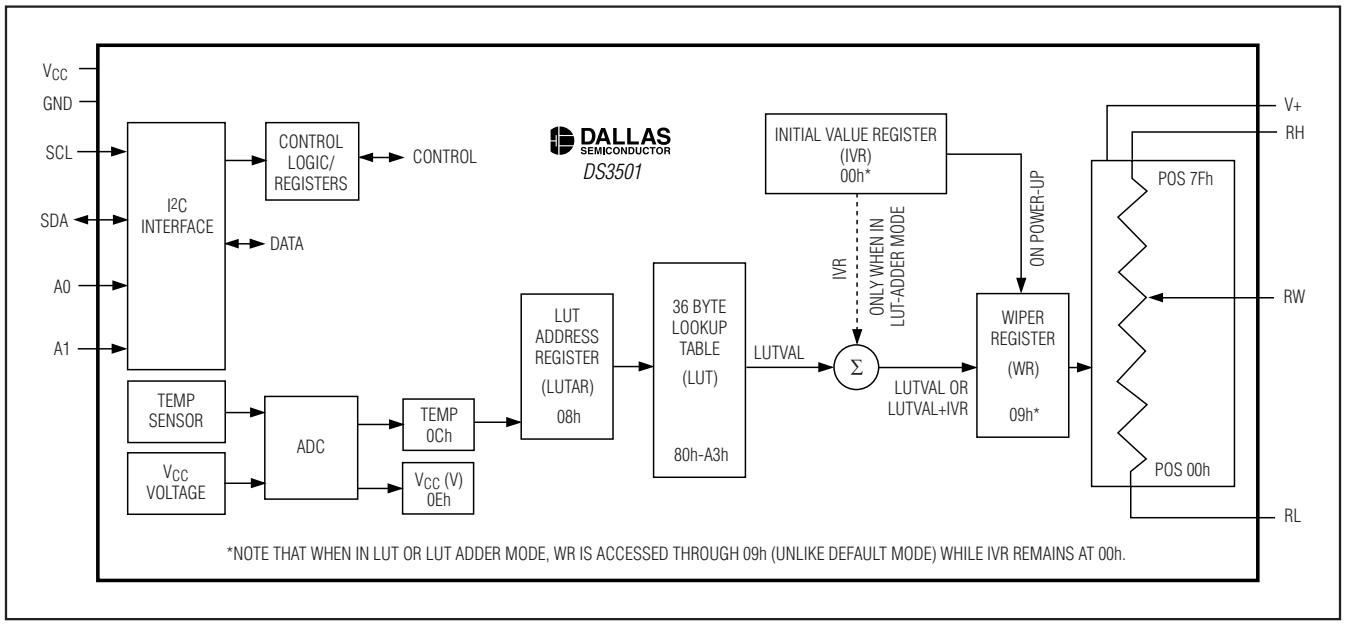
NAME	PIN	DESCRIPTION
SDA	1	I²C Serial Data. Input/output for I²C data.
GND	2	Ground Terminal
V_{CC}	3	Supply Voltage Terminal
A1, A0	4, 5	Address Select Inputs. Determines I²C slave address. Slave address is 01010A_1A_0X. (See the *Slave Address Byte and Address Pins* section for details).
RH	6	High Terminal of Potentiometer
RW	7	Wiper Terminal of Potentiometer
RL	8	Low Terminal of Potentiometer
V+	9	Wiper Bias Voltage
SCL	10	I²C Serial Clock. Input for I²C clock.

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

Block Diagrams



Default Mode Block Diagram (Update Mode bit = 0)



LUT and LUT Adder Mode Block Diagram (Update Mode bit = 1)

Detailed Description

The DS3501 operates in one of three operating modes: Default Mode, LUT Mode, or LUT Adder Mode. In Default Mode, the DS3501 is pin and software compatible with the ISL95311. The potentiometer's wiper position is controlled by the Wiper Register (WR) and the NV Initial Value Register (IVR) via the I²C interface. In LUT Mode and LUT Adder Mode, the potentiometer's wiper position is calculated/controlled as a function of the current temperature measured by the DS3501's internal temperature sensor. The difference between the two LUT modes is the way the potentiometer wiper position is calculated. A detailed description of the three modes as well as additional features of the DS3501 follow below.

Digital Potentiometer Output

The potentiometer consists of 127 resistors in series connected between the RH and RL pins. Between each resistance and at the two end points, RH and RL, solid-state switches enable RW to be connected within the resistive network. The wiper position and the output on RW are decoded based on the value in WR. If RH, RL, and RW are externally connected in a voltage-divider configuration, then the voltage on RW can be easily calculated using the following equation:

$$V_{RW} = V_{RL} + \frac{WR}{127}(V_{RH} - V_{RL})$$

where WR is the wiper position in decimal (0–127).

Temperature Conversion and Supply Voltage Monitoring

Temperature Conversion

The DS3501 features an internal 8-bit temperature sensor that is capable of driving the LUT and providing a measurement of the ambient temperature over I²C by reading address 0Ch. The sensor is functional over the entire operating temperature range and is in signed two's complement format with a resolution of 1°C/bit. See below for the temperature sensor's bit weights.

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

To calculate the temperature, treat the two's complement binary value as an unsigned binary number, then convert it to decimal. If the result is greater than or equal to 128, subtract 256 from the result.

Supply Voltage Monitoring

The DS3501 also features an internal 8-bit supply voltage (V_{CC}) monitor. A value of the supply voltage measurement can be read over I²C at the address 0Eh.

To calculate the supply voltage, simply convert the hexadecimal result into decimal and then multiply it by the LSB as shown in the *Analog Voltage Monitoring Characteristics* electrical table.

Mode Selection

The DS3501 mode of operation is determined by two bits located in Control Register 1 (CR1), which is non-volatile. In particular, the mode is determined by the Update Mode bit (CR1.0) and the Adder Mode bit (CR1.1). Table 1 illustrates how the two control bits are used to select the operating mode. When shipped from the factory, the DS3501 is programmed with the CR1.0 bit = 0, hence configuring the DS3501 in Default Mode.

Table 1. DS3501 Operating Modes

UPDATE MODE BIT (CR1.0)	ADDER MODE BIT (CR1.1)	MODE
0	X	Default Mode (default)
1	0	LUT Mode
1	1	LUT Adder Mode

Default Mode

Default Mode of the DS3501 is the simplest mode of the three. As shown in the Default Mode Block Diagram, the potentiometer is controlled by the Wiper Register/Initial Value Register (WR/IVR). Upon power-up of the DS3501, the value stored in the NV Initial Value Register (IVR) is recalled into the volatile Wiper Register (WR). The wiper can then be changed any time after by writing the desired value to the WR/IVR Register. The WR/IVR Register is located at memory address 00h and is implemented as EEPROM shadowed SRAM. This register can be visualized as an SRAM byte (the WR portion) in parallel with a EEPROM byte (the IVR portion). The operation of the register is controlled by the Shadow EEPROM ($\overline{SEE}$) bit, CR0.7. When the $\overline{SEE}$ bit = 0 (default), data written to memory address 00h by I²C actually gets stored in both SRAM (WR) and EEPROM (IVR). Conversely, when $\overline{SEE}$ = 1, only the SRAM (WR) is written to the new value. The EEPROM byte (IVR) continues to store the last value written to it when $\overline{SEE}$ was 0. Reading memory address 00h reads the value stored in WR. As shown in the Default Mode memory map (see Table 2), the $\overline{SEE}$ bit is volatile and its power-up default state is 0.

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

Table 2. Default Mode Memory Map

REGISTER	NAME	ADDRESS (HEX)	VOLATILE/NONVOLATILE	FACTORY/POWER-UP DEFAULT
WR/IVR	Wiper Register/Initial Value	00h*	NV (Shadowed)	40h
CR0	Control Register 0	02h	V	00h
CR1	Control Register 1	03h	NV (Shadowed)	00h
CR2	Control Register 2	0Ah	V	00h

**In Default Mode, both WR and IVR are accessed through memory location 00h. Refer to the Default Mode section for additional information.*

Table 3. LUT Mode and LUT Adder Mode Memory Map

REGISTER	NAME	ADDRESS (HEX)	VOLATILE/NONVOLATILE	FACTORY/POWER-UP DEFAULT
IVR	Initial Value Register	00h*	NV (Shadowed)	40h
CR0	Control Register 0	02h	V	00h
CR1	Control Register 1	03h	NV (Shadowed)	00h
LUTAR	LUT Address Register	08h	V	N/A
WR	Wiper Register	09h*	V	N/A
CR2	Control Register 2	0Ah	V	00h
TEMP	Temperature Value	0Ch	V (Read-Only)	N/A
VCC	V_{CC} Voltage Value	0Eh	V (Read-Only)	N/A
LUT0	Wiper Value for T ≤ -37°C	80h	NV	00h
LUT1	Wiper Value for -36°C to -33°C	81h	NV	00h
LUT2	Wiper Value for -32°C to -29°C	82h	NV	00h
—	—	—	—	—
LUT33	Wiper Value for +92°C to +95°C	A1h	NV	00h
LUT34	Wiper Value for +96°C to +99°C	A2h	NV	00h
LUT35	Wiper Value for T ≥ 100°C	A3h	NV	00h

**In LUT Mode and LUT Adder Mode, the WR is accessed through memory address 09h, while IVR remains at memory address 00h.*

LUT Mode

LUT Mode is selected by setting the Update Mode bit (CR1.0) to 1 and the Adder Mode bit (CR1.1) to 0. An overview of the DS3501 in this mode is illustrated in the LUT Mode and LUT Adder Mode Block Diagram. Also, the memory map for LUT Mode and LUT Adder Mode is shown in Table 3. The major difference between the two LUT modes is whether or not the value in the IVR is added to the values stored in the lookup table. The dashed line/arrow shown in the block diagram is not active in LUT mode.

When in LUT Mode, on power-up the IVR value is recalled into the WR register. This value will remain there until completion of the first temperature conversion following power-up. The temperature is measured every t_{FRAME}. The temperature value is used to calculate an index that points to the corresponding value in the lookup table. This index is referred to as the LUT Address Register (LUTAR). The value stored in the LUT at the location pointed to by LUTAR is called LUTVAL. The Wiper Register is then automatically loaded with LUTVAL. The process then repeats itself, continuously updating the wiper setting in a closed-loop fashion.

In this mode the 36-byte LUT is populated with wiper settings for each four-degree temperature window. Valid wiper settings are 00h to 7Fh. The memory map in Table 3 shows the memory address of the LUT as well as the corresponding temperature range for each byte in the LUT. Also, the LUT features one-degree hysteresis to prevent chattering if the measured temperature

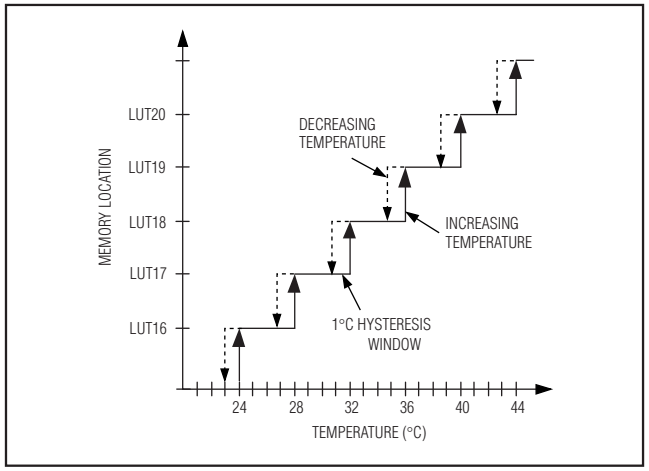


Figure 1. LUT Hysteresis

falls on the boundary between two windows. As the temperature increases, the LUT changes on even temperature values (see Figure 1). Conversely, the LUT changes on odd temperature values when the temperature is decreasing.

LUT Adder Mode

LUT Adder Mode is selected by setting the Update Mode bit (CR1.0) to 1 and the Adder Mode bit (CR1.1) to 1. This mode operates similar to LUT Mode with one major difference (see the LUT Mode and LUT Adder Mode Block Diagram). The Wiper Register is loaded with the **sum** of LUTVAL and IVR. Furthermore, in this mode, the values programmed into the LUT are signed two's complement. This allows convenient positive or negative offsetting of the nominal IVR value.

DS3501 Control Registers

The DS3501 contains three control registers (CR0, CR1, and CR2) used to configure and control modes and features.

Control Register 0 (CR0)

POWER-UP DEFAULT 00h

MEMORY TYPE Volatile

02h	$\overline{\text{SEE}}$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	bit7							bit0

bit7	**$\overline{\text{SEE}}$:** Controls functionality of shadowed NV registers (such as the WR/IVR register). 0 = Data written to shadowed NV memory is stored in both SRAM and EEPROM (default). 1 = Data written to shadowed NV memory is stored only in SRAM.
bit6:0	Reserved

Control Register 1 (CR1)

FACTORY DEFAULT 00h

MEMORY TYPE Shadowed Nonvolatile

03h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**Adder Mode**	**Update Mode**
	bit7							bit0

bit7:2	Reserved
bit1	**Adder Mode:** *This bit is valid only if the Update Mode bit = 1.* 0 = Sets the DS3501 to LUT Mode. 1 = Sets the DS3501 to LUT Adder Mode.
bit0	**Update Mode:** 0 = Sets the DS3501 to Default Mode. In this mode the DS3501 is compatible with the ISL95311 (default). 1 = Sets the DS3501 to one of the two LUT-based modes depending on the Adder Mode bit.

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

Control Register 2 (CR2)

POWER-UP DEFAULT 00h

MEMORY TYPE Volatile

	bit7							bit0
0Ah	Reserved	Reserved	Reserved	Reserved	Reserved	$\overline{\text{TEN}}$	$\overline{\text{AEN}}$	Standby

bit7:3	Reserved
bit2	**$\overline{\text{TEN}}$:** Temperature Update Enable bar. *This bit is valid only in LUT Mode and LUT Adder Mode.* 0 = Normal LUT operation. The WR is automatically loaded with LUTVAL+IVR or LUTVAL following each temperature conversion. 1 = Places the potentiometer in manual mode allowing WR (09h) to be written using I²C.
bit1	**$\overline{\text{AEN}}$:** Address Update Enable bar. *This bit is valid only in LUT Mode and LUT Adder Mode.* 0 = Normal LUT operation. LUTAR (08h) is calculated following each temperature conversion that points to the corresponding location in the LUT. 1 = Disables automatic updates of LUTAR. This allow the user to directly write to the LUTAR register in order to exercise LUT values and functionality.
bit0	**Standby:** 0 = Normal operating mode. 1 = Standby Mode. Places the DS3501 in a low-power consumption state specified by I_{STBY}. The I²C interface is still active in this state.

Standby Mode and I_{CC}

The DS3501 has three specified levels of supply current. Active current during I²C communications while in the LUT-driven mode is specified as I_{CC}, and is the "worst-case" supply current. Active current without I²C communications while in the LUT driven mode is specified as the supply current: I_{CC2}. SDA and SCL are held statically in the high-logic level while the DS3501 continues to function in LUT-driven mode. The third level is specified as standby mode, I_{STBY}. This is the lowest possible current consumption mode.

Standby mode is enabled with CR2.0 = 1. All internal operations are halted including internal temperature sensor results. Consequently, WR's position will not change, and will remain in the last state that was loaded into WR. I²C will, however, continue to function, and once CR2.0 = 0, the DS3501 will resume normal operation after the first temperature conversion cycle is complete (t_{FRAME}).

Slave Address Byte and Address Pins

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 2). The DS3501's slave address is determined by the state of the A0 and A1 address pins. These pins allow up to four devices to reside on the same I²C bus. Address pins tied to GND result in a 0 in the corresponding bit position in the slave address. Conversely, address pins tied to V_{CC} result in a 1 in the corresponding bit positions. For example, the DS3501's slave address byte is 50h when A0 and A1 pins are grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

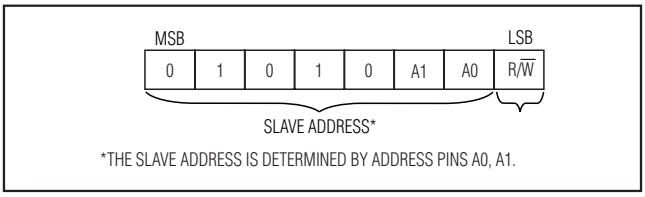


Figure 2. DS3501 Slave Address Byte

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 3 and *I²C AC Electrical Characteristics* table for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

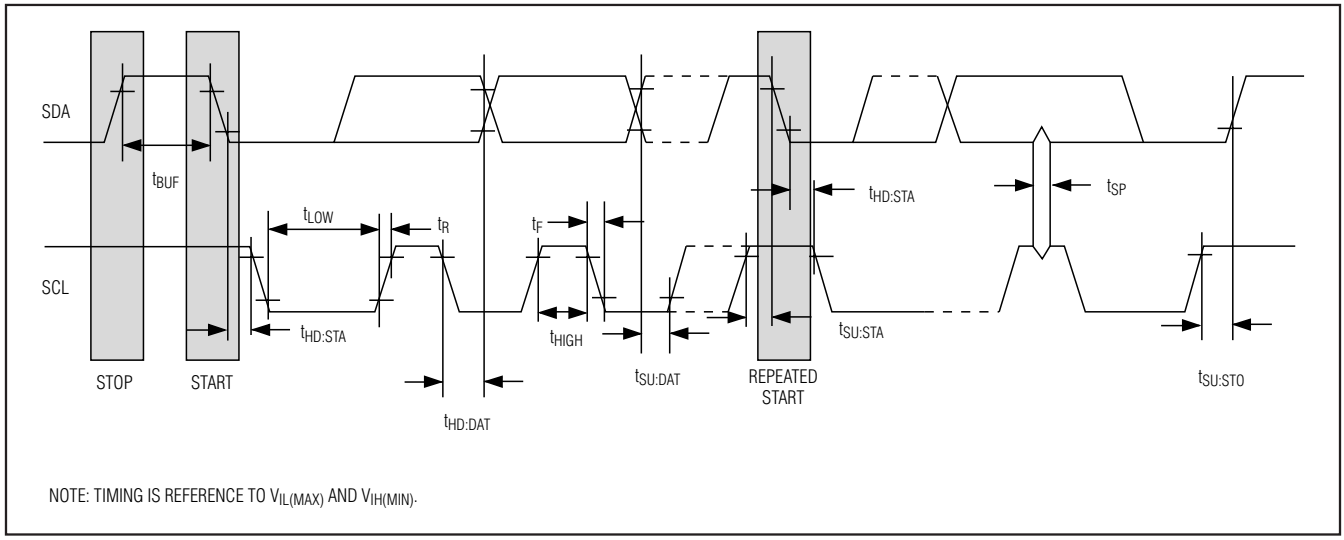


Figure 3. I²C Timing Diagram

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to ter-

minate communication so the slave will return control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The slave address byte of the DS3501 is shown in Figure 2.

When the R/$\overline{W}$ bit is 0 (such as in 50h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (51h in this case), the master is indicating it wants to read from the slave.

If an incorrect slave address is written, the DS3501 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

When writing to the DS3501, the potentiometer will adjust to the new setting once it has acknowledged the new data that is being written, and the EEPROM (if $\overline{SEE}$ = 0) will be written following the STOP condition at the end of the write command. To change the setting without changing the EEPROM, terminate the write with a repeated START condition before the next STOP condition occurs. Using a repeated START condition prevents the t_W delay required for the EEPROM write cycle to finish.

Writing multiple bytes to a slave: To write multiple bytes to a slave in one transaction, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS3501 is capable of writing 1 to 8 bytes (1 page or row) in a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). The first page begins at address 00h and subsequent pages begin at multiples of 8 (08h, 10h, 18h, etc). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time a EEPROM byte is written, the DS3501 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3501, which allows communication to continue as soon as the DS3501 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

EEPROM write cycles: The DS3501's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot) as well as at room temperature. Writing to shadowed EEPROM with $\overline{SEE}$ = 1 does not count as a EEPROM write.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

See Figure 4 for a read example using the repeated START condition to specify the starting memory location.

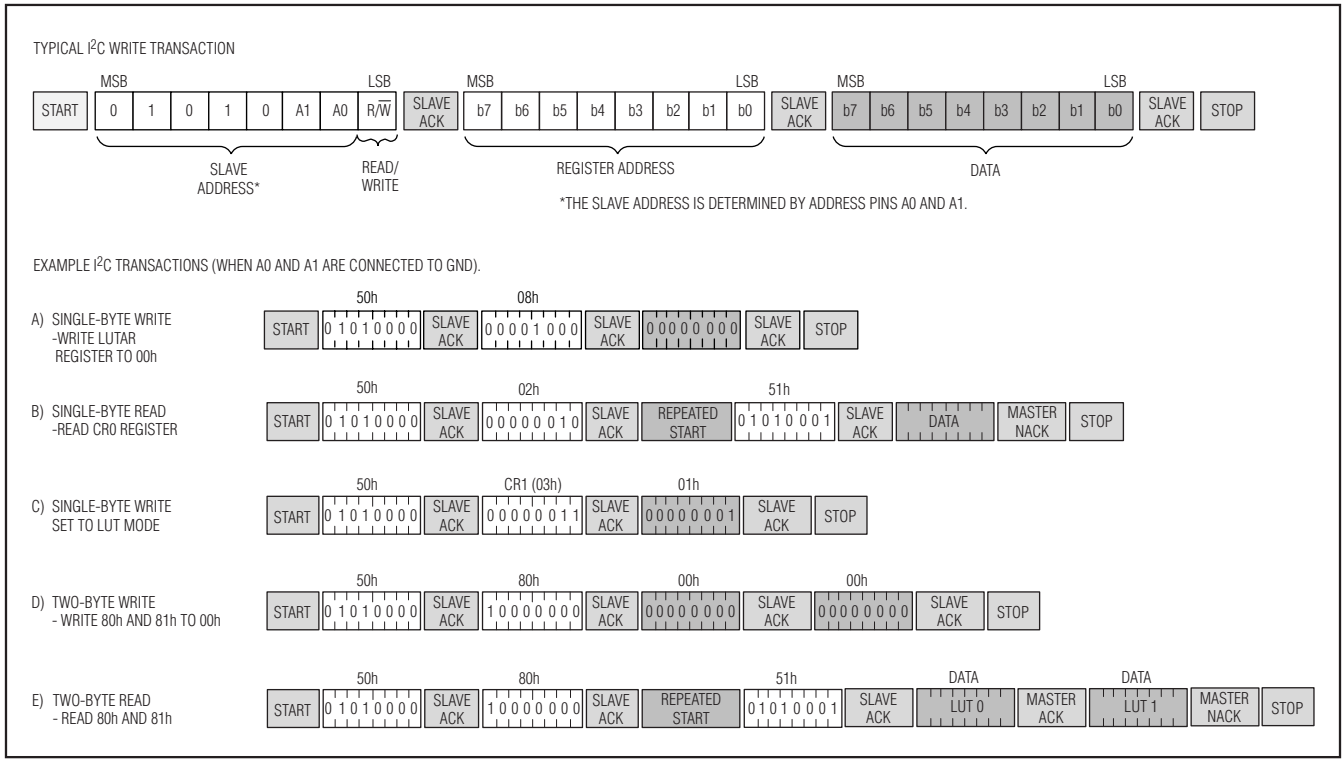


Figure 4. I²C Communication Examples

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and generates a STOP condition.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3501, decouple both the power-supply pin and the wiper-bias voltage pin with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C AC Electrical Characteristics* are within specification. A typical value for the pullup resistors is 4.7kΩ.

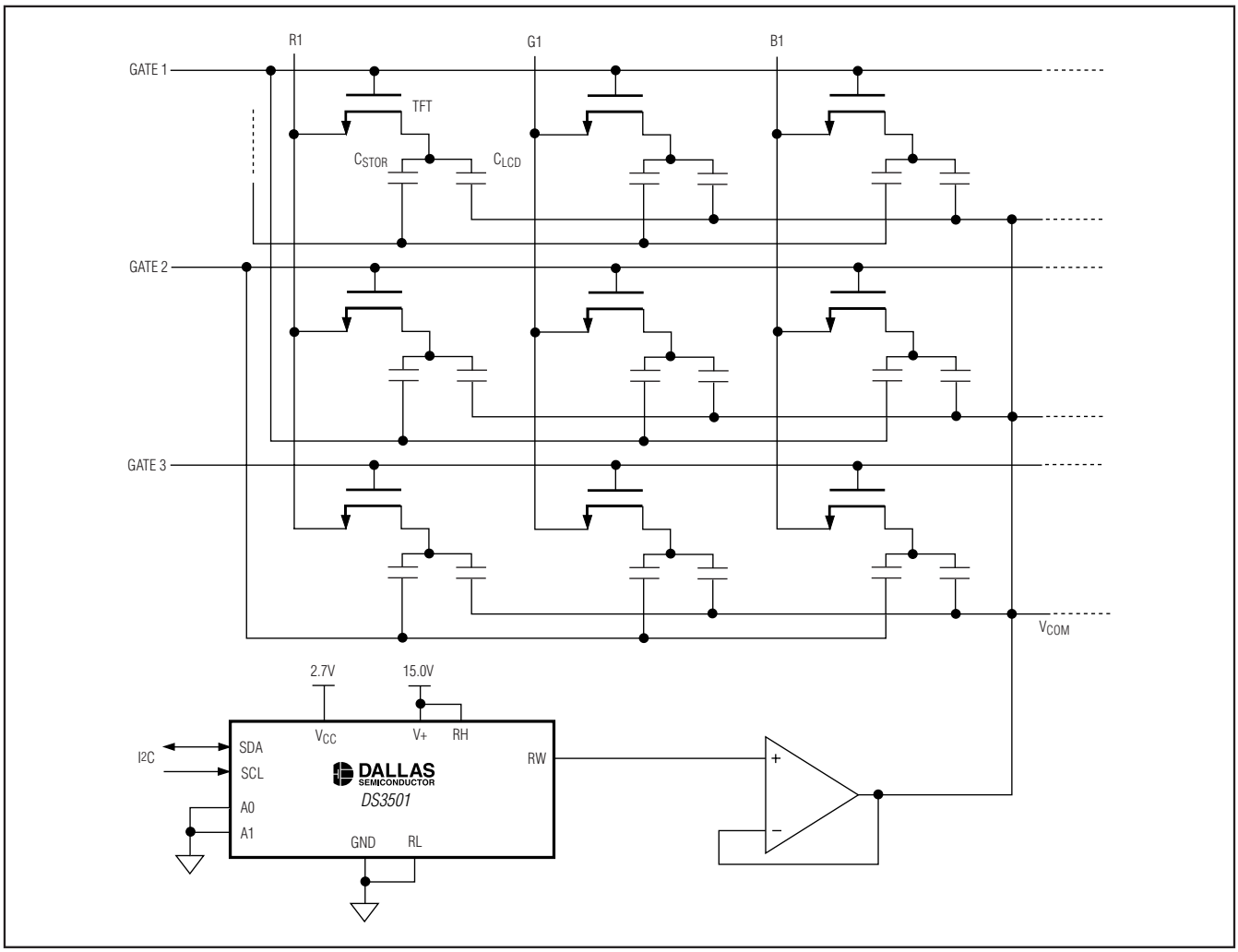
Chip Information

TRANSISTOR COUNT: 22,400

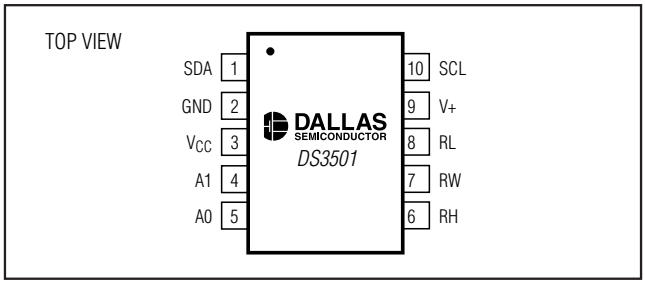
SUBSTRATE CONNECTED TO GROUND

High-Voltage, NV, I²C POT with Temp Sensor and Lookup Table

Typical Operating Circuit



Pin Configuration



Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.