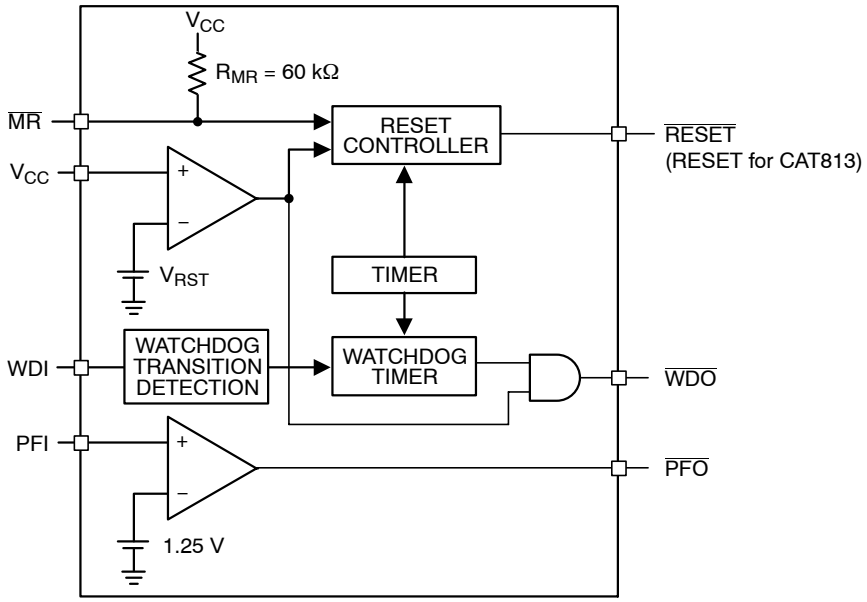


Figure 1. Functional Block Diagram

Device	RESET	RESET	MR	WDI	WDO	PFI
CAT705	@ 4.65 V		x	x	x	@ 1.25 V
CAT706	x		x	x	x	@ 1.25 V
CAT813		@ 4.65 V	x	x	x	@ 1.25 V

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Function
$\overline{MR}$	Manual Reset Input
V_{CC}	Power Supply
GND	Ground
PFI	Power Fail voltage monitor Input
$\overline{PFO}$	Power Fail Output
WDI	Watchdog Timer Input
$\overline{RESET}$	CMOS Push−Pull Active Low Reset Output (CAT705 & CAT706)
RESET	CMOS Push−Pull Active High Reset Output (CAT813)
$\overline{WDO}$	Watchdog Timer Output

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage	6.5	V
All other pins	−0.3 to (V_{CC} + 0.3)	V
Output Current RESET, $\overline{RESET}$, $\overline{WDO}$	20	mA
Continuous Power Dissipations (T_A = +70°C) SOIC 8−lead (derate 5.9 mW/°C above +70°C) MSOP 8−lead (derate 4.1 mW/°C above +70°C)	 471 330	mW
Storage Temperature	−65 to 150	°C
Lead Soldering (10 seconds max)	+300	°C
ESD Rating: Human Body Model	2000	V
ESD Rating: Machine Model	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
V_{CC} (T_A = −40°C to +85°C)	1.0 to 5.5	V
All Other Pins	−0.1 to (V_{CC} + 0.1)	V
Ambient Temperature	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Typical values at T_A = 25°C and V_{CC} = 5 V for CAT705, CAT706 and CAT813 versions. V_{CC} = 3.3 V for the CAT706 T/S versions; V_{CC} = 3.0 V for the CAT706 R version.) (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current	I_{CC}	CAT705, CAT706, CAT813		6	17	μA
		CAT706 (R/S/T Versions)		4	12	μA
Reset Threshold	V_{RST}	CAT705 & CAT813 at −40°C ≤ T_A ≤ +85°C	4.50	4.65	4.75	V
		CAT706 at −40°C ≤ T_A ≤ +85°C	4.25	4.40	4.50	V
		CAT706T at −40°C ≤ T_A ≤ +85°C	3.00	3.08	3.15	V
		CAT706S at −40°C ≤ T_A ≤ +85°C	2.85	2.93	3.00	V
		CAT706R at −40°C ≤ T_A ≤ +85°C	2.55	2.63	2.70	V
Reset Threshold Tempco (Note 1)				40		ppm/°C
Reset Threshold Hysteresis (Note 1)		CAT705 & CAT813		10		mV
		CAT706		5		mV
V_{CC} to Reset Delay (Note 2)	t_{RD}	V_{CC} = V_{TH} to (V_{TH} − 100 mV)		20		μs
Reset Active Timeout Period	t_{RP}		140	200	400	ms
$\overline{\text{RESET}}$ Output High Voltage	V_{OH}	CAT705 & CAT706, 4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = −800 μA	V_{CC} − 1.5 V			V
		CAT705 & CAT706, $V_{RST\ (max)}$ < V_{CC} < 3.6 V, I_{SOURCE} = −500 μA	0.8 x V_{CC}			
$\overline{\text{RESET}}$ Output Low Voltage	V_{OL}	CAT705 & CAT706, 4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA			0.4	V
		CAT705 & CAT706, $V_{RST\ (max)}$ < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA			0.3	
		CAT705 &CAT706, V_{CC} = 1 V, I_{SINK} = 100 μA			0.3	
RESET Output High Voltage	V_{OH}	CAT813, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = −120 μA	V_{CC} − 1.5 V			V
		CAT813, V_{CC} = $V_{RST\ max}$, I_{SOURCE} = −30 μA	0.8 x V_{CC}			
RESET Output Low Voltage	V_{OL}	CAT813, V_{CC} = $V_{RST\ min}$, I_{SINK} = 3.2 mA			0.4	V
		CAT813, V_{CC} = 1.2 V, I_{SINK} = 100 μA			0.3	
WATCHDOG INPUT						
Watchdog Timeout Period	t_{WD}		1.00	1.6	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4 V, V_{IH} = 0.8 x V_{CC}	50			ns
WDI Input Voltage (Note 3)	V_{IL}				0.3 x V_{CC}	V
	V_{IH}		0.7 x V_{CC}			
WDI Input Current (Note 3)		WDI = V_{CC}, Time Average		50	150	μA
		WDI = 0 V, Time Average	−150	−50		

1. Limits are guaranteed by design and not production tested.
2. The RESET short−circuit current is the maximum pull−up current when reset is driven low by a bidirectional output.
3. WDI is internally serviced within the watchdog period if WDI is left open.
4. $\overline{\text{RESET}}$ for CAT705 & CAT706 & RESET for CAT813.
5. Not 100% tested but guaranteed by design.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Typical values at T_A = 25°C and V_{CC} = 5 V for CAT705, CAT706 and CAT813 versions. V_{CC} = 3.3 V for the CAT706 T/S versions; V_{CC} = 3.0 V for the CAT706 R version.) (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
WATCHDOG INPUT						
WDO Output Voltage	V_{W_OH}	$V_{RST\ (max)} < V_{CC} < 3.6$ V; $I_{SOURCE} = -500$ μA	0.8 x V_{CC}			V
		4.5 V < V_{CC} < 5.5 V, $I_{SOURCE} = -800$ μA	$V_{CC} - 1.5$	$V_{CC} - 0.25$		
	V_{W_OL}	$V_{RST\ (max)} < V_{CC} < 3.6$ V, $I_{SINK} = +500$ μA			0.3	
		4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA		0.1	0.4	
WDO to WDI setup time (Note 5)	t_{WDSU}		250			ns
MANUAL RESET INPUT						
$\overline{MR}$ Input Voltage	V_{IL}				0.3 x V_{CC}	V
	V_{IH}		0.7 x V_{CC}			
$\overline{MR}$ Pull−up Current		$\overline{MR}$ = 0 V	40	70	140	μA
$\overline{MR}$ Pulse Width	t_{PB}		1			μs
$\overline{MR}$ Pull−up Resistance	R_{MR}		40	60	80	kΩ
$\overline{MR}$ low to Reset Delay (Note 4)	t_{PDLY}				5	μs
POWER−FAIL INPUT						
PFI Input Threshold		V_{CC} = 5 V	1.2	1.25	1.3	V
PFI Input Current			−25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{P_OH}	$V_{RST(max)} < V_{CC} < 3.6$ V, $I_{SOURCE} = -500$ μA	0.8 x V_{CC}			V
		4.5 V < V_{CC} < 5.5 V, $I_{SOURCE} = -800$ μA	V_{CC} − 1.5		0.4	
	V_{P_OL}	$V_{RST\ (max)} < V_{CC} < 3.6$ V, $I_{SINK} = +1.2$ mA			0.3	
		4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA			0.4	

1. Limits are guaranteed by design and not production tested.
2. The RESET short−circuit current is the maximum pull−up current when reset is driven low by a bidirectional output.
3. WDI is internally serviced within the watchdog period if WDI is left open.
4. $\overline{RESET}$ for CAT705 & CAT706 & RESET for CAT813.
5. Not 100% tested but guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

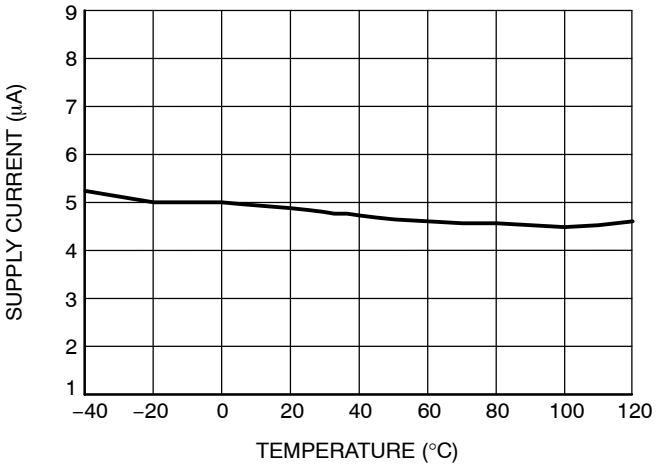


Figure 2. V_{CC} Supply Current vs. Temperature

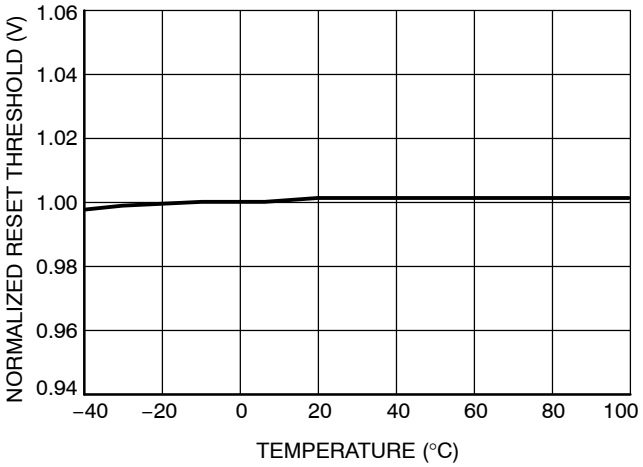


Figure 3. Normalized Reset Threshold Voltage vs. Temperature

FUNCTIONAL DESCRIPTION

Processor Reset

The CAT705, CAT706 & CAT813 detect supply voltage (V_{CC}) conditions that are below the specified voltage trip value (V_{RST}) and provide a reset output to maintain correct system operation. On power−up, $\overline{\text{RESET}}$ (or RESET for the CAT813) are kept active for a minimum delay t_{RP} of 140 ms after the supply voltage (V_{CC}) rises above V_{RST} to allow the power supply and processor to stabilize. When V_{CC} drops below the voltage trip value (V_{RST}), the reset output signals $\overline{\text{RESET}}$ (or RESET) are pulled active. $\overline{\text{RESET}}$ (or RESET) is specifically designed to provide the reset input signals for processors. This provides reliable and consistent operation as power is turned on, off or during brownout conditions by maintaining the processor operation in known conditions.

Manual Reset

The CAT705, CAT706 & CAT813 each have a Manual Reset ($\overline{\text{MR}}$) input to allow for alternative control of the reset outputs. The $\overline{\text{MR}}$ input is designed for direct connection to a pushbutton (see Figure 4). The $\overline{\text{MR}}$ input is internally pulled up by 60 kΩ resistor and must be pulled low to cause the reset output to go active. Internally, this input is debounced and timed such that $\overline{\text{RESET}}$ (or RESET) signals of at least 140 ms minimum will be generated. The min 140 ms t_{RP} delay commences as the Manual Reset input is released from the low level. (see Figure 5).

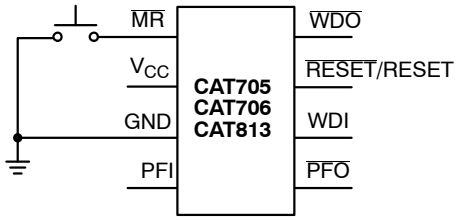


Figure 4. Pushbutton RESET

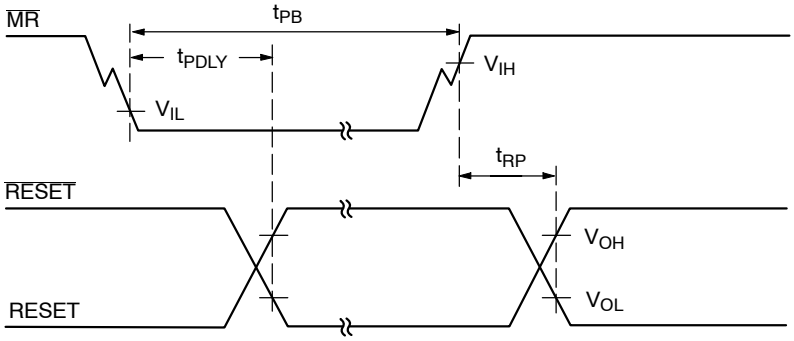


Figure 5. Timing Diagram – Pushbutton RESET

WATCHDOG TIMER

The CAT705, CAT706, & CAT813 provide a Watchdog input (WDI). The watchdog timer function controls the watchdog output ($\overline{WDO}$) signal and forces the $\overline{WDO}$ to be low (active) when the WDI input does not have a transition from low−to−high or high−to−low within 1.6 s typical. If a transition occurs on the WDI input pin prior to the watchdog time−out, the watchdog timer is restarted. The timing diagram is shown in Figure 6. The watchdog timer starts as soon as reset condition becomes inactive.

When the V_{CC} supply drops below the reset threshold, the $\overline{WDO}$ output becomes active and goes low independently of the watchdog timing stage.

Figure 7 below shows a typical implementation of a watchdog function. Any processor signal that repeats dependant on the normal operation of the processor or directed by the software operating on the processor can be used to strobe the watchdog input. The most reliable is a dedicated I/O output transitioned by a specific software instruction.

The watchdog can be disabled by floating (or tri−stating) the WDI input (see Figure 8). If the watchdog is disabled the WDI pin will be pulled low for the first 7/8th's of the watchdog period (t_{WD}) and pulled high for the last 1/8th of the watchdog period. This pulling low of the WDI input and then high is used to detect an open or tri−state condition and will continue to repeat until the WDI input is driven high or low.

For most efficient operation of devices with the watchdog function the WDI input should be held low the majority of the time and only strobed high as required to reset the watchdog timer.

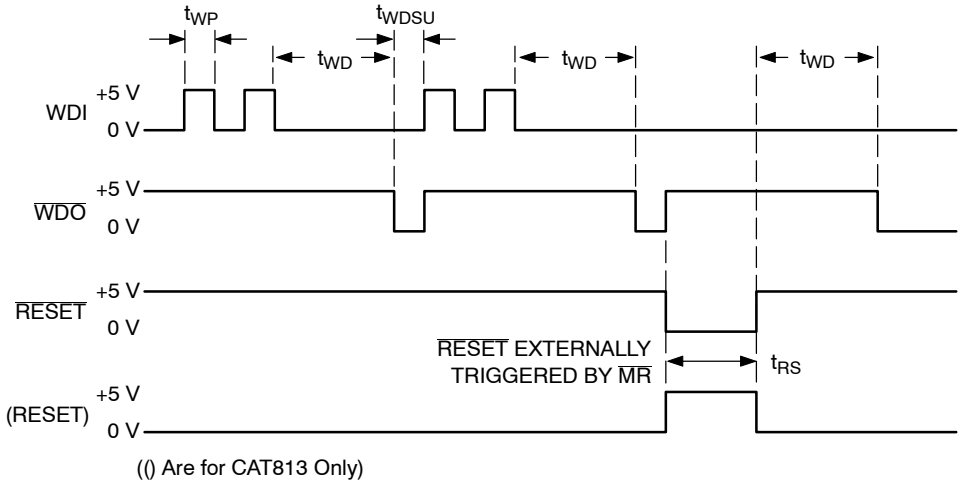


Figure 6. Watchdog Timing Diagram

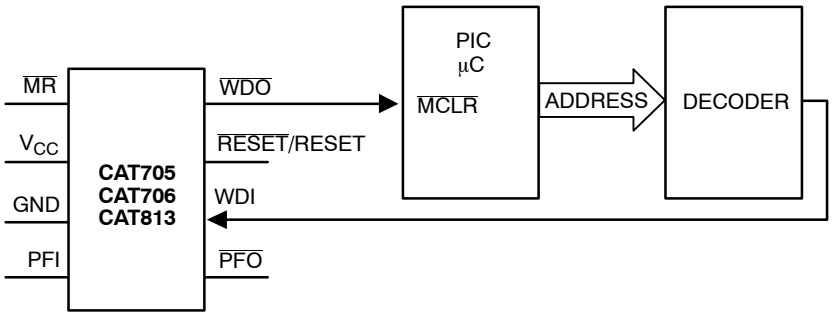


Figure 7. Watchdog Timer Circuit

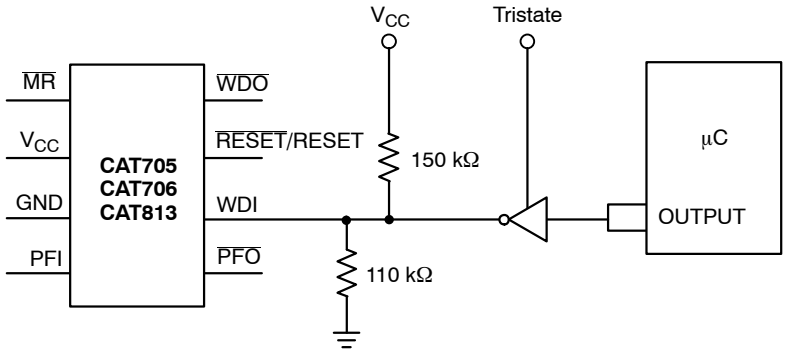


Figure 8. Watchdog Disable Circuit

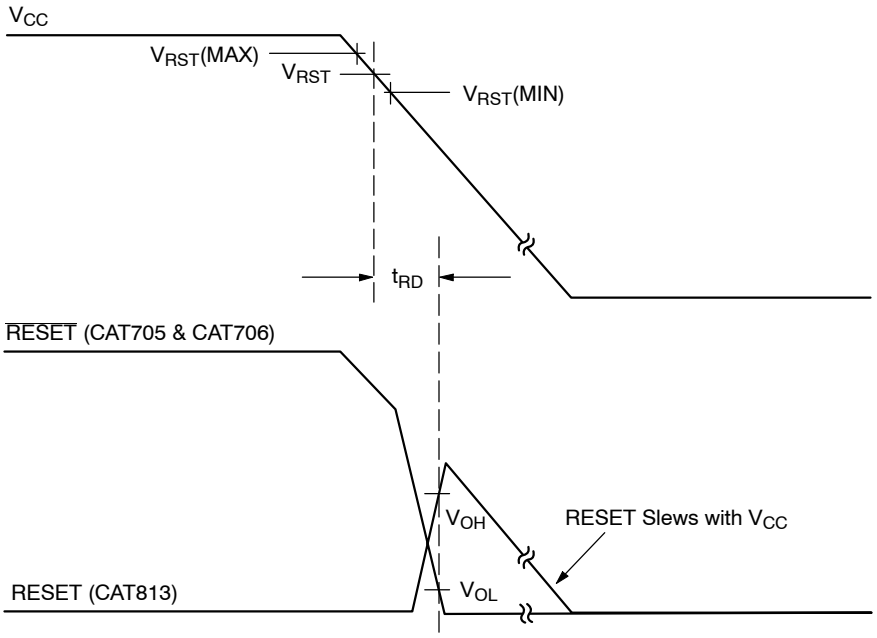


Figure 9. Timing Diagram – Power Down

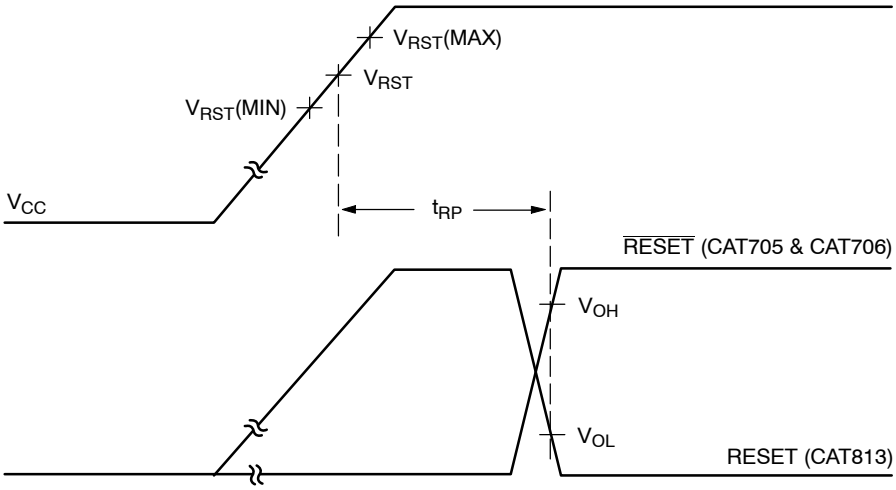


Figure 10. Timing Diagram – Power Up

APPLICATION NOTES

μP's with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output can be pulled low by processors like the 68HC11 allowing for a system reset issued by the processor. The maximum pullup current that can be sourced by the CAT705 & CAT706 1.5 mA (and by the CAT706 T/R/S is 800 μA) allowing the processor to pull the output low even when the CAT70x is pulling it high.

Power Transients

Generally short duration negative−going transients of less than 2 μs on the power supply at V_{RST} minimum will not cause a reset condition. However the lower the voltage of the transient the shorter the required time to cause a reset output. These issues can usually be remedied by the proper location of bypass capacitance on the circuit board.

Output Valid Conditions

The $\overline{\text{RESET}}$ output uses a push−pull output which can maintain a valid output down to a **V_{CC} of 1.0 volts**. To sink current below 0.8 V a resistor can be connected from $\overline{\text{RESET}}$ to Ground (see Figure 11.) This arrangement will maintain a valid value on the $\overline{\text{RESET}}$ output during both power up and down but will draw current when the $\overline{\text{RESET}}$ output is in the high state. A resistor value of about 100 kΩ should be adequate in most situations to maintain a low condition valid output down to V_{CC} equal to 1.0 V.

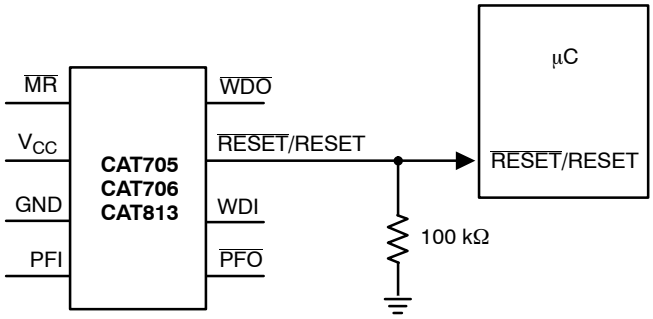


Figure 11. $\overline{\text{RESET}}$ Valid for V_{CC} < 1.0 V

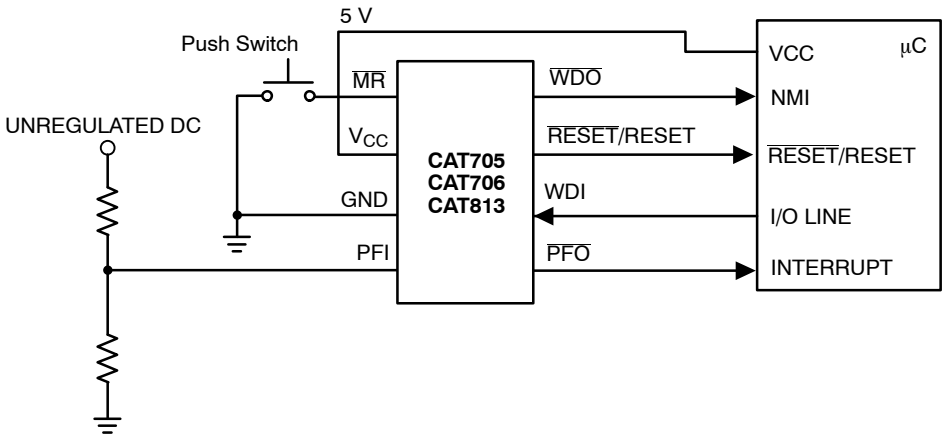
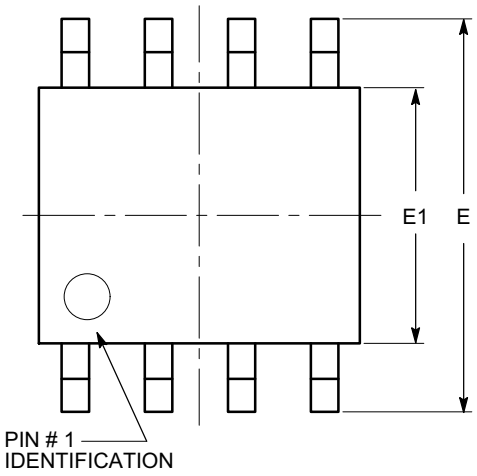


Figure 12. Typical Operating Circuit

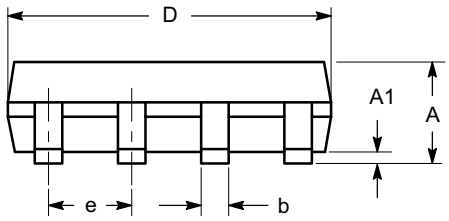
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

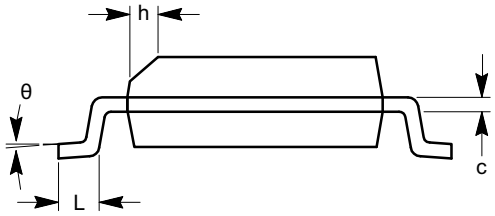


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

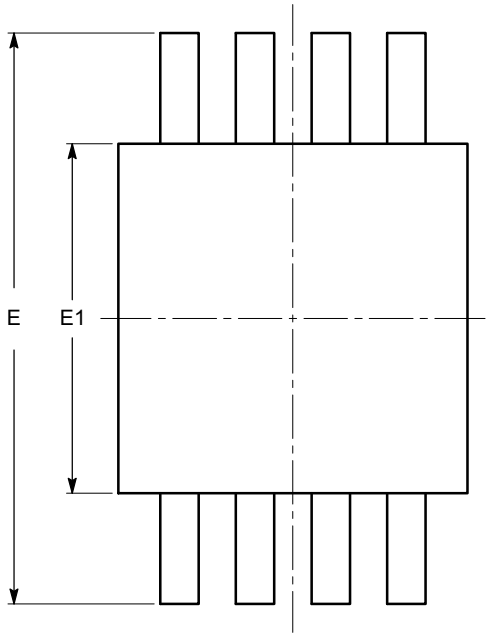


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

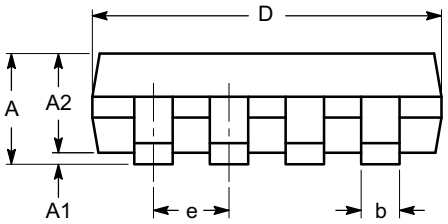
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD−01
ISSUE O

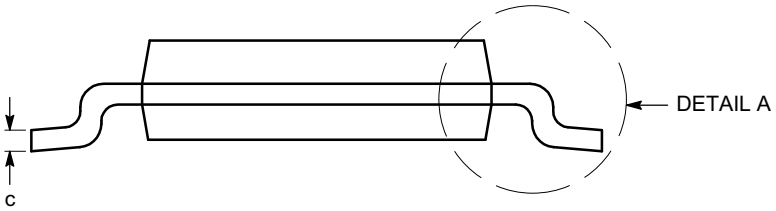


TOP VIEW

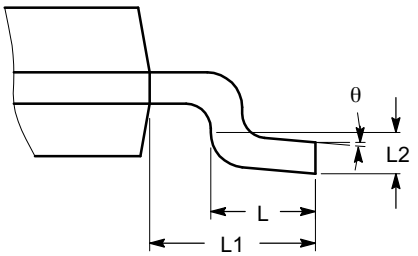
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0º		6º



SIDE VIEW



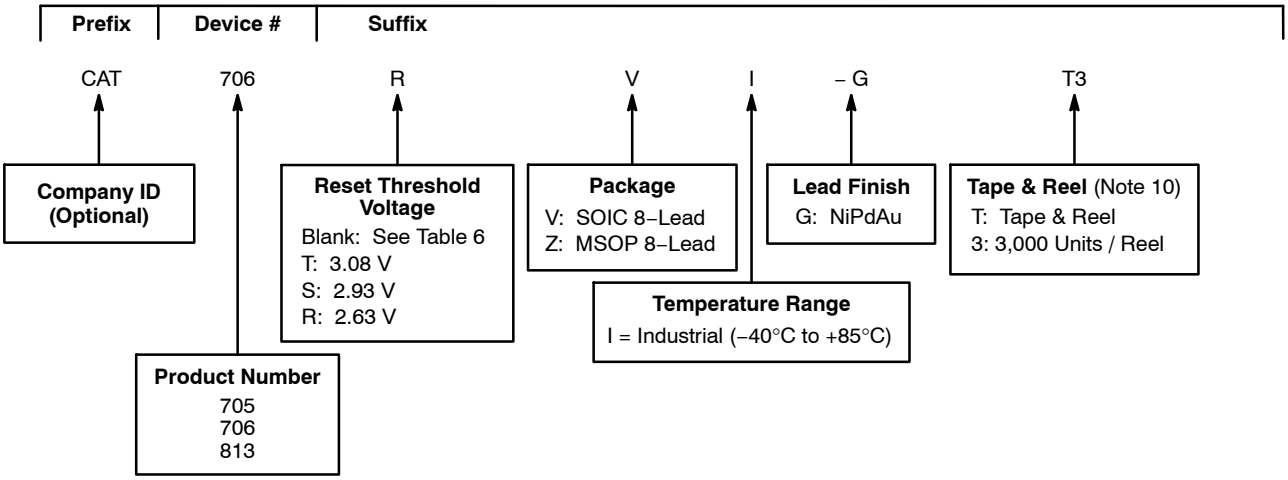
END VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

Example of Ordering Information (Notes 6 – 9)



6. All packages are RoHS−compliant (Lead−free, Halogen−free).
7. The standard lead finish is NiPdAu.
8. The device used in the above example is a CAT706RVI−GT3 (2.63 V, SOIC 8−Lead, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
9. Contact factory for package availability.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 5. TOP MARKING INFORMATION (For All Thresholds)

Device #	Package	Top Marking
NiPdAu FINISH (−G)		
CAT705	MSOP	ABRT
CAT706	MSOP	ABRT
CAT813	MSOP	ABRS
CAT705	SOIC	CAT705V
CAT706	SOIC	CAT706V
CAT813	SOIC	CAT813V

Table 6. ORDERING PART NUMBER

Order Part Number	Threshold Voltage
CAT705VI−G	4.65 V
CAT705ZI−G	
CAT706VI−G	4.40 V
CAT706ZI−G	
CAT706RVI−G	2.63 V
CAT706RZI−G	
CAT706SVI−G	2.93 V
CAT706SZI−G	
CAT706TVI−G	3.08 V
CAT706TZI−G	
CAT813VI−G	4.65 V
CAT813ZI−G	

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative