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DOCUMENTATION

Data Sheet

- ADG467: Octal Channel Protectors Data Sheet

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Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

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- ADG467 Material Declaration
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- Quality And Reliability
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REVISION HISTORY

2/11—Rev. A to Rev. B

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	ADG467 +25°C	ADG467 −40°C to +85°C	Unit	Test Conditions/Comments
FAULT PROTECTED CHANNEL				
Fault-Free Analog Signal Range	V_{SS} + 1.5		V typ	Output open circuit
	V_{DD} − 1.5		V typ	
	V_{SS} + 1.7		V typ	Output loaded, 1 mA
	V_{DD} − 1.7		V typ	
R_{ON}	62	80	Ω typ	−10 V ≤ V_{Sx} ≤ +10 V, I_{Sx} = 1 mA
		95	Ω max	
R_{ON} Flatness		6	Ω max	−5 V ≤ V_{Sx} ≤ +5 V
R_{ON} Match between Channels	5	6	Ω max	V_{Sx} = ±10 V, I_{Sx} = 1 mA
LEAKAGE CURRENTS				
Channel Output Leakage, $I_{S(ON)}$				V_{Sx} = V_{Dx} = ±10 V
(Without Fault Condition)	±0.04	±0.2	nA typ	
	±1	±5	nA max	
Channel Input Leakage, $I_{D(ON)}$				V_{Sx} = ±25 V
(with Fault Condition)	±0.2	±0.4	nA typ	V_{Dx} = open circuit
	±2	±5	nA max	
Channel Input Leakage, $I_{D(OFF)}$				V_{DD} = 0 V, V_{SS} = 0 V
(with Power Off and Fault)	±0.5	±2	nA typ	V_{Sx} = ±35 V
	±2	±10	nA max	V_{Dx} = open circuit
Channel Input Leakage, $I_{D(OFF)}$				V_{DD} = 0 V, V_{SS} = 0 V
(with Power Off and Output Short Circuit)	±0.006	±0.16	µA typ	V_{Sx} = ±35 V, V_{Dx} = 0 V
	±0.015	±0.5	µA max	
POWER REQUIREMENTS				
I_{DD}	±0.05		µA typ	
	±0.5	±8	µA max	
I_{SS}	±0.05		µA typ	
	±0.5	±8	µA max	
V_{DD}/V_{SS}		±4.5/±20	V min/max	

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to V_{SS}	+44 V
V_{Sx}, V_{Dx}, Analog Input Overvoltage with Power On[1]	V_{SS} − 20 V to V_{DD} + 20 V
V_{Sx}, V_{Dx}, Analog Input Overvoltage with Power Off[1]	−40 V to +40 V
Continuous Current, V_{Sx}, V_{Dx}	20 mA
Peak Current, V_{Sx}, V_{Dx} (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Junction Temperature	+150°C
SOIC Package	
θ_{JA}, Thermal Impedance	160°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C
SSOP Package	
θ_{JA}, Thermal Impedance	130°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

[1] Overvoltages at V_{Sx} or V_{Dx} are clamped by the channel protector; see the Circuit Information section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

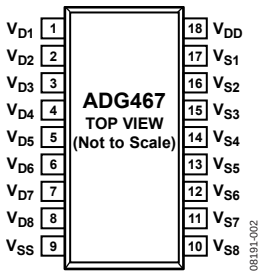


Figure 2. 18-Lead SOIC Pin Configuration

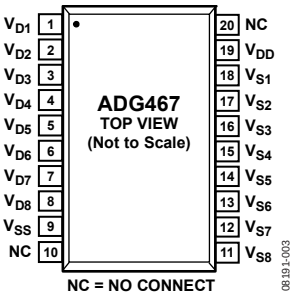


Figure 3. 20-Lead SSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.			
SOIC	**SSOP**	**Mnemonic**	**Description**
1	1	V_{D1}	Drain Terminal 1. This pin can be an input or an output.
2	2	V_{D2}	Drain Terminal 2. This pin can be an input or an output.
3	3	V_{D3}	Drain Terminal 3. This pin can be an input or an output.
4	4	V_{D4}	Drain Terminal 4. This pin can be an input or an output.
5	5	V_{D5}	Drain Terminal 5. This pin can be an input or an output.
6	6	V_{D6}	Drain Terminal 6. This pin can be an input or an output.
7	7	V_{D7}	Drain Terminal 7. This pin can be an input or an output.
8	8	V_{D8}	Drain Terminal 8. This pin can be an input or an output.
9	9	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
N/A	10	NC	No Connect.
10	11	V_{S8}	Source Terminal 1. This pin can be an input or an output.
11	12	V_{S7}	Source Terminal 2. This pin can be an input or an output.
12	13	V_{S6}	Source Terminal 3. This pin can be an input or an output.
13	14	V_{S5}	Source Terminal 4. This pin can be an input or an output.
14	15	V_{S4}	Source Terminal 5. This pin can be an input or an output.
15	16	V_{S3}	Source Terminal 6. This pin can be an input or an output.
16	17	V_{S2}	Source Terminal 7. This pin can be an input or an output.
17	18	V_{S1}	Source Terminal 8. This pin can be an input or an output.
18	19	V_{DD}	Most Positive Power Supply Potential.
N/A	20	NC	No Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

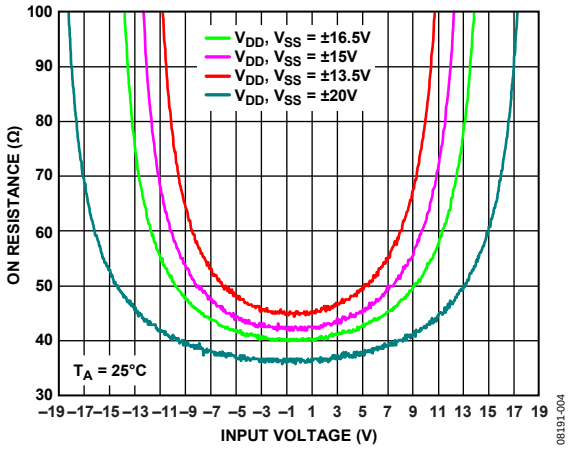


Figure 4. On Resistance as a Function of V_{DD} and V_{Sx} (Input Voltage), Dual Supply

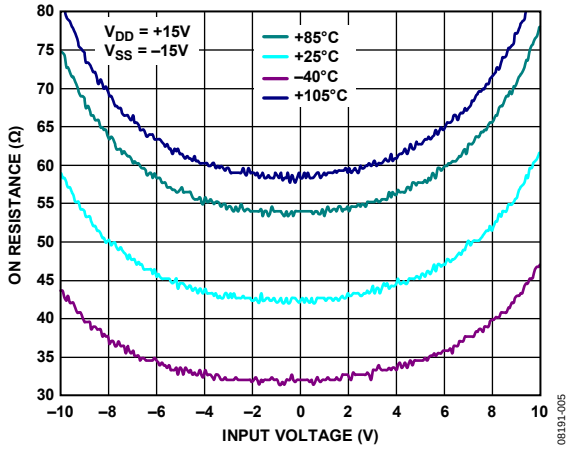


Figure 5. On Resistance as a Function of Temperature and V_{Sx} (Input Voltage)

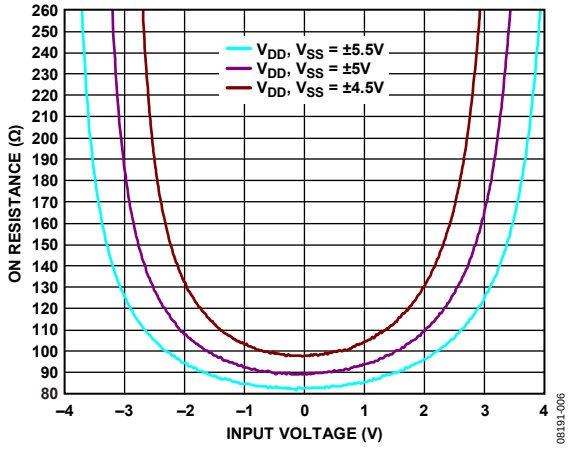


Figure 6. On Resistance as a Function of V_{DD} and V_{Sx} (Input Voltage), 5 V Dual Supply

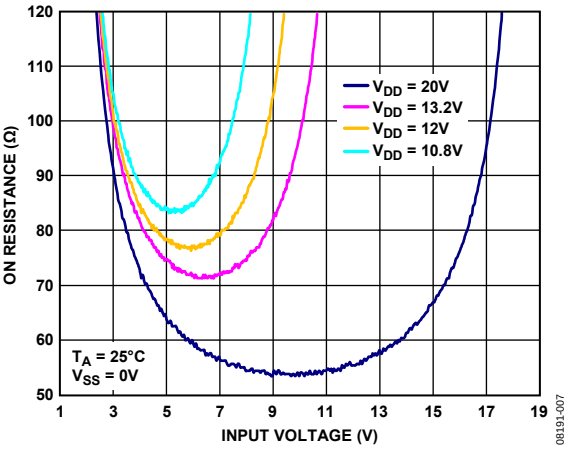


Figure 7. On Resistance as a Function of V_{DD} and V_{Sx} (Input Voltage), Single Supply

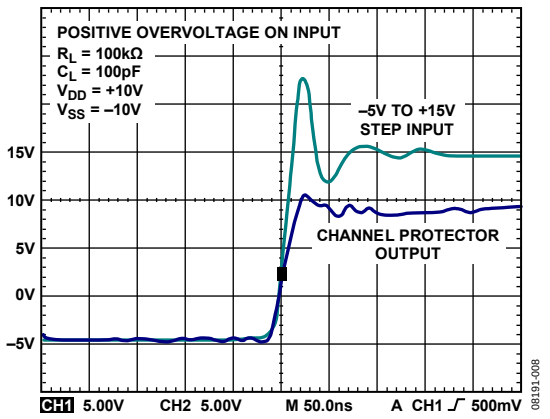


Figure 8. Positive Overvoltage Transience Response

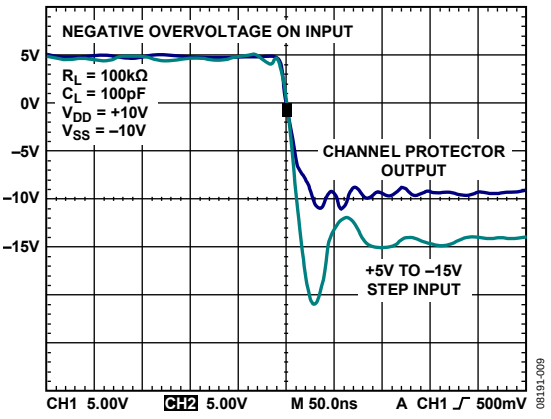


Figure 9. Negative Overvoltage Transience Response

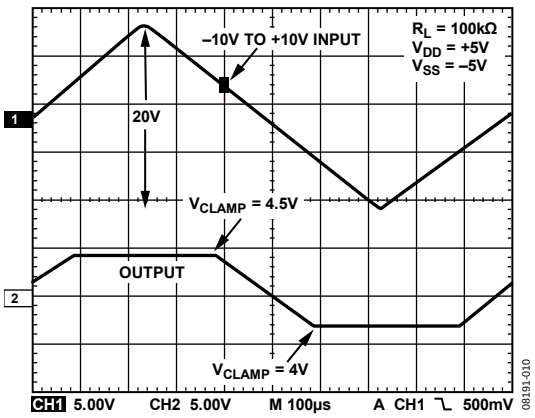


Figure 10. Overvoltage Ramp

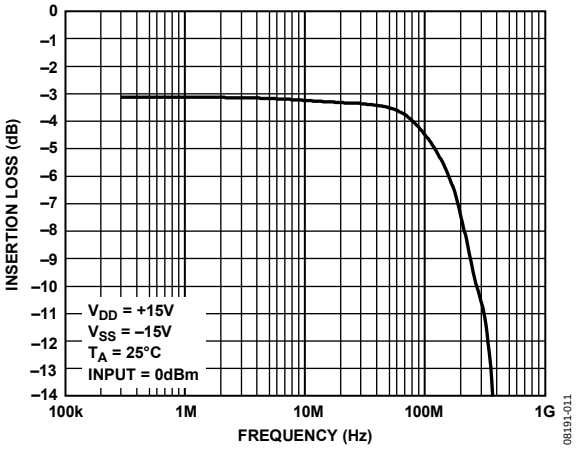


Figure 11. Frequency Response (Magnitude)

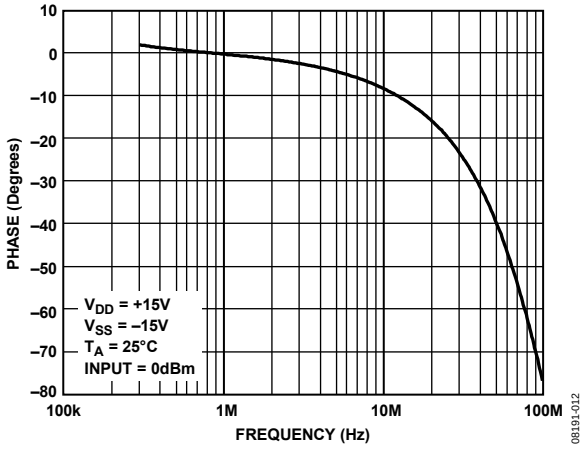


Figure 12. Frequency Response (Phase)

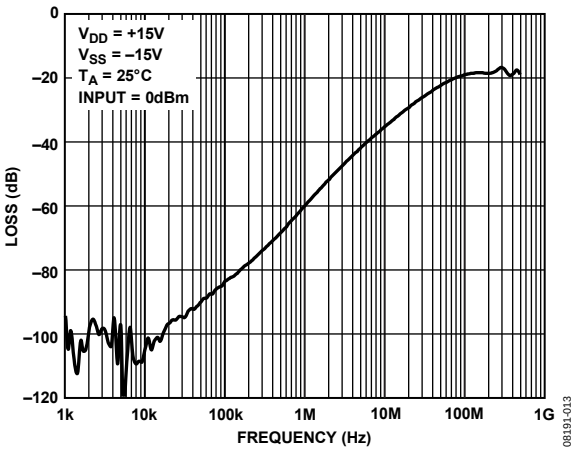


Figure 13. Crosstalk Between Adjacent Channels

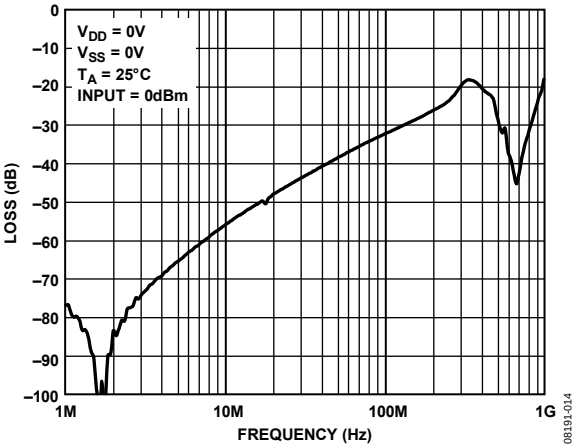


Figure 14. Off Isolation

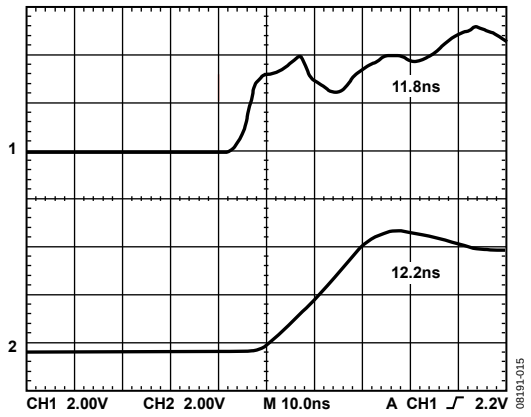


Figure 15. Propagation Delay

TEST CIRCUITS

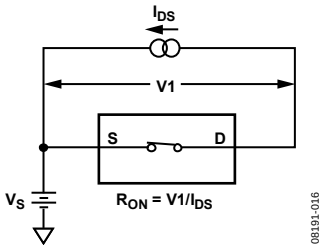


Figure 16. On Resistance

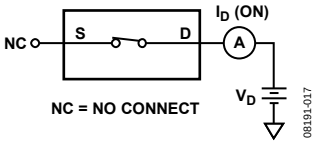


Figure 17. On Leakage

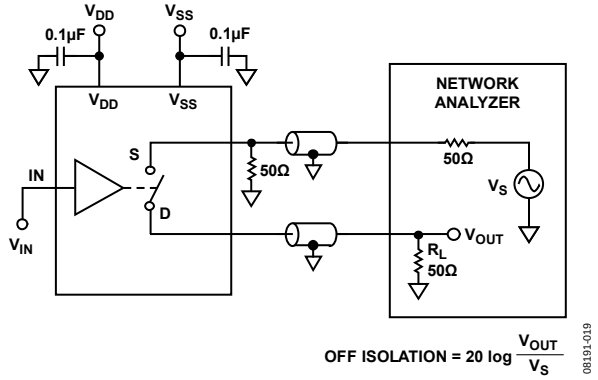


Figure 19. Off Isolation

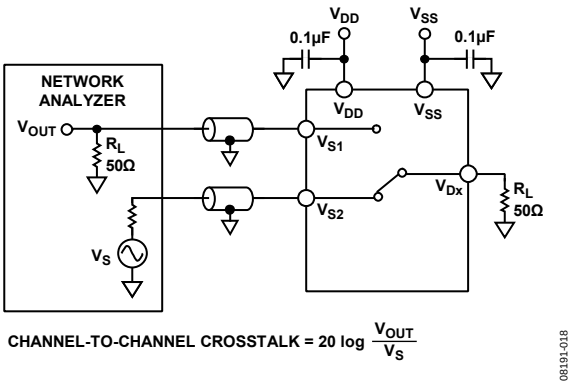


Figure 18. Channel-to-Channel Crosstalk

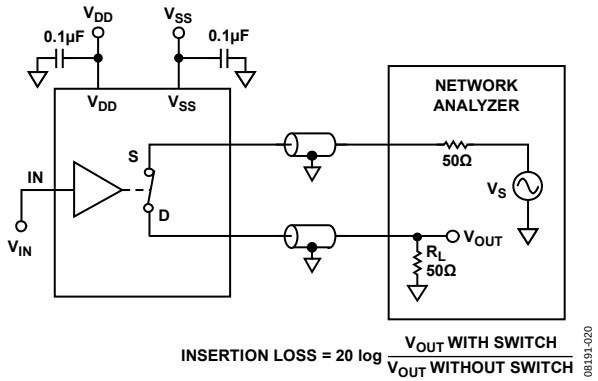


Figure 20. Bandwidth

CIRCUIT INFORMATION

Figure 21 shows a simplified schematic of a channel protector circuit. The circuit is made up of four MOS transistors—two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and thus increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation, the channel protectors have an on resistance of 62 Ω typical. The channel protectors are very low power devices, and even under fault conditions, the supply current is limited to sub microampere levels. All transistors are dielectrically isolated from each other using a trench isolation method. This makes it impossible to latch up the channel protectors. For further details, see the Trench Isolation section.

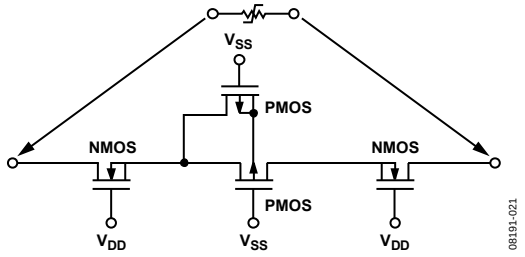
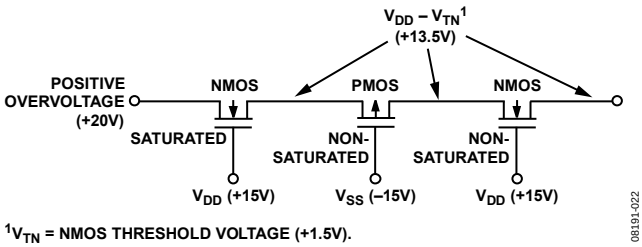


Figure 21. The Channel Protector Circuit

OVERVOLTAGE PROTECTION

When a fault condition occurs on the input of a channel protector, the voltage on the input has exceeded some threshold voltage set by the supply rail voltages. The threshold voltages are related to the supply rails as follows. For a positive overvoltage, the threshold voltage is given by $V_{DD} - V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistor (1.5 V typical). In the case of a negative overvoltage, the threshold voltage is given by $V_{SS} - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (−1.5 V typical). If the input voltage exceeds these threshold voltages, the output of the channel protector (no load) is clamped at these threshold voltages. However, the channel protector output clamps at a voltage value that is inside these thresholds if the output is loaded. For example, with an output load of 1 kΩ, V_{DD} = 15 V, and a positive overvoltage on the input, the output clamps at $V_{DD} - V_{TN} - \Delta V$ = 15 V − 1.5 V − 0.6 V = 12.9 V, where ΔV is due to an I × R voltage drop across the channels of the MOS devices (see Figure 23). As can be seen from Figure 23, the current during fault condition is determined by the load on the output (that is, V_{CLAMP}/R_L). However, if the supplies are off, the fault current is limited to the nano-ampere level.

Figure 22, Figure 24, and Figure 25 show the operating conditions of the signal path transistors during various fault conditions. Figure 22 shows how the channel protectors operate when a positive overvoltage is applied to the channel protector.



$^1V_{TN}$ = NMOS THRESHOLD VOLTAGE (+1.5V).

Figure 22. Positive Overvoltage on the Channel Protector

The first NMOS transistor goes into a saturated mode of operation as the voltage on its drain exceeds the gate voltage (V_{DD}) − the threshold voltage (V_{TN}). This situation is shown in Figure 23. The potential at the source of the NMOS device is equal to $V_{DD} - V_{TN}$. The other MOS devices are in a nonsaturated mode of operation.

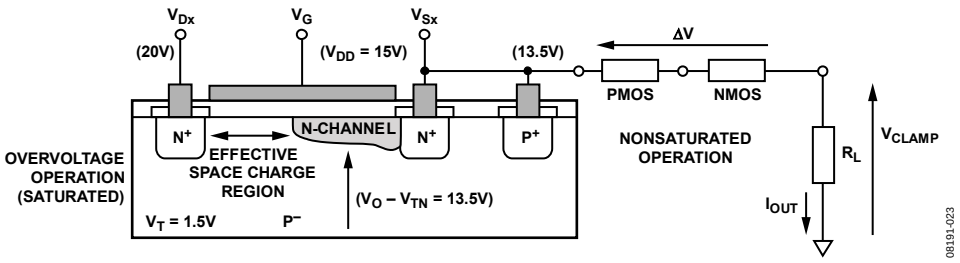


Figure 23. Positive Overvoltages Operation of the Channel Protector

When a negative overvoltage is applied to the channel protector circuit, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds $V_{SS} - V_{TP}$ (see Figure 24). As in the case of the positive overvoltage, the other MOS devices are nonsaturated.

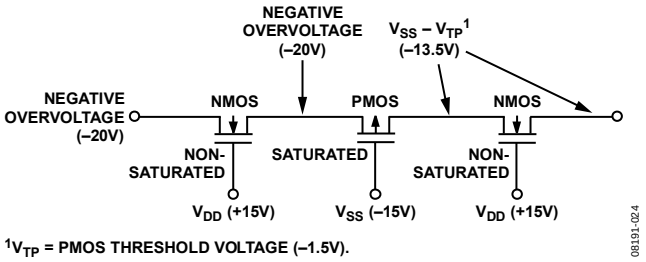


Figure 24. Negative Overvoltage on the Channel Protector

The channel protector is also functional when the supply rails are down (for example, power failure) or momentarily unconnected (for example, rack system). This is where the channel protector has an advantage over more conventional protection methods such as diode clamping (see the Applications Information section). When V_{DD} and V_{SS} equal 0 V, all transistors are off and the current is limited to subnano-ampere levels (see Figure 25).

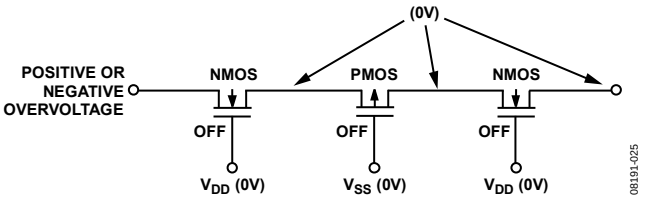


Figure 25. Channel Protector Supplies Equal to 0 V

TRENCH ISOLATION

The MOS devices that make up the channel protector are isolated from each other by an oxide layer (trench) (see Figure 26). When the NMOS and PMOS devices are not electrically isolated from each other, parasitic junctions between CMOS transistors may cause latch-up. Latch-up is caused when P-N junctions that are normally reverse biased become forward biased, causing large currents to flow, which can be destructive.

CMOS devices are normally isolated from each other by junction isolation. In junction isolation, the N and P wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed; the result is a latch-up-proof circuit.

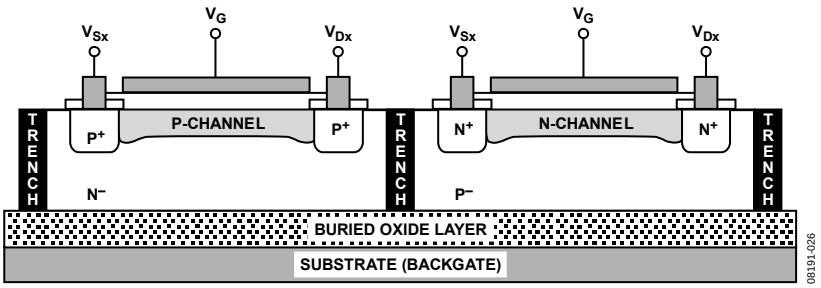


Figure 26. Trench Isolation

APPLICATIONS INFORMATION

OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION

The ADG467 is ideal for use in applications where input overvoltage protection is required and correct power supply sequencing cannot always be guaranteed. The overvoltage protection ensures that the output voltage of the channel protector does not exceed the threshold voltages set by the supplies (see the Circuit Information section) when there is an overvoltage on the input. When the input voltage does not exceed these threshold voltages, the channel protector behaves like a series resistor (62 Ω typical). The resistance of the channel protector does vary slightly with operating conditions (see the Typical Performance Characteristics section).

The power sequencing protection is provided by the channel protector, which becomes a high resistance device when the supplies to the channel protector are not connected. Under this condition, all transistors in the channel protector are off and the only currents that flow are leakage currents, which are at the microampere level.

Figure 27 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a hot insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application, it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to latch up. This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector (see Figure 27) to ensure that the rest of the circuitry is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails of the board when it is being disconnected. This ensures that signals on the inputs of the CMOS devices never exceed the supplies.

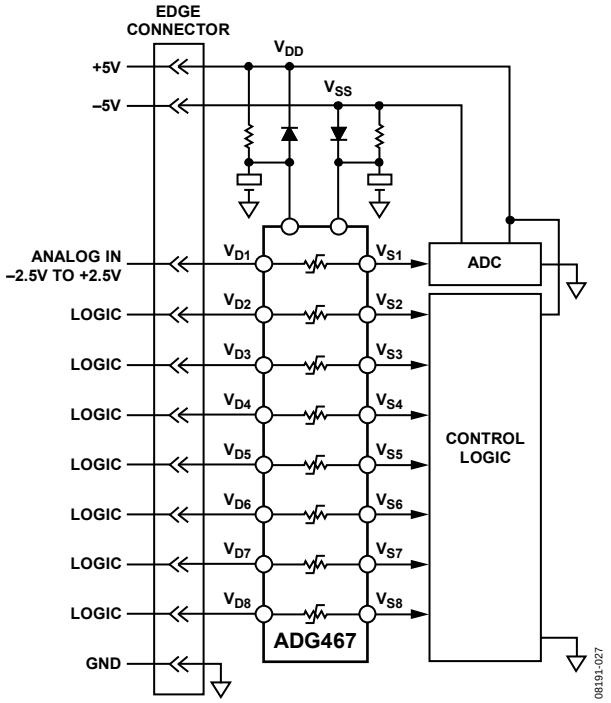


Figure 27. Overvoltage and Power Supply Sequencing Protection

HIGH VOLTAGE SURGE SUPPRESSION

The ADG467 is not intended for use in high voltage applications like surge suppression. The ADG467 has breakdown voltages in excess of V_{SS} − 20 V and V_{DD} + 20 V on the inputs when the power supplies are connected. When the power supplies are disconnected, the breakdown voltages on the input of the channel protector are ±40 V. In applications where inputs are likely to be subject to overvoltages exceeding the breakdown voltages specified for the channel protectors, transient voltage suppressors (TVSs) should be used. These devices are commonly used to protect vulnerable circuits from electric overstress such as that caused by electrostatic discharge, inductive load switching, and induced lightning. However, TVSs can have a substantial standby (leakage) current (300 µA typical) at the reverse standoff voltage. The reverse stand-off voltage of a TVS is the normal peak operating voltage of the circuit. Also, a TVS offers no protection against latch-up of sensitive CMOS devices when the power supplies are off. The ideal solution is to use a channel protector in conjunction with a TVS to provide the optimal leakage current specification and circuit protection.

Figure 28 shows an input protection scheme that uses both a TVS and a channel protector. The TVS is selected with a reverse standoff voltage that is much greater than the operating voltage of the circuit (TVSs with higher breakdown voltages tend to have better standby leakage current specifications) but is inside the breakdown voltage of the channel protector. This circuit protects the circuitry regardless of whether the power supplies are present.

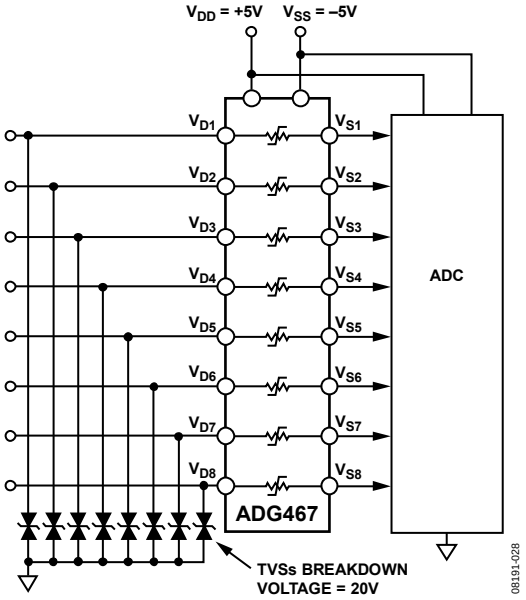
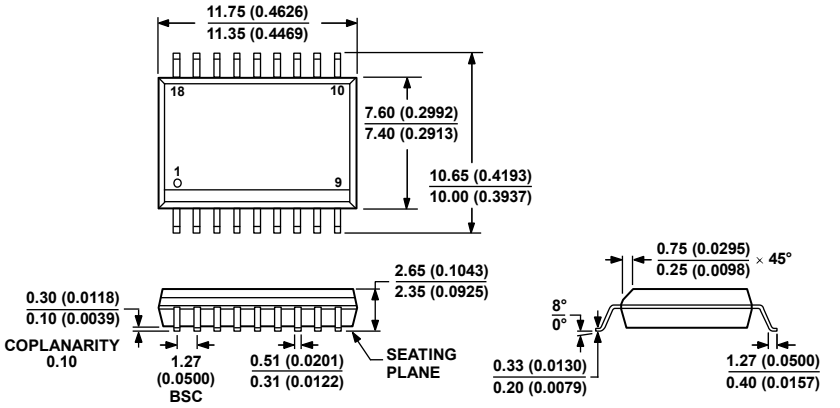


Figure 28. High Voltage Protection

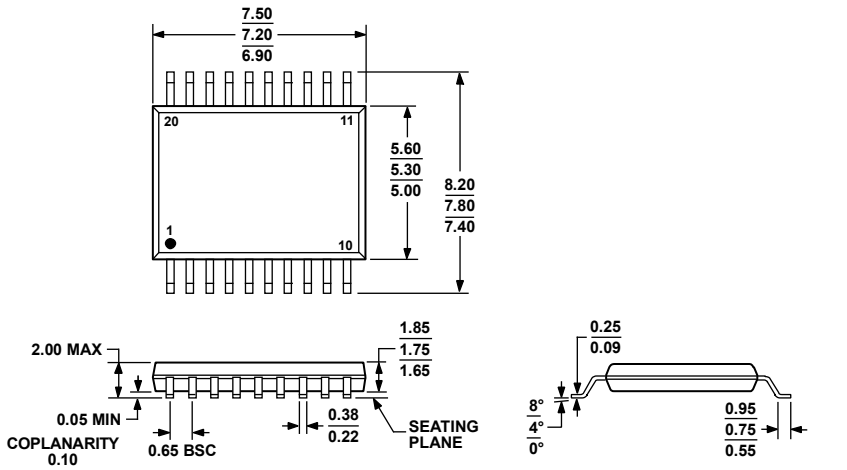
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 29. 18-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-18)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150-AE

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Figure 30. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG467BR	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BR-REEL	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BR-REEL7	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ-REEL	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRZ-REEL7	−40°C to +85°C	18-Lead Standard Small Outline Package [SOIC_W]	RW-18
ADG467BRS	−40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRS-REEL	−40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRSZ	−40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20
ADG467BRSZ-REEL	−40°C to +85°C	20-Lead Shrink Small Outline Package [SSOP]	RS-20

[1] Z = RoHS Compliant Part.

NOTES

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