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8/2018—Rev. B to Rev. C

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12/2017—Rev. A to Rev. B

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1/1997—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V, V_{SS} = −15 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Symbols	25°C Min	25°C Typ	25°C Max	−40°C to +85°C Min	−40°C to +85°C Typ	−40°C to +85°C Max	Unit	Test Conditions/Comments
FAULT PROTECTED CHANNEL									
Fault Free Analog Signal Range[1]					V_{SS} + 1.5		V_{DD} − 1.5	V	Output open circuit
On Resistance	R_{ON}		80	99.5			126.5	Ω	−10 V ≤ V_S[2] ≤ +10 V, I_S = 1 mA
R_{ON} Flatness				8.5			9	Ω	−5 V ≤ V_S[2] ≤ +5 V
LEAKAGE CURRENTS									
Channel Output Leakage (Without Fault Condition)	$I_{S (ON)}$		±0.1	±1		±1	±5	nA	V_S[2] = V_D[2] = ±10 V
Channel Input Leakage (With Fault Condition)	$I_{D (ON)}$		±0.2	±2		±0.4	±5	nA	V_S[2] = ±25 V, V_D[2] = open circuit
Channel Input Leakage (With Power Off and Fault)	$I_{D (OFF)}$		±0.5	±2		±2	±10	nA	V_{DD} = 0 V, V_{SS} = 0 V, V_S[2] = ±35 V, V_D[2] = open circuit
Channel Input Leakage (With Power Off and Output Short Circuit)	$I_{D (OFF)}$		±0.005	±0.015		±0.1	±0.5	µA	V_{DD} = 0 V, V_{SS} = 0 V, V_S[2] = ±35 V, V_D[2] = 0 V
POWER REQUIREMENTS									
Positive Supply Current	I_{DD}		±0.05	±0.5			±5	µA	
Negative Supply Current	I_{SS}		±0.05	±0.5			±5	µA	
Positive/Negative Power Supply	V_{DD}/V_{SS}	0		±20	0		±20	V	

[1] Guaranteed by design, not subject to production test.
[2] V_S is the voltage at the source of the switch and V_D is the voltage at the drain of the switch.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to V_{SS}	44 V
V_S, V_D, Analog Input Overvoltage with Power On[1]	V_{SS} – 20 V to V_{DD} + 20 V
V_S, V_D, Analog Input Overvoltage with Power Off[1]	–40 V to +40 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] The channel protector clamps overvoltages at the source (S) or the drain (D) of the switch. See the Theory of Operation section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
6-Lead SOT-23[1]	230	92	°C/W
8-Lead MSOP[2]	206	44	°C/W

[1] Thermal impedance simulated values are based on JEDEC 1S 2-layer test board. See EIA/JEDEC standard JESD51.
[2] Thermal impedance simulated values are based on JEDEC 2S2P 4-layer test board. See EIA/JEDEC standard JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

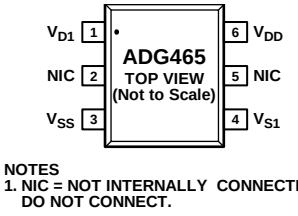

Figure 2. 6-Lead SOT-23 Pin Configuration

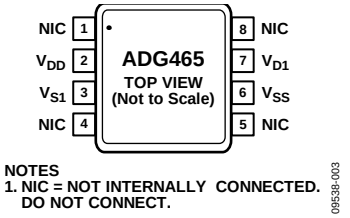

Figure 3. 8-Lead MSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
6-Lead SOT-23	**8-Lead MSOP**	**Mnemonic**	**Description**
1	7	V_{D1}	One Terminal of the Channel Protector. The channel protector is bidirectional so this terminal can be used as an input or an output.
2, 5	1, 4, 5, 8	NIC	Not Internally Connected. Do not connect.
3	6	V_{SS}	Negative Power Supply (0 V to −20 V). The clamping point for a negative overvoltage is also defined as V_{SS}. See the Overvoltage Protection section.
4	3	V_{S1}	One Terminal of the Channel Protector. The channel protector is bidirectional so this terminal can be used as an input or an output.
6	2	V_{DD}	Positive Power Supply (0 V to 20 V). The clamping point for a positive overvoltage is also defined as V_{DD}. See the Overvoltage Protection section.

TYPICAL PERFORMANCE CHARACTERISTICS

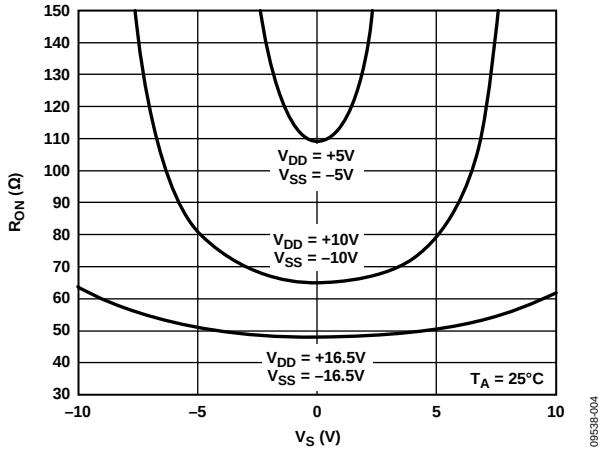

Figure 4. On Resistance (R_{ON}) vs. Input Voltage (V_S) as a Function of V_{DD}/V_{SS}

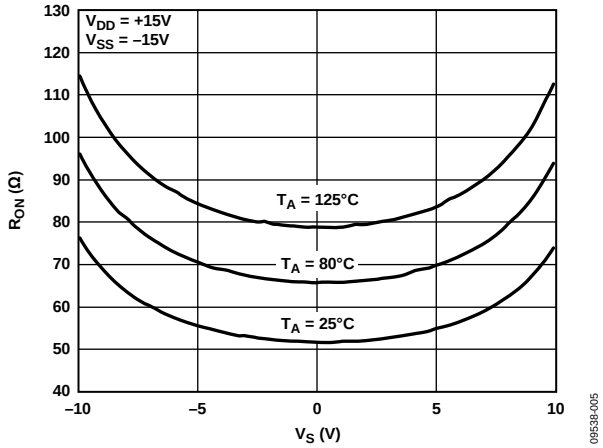

Figure 5. On Resistance (R_{ON}) vs. Input Voltage (V_S) as a Function of Temperature

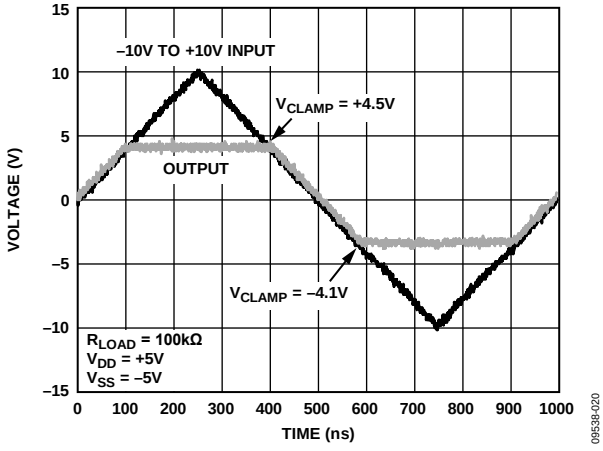

Figure 6. Overvoltage Ramp

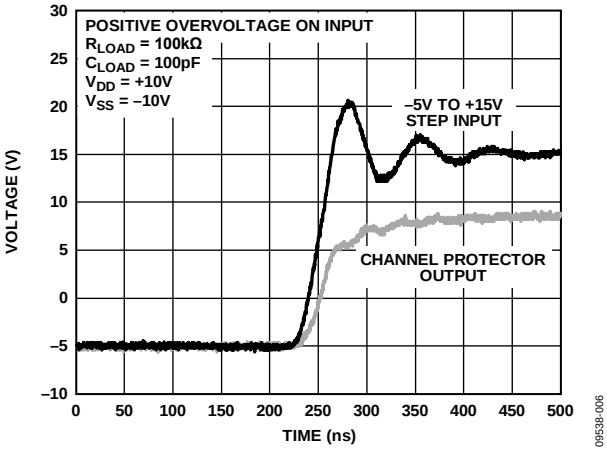

Figure 7. Positive Overvoltage Transience Response

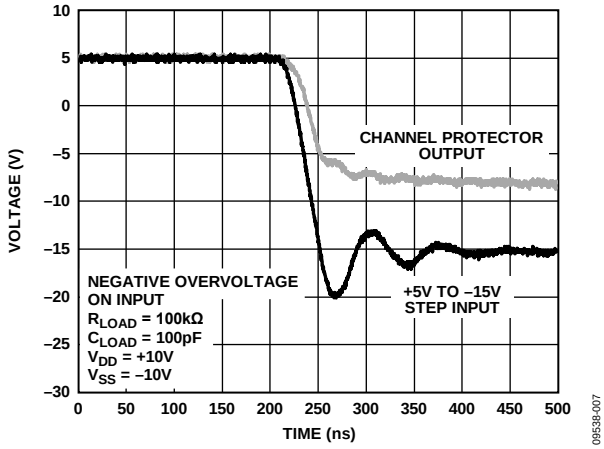

Figure 8. Negative Overvoltage Transience Response

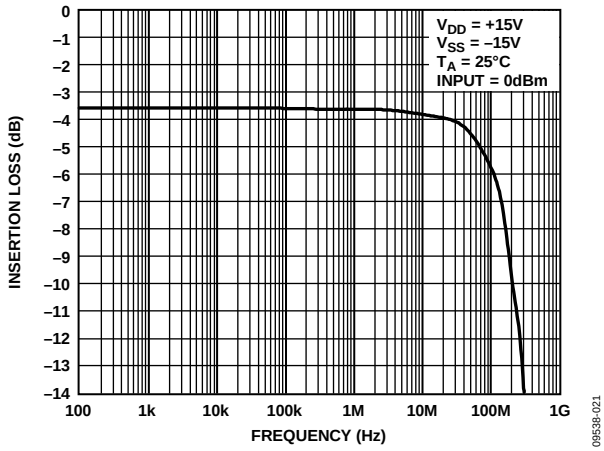

Figure 9. Frequency Response (Magnitude)

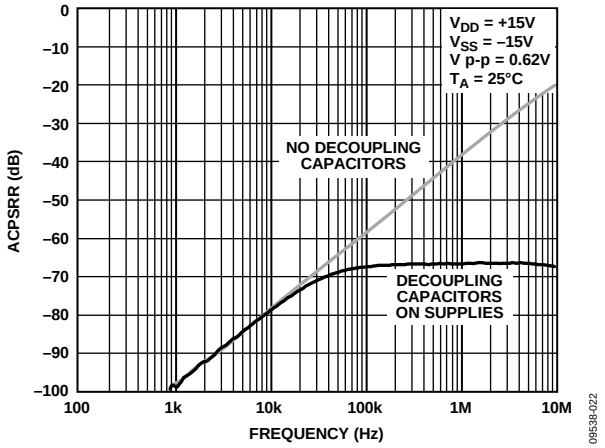

Figure 10. AC Power Supply Rejection Ratio (ACPSRR) vs. Frequency, ±15 V Dual Supply

TEST CIRCUITS

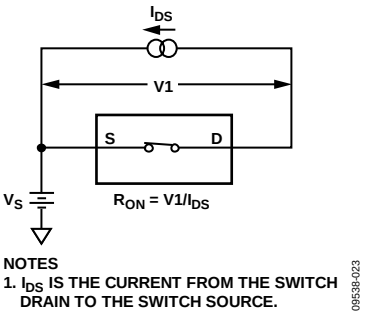

Figure 11. On Resistance

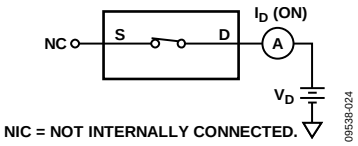

Figure 12. On Leakage

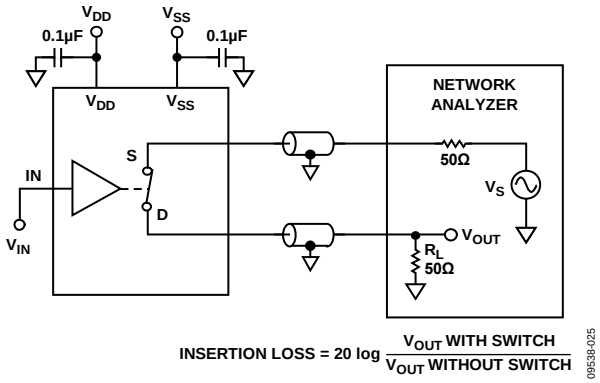

Figure 13. Bandwidth

THEORY OF OPERATION

Figure 14 shows a simplified schematic of a channel protector circuit. The circuit is comprised of four metal-oxide semiconductor (MOS) transistors: two negative metal-oxide semiconductor (NMOS) and two positive metal-oxide semiconductor (PMOS). One of the PMOS devices does not lie directly in the signal path; however, it connects the source of the second PMOS device to its back gate, which has the effect of lowering the threshold voltage and increasing the input signal range of the channel for normal operation. The source and back gate of the NMOS devices are connected for the same reason. During normal operation, the channel protectors have a resistance of 80 Ω typical. The channel protectors are low power devices; even under fault conditions, the supply current is limited to submicroampere levels. All transistors are dielectrically isolated from each other using trench isolation. Using trench isolation makes it impossible to latch up the channel protectors. For further details, see the Trench Isolation section.

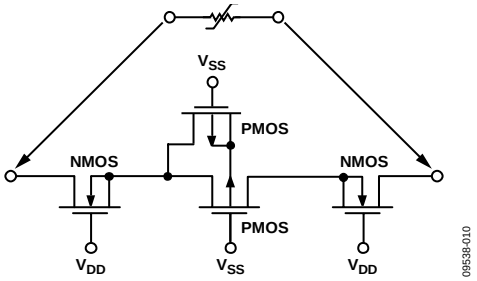

Figure 14. Channel Protector Circuit Schematic

OVERVOLTAGE PROTECTION

When a fault condition occurs on the input of a channel protector, the voltage on the input exceeds some threshold voltage set by the supply rail voltages. The threshold voltages (V_{TP} and V_{TN}) are related to the supply rails. For a positive overvoltage, the threshold voltage is given by $V_{DD} - V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistor (1.5 V typical). For a negative overvoltage, the threshold voltage is given by $V_{SS} - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (1.5 V typical). If the input voltage exceeds these threshold voltages, the output of the channel protector (with no load) is clamped at these threshold voltages. However, the channel protector output clamps at a voltage inside these thresholds if the output is loaded. For example, with an output load of 1 kΩ, V_{DD} = 15 V and a positive overvoltage. The output clamps at $V_{DD} - V_{TN} - \Delta V$ = 15 V − 1.5 V − 0.6 V = 12.9 V, where ΔV is due to IR voltage drops across the channels of the MOS devices (see Figure 16). As shown in Figure 16, the current during fault condition is determined by the load on the output (that is, V_{CLAMP}/R_L). However, if the supplies are off, the fault current is limited to the nanoampere level.

Figure 15, Figure 18, and Figure 19 show the operating conditions of the signal path transistors during various fault conditions. Figure 15 shows how the channel protectors operate when a positive overvoltage is applied to the channel protector.

The first NMOS transistor goes into a saturated mode of operation as the voltage on its drain exceeds the gate voltage (V_{DD}) − the threshold voltage, V_{TN} (see Figure 16). The potential at the source of the NMOS device is equal to $V_{DD} - V_{TN}$. The other MOS devices are in a nonsaturated mode of operation.

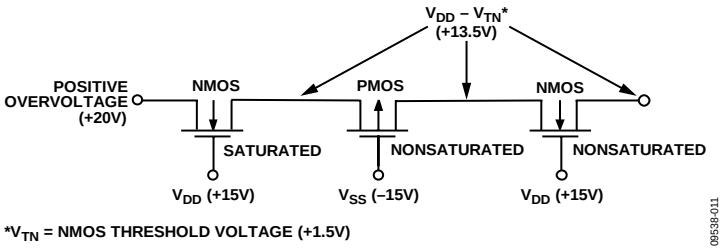

Figure 15. Positive Overvoltage on the Channel Protector

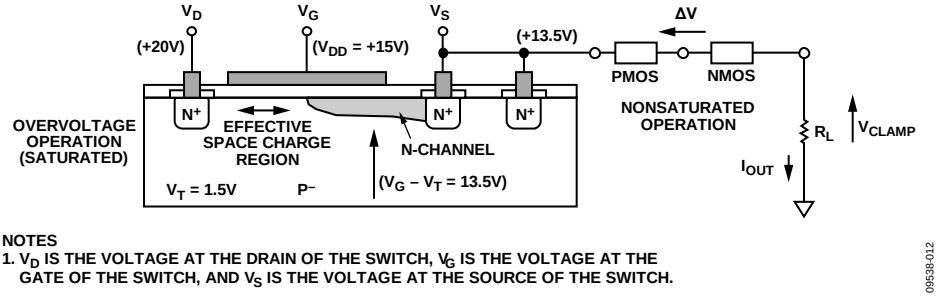

Figure 16. Negative Overvoltage Operation on the Channel Protector

When a negative overvoltage is applied to the channel protector circuit, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds $V_{SS} - V_{TP}$ (see Figure 18). As in the case of the positive overvoltage, the other MOS devices are in a nonsaturated mode of operation.

The channel protector is also functional when the supply rails are down (for example, power failure) or momentarily unconnected (for example, rack system). The channel protector is in the off high impedance state with no supply rail voltage applied, this known power supply state is where the channel protector has an advantage over more conventional protection methods, such as diode clamping (see the Applications Information section). When V_{DD} and V_{SS} equal 0 V, all transistors are off, and the current is limited to microampere levels (see Figure 19).

TRENCH ISOLATION

The MOS devices that make up the channel protector are isolated from each other by an oxide layer (trench, see Figure 17). When the NMOS and PMOS devices are not electrically isolated from each other, there is a latch-up possibility caused by parasitic junctions between complementary metal-oxide semiconductor (CMOS) transistors. Latch up is caused when PN junctions that are normally reverse biased become forward biased, causing large currents to flow, which can be destructive.

CMOS devices are normally isolated from each other by junction isolation. In junction isolation, the N and P wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. Two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch up. With trench isolation, this diode is removed, resulting in a latch-up proof circuit.

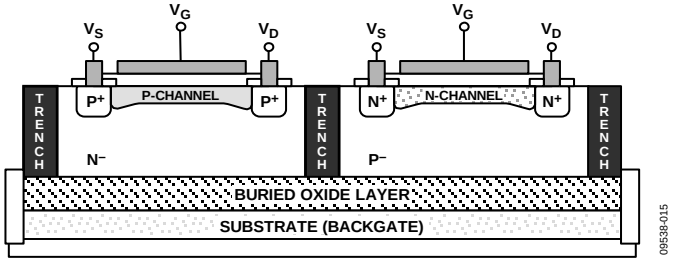

Figure 17. Trench Isolation

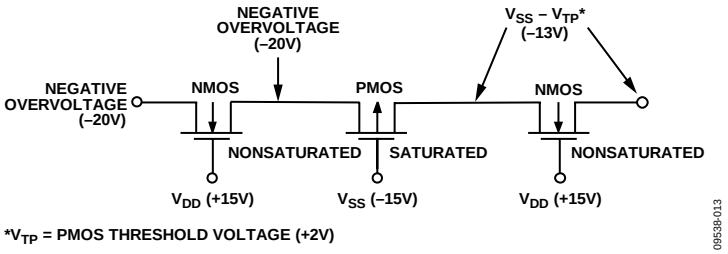

Figure 18. Negative Overvoltage on the Channel Protector

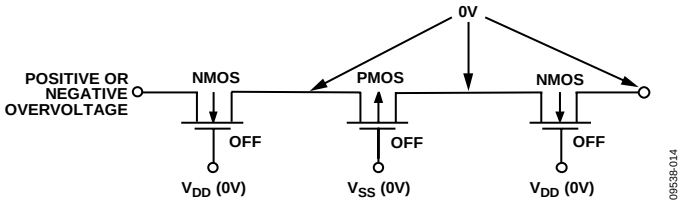

Figure 19. Channel Protector Supplies Equal to 0 V

APPLICATIONS INFORMATION

OVERVOLTAGE AND POWER SUPPLY SEQUENCING PROTECTION

The ADG465 is ideal for use in applications where input overvoltage protection is required and correct power supply sequencing cannot always be guaranteed. The overvoltage protection ensures that the output voltage of the channel protector does not exceed the threshold voltages set by the supplies (see the Theory of Operation section) when there is an overvoltage on the input. When the input voltage does not exceed these threshold voltages, the channel protector behaves like a series resistor (80 Ω typical). The resistance of the channel protector does vary slightly with operating conditions (see the Typical Performance Characteristics section).

When a voltage is not applied to V_{DD} and V_{SS}, the channel protector is in an off state and presents high impedance, which is particularly useful when considering power sequencing and protection of downstream circuitry during a system power up. When there is no voltage applied to the supply rails, all transistors in the channel protector are off, and the only currents that flow are leakage currents, which are at the microampere levels.

Figure 20 shows a typical application requiring overvoltage and power supply sequencing protection. The application shows a hot insertion rack system that involves plugging a circuit board or module into a live rack via an edge connector. In this type of application, it is not possible to guarantee correct power supply sequencing. Power supplies must be connected prior to any external signals for correct power supply sequencing. Incorrect power sequencing can cause a CMOS device to latch up, which is true of most CMOS devices, regardless of the functionality (see the Trench Isolation section). Use RC networks on the supplies of the channel protector (see Figure 20) to ensure that the rest of the circuitry is powered up before the channel protectors. The outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protectors never exceed the supply rails of the board when it is disconnected, and ensure that any signals on the inputs of the CMOS devices never exceed the supplies.

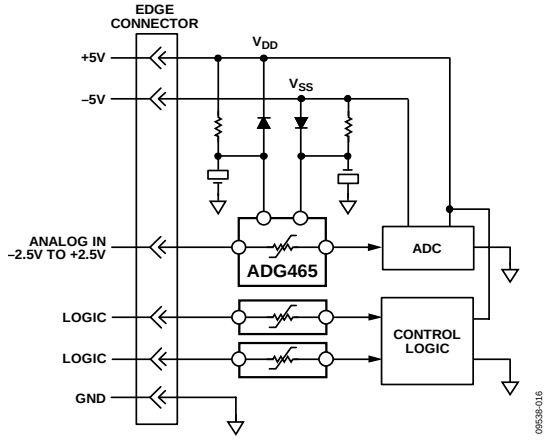

Figure 20. Overvoltage and Power Supply Sequencing Protection

HIGH VOLTAGE SURGE SUPPRESSION

The ADG465 is not intended for use in high voltage applications, such as surge suppression. The ADG465 has breakdown voltages of V_{SS} − 20 V and V_{DD} + 20 V on the inputs when the power supplies are connected. When the power supplies are disconnected, the breakdown voltages on the input of the channel protector are ±40 V. In applications where inputs are likely to be subject to overvoltages exceeding the breakdown voltages quoted for the channel protectors, use transient voltage suppressors (TVSs). These devices protect vulnerable circuits from electric overstress such as that caused by electrostatic discharge, inductive load switching, and induced lightning. However, TVSs can have a substantial standby (leakage) current (300 µA typical) at the reverse standoff voltage. The reverse standoff voltage of a TVS is the normal peak operating voltage of the circuit. In addition, TVSs offer no protection against latch up of sensitive CMOS devices when the power supplies are off. To provide the best leakage current specification and circuit protection, the best solution is to use a channel protector in conjunction with a TVS.

Figure 21 shows an input protection scheme that uses both a TVS and channel protector. The TVS is selected with a reverse standoff voltage much greater than the operating voltage of the circuit (TVSs with higher breakdown voltages tend to have better standby leakage current specifications); however, inside the breakdown voltage of the channel protector. This circuit protects the circuitry whether or not the power supplies are present.

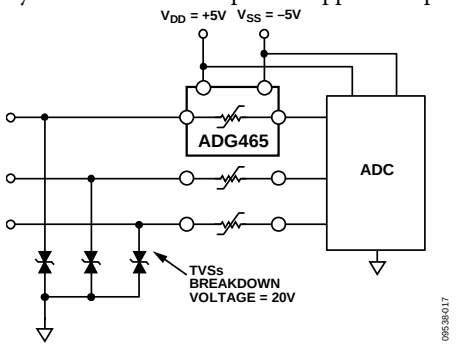

Figure 21. High Voltage Protection

OUTLINE DIMENSIONS

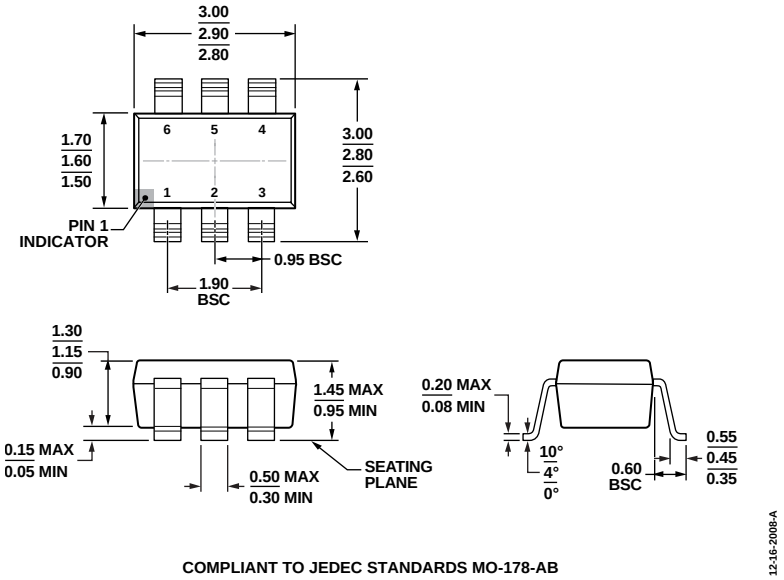

Figure 22. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

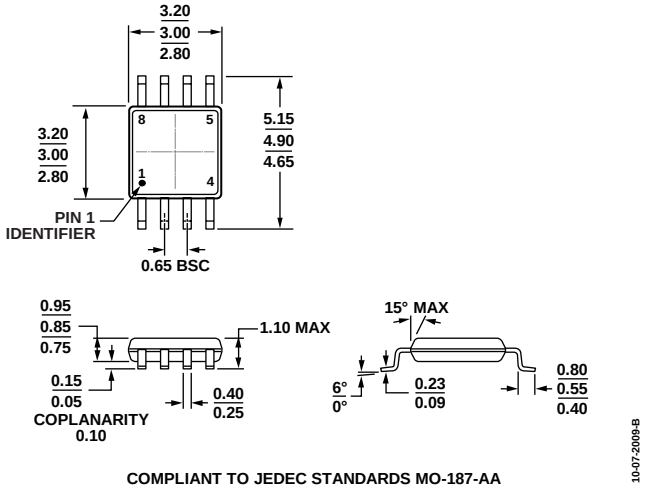

Figure 23. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Marking Code	Package Option
ADG465BRTZ-REEL7	−40°C to +85°C	6-Lead Small Outline Transistor Package [SOT-23], Reel	S1E	RJ-6
ADG465BRMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP], Reel	S1E	RM-8

[1] Z = RoHS Compliant Part.

D09538-0-8/18(C)