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REVISION HISTORY

8/2016—Rev. 0 to Rev. A

Changed CP-32-2 to CP-32-7	Throughout
Changes to Figure 4	9
Changes to Figure 6	11
Updated Outline Dimensions	21
Changes to Ordering Guide	21

10/2009—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	4.5			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	5.5	6.7	7.5	Ω max	$V_{DD} = \pm 4.5\text{ V}$, $V_{SS} = \pm 4.5\text{ V}$
On Resistance Match Between Channels (ΔR_{ON})	0.2			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.8	0.9	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.1			Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	1.4	1.7	2	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	±0.02			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	±0.15	±0.5	±3	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	±0.05			nA typ	
	±0.2	±3	±25	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27
Channel On Leakage, I_D , I_S (On)	±0.1			nA typ	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 28
	±0.3	±3	±25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.003			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, $t_{TRANSITION}$	175			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	214	247	275	ns max	$V_S = 2.5\text{ V}$; see Figure 29
t_{ON} (EN)	132			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	162	180	188	ns max	$V_S = 2.5\text{ V}$; see Figure 31
t_{OFF} (EN)	124			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	153	176	202	ns max	$V_S = 2.5\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	42			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			15	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$; see Figure 30
Charge Injection	27			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33
Channel-to-Channel Crosstalk	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	$R_L = 110\ \Omega$, 5 V p-p, $f = 20\text{ Hz}$ to 20 kHz ; see Figure 36
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34
ADG1606	21			MHz typ	
ADG1607	37			MHz typ	
C_S (Off)	18			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG1606	248			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG1607	123			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)					
ADG1606	271			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG1607	146			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
			1.0	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}			±3.3/±8	V min/max	

¹ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	4			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	5	6.2	7	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels (ΔR_{ON})	0.2			Ω typ	$V_S = 10\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.8	0.9	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1.3	1.6	1.9	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02			nA typ	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.15	± 0.5	± 3	nA max	$V_S = 1\text{ V/10 V}$, $V_D = 10\text{ V/1 V}$; see Figure 27
Drain Off Leakage, I_D (Off)	± 0.05			nA typ	$V_S = 1\text{ V/10 V}$, $V_D = 10\text{ V/1 V}$; see Figure 27
ADG1606	± 0.2	± 3	± 25	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 28
	± 0.3	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	± 0.003			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	143			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	170	198	221	ns max	$V_S = 8\text{ V}$; see Figure 29
t_{ON} (EN)	108			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	128	136	142	ns max	$V_S = 8\text{ V}$; see Figure 31
t_{OFF} (EN)	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	109	132	150	ns max	$V_S = 8\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	40			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			15	ns min	$V_{S1} = V_{S2} = 8\text{ V}$; see Figure 30
Charge Injection	33			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33
Channel-to-Channel Crosstalk	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.04			% typ	$R_L = 110\ \Omega$, 5 V p-p , $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 36
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34
ADG1606	22			MHz typ	
ADG1607	38			MHz typ	
C_S (Off)	18			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG1606	240			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
ADG1607	120			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)					
ADG1606	263			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
ADG1607	143			pF typ	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 12\text{ V}$
			1.0	μA max	Digital inputs = 0 V or V_{DD}
ADG1606	300			μA typ	Digital inputs = 5 V
			480	μA max	
ADG1607	370			μA typ	Digital inputs = 5 V
			600	μA max	
V_{DD}			3.3/16	V min/max	

¹ Guaranteed by design, not subject to production test.

5 V SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	8.5			Ω typ	$V_S = 0\text{ V to } 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	9.5	11.5	12.5	Ω max	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels (ΔR_{ON})	0.3			Ω typ	$V_S = 0\text{ V to } 4.5\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.1	1.2	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.8			Ω typ	$V_S = 0\text{ V to } 4.5\text{ V}$, $I_S = -10\text{ mA}$
	2.4	2.7	3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = 5.5\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.15	± 0.5	± 3	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	± 0.02			nA typ	
ADG1606	± 0.2	± 3	± 25	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 27
Channel On Leakage, I_D , I_S (On)	± 0.05			nA typ	$V_S = V_D = 1\text{ V or } 4.5\text{ V}$; see Figure 28
	± 0.3	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	± 0.003			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	220			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	280	324	360	ns max	$V_S = 2.5\text{ V}$; see Figure 29
t_{ON} (EN)	160			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	202	221	234	ns max	$V_S = 2.5\text{ V}$; see Figure 31
t_{OFF} (EN)	154			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	197	232	259	ns max	$V_S = 2.5\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	45			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			15	ns min	$V_{S1} = V_{S2} = 2.5\text{ V}$; see Figure 30
Charge Injection	12			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33
Channel-to-Channel Crosstalk	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.35			% typ	$R_L = 110\ \Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$, $V_S = 3.5\text{ V p-p}$; see Figure 36
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34
ADG1606	19			MHz typ	
ADG1607	34			MHz typ	
C_S (Off)	20			pF typ	$V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG1606	270			pF typ	$V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$
ADG1607	137			pF typ	$V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)					
ADG1606	300			pF typ	$V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$
ADG1607	160			pF typ	$V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 5.5\text{ V}$
			1.0	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}			3.3/16	V min/max	

¹ Guaranteed by design, not subject to production test.

3.3 V SINGLE SUPPLY

$V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	14	14.5	15.5	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$; see Figure 26 $V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels (ΔR_{ON})	0.6	0.7	0.8	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	5	5.5	6	Ω typ	$V_S = 0\text{ V}$ to V_{DD} , $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.01			nA typ	$V_{DD} = 3.6\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.15	± 0.5	± 3	nA max	$V_S = 0.6\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/0.6\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	± 0.02			nA typ	$V_S = 0.6\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/0.6\text{ V}$; see Figure 27
ADG1606	± 0.2	± 3	± 25	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.05			nA typ	$V_S = V_D = 0.6\text{ V}$ or 3 V ; see Figure 28
	± 0.3	± 3	± 25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	± 0.003			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	353			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	482	536	575	ns max	$V_S = 1.5\text{ V}$; see Figure 29
t_{ON} (EN)	263			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	362	385	396	ns max	$V_S = 1.5\text{ V}$; see Figure 31
t_{OFF} (EN)	262			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	348	391	424	ns max	$V_S = 1.5\text{ V}$; see Figure 31
Break-Before-Make Time Delay, t_{BBM}	74			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			15	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 30
Charge Injection	6			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32
Off Isolation	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33
Channel-to-Channel Crosstalk	−62			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35
Total Harmonic Distortion + Noise (THD + N)	0.6			% typ	$R_L = 110\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 2\text{ V p-p}$; see Figure 36
−3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34
ADG1606	17			MHz typ	
ADG1607	31			MHz typ	
C_S (Off)	22			pF typ	$V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG1606	290			pF typ	$V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$
ADG1607	145			pF typ	$V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$
C_D , C_S (On)					
ADG1606	350			pF typ	$V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$
ADG1607	168			pF typ	$V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 3.6\text{ V}$
			1.0	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}			3.3/16	V min/max	

¹ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D**Table 5. ADG1606**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	259	168	105	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	357	217	122	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	273	175	108	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	378	224	122	mA maximum
$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	199	136	91	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	276	178	108	mA maximum
$V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	164	119	80	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	227	154	98	mA maximum

Table 6. ADG1607

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	192	133	91	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	266	175	108	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	203	140	91	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	280	178	108	mA maximum
$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	147	108	70	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	206	140	94	mA maximum
$V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 97.9^\circ\text{C/W}$)	122	91	56	mA maximum
LFCSP ($\theta_{JA} = 46^\circ\text{C/W}$)	168	119	84	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ²	GND − 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	1.1 A (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D ³	Data + 15%
Operating Temperature Range Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

² Overvoltages at the Ax, EN, Sx, or Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

³ See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead TSSOP	97.9	14	°C/W
32-Lead LFCSP	46		°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

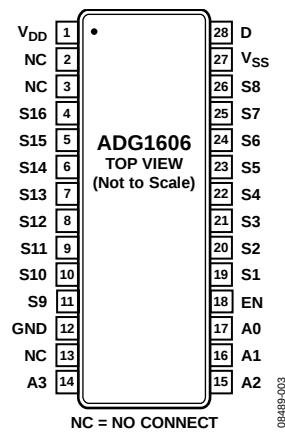
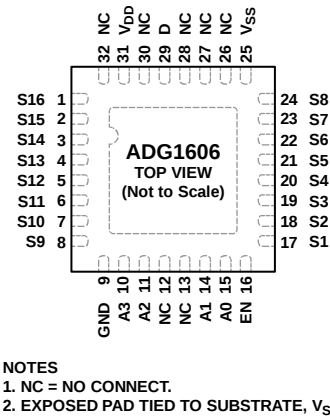


Figure 3. ADG1606 TSSOP Pin Configuration



NOTES

1. NC = NO CONNECT.
2. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .

Figure 4. ADG1606 LFCSP Pin Configuration

Table 9. ADG1606 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	31	V_{DD}	Most Positive Power Supply Potential.
2, 3, 13	12, 13, 26, 27, 28, 30, 32	NC	No Connect.
4	1	S16	Source Terminal 16. This pin can be an input or an output.
5	2	S15	Source Terminal 15. This pin can be an input or an output.
6	3	S14	Source Terminal 14. This pin can be an input or an output.
7	4	S13	Source Terminal 13. This pin can be an input or an output.
8	5	S12	Source Terminal 12. This pin can be an input or an output.
9	6	S11	Source Terminal 11. This pin can be an input or an output.
10	7	S10	Source Terminal 10. This pin can be an input or an output.
11	8	S9	Source Terminal 9. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
14	10	A3	Logic Control Input.
15	11	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1	Source Terminal 1. This pin can be an input or an output.
20	18	S2	Source Terminal 2. This pin can be an input or an output.
21	19	S3	Source Terminal 3. This pin can be an input or an output.
22	20	S4	Source Terminal 4. This pin can be an input or an output.
23	21	S5	Source Terminal 5. This pin can be an input or an output.
24	22	S6	Source Terminal 6. This pin can be an input or an output.
25	23	S7	Source Terminal 7. This pin can be an input or an output.
26	24	S8	Source Terminal 8. This pin can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	29	D	Drain Terminal. This pin can be an input or an output.
	EPAD	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS} .

Table 10. **ADG1606** Truth Table

A3	A2	A1	A0	EN	On Switch
X ¹	X ¹	X ¹	X ¹	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

¹X = don't care.

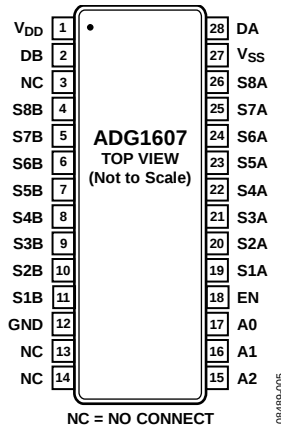
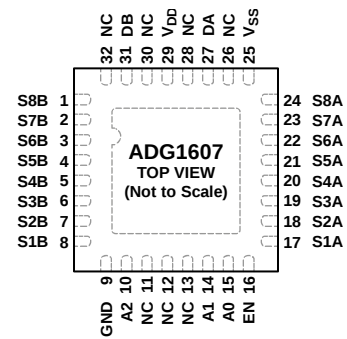


Figure 5. ADG1607 TSSOP Pin Configuration



NOTES

1. NC = NO CONNECT.
2. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .

Figure 6. ADG1607 LFCSP Pin Configuration

Table 11. ADG1607 Pin Function Descriptions

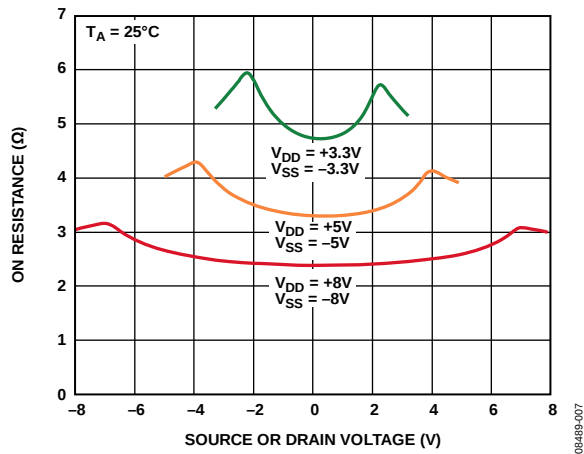
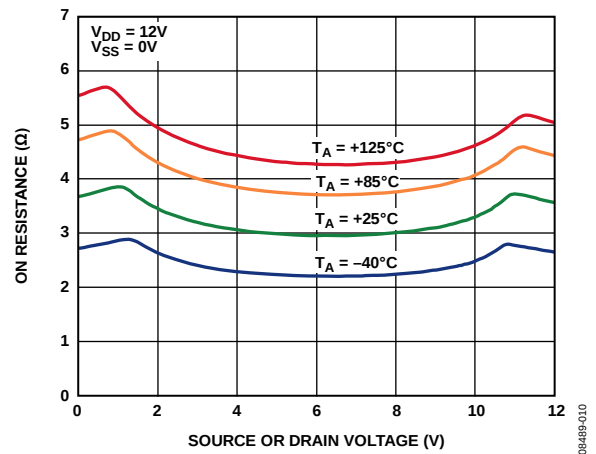
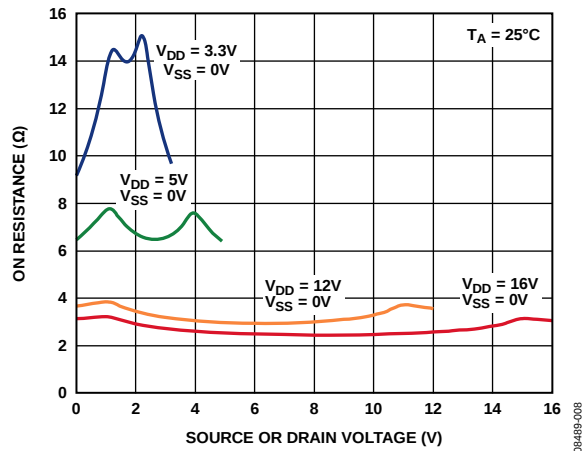
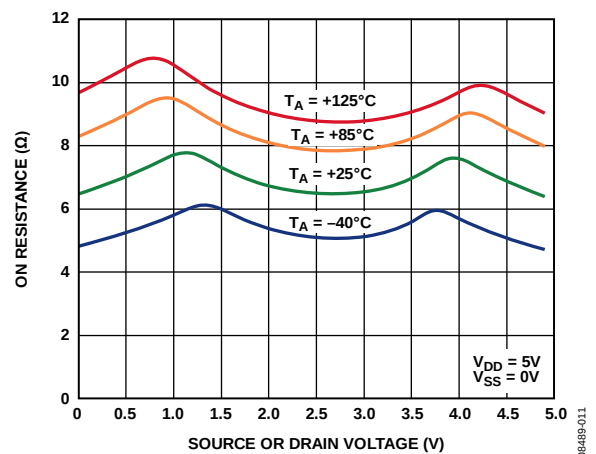
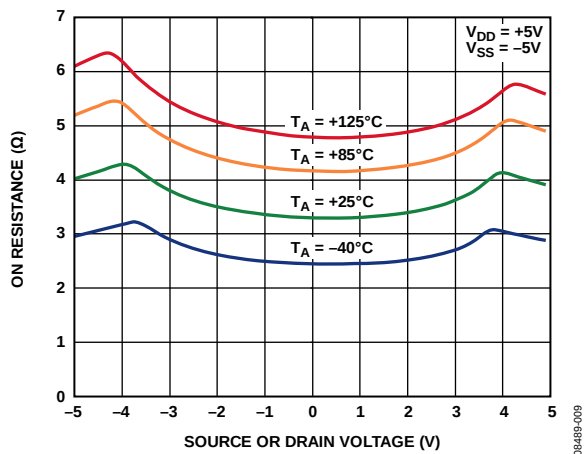
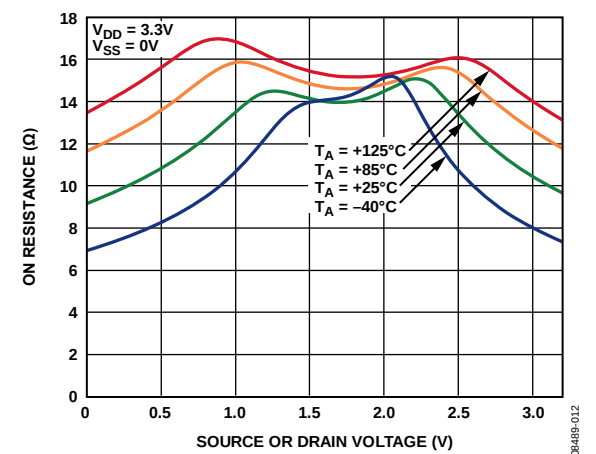
Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	29	V_{DD}	Most Positive Power Supply Potential.
2	31	DB	Drain Terminal B. This pin can be an input or an output.
3, 13, 14	11, 12, 13, 26, 28, 30, 32	NC	No Connect.
4	1	S8B	Source Terminal 8B. This pin can be an input or an output.
5	2	S7B	Source Terminal 7B. This pin can be an input or an output.
6	3	S6B	Source Terminal 6B. This pin can be an input or an output.
7	4	S5B	Source Terminal 5B. This pin can be an input or an output.
8	5	S4B	Source Terminal 4B. This pin can be an input or an output.
9	6	S3B	Source Terminal 3B. This pin can be an input or an output.
10	7	S2B	Source Terminal 2B. This pin can be an input or an output.
11	8	S1B	Source Terminal 1B. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
15	10	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1A	Source Terminal 1A. This pin can be an input or an output.
20	18	S2A	Source Terminal 2A. This pin can be an input or an output.
21	19	S3A	Source Terminal 3A. This pin can be an input or an output.
22	20	S4A	Source Terminal 4A. This pin can be an input or an output.
23	21	S5A	Source Terminal 5A. This pin can be an input or an output.
24	22	S6A	Source Terminal 6A. This pin can be an input or an output.
25	23	S7A	Source Terminal 7A. This pin can be an input or an output.
26	24	S8A	Source Terminal 8A. This pin can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	27	DA	Drain Terminal A. This pin can be an input or an output.
	EPAD	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS} .

Table 12. ADG1607 Truth Table

A2	A1	A0	EN	On Switch Pair
X ¹	X ¹	X ¹	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

¹X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 7. On Resistance as a Function of V_D (V_S) for Dual SupplyFigure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single SupplyFigure 8. On Resistance as a Function of V_D (V_S) for Single SupplyFigure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Single SupplyFigure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, ± 5 V Dual SupplyFigure 12. On Resistance as a Function of V_D (V_S) for Different Temperatures, 3.3 V Single Supply

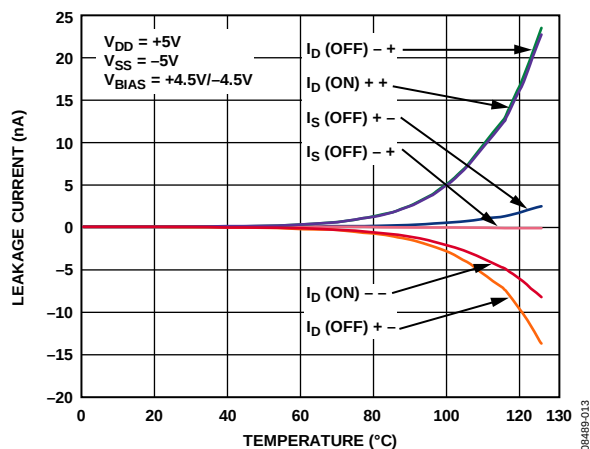


Figure 13. Leakage Currents as a Function of Temperature, ± 5 V Dual Supply

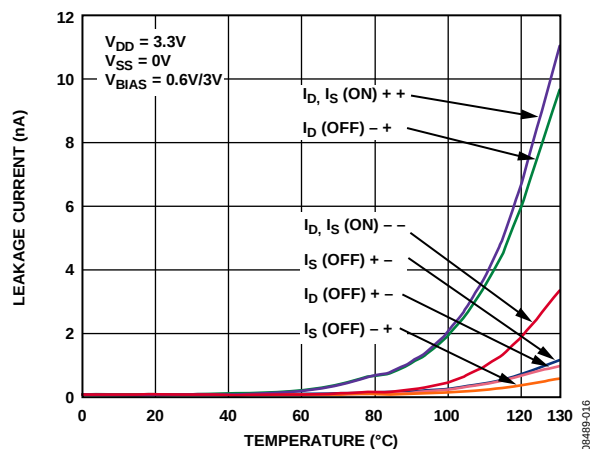


Figure 16. Leakage Currents as a Function of Temperature, 3.3 V Single Supply

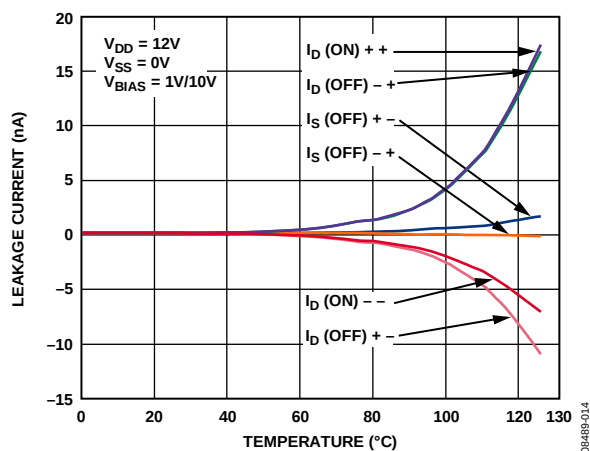


Figure 14. Leakage Currents as a Function of Temperature, 12 V Single Supply

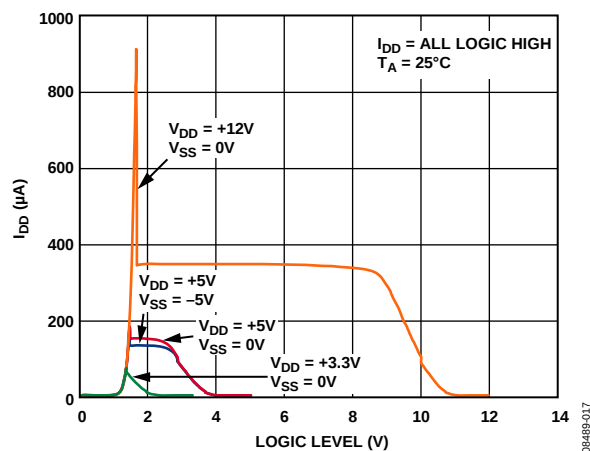


Figure 17. I_{DD} vs. Logic Level

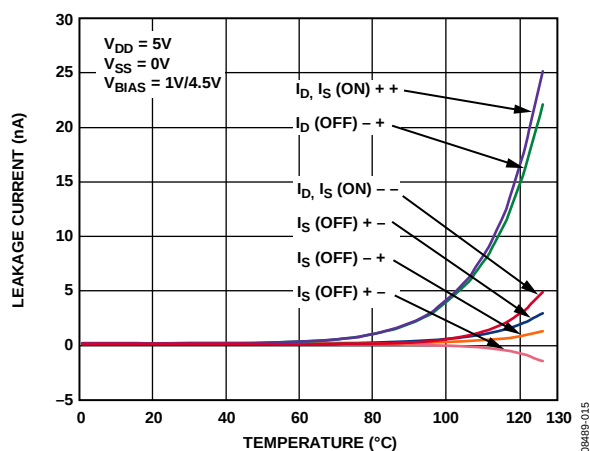


Figure 15. Leakage Currents as a Function of Temperature, 5 V Single Supply

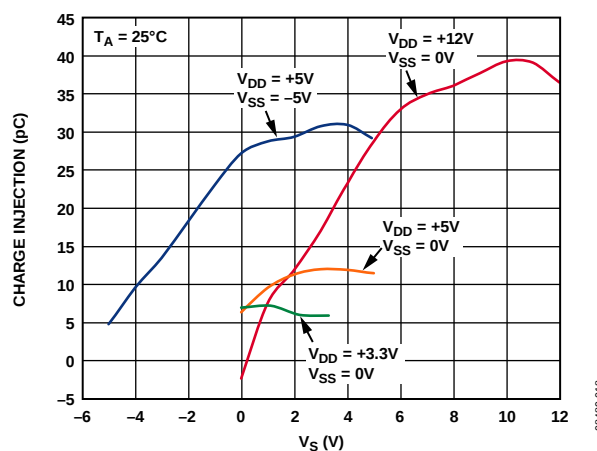


Figure 18. Charge Injection vs. Source Voltage

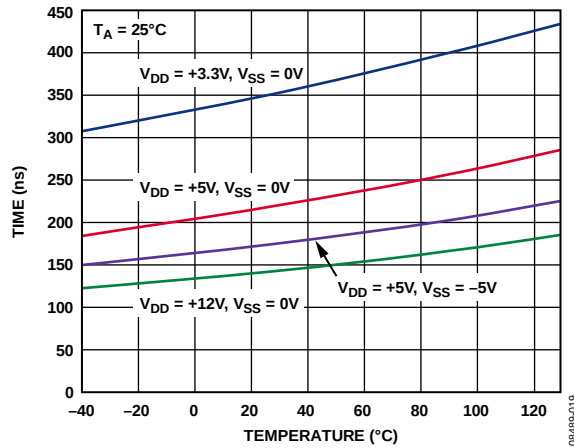


Figure 19. Transition Time vs. Temperature

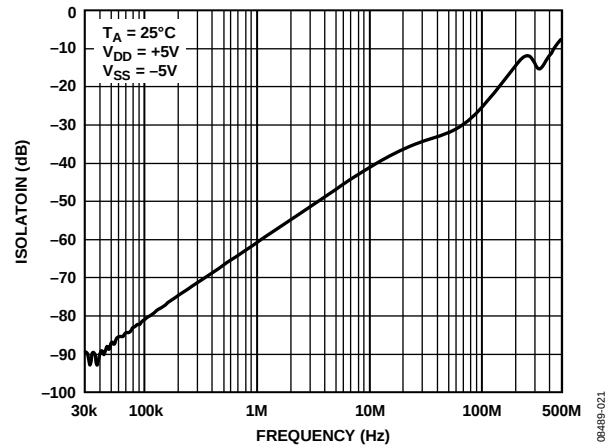


Figure 21. ADG1606 Crosstalk vs. Frequency

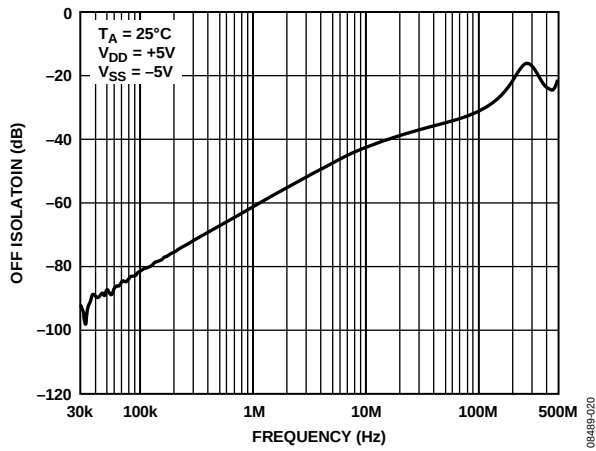


Figure 20. Off Isolation vs. Frequency

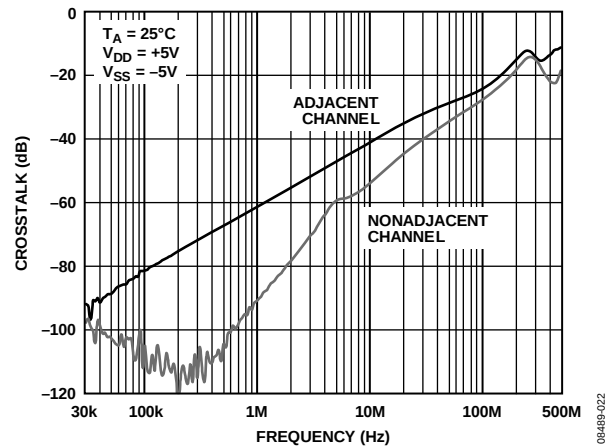


Figure 22. ADG1607 Crosstalk vs. Frequency

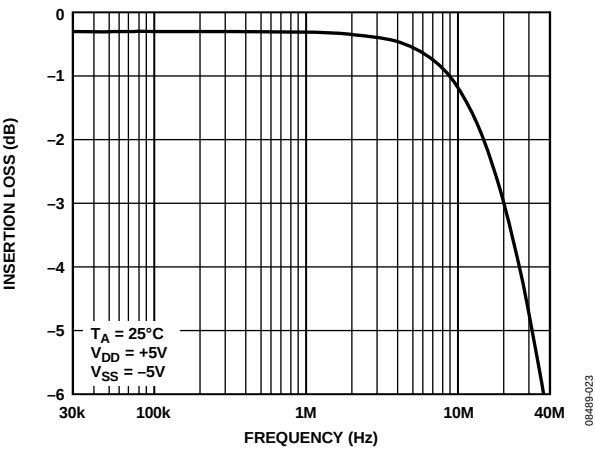


Figure 23. ADG1606 On Response vs. Frequency

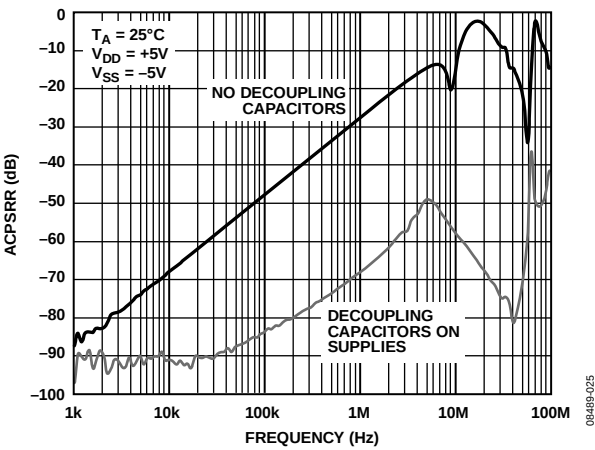


Figure 25. ACPSRR vs. Frequency

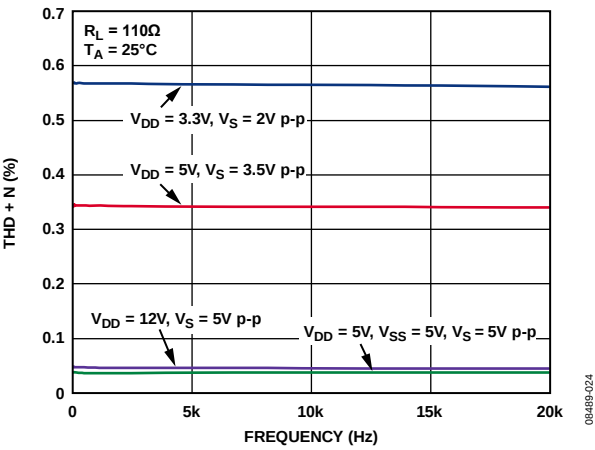


Figure 24. THD + N vs. Frequency

TEST CIRCUITS

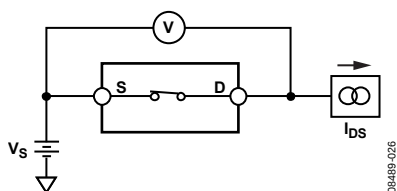


Figure 26. On Resistance

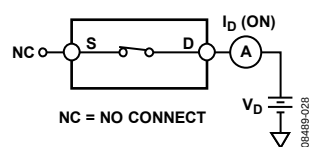


Figure 28. On Leakage

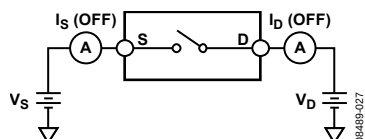
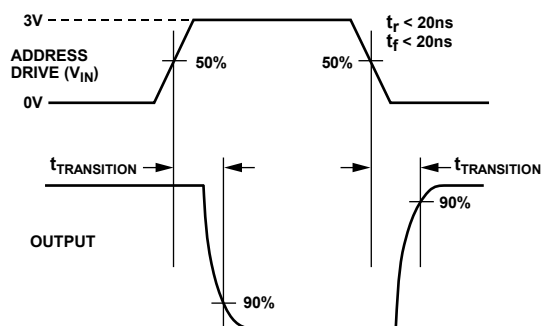
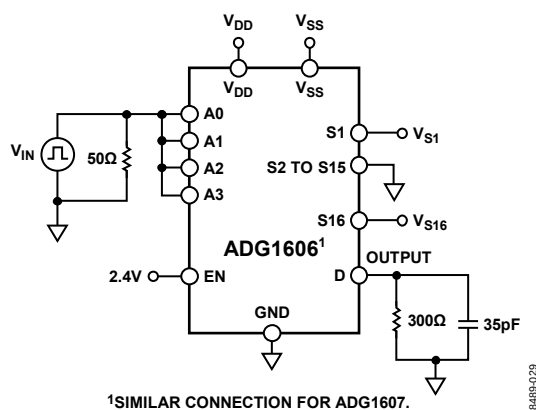
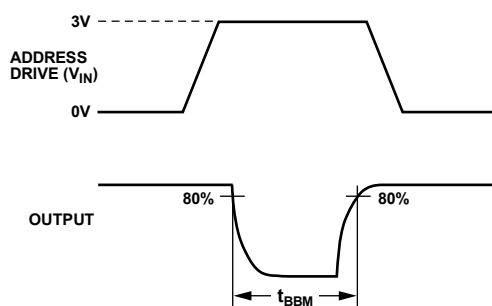
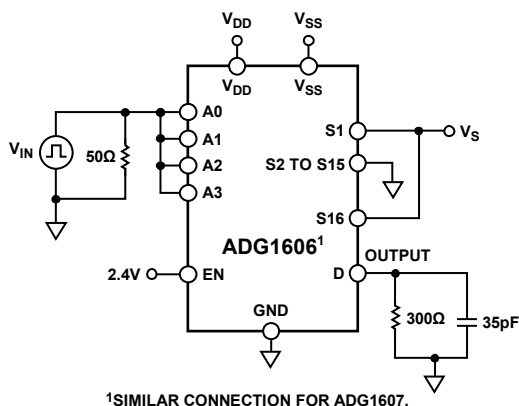


Figure 27. Off Leakage

Figure 29. Address to Output Switching Times, $t_{\text{TRANSITION}}$ ¹SIMILAR CONNECTION FOR ADG1607.Figure 30. Break-Before-Make Delay, t_{BBM} ¹SIMILAR CONNECTION FOR ADG1607.

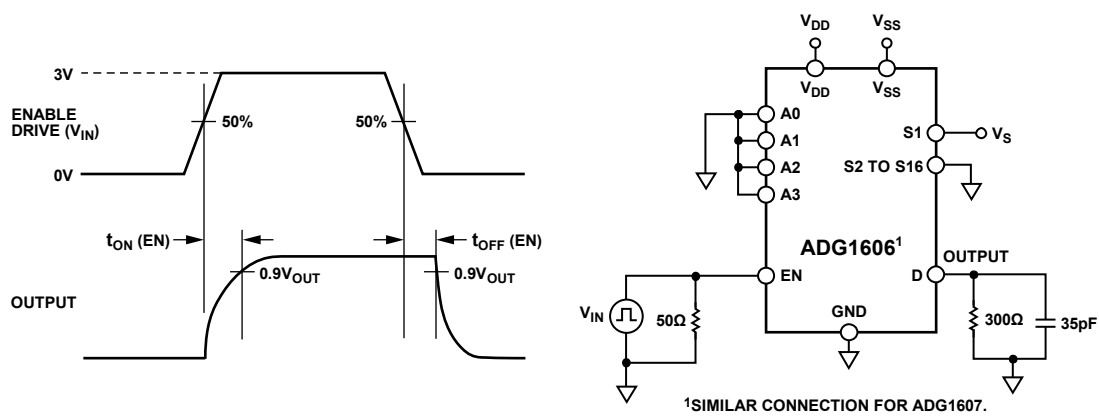


Figure 31. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

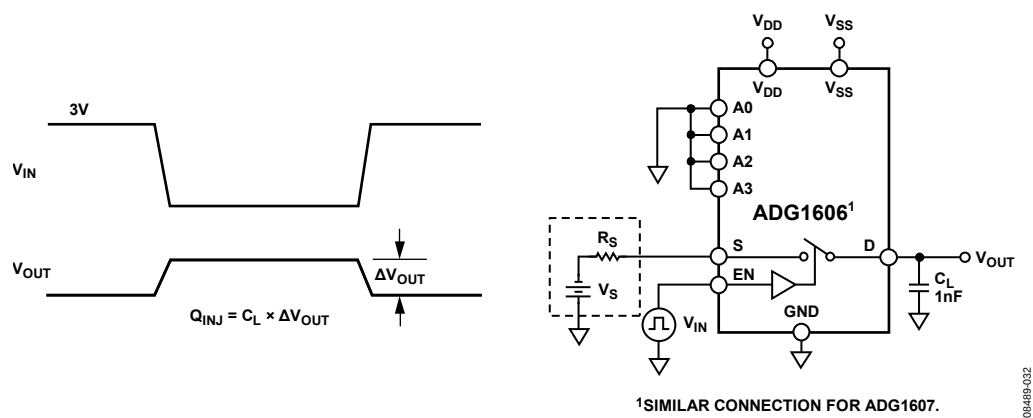


Figure 32. Charge Injection

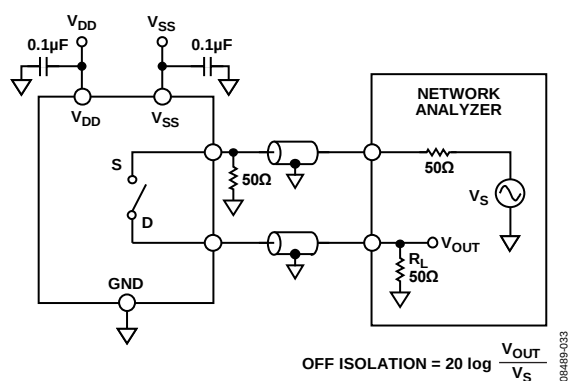


Figure 33. Off Isolation

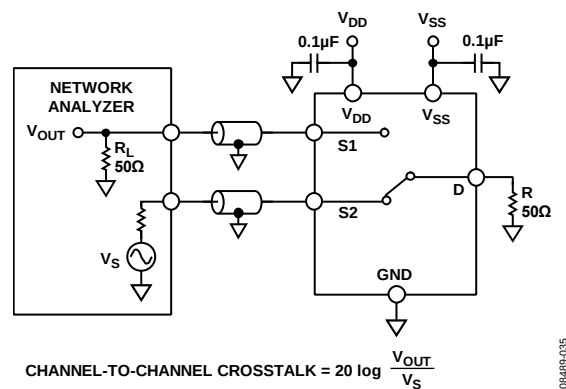


Figure 35. Channel-to-Channel Crosstalk

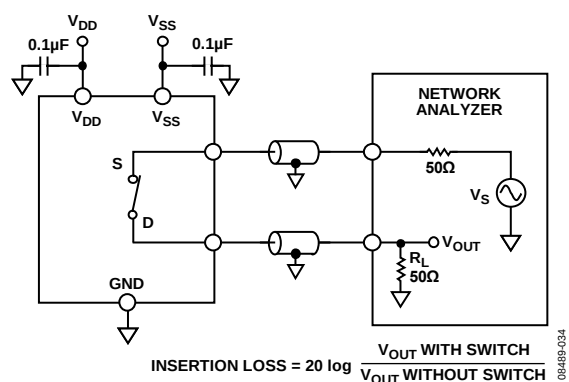


Figure 34. Bandwidth

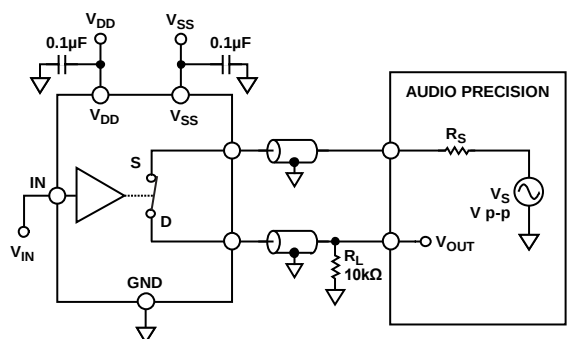


Figure 36. THD + N

TERMINOLOGY

R_{ON}

Ohmic resistance between the D and S terminals.

ΔR_{ON}

Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

C_S (Off)

Channel input capacitance for the off condition.

C_D (Off)

Channel output capacitance for the off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% points of the switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

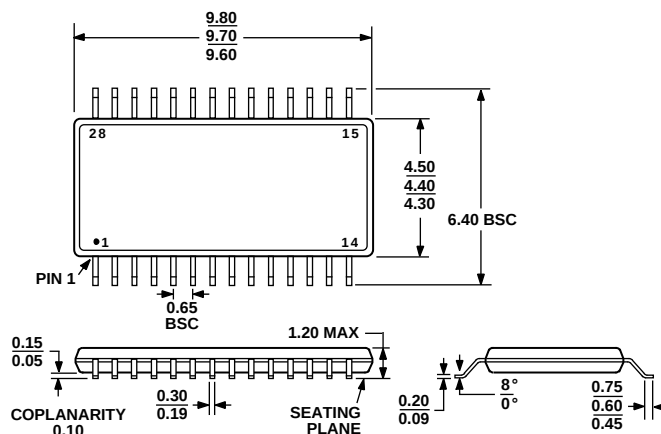
THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

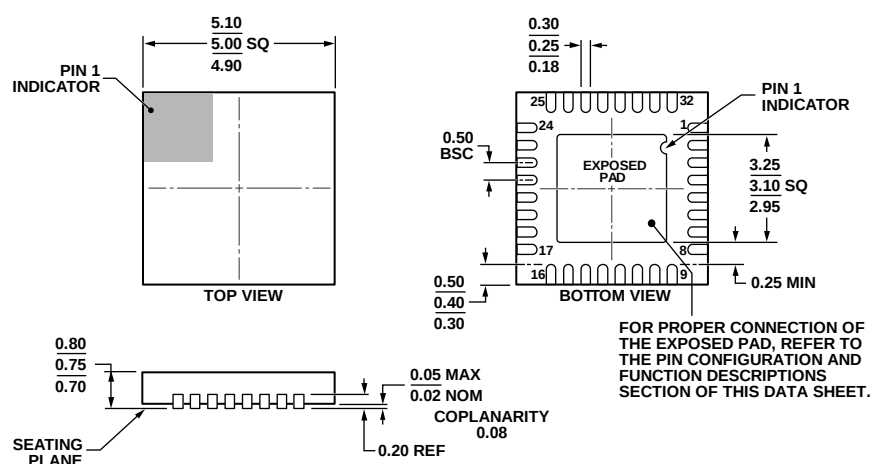
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 37. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 38. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)

Dimensions shown in millimeters

112408-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG1606BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1606BRUZ-REEL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1606BCPZ-REEL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
ADG1607BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1607BRUZ-REEL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG1607BCPZ-REEL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7

¹ Z = RoHS Compliant Part.

NOTES