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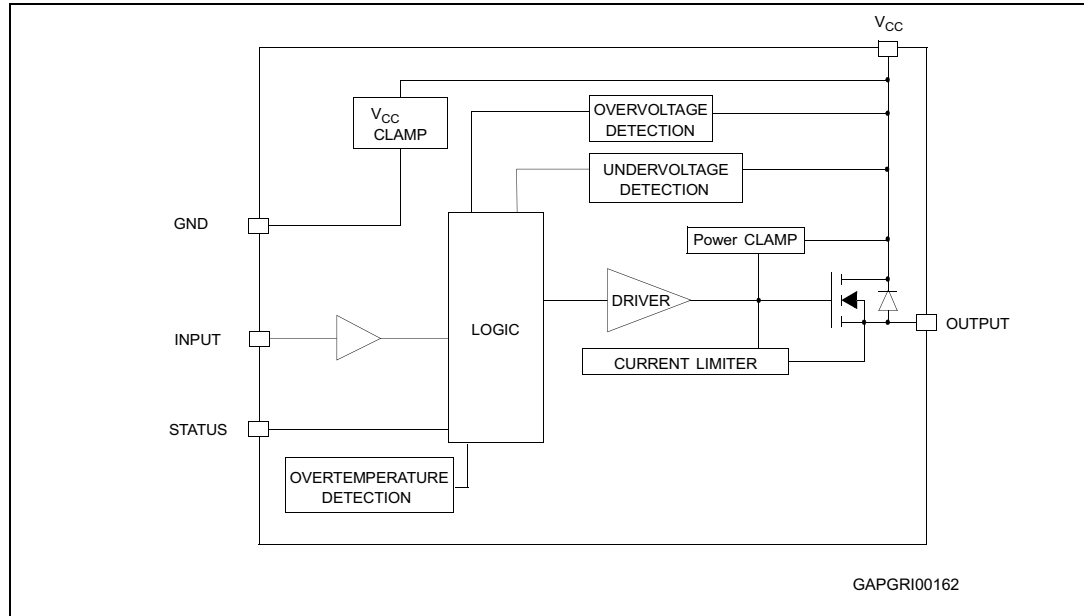
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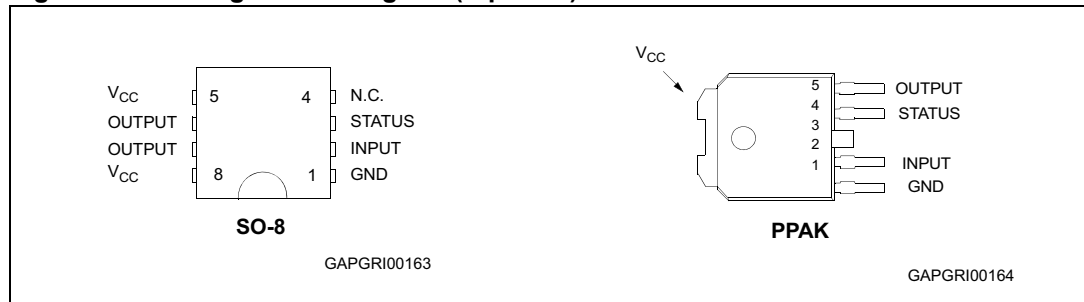
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# 1 Block diagram and pin description

**Figure 1. Block diagram**



**Figure 2. Configuration diagram (top view)**

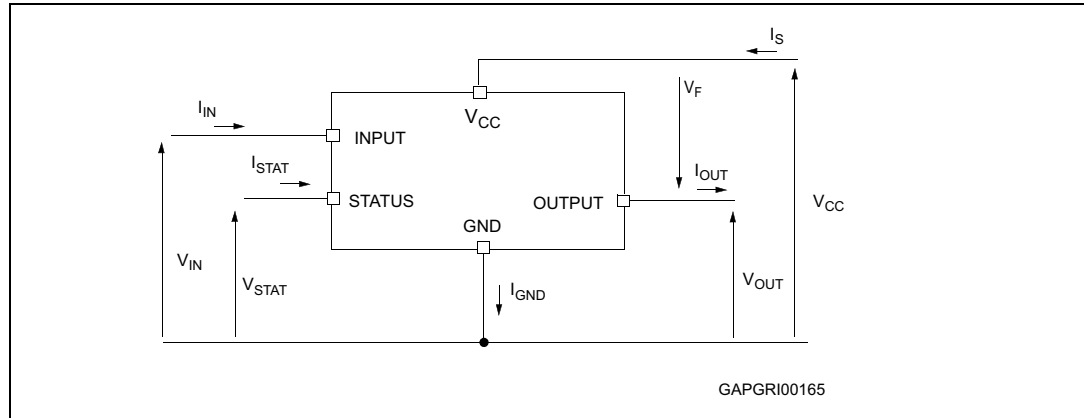


**Table 2. Suggested connections for unused and n.c. pins**

Connection / Pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To Ground		X		Through 10KΩ resistor

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
$V_{CC}$	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	- 0.3		V
$-I_{GND}$	DC reverse ground pin current	- 200		mA
$I_{OUT}$	DC output current	Internally Limited		A
$-I_{OUT}$	Reverse DC output current	- 6		A
$I_{IN}$	DC input current	+/- 10		mA
$V_{IN}$	Input voltage range	$-3/+V_{CC}$		V
$V_{STAT}$	DC Status voltage	$+V_{CC}$		V
$V_{ESD}$	Electrostatic discharge (human body model: $R=1.5KW$ ; $C=100pF$ )			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	$-V_{CC}$	5000		V

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
$P_{tot}$	Power dissipation $T_C=25^\circ\text{C}$	4.2	41.7	W
$E_{MAX}$	Maximum switching energy ( $L=77.5\text{mH}$ ; $R_L=0\Omega$ ; $V_{bat}=13.5\text{V}$ ; $T_{jstart}=150^\circ\text{C}$ ; $I_L=1.5\text{A}$ )	121		mJ
$E_{MAX}$	Maximum switching energy ( $L=125\text{mH}$ ; $R_L=0\Omega$ ; $V_{bat}=13.5\text{V}$ ; $T_{jstart}=150^\circ\text{C}$ ; $I_L=1.5\text{A}$ )		195	mJ
$T_j$	Junction operating temperature	Internally limited		$^\circ\text{C}$
$T_C$	Case operating temperature	- 40 to 150		$^\circ\text{C}$
$T_{stg}$	Storage temperature	- 55 to 150		$^\circ\text{C}$
$L_{max}$	Max inductive load ( $V_{CC}=30\text{ V}$ ; $I_{LOAD}=0.5\text{ A}$ ; $T_{amb}=100^\circ\text{C}$ ; $R_{th_{case>ambient}}\leq 25^\circ\text{C/W}$ )		2	H

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter		Value		Unit
			SO-8	PPAK	
$R_{thj-case}$	Thermal resistance junction-case	Max	-	3	$^\circ\text{C/W}$
$R_{thj-lead}$	Thermal resistance junction-lead	Max	30	-	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	Max	93 <sup>(1)</sup>	78 <sup>(2)</sup>	$^\circ\text{C/W}$
		Max	82 <sup>(3)</sup>	45 <sup>(4)</sup>	$^\circ\text{C/W}$

1. When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area (at least 35m thick) connected to all  $V_{CC}$  pins
2. When mounted on FR4 printed circuit board with 2 cm<sup>2</sup> of copper area (at least 35m thick).
3. When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area (at least 35m thick) connected to all  $V_{CC}$  pins.
4. When mounted on FR4 printed circuit board with 6 cm<sup>2</sup> of copper area (at least 35m thick).

## 2.3 Electrical characteristics

Values specified in this section are for  $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$  unless otherwise specified.

**Table 5. Power**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5		36	V
$V_{USD}$	Undervoltage shut-down		3	4	5.5	V
$V_{OV}$	Overvoltage shut-down		36	42		V
$R_{ON}$	On state resistance	$I_{OUT} = 0.5A$ ; $T_j = 25^{\circ}C$ $I_{OUT} = 0.5A$			135 270	m $\Omega$ m $\Omega$
$I_S$	Supply current	Off State; $V_{CC} = 24V$ ; $T_{case} = 25^{\circ}C$ On State; $V_{CC} = 24V$ On State; $V_{CC} = 24V$ ; $T_{case} = 100^{\circ}C$		10 1.5	20 3.5 2.6	$\mu A$ mA mA
$I_{LGND}$	Output current at turn-off	$V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24V$ ; $V_{OUT} = 0V$			1	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	$\mu A$
$I_{L(off2)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$			5	$\mu A$
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$			3	$\mu A$

**Table 6. Switching ( $V_{CC} = 24 V$ )**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 48\Omega$ from $V_{IN}$ rising edge to $V_{OUT} = 2.4V$	-	10	-	$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 48\Omega$ from $V_{IN}$ falling edge to $V_{OUT} = 21.6V$	-	40	-	$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 2.4V$ to $V_{OUT} = 19.2V$	-	See <a href="#">Figure 17</a>	-	V/ $\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 21.6V$ to $V_{OUT} = 2.4V$	-	See <a href="#">Figure 18</a>	-	V/ $\mu s$

**Table 7. Input pin**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{INL}$	Input low level				1.25	V
$I_{INL}$	Low level input current	$V_{IN} = 1.25V$	1			$\mu A$
$V_{INH}$	Input high level		3.25			V

Table 7. Input pin (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{INH}$	High level input current	$V_{IN}=3.25V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$I_{IN}$	Input current	$V_{IN}=V_{CC}=36V$			200	$\mu A$

Table 8.  $V_{CC}$  output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT}=0.6A; T_j=150^\circ C$	-	-	0.6	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{STAT}$	Status Low Output Voltage	$I_{STAT}=1.6 mA$	-	-	0.5	V
$I_{LSTAT}$	Status Leakage Current	Normal Operation; $V_{STAT}=V_{CC}=36V$	-	-	10	$\mu A$
$C_{STAT}$	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$	-	-	30	pF

Table 10. Protections<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shut-down temperature	-	150	175	200	$^\circ C$
$T_R$	Reset temperature	-	135			$^\circ C$
$T_{hyst}$	Thermal hysteresis	-	7	15		$^\circ C$
$T_{SDL}$	Status delay in overload condition	$T_j > T_{jsh}$			20	$\mu s$
$I_{lim}$	DC short circuit current	$V_{CC}=24V; R_{LOAD}=10m\Omega$	0.7		2	A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT}=0.5 A; L=6mH$	$V_{CC}-47$	$V_{CC}-52$	$V_{CC}-57$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.



Figure 4. Status timings

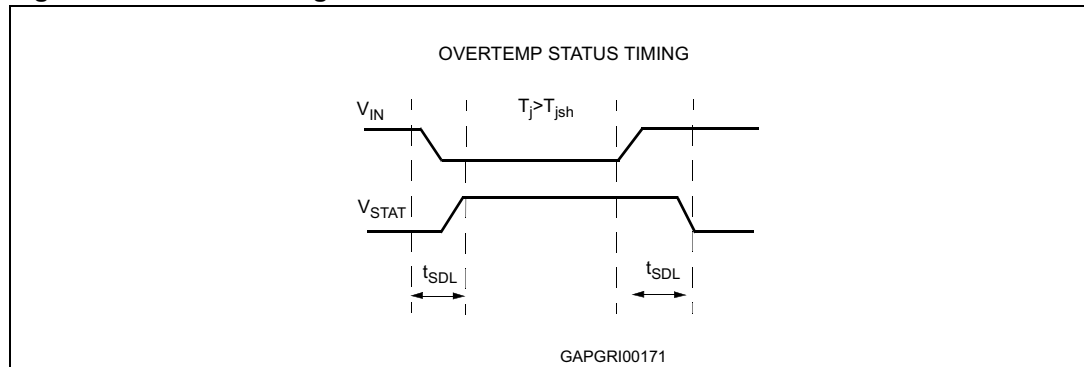


Figure 5. Switching time waveforms

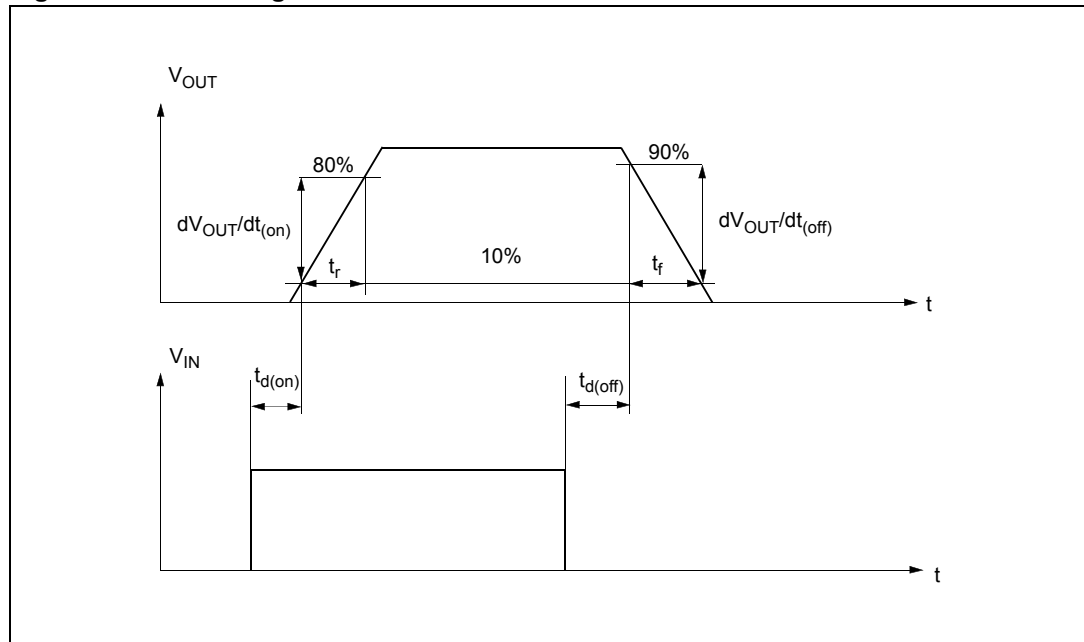


Table 11. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H $(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Table 12. Electrical transient requirements on V<sub>CC</sub> pin (part 1/3)

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Table 13. Electrical transient requirements on V<sub>CC</sub> pin (part 2/3)

ISO T/R 7637/1 Test Pulse	TEST LEVELS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 14. Electrical transient requirements on V<sub>CC</sub> pin (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Peak short circuit current test circuit

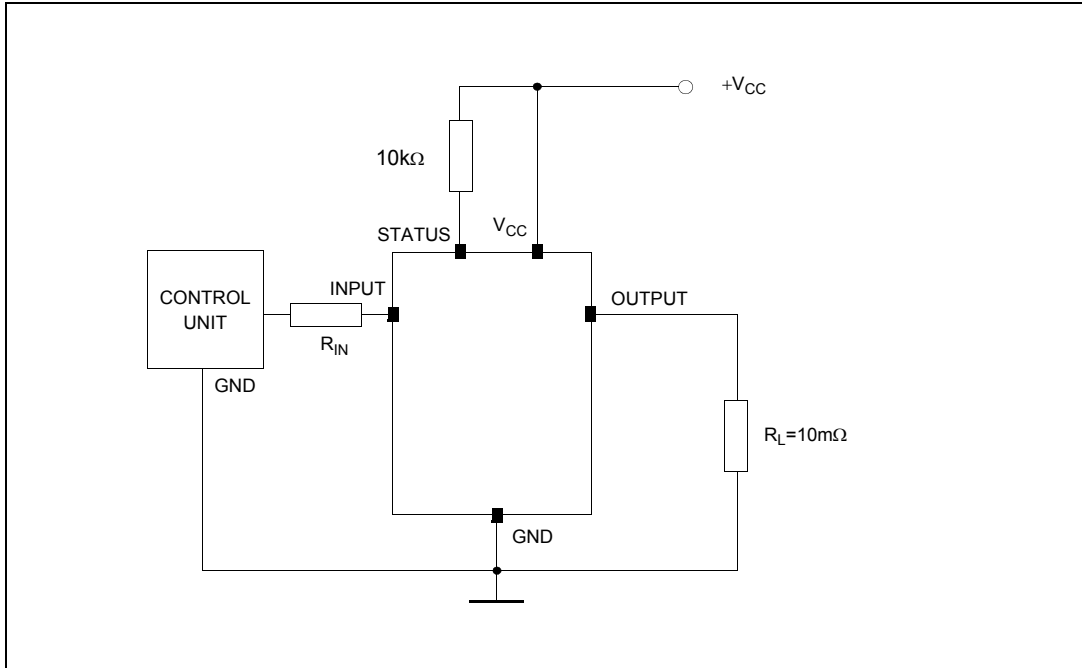


Figure 7. Avalanche energy test circuit

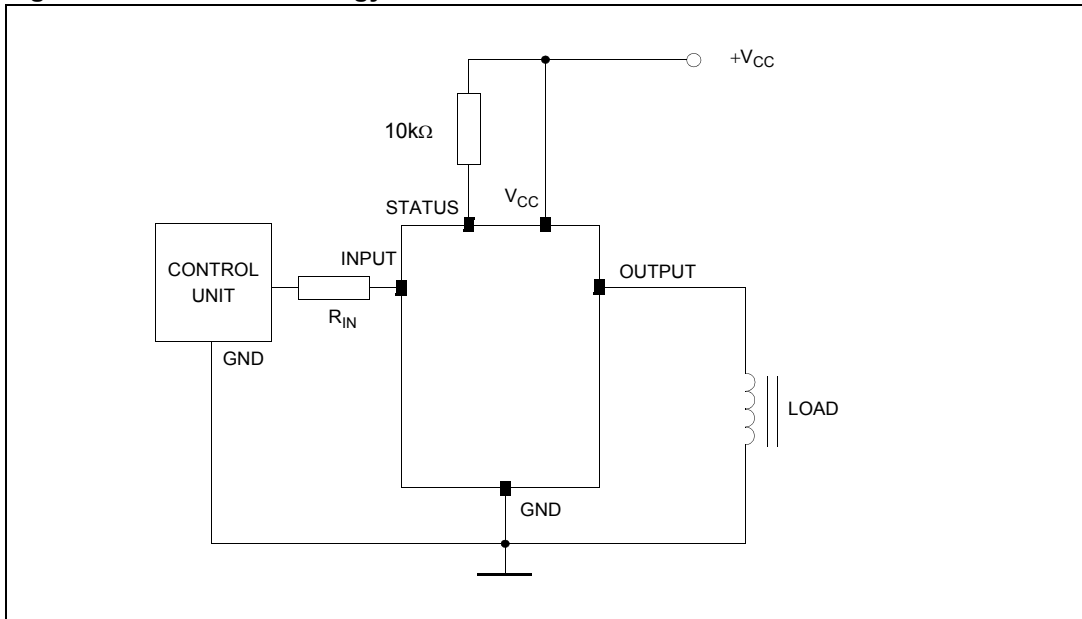
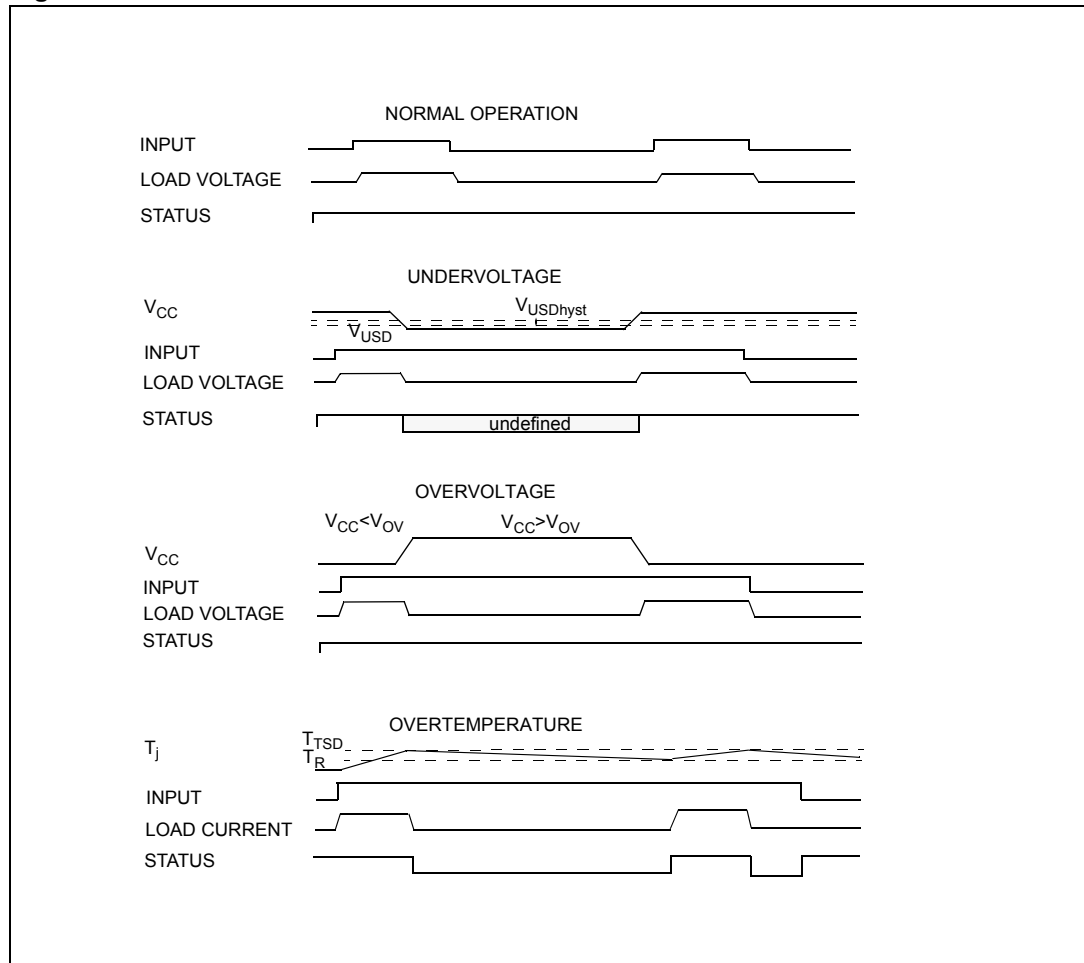
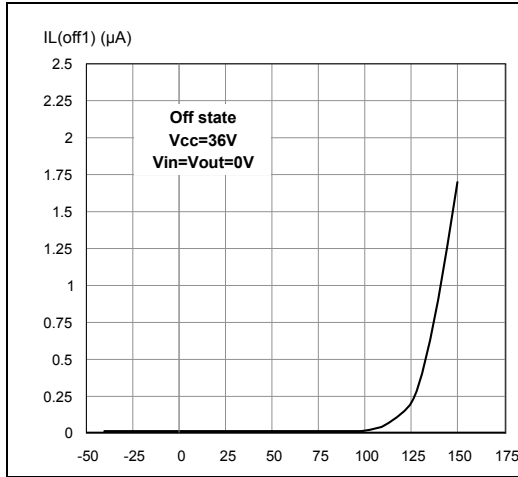


Figure 8. Waveforms

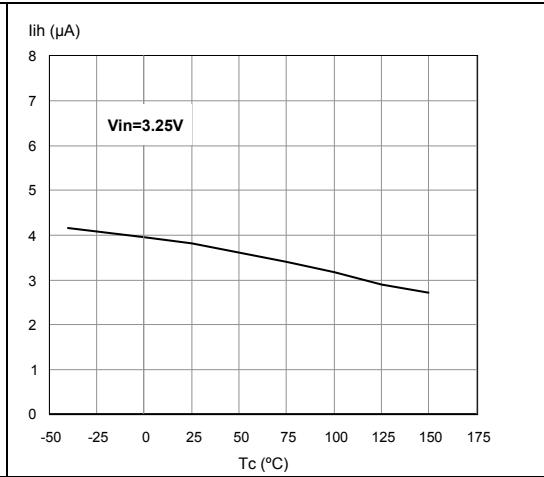


### 3 Electrical characteristics curves

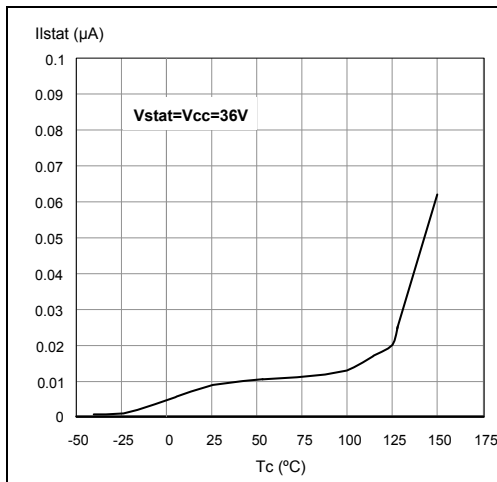
**Figure 9. Off-state output current**



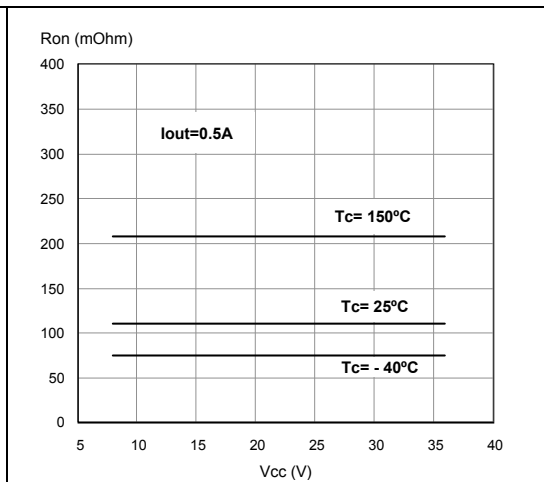
**Figure 10. High level input current**



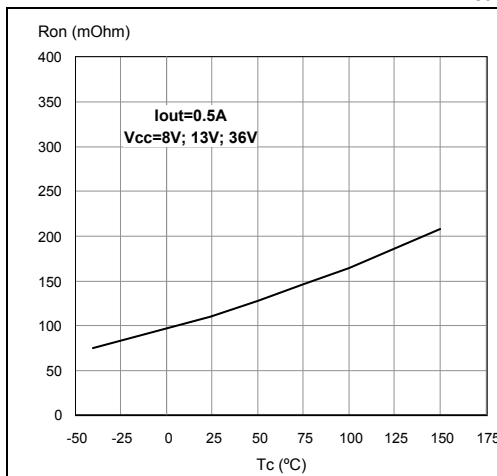
**Figure 11. Status leakage current**



**Figure 12. On state resistance vs Vcc**



**Figure 13. On-state resistance Vs T<sub>case</sub>**



**Figure 14. Input high level**

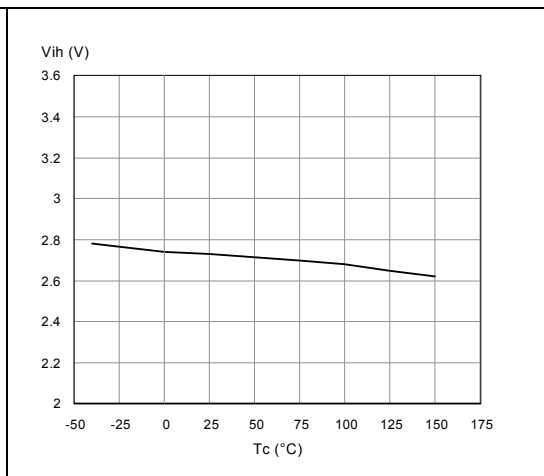


Figure 15. Input low level

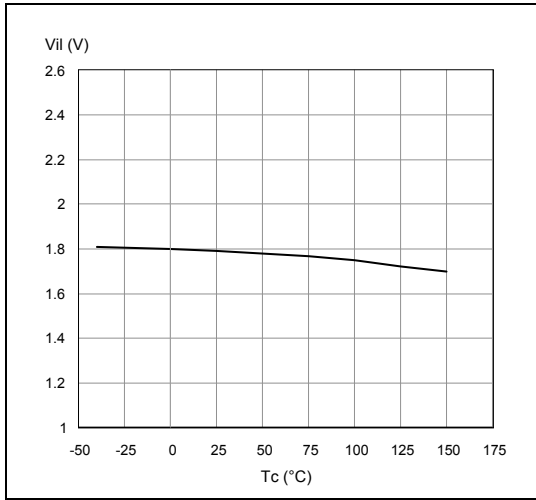


Figure 16. Input hysteresis voltage

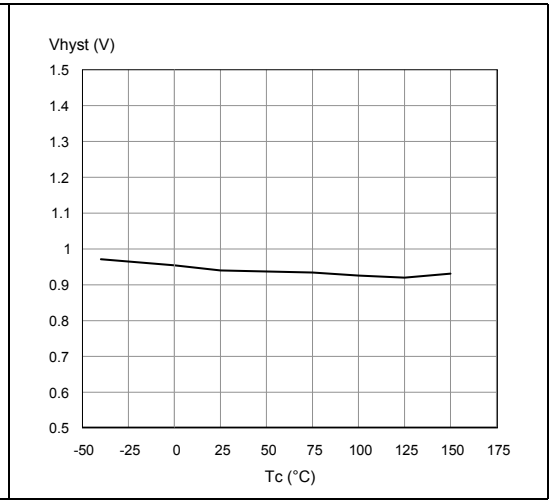


Figure 17. Turn-on voltage slope

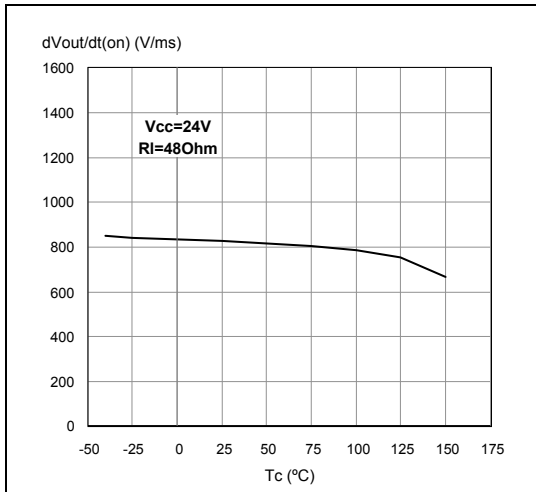


Figure 18. Turn-off voltage slope

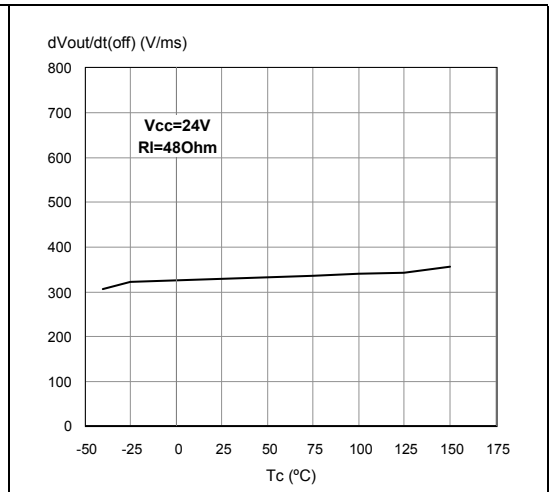


Figure 19. Overvoltage shutdown

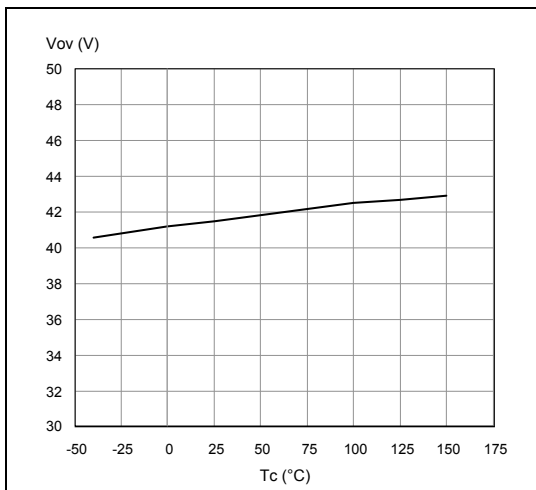
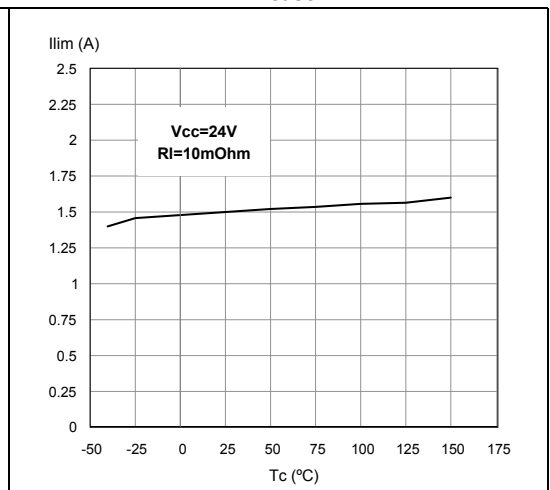
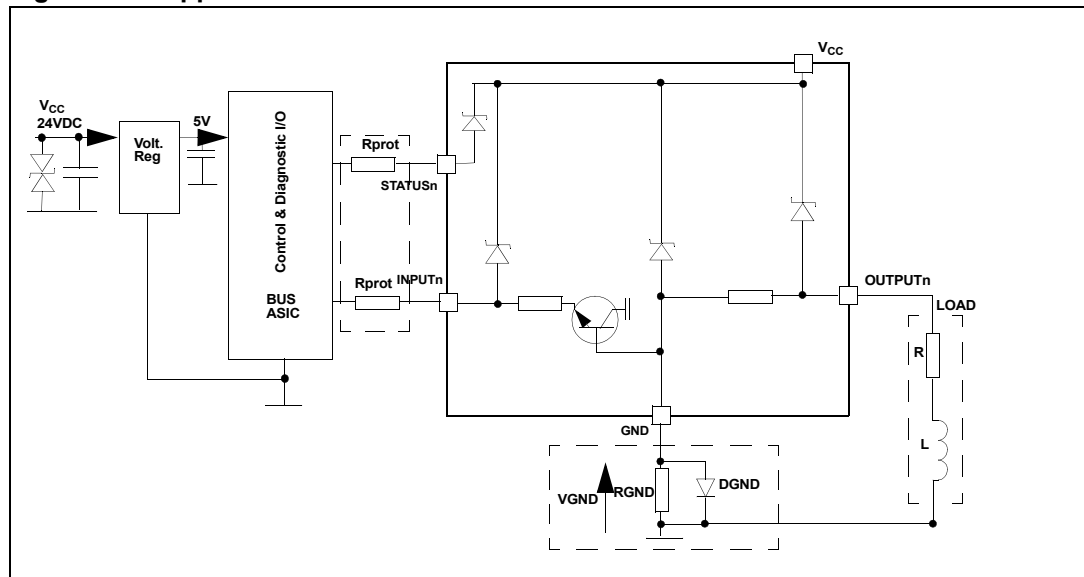


Figure 20. I<sub>LIM</sub> vs T<sub>case</sub>



### 3.1 Application information

Figure 21. Application schematic



### 3.2 GND protection network against reverse battery

#### 3.2.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only). This can be used with any type of load

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub><0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I<sub>S(on)max</sub> becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R<sub>GND</sub> will produce a shift (I<sub>S(on)max</sub> \* R<sub>GND</sub>) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize [Section 3.3](#).

### 3.3 Solution 2: a diode (DGND) in the ground line

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\pm 600mV$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

#### 3.3.1 MCU I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

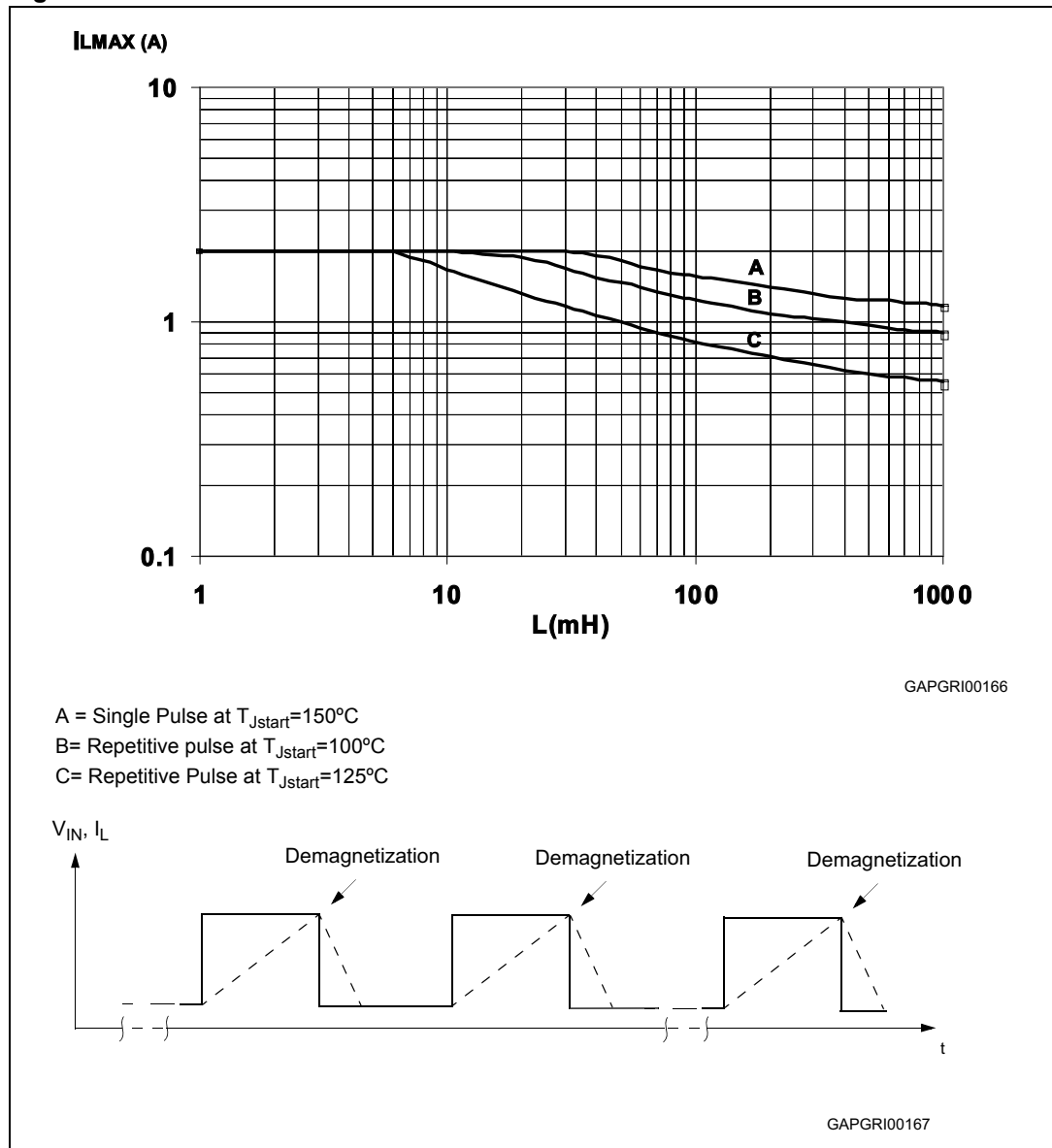
$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended  $R_{prot}$  value is  $10k\Omega$ .



### 3.4 SO-8 maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

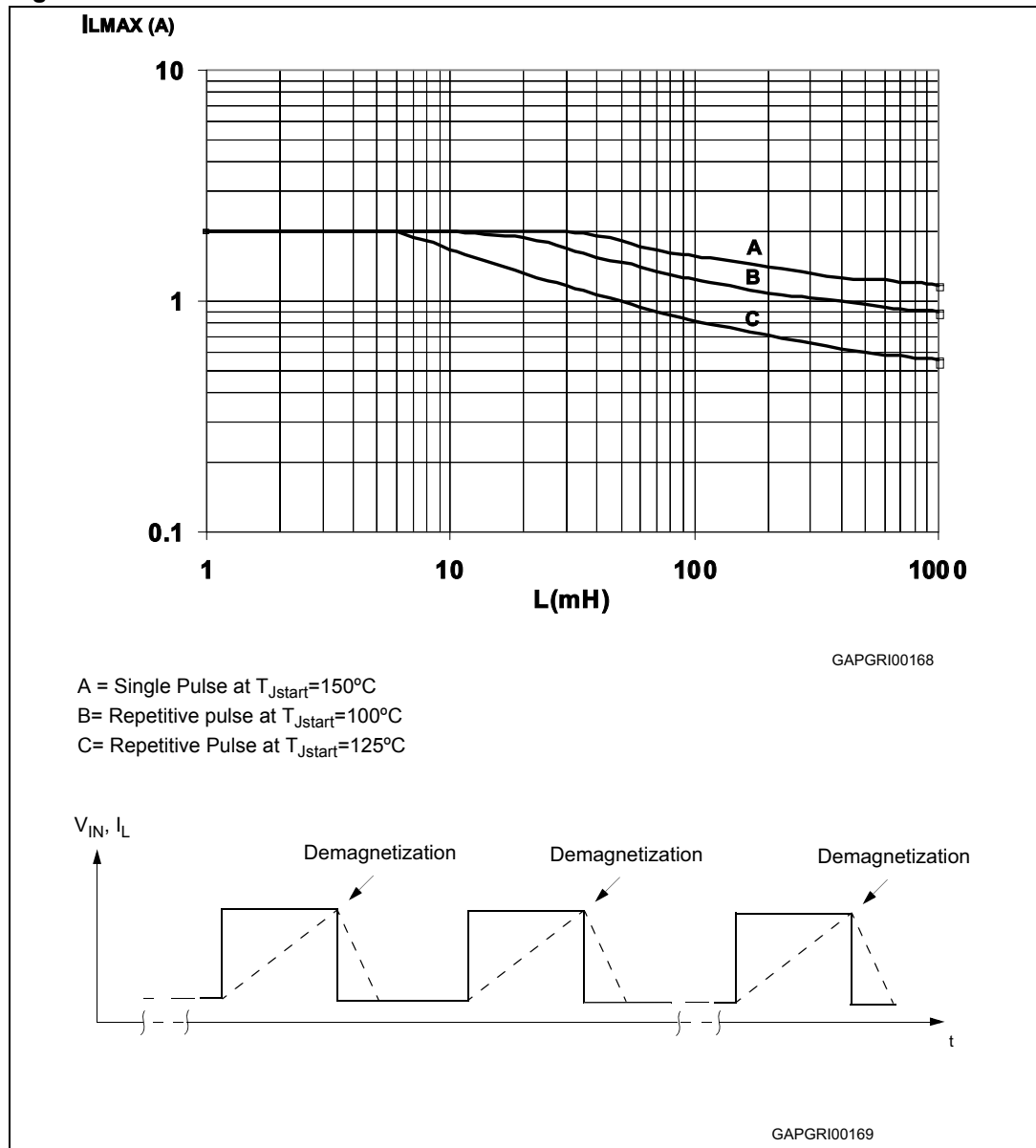
Figure 22. SO-8 Maximum turn-off current versus load inductance



Note: Values are generated with  $R_L=0\Omega$ . In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

### 3.5 PPAK maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

Figure 23. PPAK maximum turn-off current versus load inductance

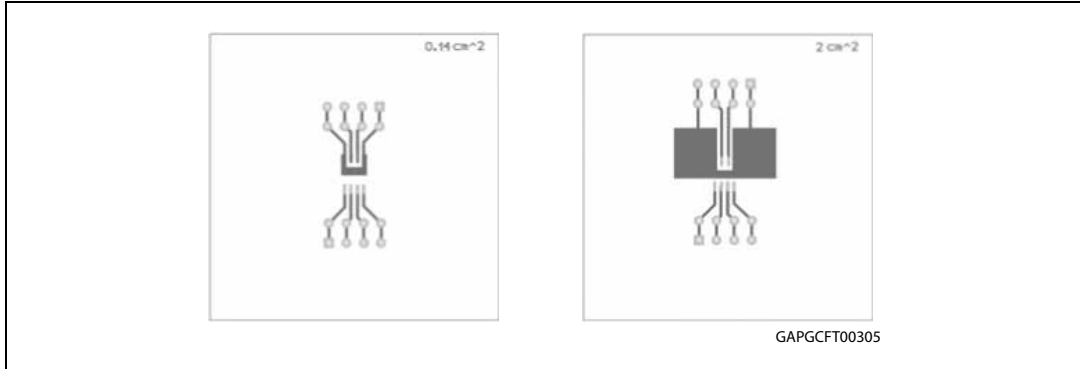


Note: Values are generated with  $R_L=0\Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

## 4 Package and PCB thermal data

### 4.1 SO-8 thermal data

Figure 24. SO-8 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.14cm<sup>2</sup>, 2cm<sup>2</sup>).

Figure 25. SO-8  $R_{thj-amb}$  vs PCB copper area in open box free air condition

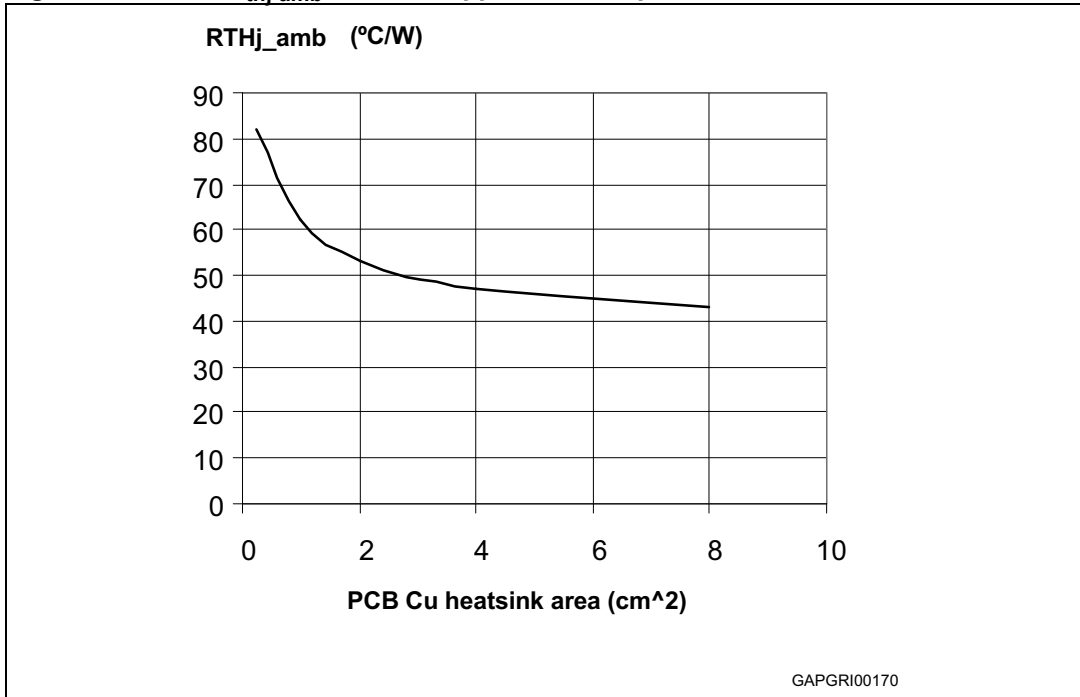
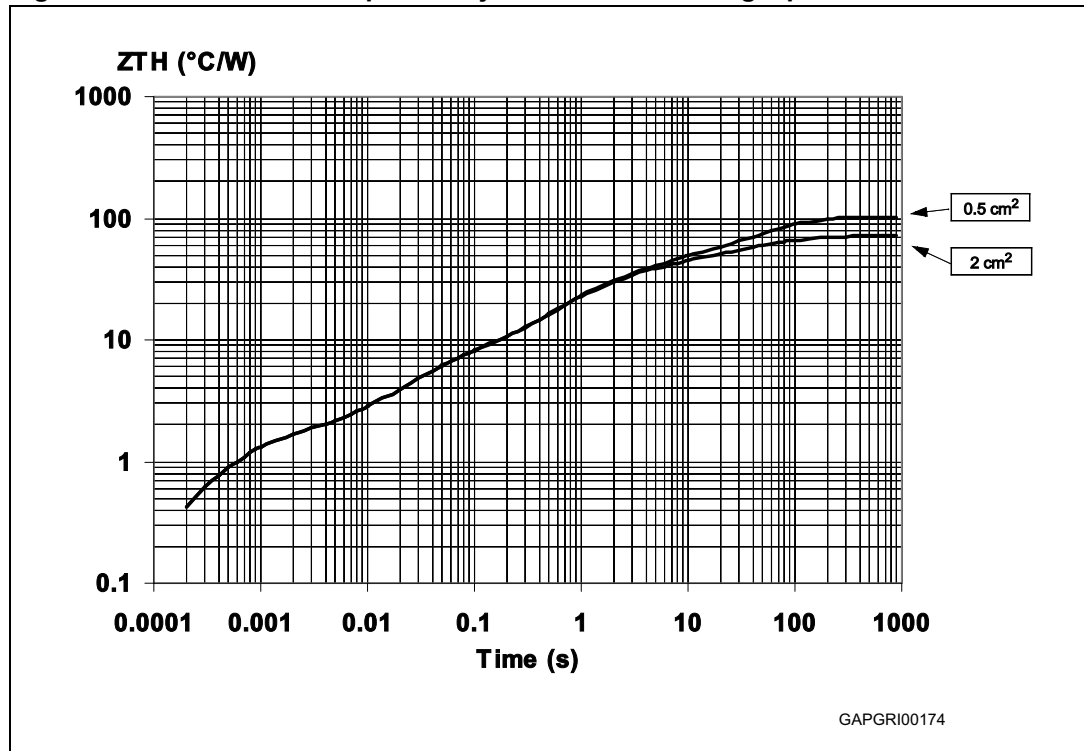


Figure 26. SO-8 thermal impedance junction ambient single pulse



**Equation 1 pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 27. Thermal fitting model of a single channel HSD in SO-8

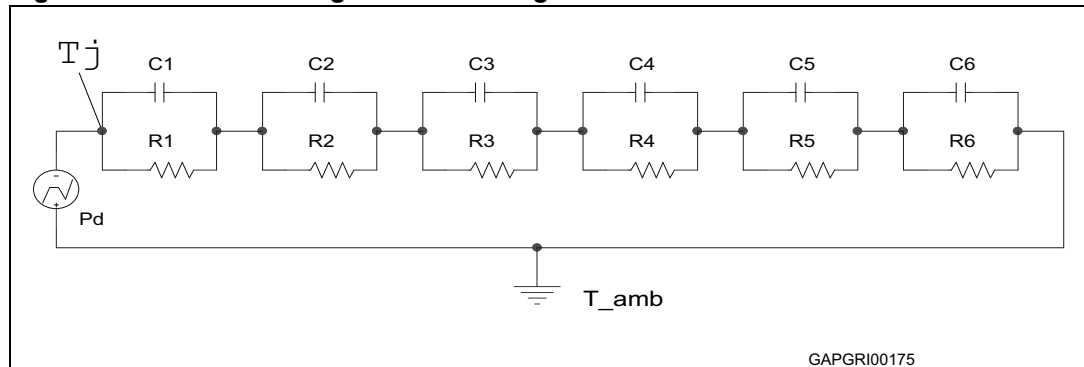


Table 15. Thermal parameter

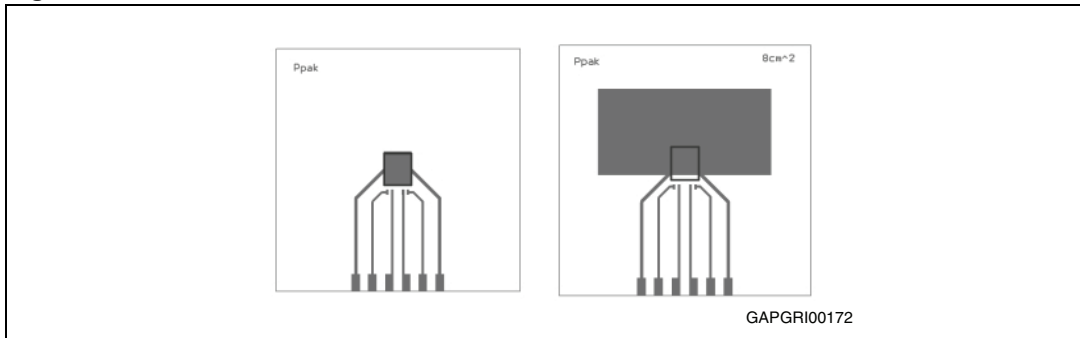
Area/island (cm <sup>2</sup> )	0.14	2
R1 (°C/W)	0.24	-
R2 (°C/W)	1.2	-
R3 (°C/W)	4.5	-
R4 (°C/W)	21	-

Table 15. Thermal parameter (continued)

Area/island (cm <sup>2</sup> )	0.14	2
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00015	
C2 (W.s/°C)	0.0005	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

## 4.2 PPAK thermal data

Figure 28. PPAK PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 60mm x 60mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: 0.44cm<sup>2</sup>, 8cm<sup>2</sup>).

Figure 29. PPAK  $R_{thj-amb}$  vs PCB copper area in open box free air condition

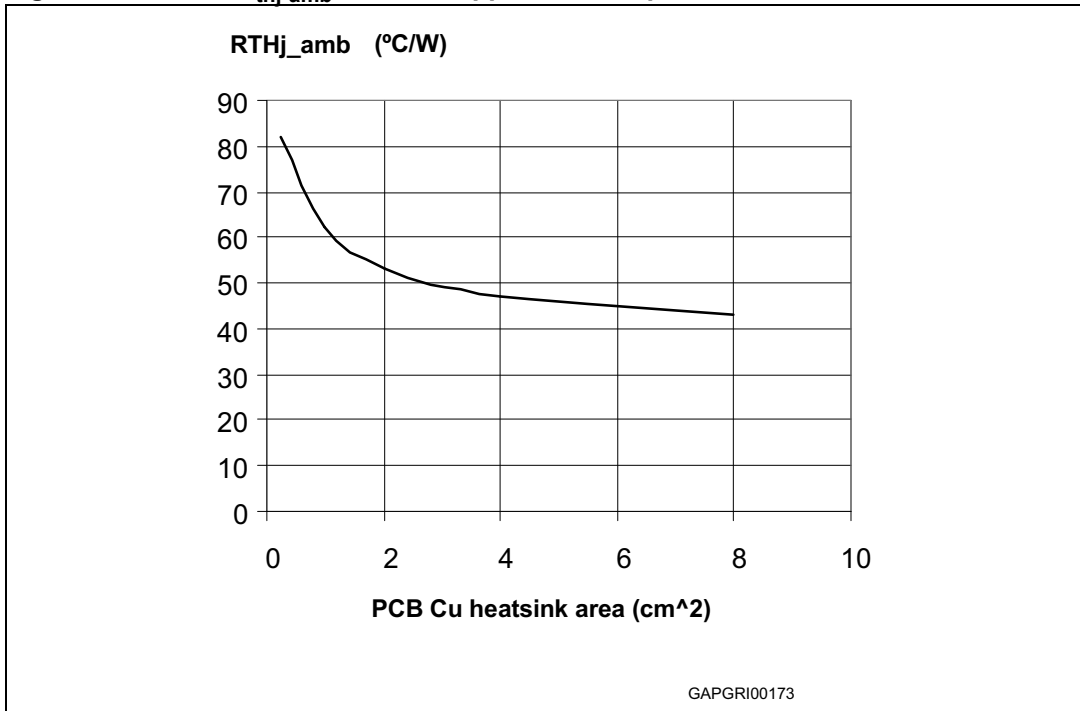
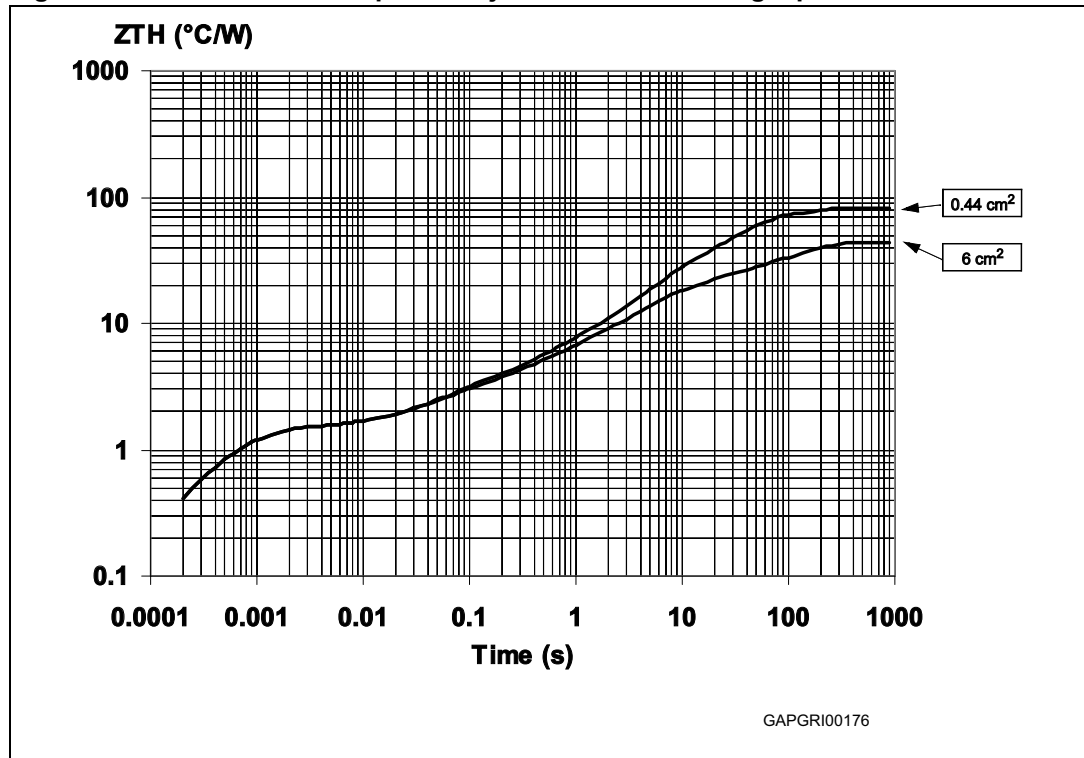


Figure 30. PPAK thermal impedance junction ambient single pulse



**Equation 2 Pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 31. Thermal fitting model of a single channel HSD in PPAK

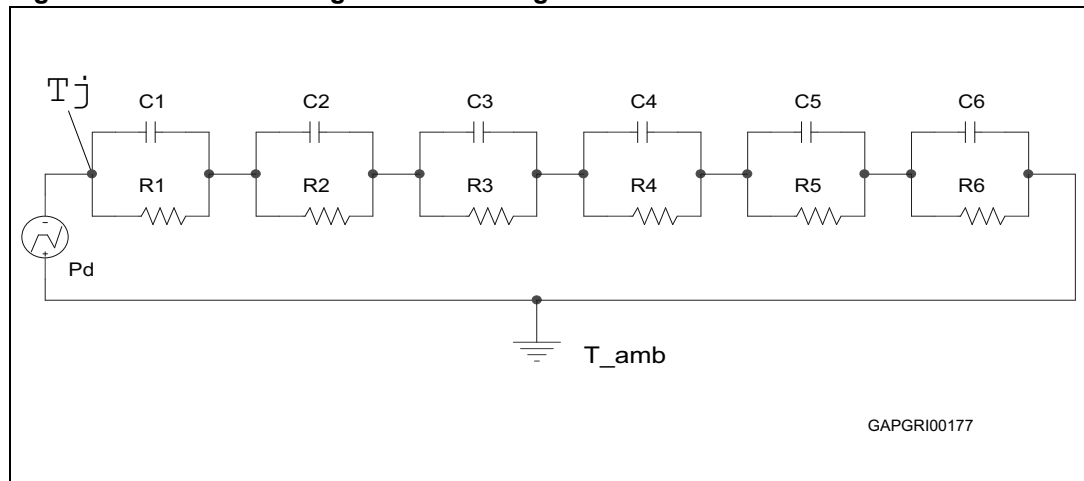


Table 16. Thermal parameter

<b>Ara/island (cm<sup>2</sup>)</b>	<b>0.44</b>	<b>6</b>
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5



## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 SO-8 package mechanical data

Figure 32. SO-8 package dimensions

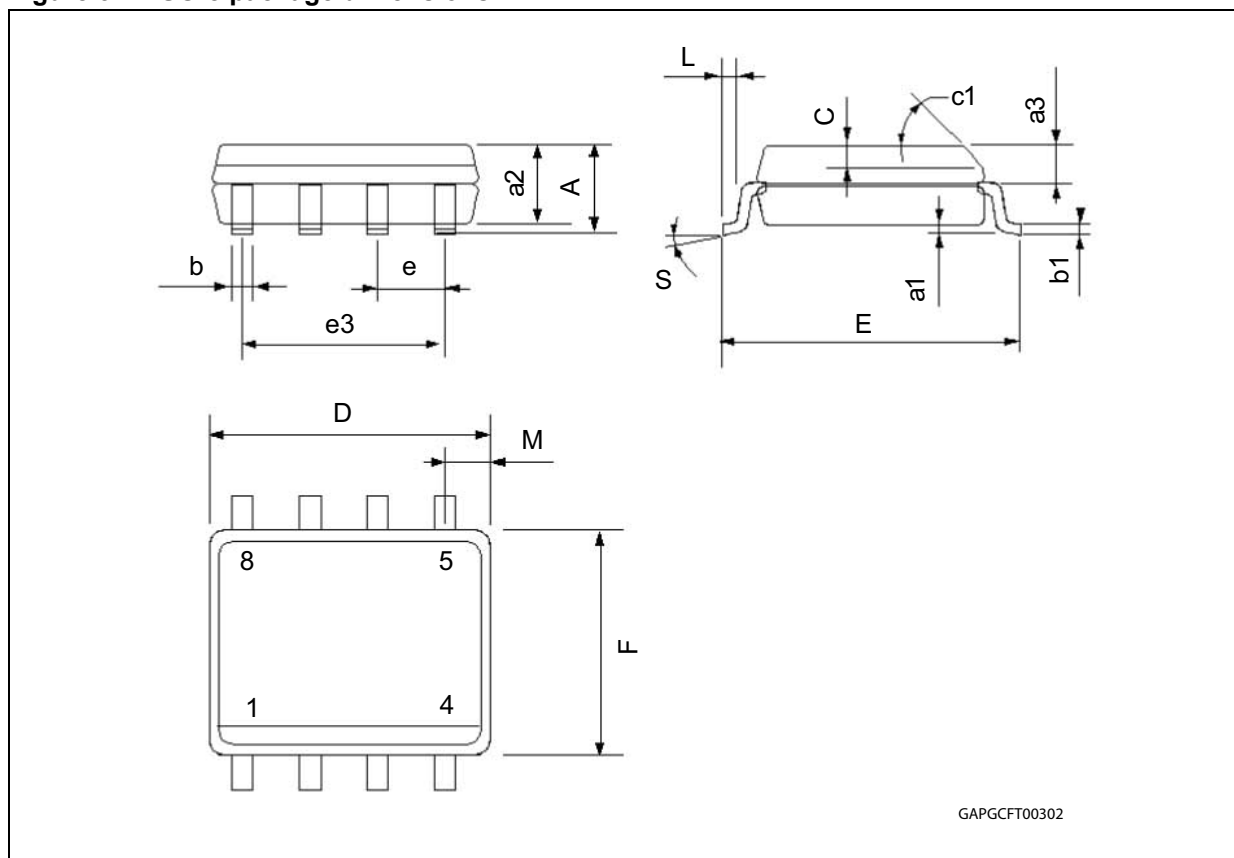


Table 17. SO-8 mechanical data

Symbol	millimeters		
	Min	Typ	Max
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85

Table 17. SO-8 mechanical data (continued)

Symbol	millimeters		
	Min	Typ	Max
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

### 5.3 PPAK package mechanical data

Figure 33. PPAK package dimensions

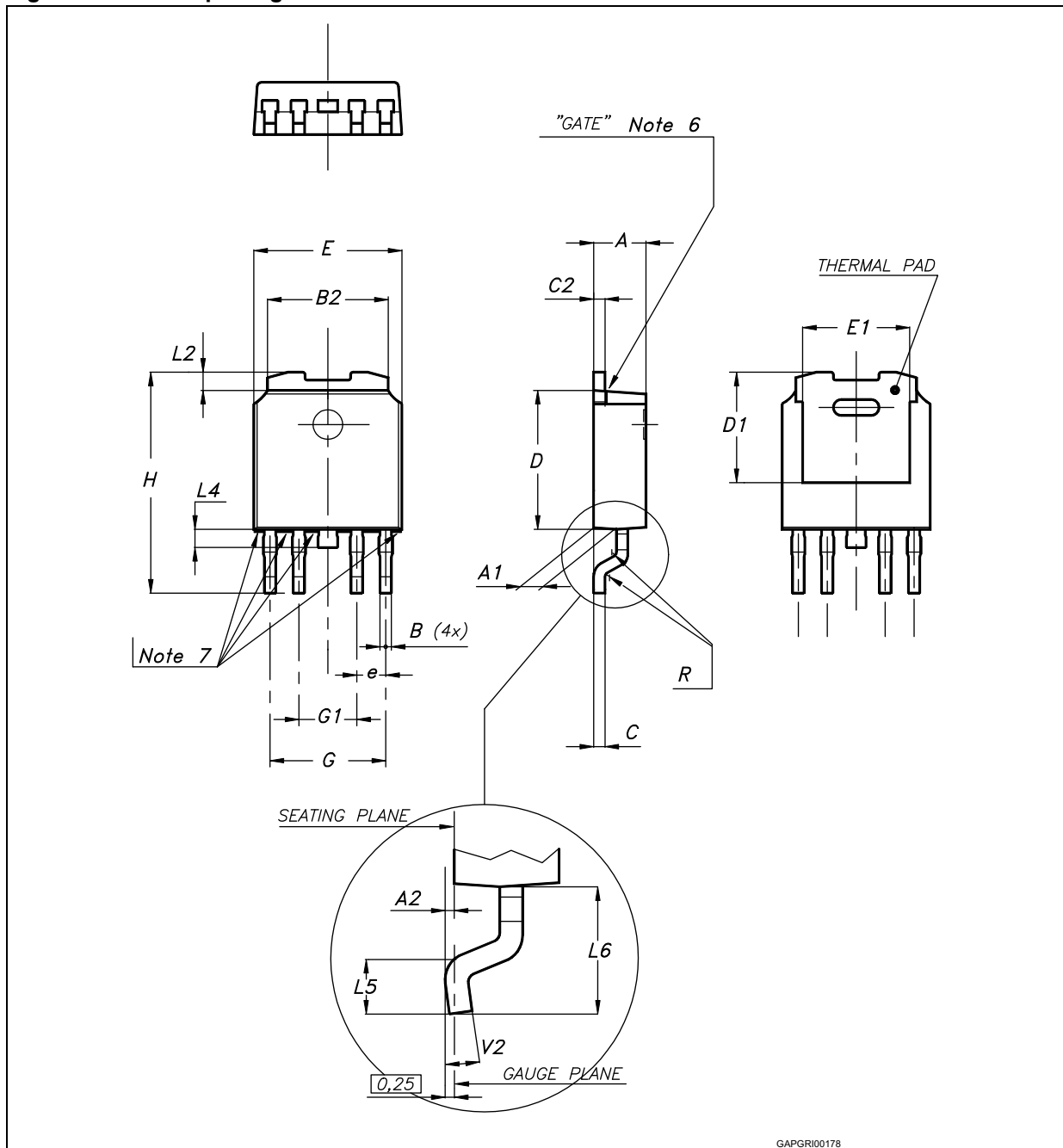


Table 18. PPAK mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
L5	1		
L6		2.80	
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		

Figure 34. SO-8 tube shipment (no suffix)

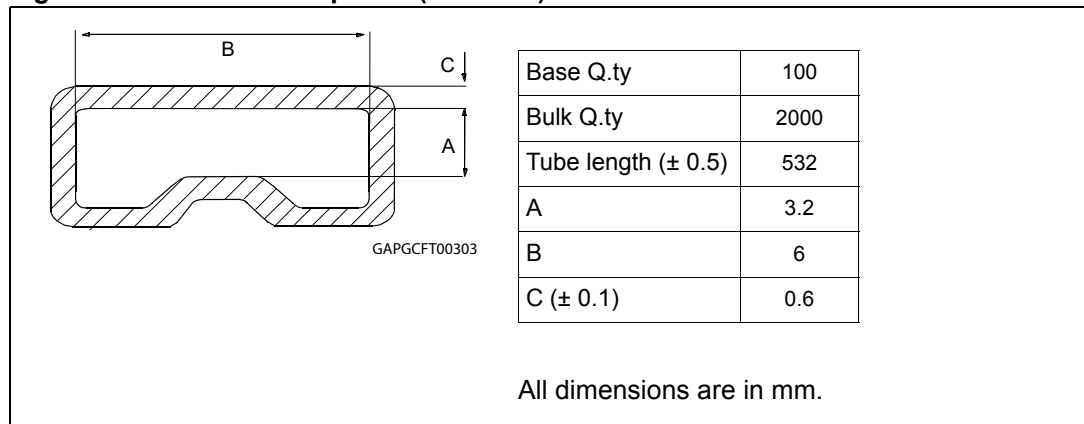


Figure 35. SO-8 tape and reel shipment (suffix "TR")

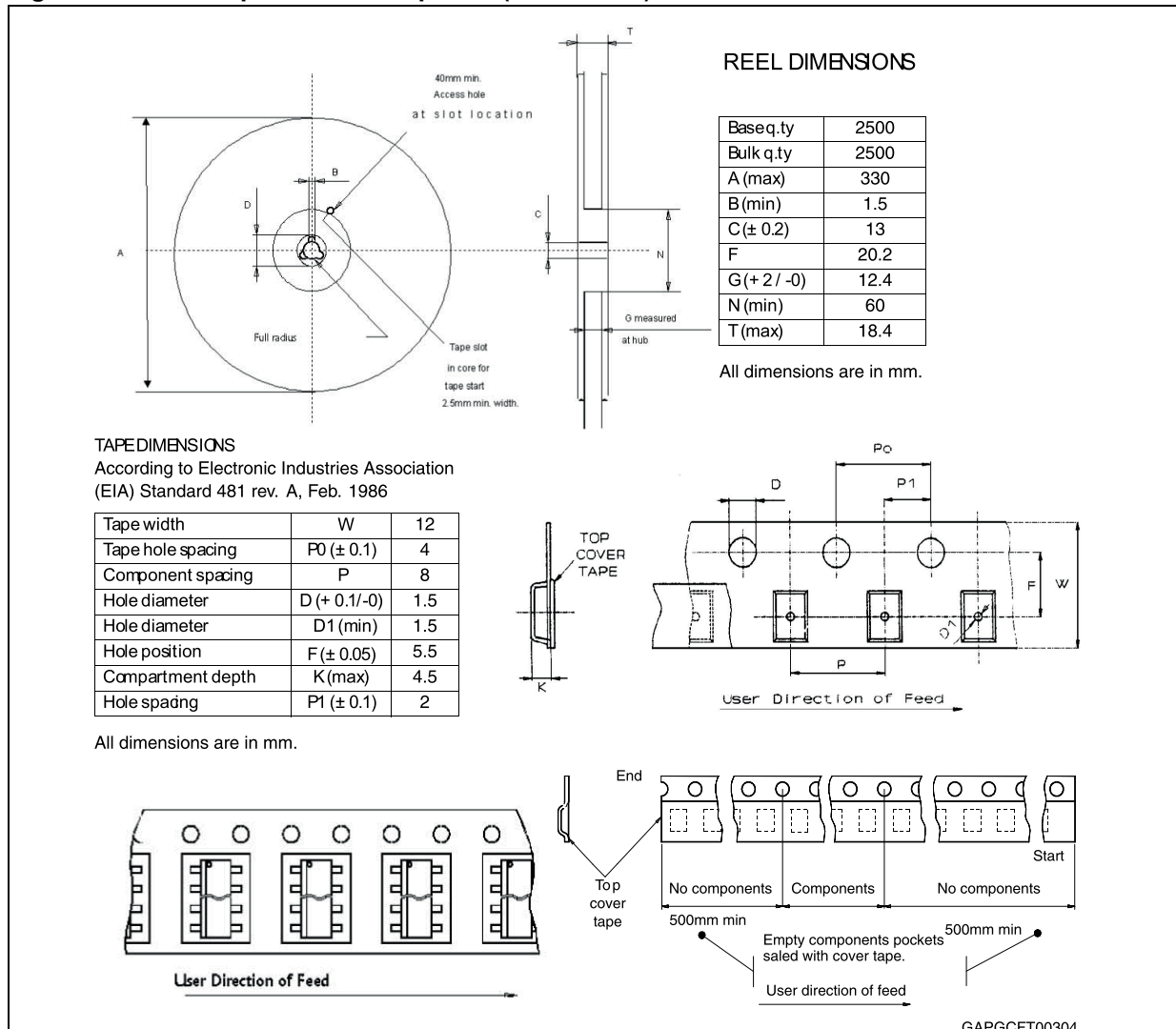


Figure 36. PPAK suggested pad layout and tube shipment (no suffix)

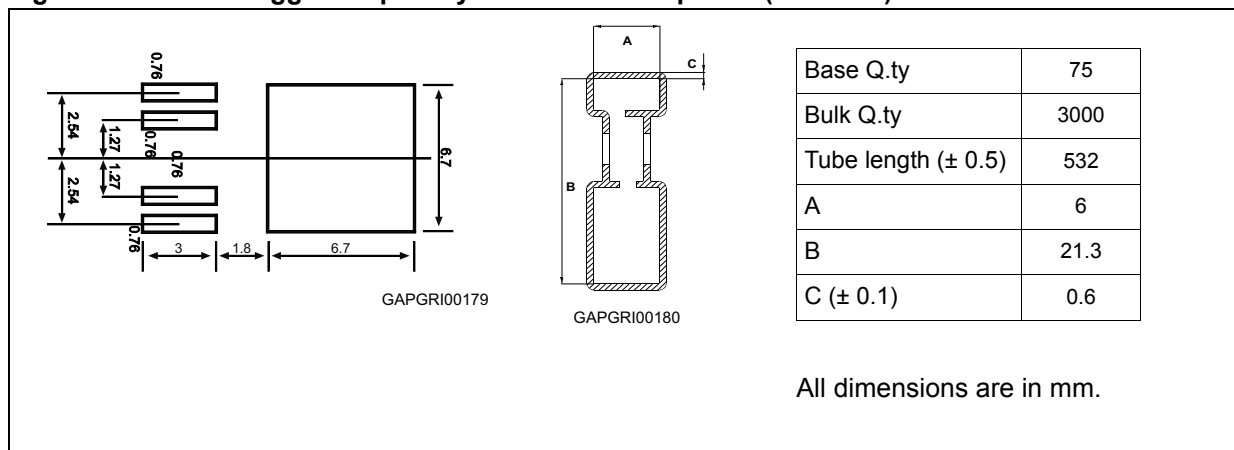
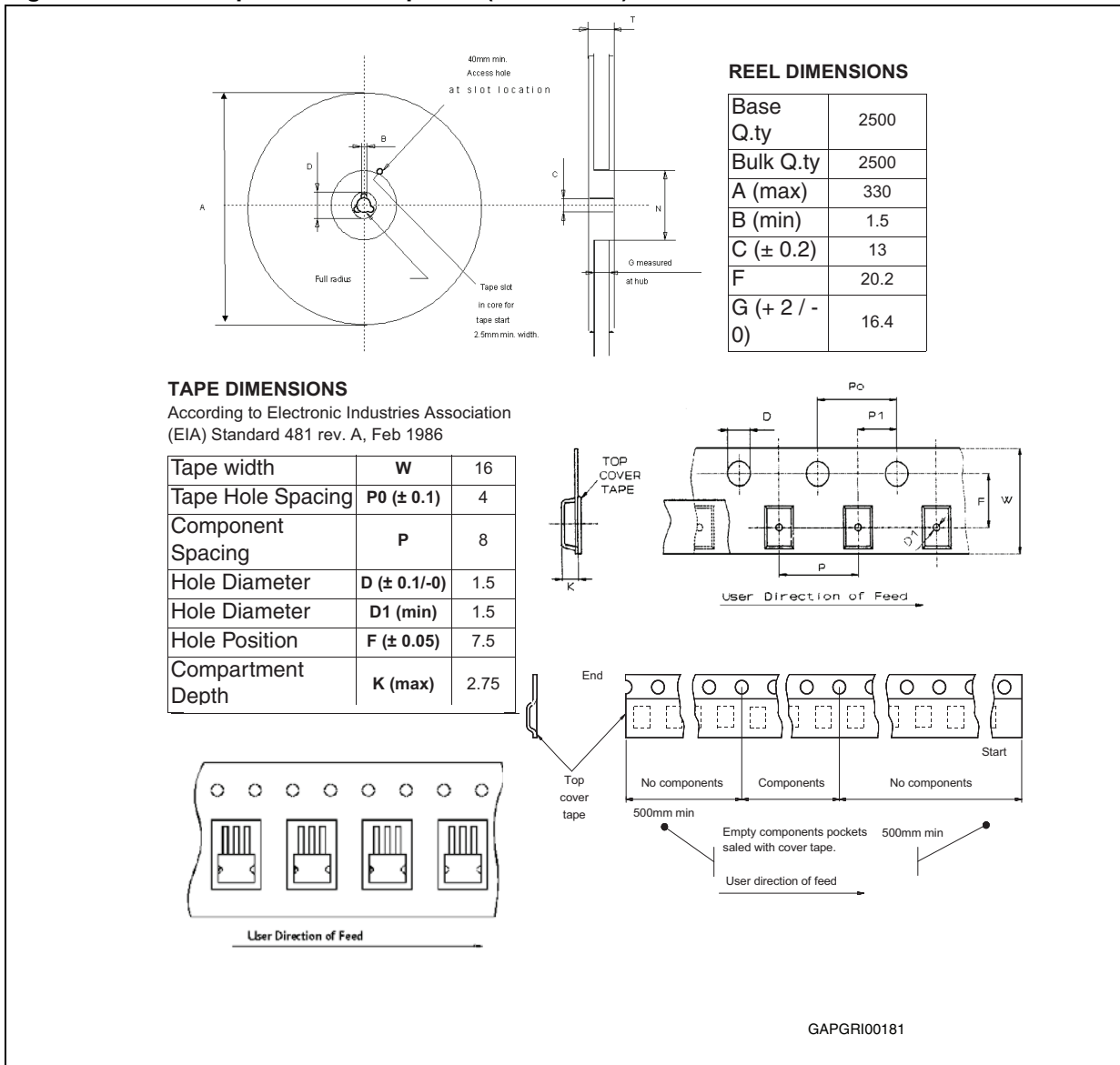


Figure 37. PPAK tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 19. Revision history**

Date	Revision	Changes
7-Oct-2004	1	Initial release.
02-May-2012	2	Update entire document following new ST template. Update <a href="#">Figure 33</a> and <a href="#">Table 18</a> .
20-Sep-2013	3	Updated Disclaimer.

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