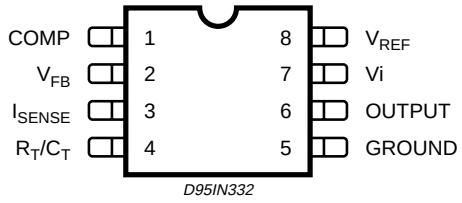
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (Ii < 30mA)	Self Limiting	
I_O	Output Current	±1	A
E_O	Output Energy (capacitive load)	5	µJ
	Analog Inputs (pins 2, 3)	– 0.3 to 5.5	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ °C (Minidip)	1.25	W
P_{tot}	Power Dissipation at Tamb ≤ 25 °C (SO8)	800	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_J	Junction Operating Temperature	– 40 to 150	°C
T_L	Lead Temperature (soldering 10s)	300	°C

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTION (top view)

Minidip/SO8



PIN FUNCTIONS

No	Function	Description
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to Vref and cpacitor C_T to ground. Operation to 500kHz is possible.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

ORDERING NUMBERS

SO8	Minidip
UC2842BD1; UC3842BD1 UC2843BD1; UC3843BD1 UC2844BD1; UC3844BD1 UC2845BD1; UC3845BD1	UC2842BN; UC3842BN UC2843BN; UC3843BN UC2844BN; UC3844BN UC2845BN; UC3845BN

THERMAL DATA

Symbol	Description		Minidip	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient.	max.	100	150	°C/W

ELECTRICAL CHARACTERISTICS ([note 1] Unless otherwise stated, these specifications apply for $-25 \le T_{amb} \le 85°C$ for UC284XB; $0 \le T_{amb} \le 70°C$ for UC384XB; $V_i = 15V$ (note 5); $R_T = 10K$; $C_T = 3.3nF$)

Symbol	Parameter	Test Conditions	UC284XB			UC384XB			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	$T_j = 25°C$ $I_o = 1mA$	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	$12V \le V_i \le 25V$		2	20		2	20	mV
ΔV_{REF}	Load Regulation	$1 \le I_o \le 20mA$		3	25		3	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2			0.2		mV/°C
	Total Output Variation	Line, Load, Temperature	4.9		5.1	4.82		5.18	V
e_N	Output Noise Voltage	$10Hz \le f \le 10KHz$ $T_j = 25°C$ (note 2)		50			50		µV
	Long Term Stability	$T_{amb} = 125°C$, 1000Hrs (note 2)		5	25		5	25	mV
I_{SC}	Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
OSCILLATOR SECTION									
f_{OSC}	Frequency	$T_j = 25°C$ $T_A = T_{low}$ to T_{high} $T_J = 25°C$ ($R_T = 6.2k$, $C_T = 1nF$)	49 48 225	52 – 250	55 56 275	49 48 225	52 – 250	55 56 275	KHz KHz KHz
$\Delta f_{OSC}/\Delta V$	Frequency Change with Volt.	$V_{CC} = 12V$ to 25V	–	0.2	1	–	0.2	1	%
$\Delta f_{OSC}/\Delta T$	Frequency Change with Temp.	$T_A = T_{low}$ to T_{high}	–	1	–	–	0.5	–	%
V_{OSC}	Oscillator Voltage Swing	(peak to peak)	–	1.6	–	–	1.6	–	V
I_{dischg}	Discharge Current (V_{OSC} =2V)	$T_J = 25°C$ $T_A = T_{low}$ to T_{high}	7.8 7.5	8.3 –	8.8 8.8	7.8 7.6	8.3 –	8.8 8.8	mA mA
ERROR AMP SECTION									
V_2	Input Voltage	$V_{PIN1} = 2.5V$	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input Bias Current	$V_{FB} = 5V$		-0.1	-1		-0.1	-2	µA
	A_{VOL}	$2V \le V_o \le 4V$	65	90		65	90		dB
BW	Unity Gain Bandwidth	$T_J = 25°C$	0.7	1		0.7	1		MHz
PSRR	Power Supply Rejec. Ratio	$12V \le V_i \le 25V$	60	70		60	70		dB
I_o	Output Sink Current	$V_{PIN2} = 2.7V$ $V_{PIN1} = 1.1V$	2	12		2	12		mA
I_o	Output Source Current	$V_{PIN2} = 2.3V$ $V_{PIN1} = 5V$	-0.5	-1		-0.5	-1		mA
	V_{OUT} High	$V_{PIN2} = 2.3V$; $R_L = 15K\Omega$ to Ground	5	6.2		5	6.2		V
	V_{OUT} Low	$V_{PIN2} = 2.7V$; $R_L = 15K\Omega$ to Pin 8		0.8	1.1		0.8	1.1	V
CURRENT SENSE SECTION									
G_V	Gain	(note 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
V_3	Maximum Input Signal	$V_{PIN1} = 5V$ (note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	$12 \le V_i \le 25V$ (note 3)		70			70		dB
I_b	Input Bias Current			-2	-10		-2	-10	µA
	Delay to Output			150	300		150	300	ns

ELECTRICAL CHARACTERISTICS (continued)

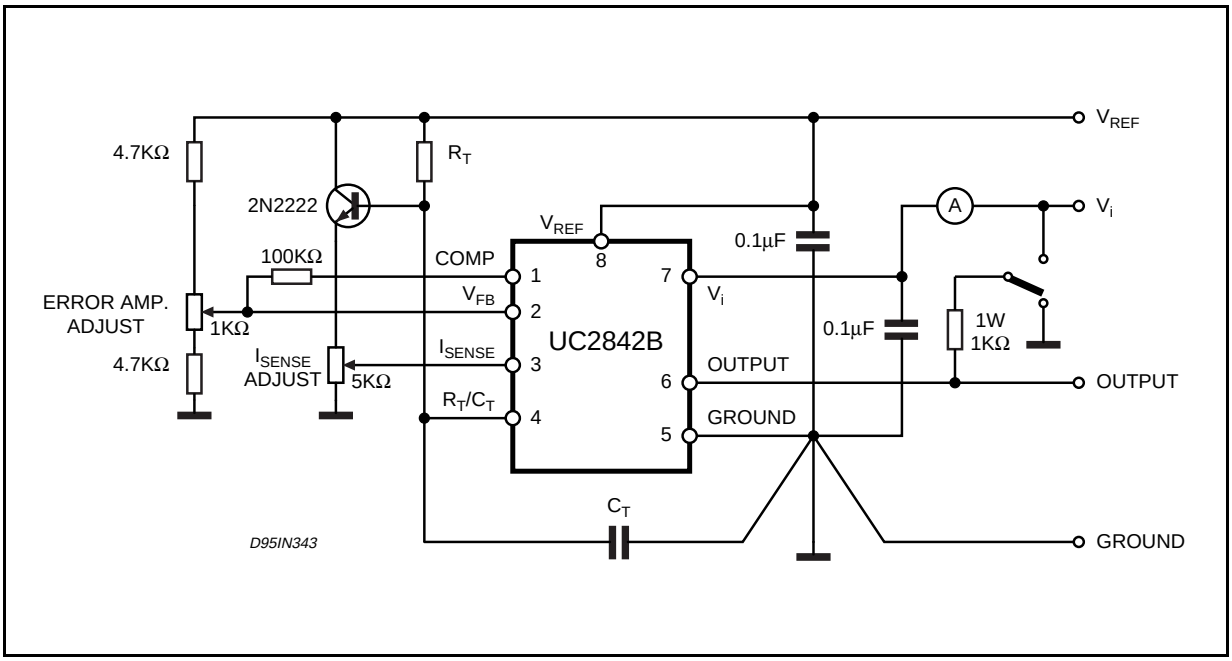
Symbol	Parameter	Test Conditions	UC284XB			UC384XB			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OUTPUT SECTION									
V_{OL}	Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200mA		1.6	2.2		1.6	2.2	V
V_{OH}	Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200mA	12	13.5		12	13.5		V
V_{OLS}	UVLO Saturation	VCC = 6V; I_{SINK} = 1mA		0.1	1.1		0.1	1.1	V
t_r	Rise Time	T_j = 25°C C_L = 1nF (2)		50	150		50	150	ns
t_f	Fall Time	T_j = 25°C C_L = 1nF (2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842B/4B	15	16	17	14.5	16	17.5	V
		X843B/5B	7.8	8.4	9.0	7.8	8.4	9.0	V
	Min Operating Voltage After Turn-on	X842B/4B	9	10	11	8.5	10	11.5	V
		X843B/5B	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM SECTION									
	Maximum Duty Cycle	X842B/3B	94	96	100	94	96	100	%
		X844B/5B	47	48	50	47	48	50	%
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current	V_i = 6.5V for UCX843B/45B		0.3	0.5		0.3	0.5	mA
		V_i = 14V for UCX842B/44B		0.3	0.5		0.3	0.5	mA
I_i	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0V		12	17		12	17	mA
V_{iz}	Zener Voltage	I_i = 25mA	30	36		30	36		V

Notes :
1. Max package power dissipation limits must be respected; low duty cycle pulse techniques are used during test maintain T_j as close to T_{amb} as possible.
2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{PIN2} = 0.
4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} \quad ; 0 \le V_{PIN3} \le 0.8\ V$$

5. Adjust V_i above the start threshold before setting at 15 V.

Figure 1: Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 2: Timing Resistor vs. Oscillator Frequency

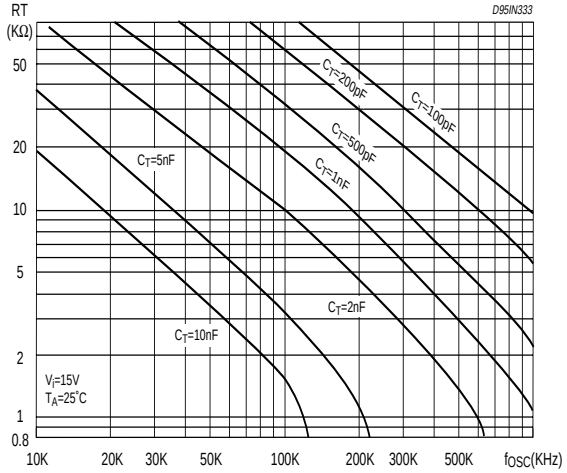


Figure 3: Output Dead-Time vs. Oscillator Frequency

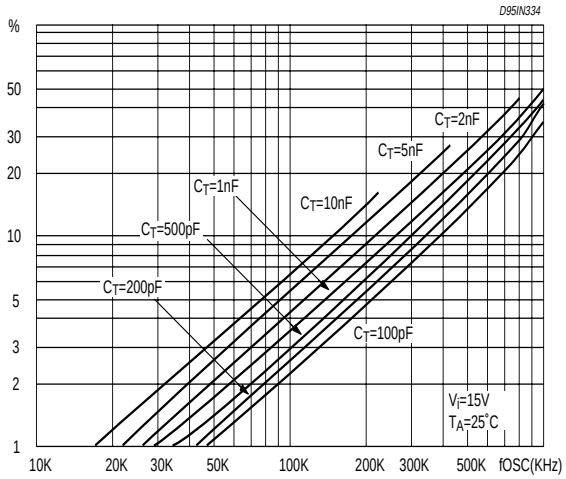


Figure 4: Oscillator Discharge Current vs. Temperature.

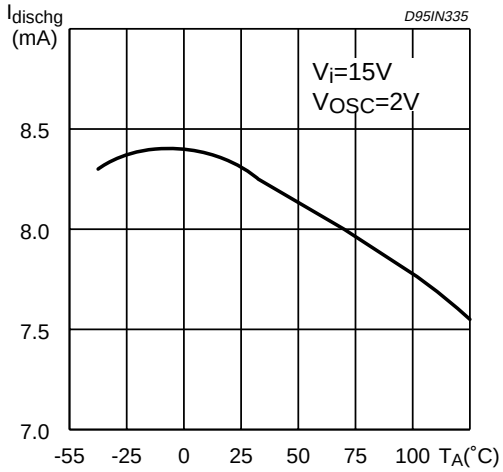


Figure 5: Maximum Output Duty Cycle vs. Timing Resistor.

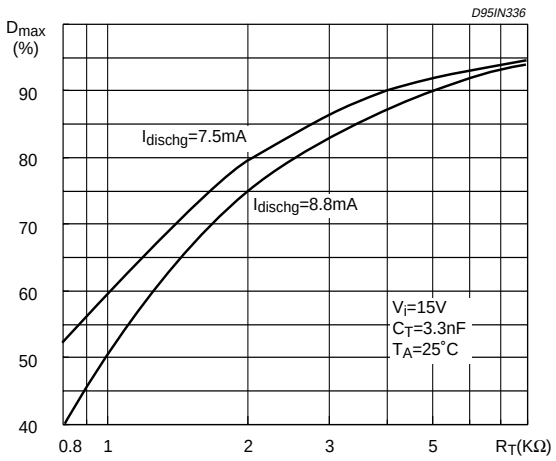


Figure 6: Error Amp Open-Loop Gain and Phase vs. Frequency.

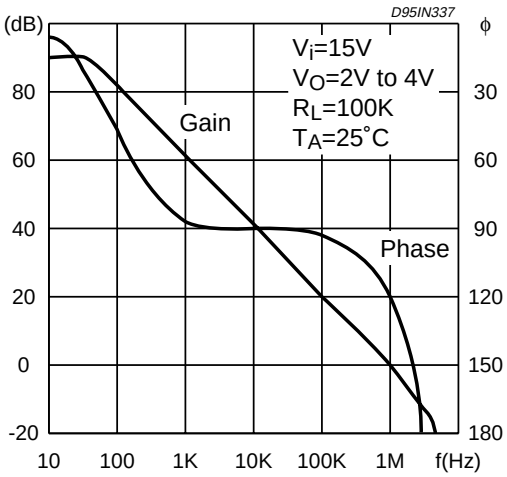


Figure 7: Current Sense Input Threshold vs. Error Amp Output Voltage.

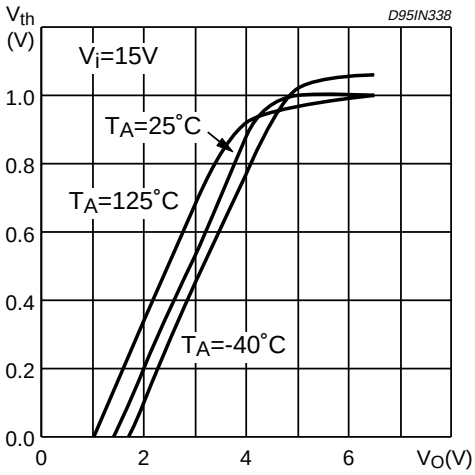


Figure 8: Reference Voltage Change vs. Source Current.

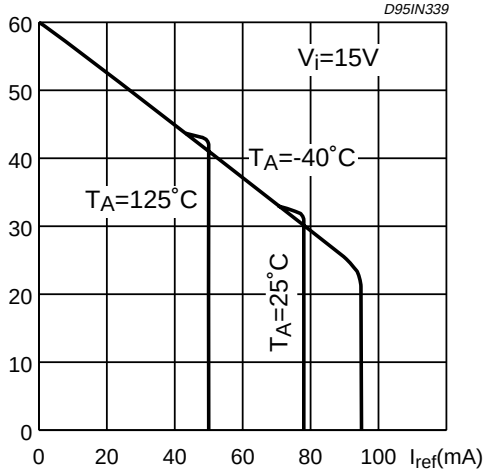


Figure 9: Reference Short Circuit Current vs. Temperature.

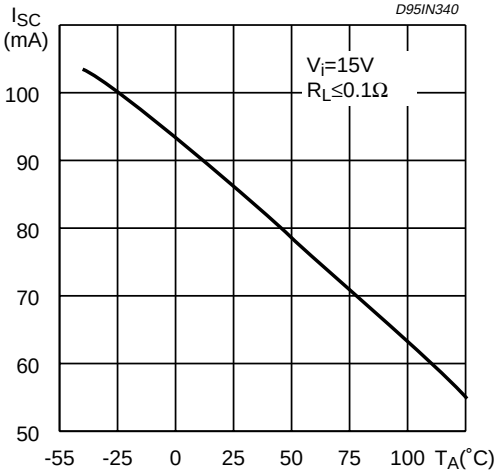


Figure 10: Output Saturation Voltagevs. Load Current.

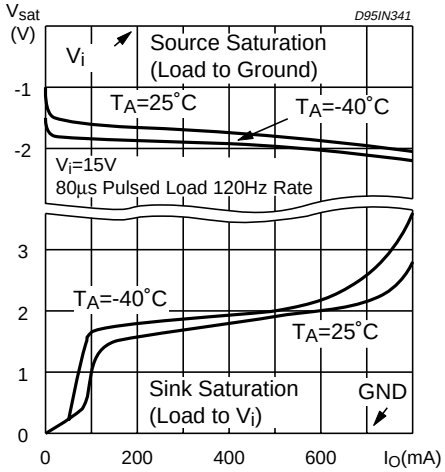


Figure 11: Supply Current vs. Supply Voltage.

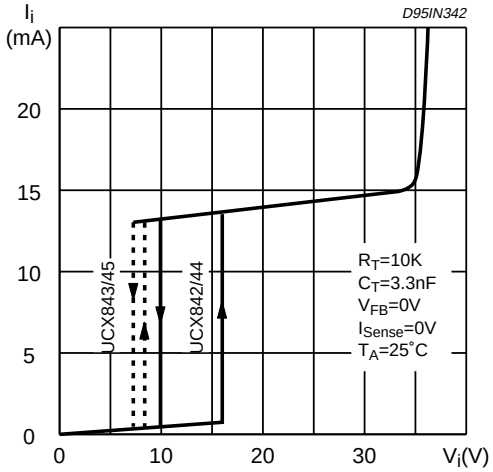


Figure 12: Output Waveform.

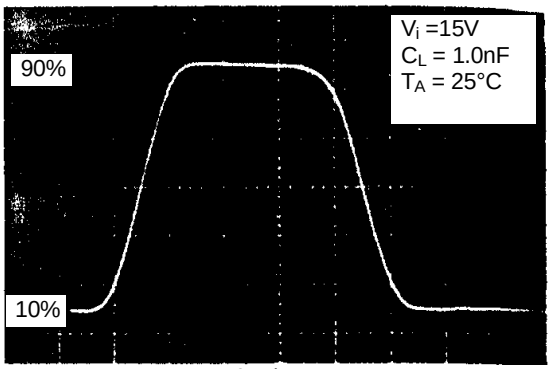


Figure 13: Output Cross Conduction

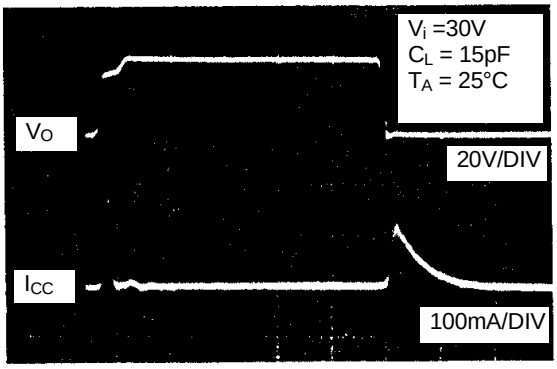


Figure 14: Oscillator and Output Waveforms.

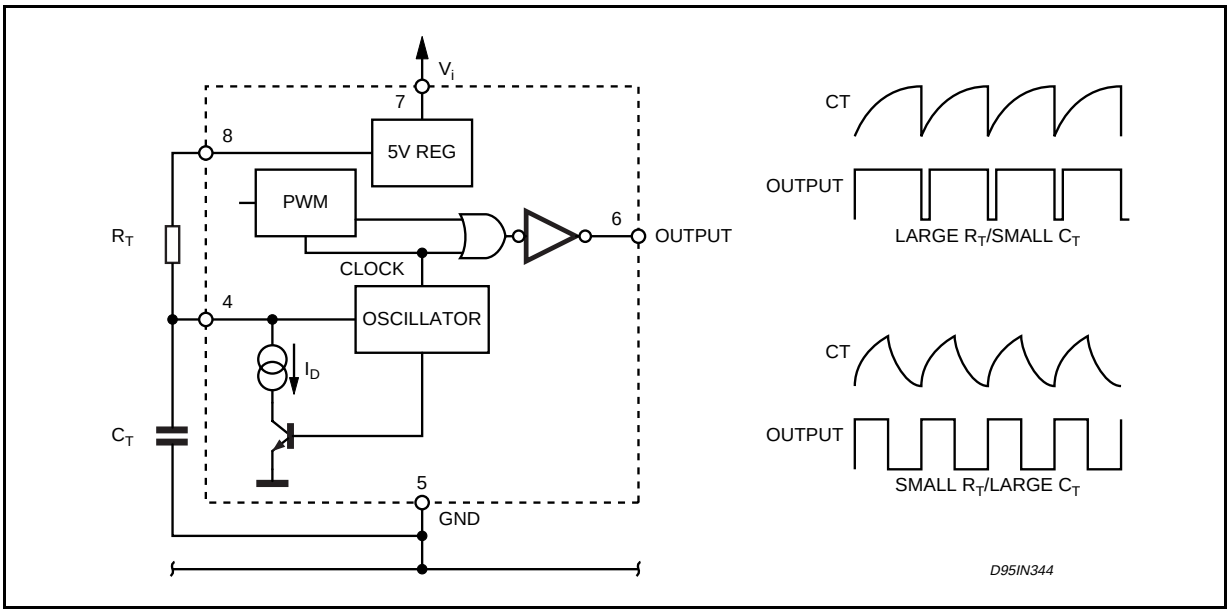


Figure 15 : Error Amp Configuration.

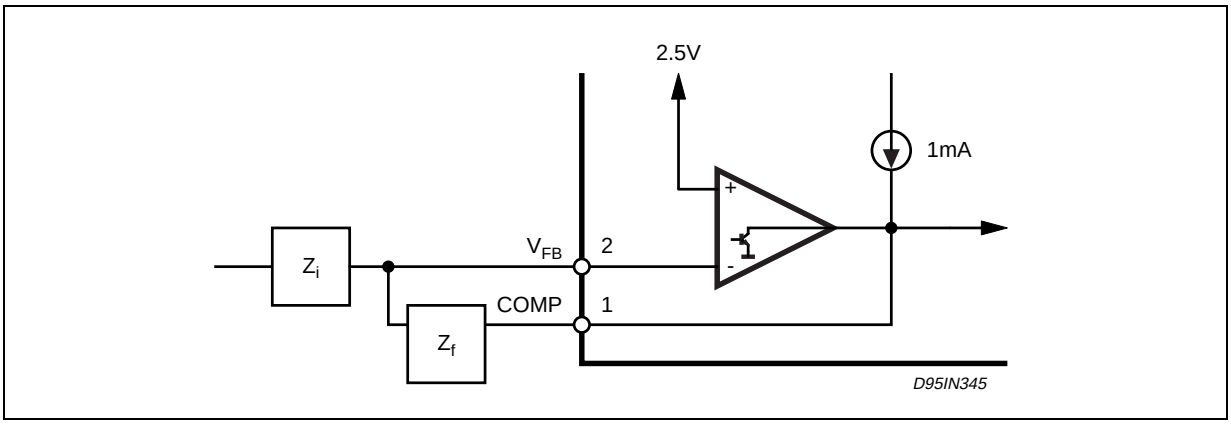


Figure 16 : Under Voltage Lockout.

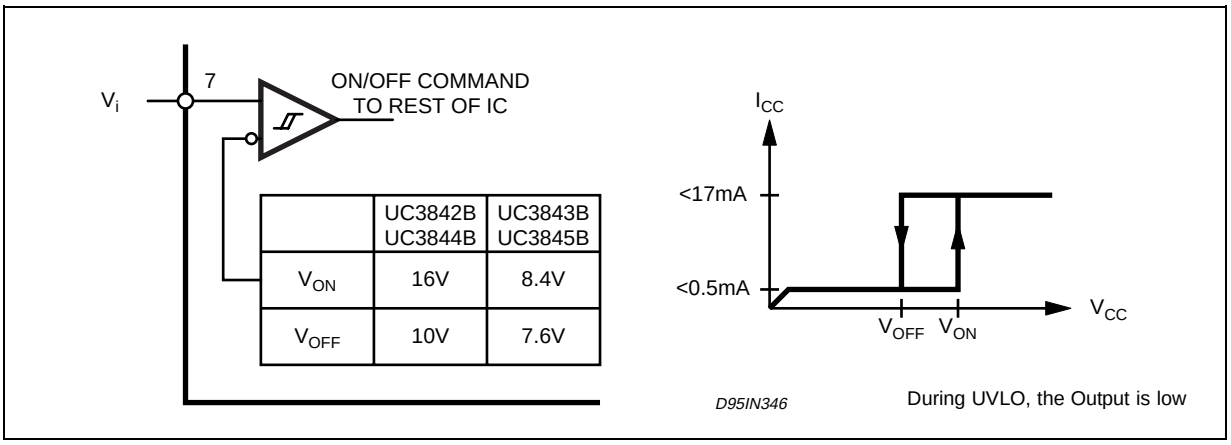
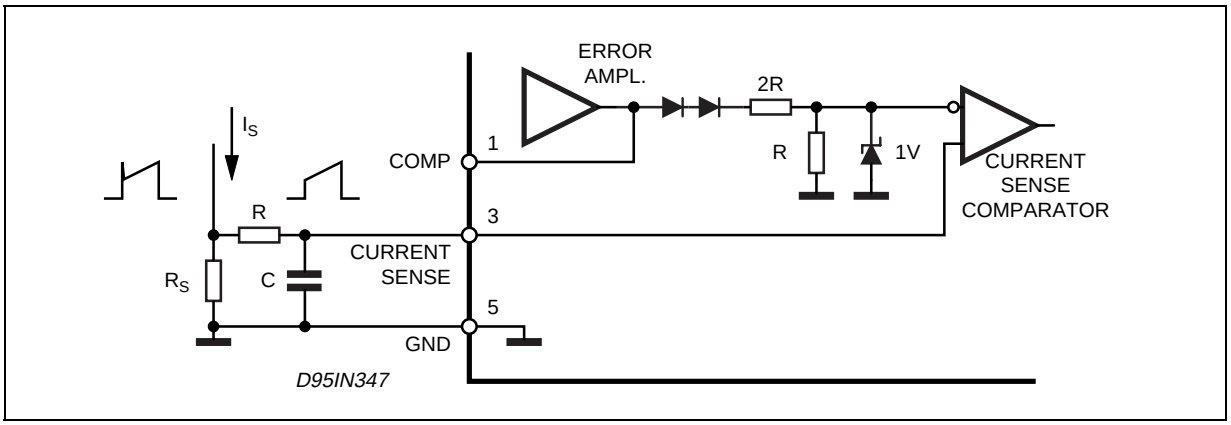


Figure 17 : Current Sense Circuit .



Peak current (i_s) is determined by the formula

$$I_{S\,max} \approx \frac{1.0\ V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 18 : Slope Compensation Techniques.

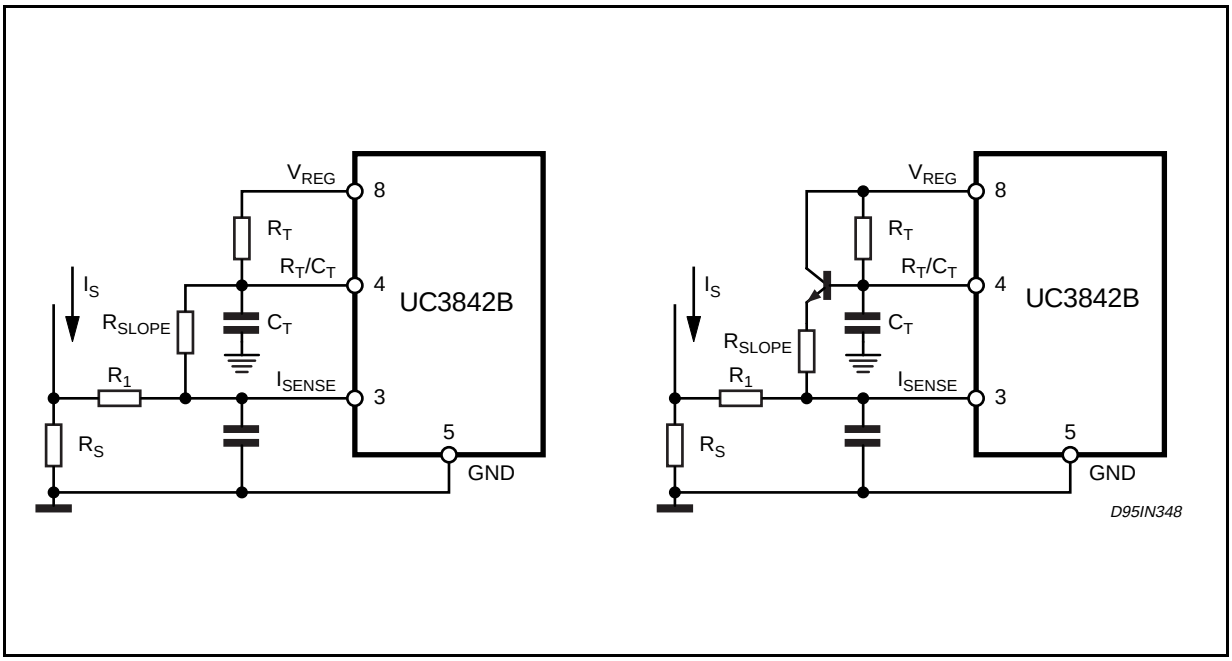


Figure 19 : Isolated MOSFET Drive and Current Transformer Sensing.

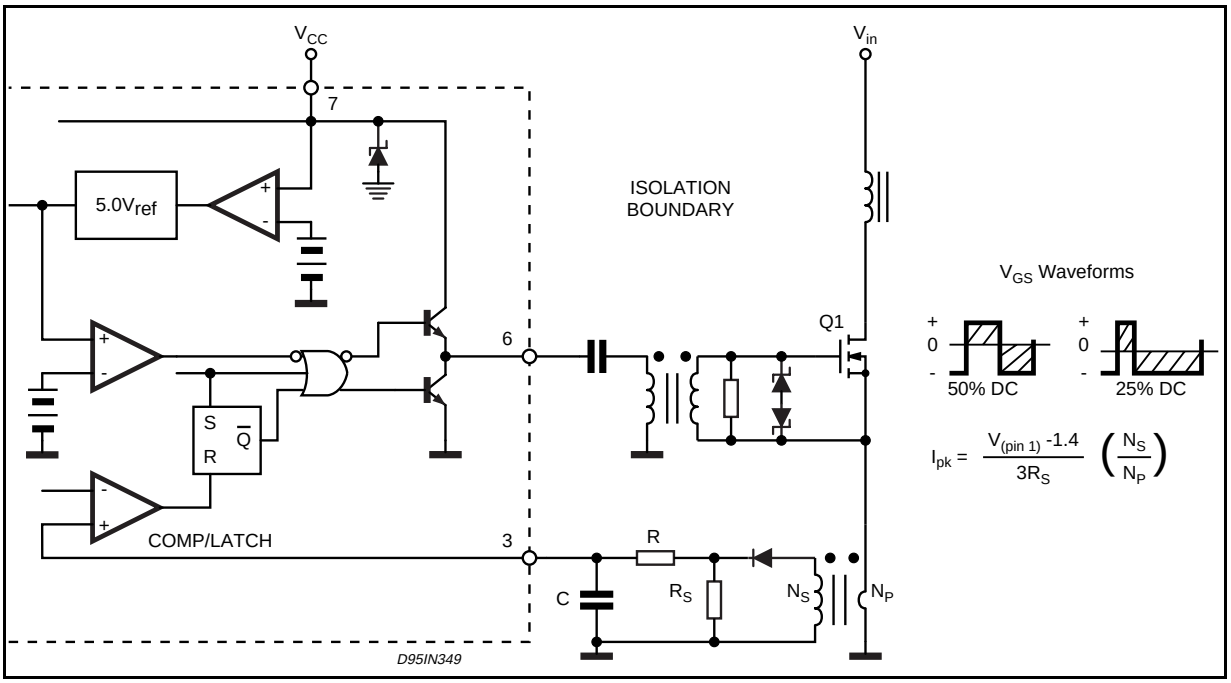
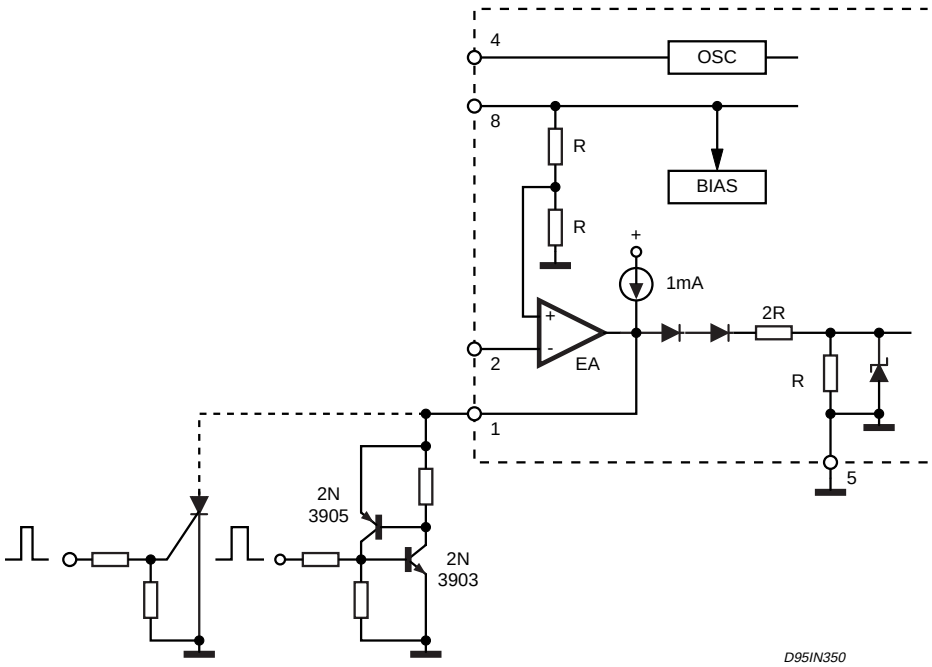
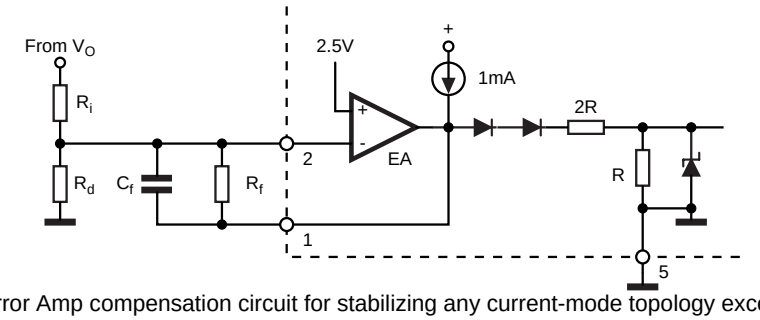


Figure 20 : Latched Shutdown.

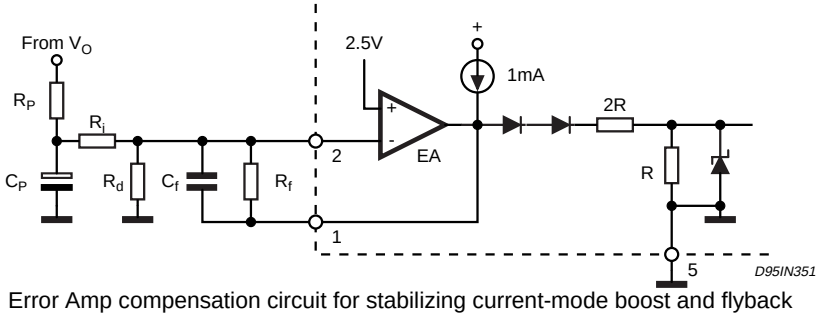


SCR must be selected for a holding current of less than 0.5mA at $T_{A(min)}$.
The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

Figure 21: Error Amplifier Compensation

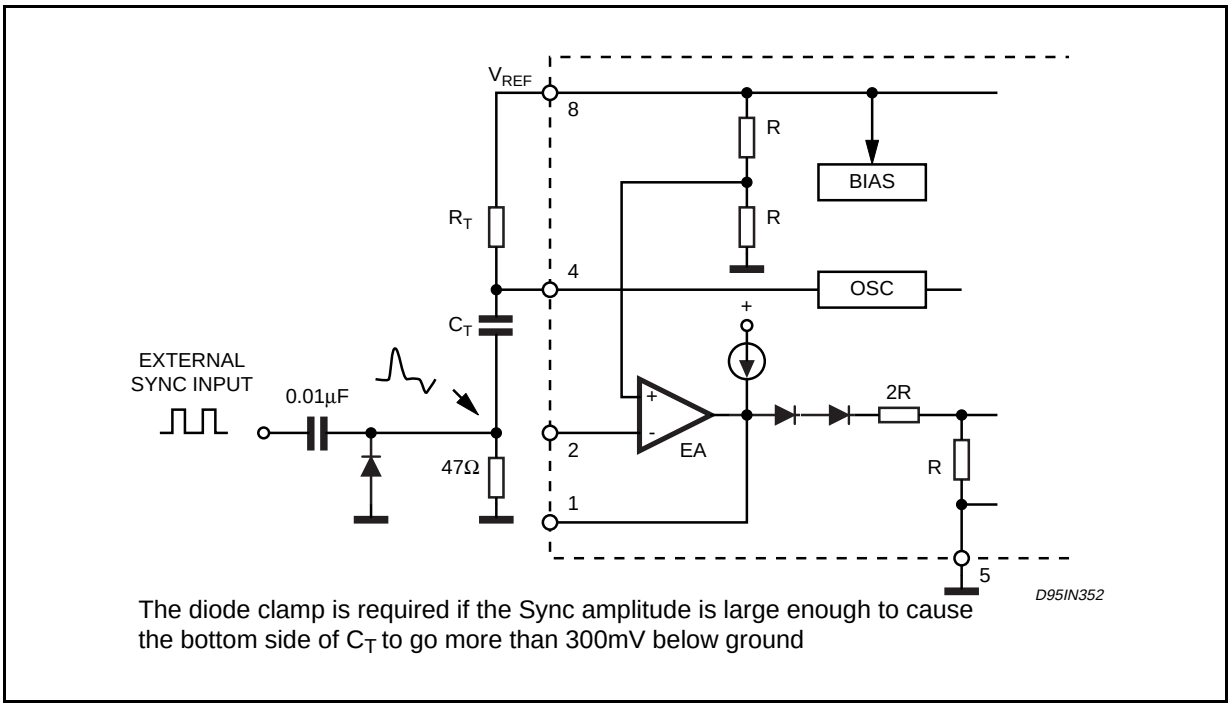


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



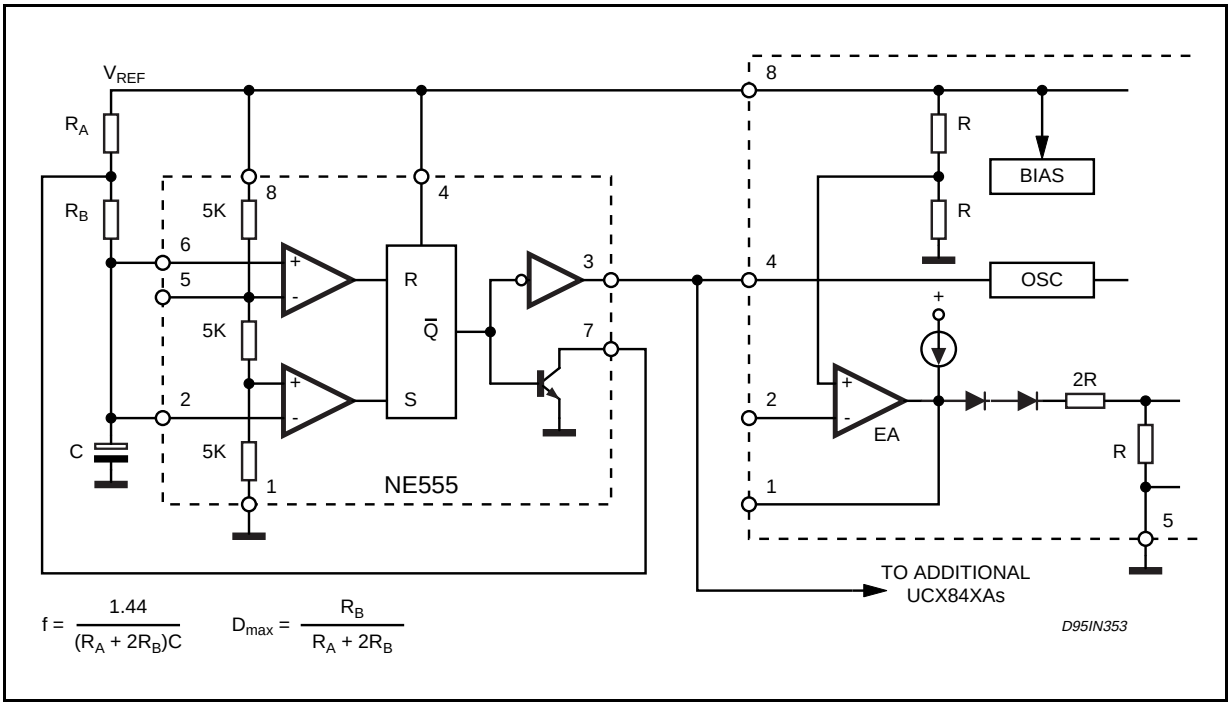
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 22: External Clock Synchronization.



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300mV below ground

Figure 23: External Duty Cycle Clamp and Multi Unit Synchronization.



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 24: Soft-Start Circuit

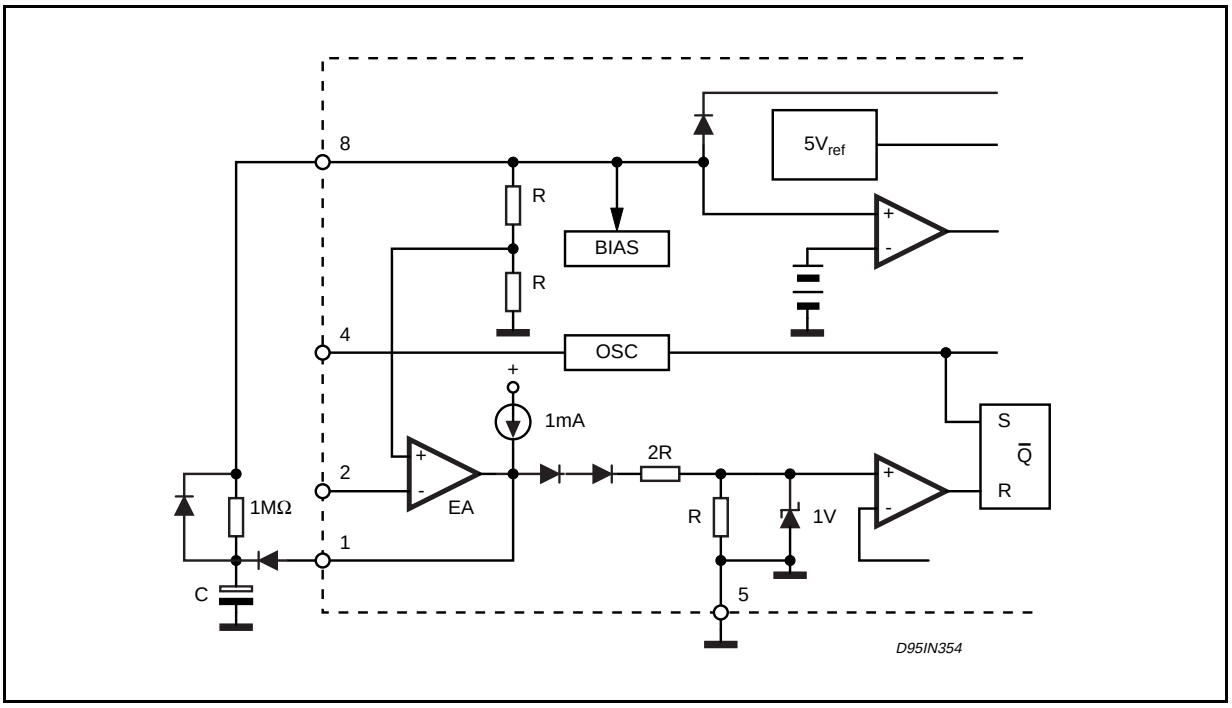
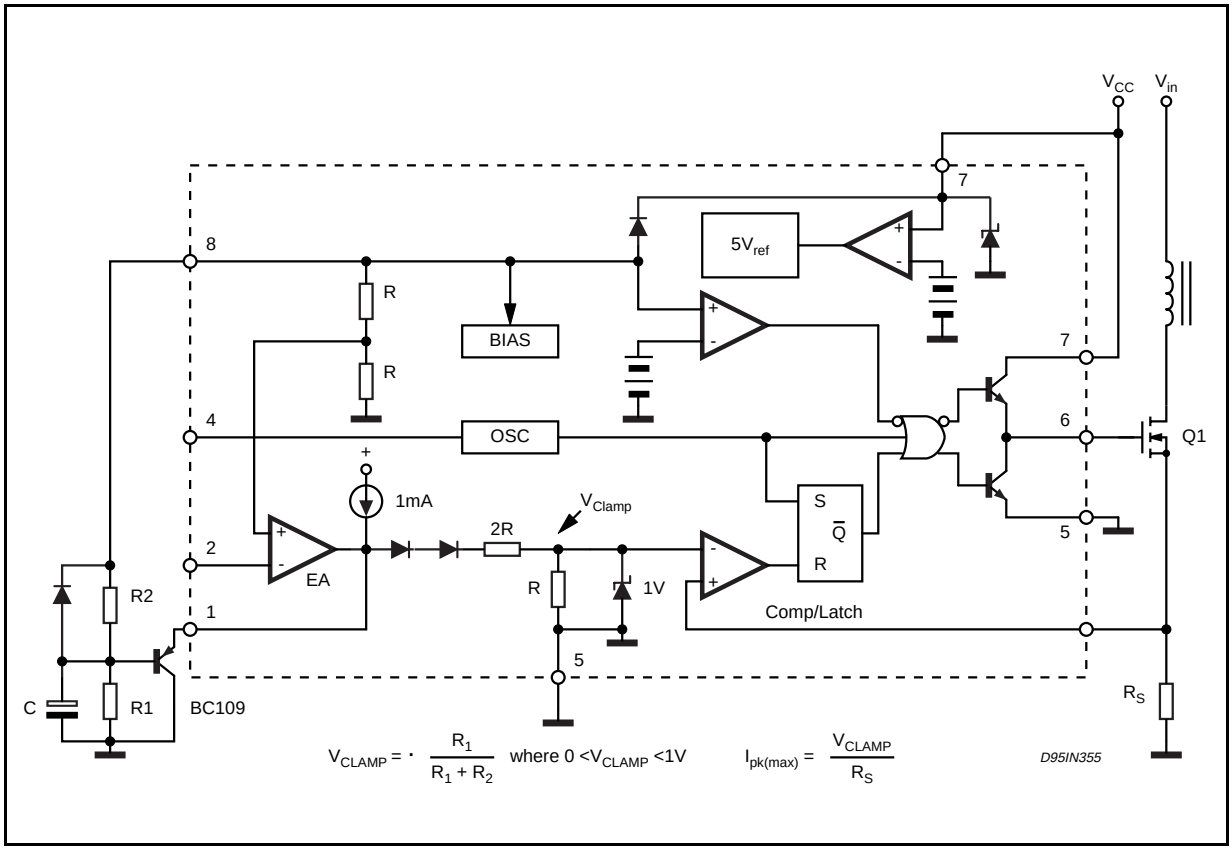


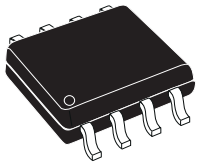
Figure 25: Soft-Start and Error Amplifier Output Duty Cycle Clamp.



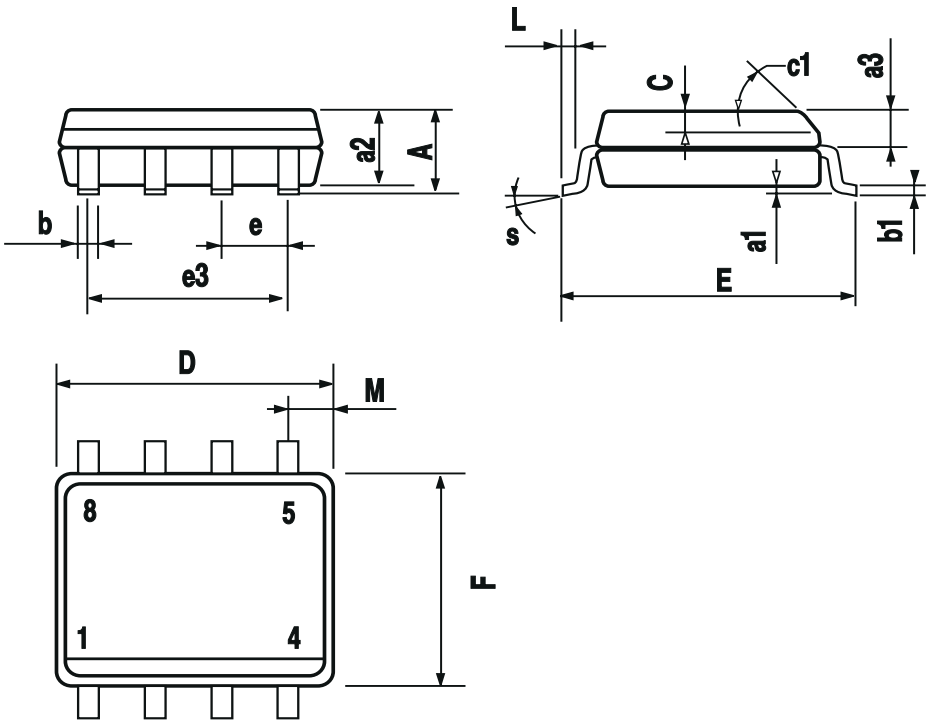
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA

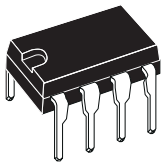


SO8



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



Minidip